INTERNATIONAL STANDARD

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Road vehicles— FlexRay communications system —

Part 5: Electrical physical layer conformance test specification

Véhicules routiers — Système de communications FlexRay —

Partie 5: Spécification d'essai de conformité de la couche d'application électrique

Reference number
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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The main task of technical committees is to prepare International Standards. Draft International Standards adopted by the technical committees are circulated to the member bodies for voting. Publication as an International Standard requires approval by at least 75 % of the member bodies casting a vote.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights.

ISO 17458-5 was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 3, *Electrical and electronic equipment*.

ISO 17458 consists of the following parts, under the general title *Road vehicles — FlexRay communications system*:

— *Part 1: General information and use case definition*

— *Part 2: Data link layer specification*

— *Part 3: Data link layer conformance test specification*

— *Part 4: Electrical physical layer specification*

— *Part 5: Electrical physical layer conformance test specification*

Introduction

The FlexRay communications system is an automotive focused high speed network and was developed with several main objectives which were defined beyond the capabilities of established standardized bus systems like CAN and some other proprietary bus systems. Some of the basic characteristics of the FlexRay protocol are synchronous and asynchronous frame transfer, guaranteed frame latency and jitter during synchronous transfer, prioritization of frames during asynchronous transfer, single or multi-master clock synchronization, time synchronization across multiple networks, error detection and signalling, and scalable fault tolerance.

The FlexRay communications system is defined for advanced automotive control applications. It serves as a communication infrastructure for future generation high-speed control applications in vehicles by providing:

— A message exchange service that provides deterministic cycle based message transport;

— Synchronization service that provides a common time base to all nodes;

— Start-up service that provides an autonomous start-up procedure;

— Error management service that provides error handling and error signalling;

— Wakeup service that addresses the power management needs.

This bus system has been developed with several main objectives which were defined beyond the capabilities of existing bus systems like CAN and some other proprietary bus systems. This advanced automotive communication system specifies support for:

— Scalable static and dynamic message transmission (deterministic and flexible);

— High net data rate of 5 Mbit/sec; gross data rate approximately 10 Mbit/sec;

— Scalable fault-tolerance (single and dual channel);

— Error containment on the physical layer through an independent Bus Guardian;

— Fault tolerant clock synchronisation (global time base).

Since start of development the automotive industry world wide supported the specification development. The FlexRay communications system has been successfully implemented in production vehicles today.

The ISO 17458 series specifies the use cases, the communication protocol and physical layer requirements of an in-vehicle communication network called "FlexRay communications system".

This part of ISO 17458 has been established in order to define the use cases for vehicle communication systems implemented on a FlexRay data link.

To achieve this, it is based on the Open Systems Interconnection (OSI) Basic Reference Model specified in ISO/IEC 7498-1 [1] and ISO/IEC 10731 [6], which structures communication systems into seven layers. When mapped on this model, the protocol and physical layer requirements specified by ISO 17458 are broken into:

— Diagnostic services (layer 7), specified in ISO 14229-1 [7], ISO 14229-4 [9];

— Presentation layer (layer 6), vehicle manufacturer specific;

— Session layer services (layer 5), specified in ISO 14229-2 [8];

— Transport layer services (layer 4), specified in ISO 10681-2 [5];

— Network layer services (layer 3), specified in ISO 10681-2 [5];

— Data link layer (layer 2), specified in ISO 17458-2, ISO 17458-3;

— Physical layer (layer 1), specified in ISO 17458-4, ISO 17458-5;

in accordance with Table 1.

Table 1 — FlexRay communications system specifications applicable to the OSI layers

Applicability	OSI 7 layers	FlexRay communications system	Vehicle manufacturer enhanced diagnostics
Seven layer according to ISO 7498-1 and ISO/IEC 10731	Application (layer 7)	vehicle manufacturer specific	ISO 14229-1, ISO 14229-4
	Presentation (layer 6)	vehicle manufacturer specific	vehicle manufacturer specific
	Session (layer 5)	vehicle manufacturer specific	ISO 14229-2
	Transport (layer 4)	vehicle manufacturer specific	ISO 10681-2
	Network (layer 3)	vehicle manufacturer specific	
	Data link (layer 2)	ISO 17458-2, ISO 17458-3	
	Physical (layer 1)	ISO 17458-4, ISO 17458-5	

Table 1 shows ISO 17458 Parts 2 – 5 being the common standards for the OSI layers 1 and 2 for the FlexRay communications system and the vehicle manufacturer enhanced diagnostics.

The FlexRay communications system column shows vehicle manufacturer specific definitions for OSI layers 3 – 7.

The vehicle manufacturer enhanced diagnostics column shows application layer services covered by ISO 14229-4 which have been defined in compliance with diagnostic services established in ISO 14229-1, but are not limited to use only with them. ISO 14229-4 is also compatible with most diagnostic services defined in national standards or vehicle manufacturer's specifications. The presentation layer is defined vehicle manufacturer specific. The session layer services are covered by ISO 14229-2. The transport protocol and network layer services are specified in ISO 10681.

Road vehicles — FlexRay communications system — Part 5: Electrical physical layer conformance test specification

IMPORTANT — According to ISO 17458-4, the FlexRay communications system was specified focusing on a data rate of 10 Mbit/s. Therefore this conformance test specification regards the use of systems with a data rate of 10 Mbit/s only whereas the physical layer also works properly in systems with data rates in the range from 2,5 Mbit/s to 10 Mbit/s according to ISO 17458-4.

1 Scope

This part of ISO 17458 specifies the conformance test for the electrical physical layer of the FlexRay communications system.

This part of ISO 17458 defines a test that considers ISO 9646 and ISO 17458-4.

The purpose of this part of ISO 17458 is to provide a standardized way to verify whether FlexRay Bus Driver and Active Star products are compliant to ISO 17458-4. The primary motivation is to ensure a level of interoperability of FlexRay Bus Drivers and Active Stars from different sources in a system environment.

This part of ISO 17458 provides all necessary technical information to ensure that test results will be identical even on different test systems, provided that the particular test suite and the test system are compliant to the content of this part of ISO 17458.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 17458-1, *Road vehicles — FlexRay communications system — Part 1: General information and use case definition*

ISO 17458-2, *Road vehicles — FlexRay communications system — Part 2: Data link layer specification*

ISO 17458-4, *Road vehicles — FlexRay communications system — Part 4: Electrical physical layer specification*

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 17458-1, ISO 17458-2, ISO 17458-4 and the following apply.

3.1.1
bus driver – communication controller interface
BD-CC-interface
see "*BD-BD interface*" when replacing one *BD* by a *CC*

3.1.2
cable
term that summarises all necessary components to implement a FlexRay *transmission line*:
two twisted or untwisted wires to be connected to *BP* and *BM*, isolators to mount the wires, an optional shield, an optional wire to strengthen the shield, an optional sheath, etc.

3.1.3
communication controller – bus driver interface
CC-BD-interface
see "*BD-CC-interface*"

3.1.4
communication channel
FlexRay allows a single *CC* to distribute data-frames independent from each other on two different hardware paths or *topologies*. From an abstract view each path is named "*communication channel*".

3.2 Abbreviated terms

LT lower tester

UT upper tester

4 Document reference according to OSI model

Figure 1 depicts the FlexRay document reference according to OSI model.

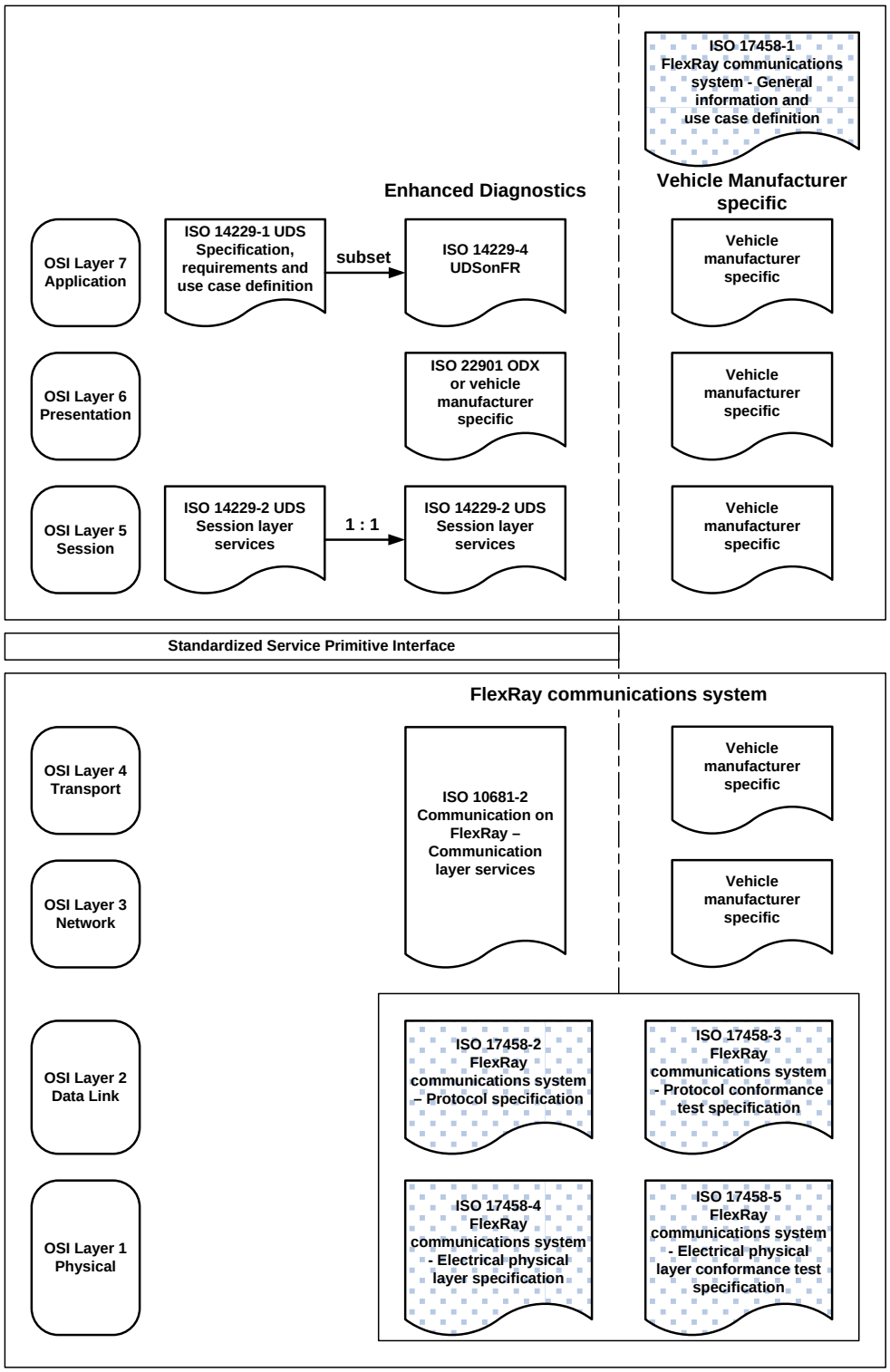


Figure 1 — FlexRay document reference according to OSI model

5 Conventions

5.1 General

ISO 17458, ISO 10681 and ISO 14229-4 are based on the conventions specified in the OSI Service Conventions (ISO/IEC 10731) as they apply for physical layer, protocol, network & transport protocol and diagnostic services.

5.2 Notational conventions

Notational conventions are listed in ISO 17458-4.

6 Test environment

6.1 Test case architecture

Each test case is specified with the following parts that must all be described unambiguous:

— Test case name
a name for this test case.

— Test purpose
a description of the motivation for this test case.

— Configuration
the state of the test environment for this test case.

— Preamble (setup state)
the steps to do before the specified test case could be executed.

— Test execution
the description of the execution of this test case.

— Postamble
the steps to do after the specified test case in order to have a defined state.

— Pass criteria
the criteria to judge the test result.

— Test instances
this is an optional part and contains test cases, that are summarised in tabular form because they are executed separately with only minor changes in comparison to the first test case within this group.

Every test case is independent from the other test cases.

Several test cases are performed with the presence of stress conditions in order to check the robustness of the IUT. These stress conditions are specified in detail in Clause 7.

The test parameters are FlexRay variables or constants that are defined in ISO 17458-4. These test parameters are specified in detail in Clause 8.

Every test case starts at the beginning of the preamble and ends after the postamble. There is no delay between the preamble and the test execution and between the test execution and the postamble.

The pass criteria are related only to the test execution.

Product specific items are not part of this International Standard.

6.2 Test method

6.2.1 General

The FlexRay BD has several interfaces, that are supplied by specified power supplies and stimuli and observed by external components (signal measurements). The requirements for those generators and signal measurements are specified in 6.5.

The interfaces of the BD are separated in two parts:

— Analog interface
bus (service provider) and supply pins.

— Digital interface
the pins for connecting the BD with the FlexRay protocol components.

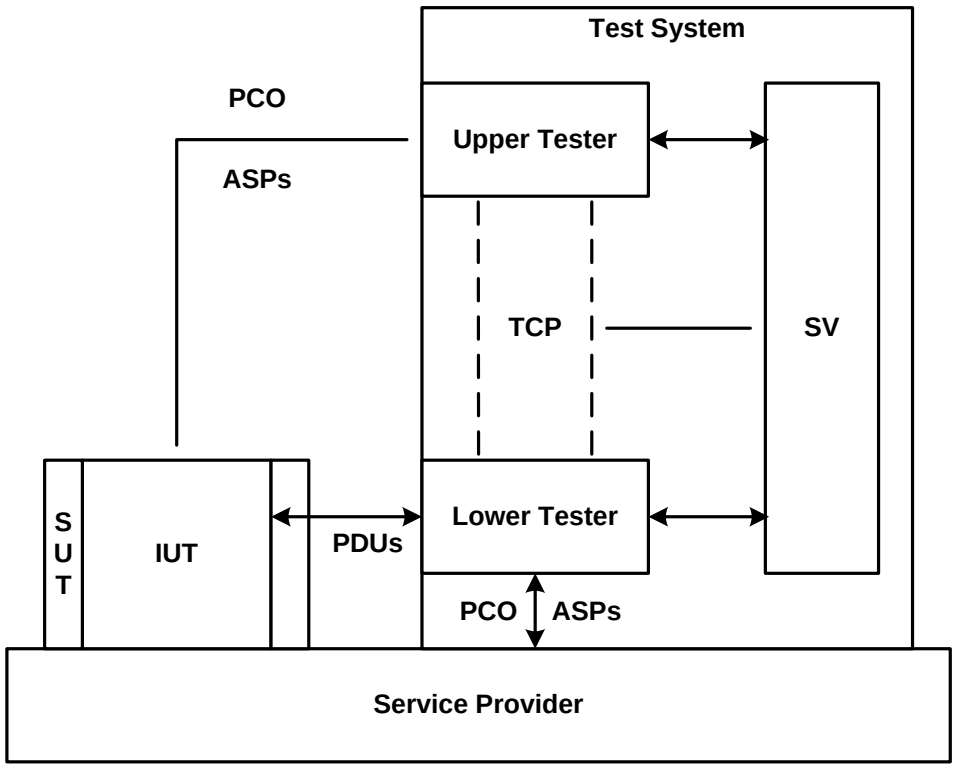
Each test case describes the used pins for supplying, stimulation and observation.

The used test method for the FlexRay PL regarding [2] is the local test method, see also Figure 2.

The local test method contains a Lower Tester (LT) for the analog interface (bus) and an Upper Tester (UT) for the digital interface. Both are part of the test system. The coordination of the test cases is done by the test coordination procedure (TCP).

The whole test is controlled by the supervisor (SV) that is also part of the test system. The SV controls the UT and LT with the TCP.

Figure 2 depicts the local test method of ISO 9646-1:1994.



Key

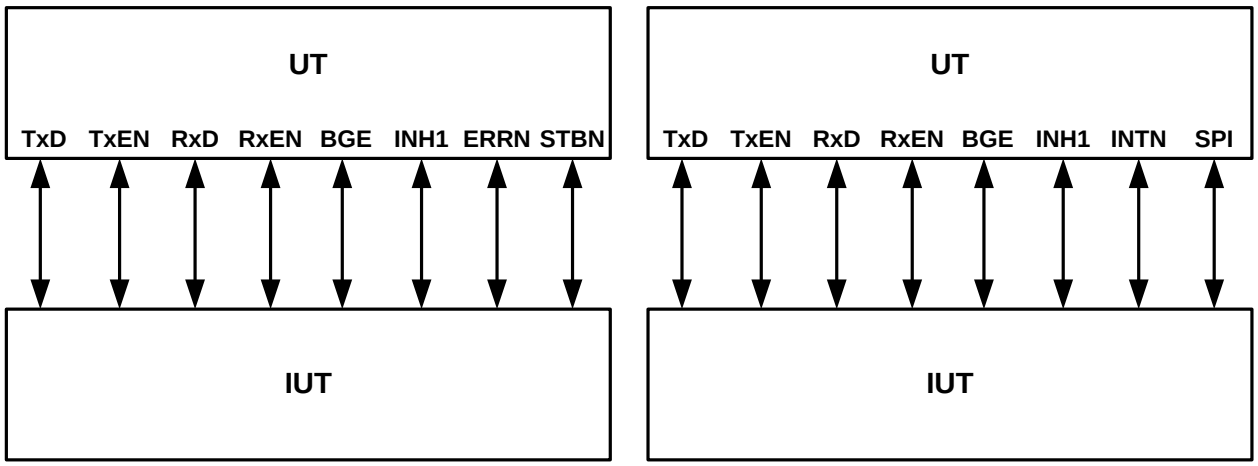
ASP	Abstract service primitive
IUT	Implementation under test
PCO	Point of control and observation
PDU	Prodocol data unit
SV	Supervisor
SUT	System under test
TCP	Test control procedure

Figure 2 — Local test method

6.2.2 Upper Tester

The UT has to provide test data, control and observe the IUT at its upper interface. The implementation has to keep in mind the possibility of two different host interfaces of the IUT as specified in ISO 17458-4.

Figure 3 shows the mandatory signals of the IUT that the conformance test considers:



a) Option A **b) Option B**

Components

IUT	Implementation Under Test
UT	Upper Tester

Connections and supplies

BGE	Bus guardian enable
ERRN	Error not
INH1	Inhibit 1
INTN	Inhibit n
RxD	Receive data
RxEN	Receive enable
SPI	Serial peripheral interface
STBN	Standby not
TxD	Transmit data
TxEN	Transmit enable not

Figure 3 — Upper Tester

The tasks of the UT are:

— Provide test data streams

— Change the mode of the IUT

— Observe and acquire the error line

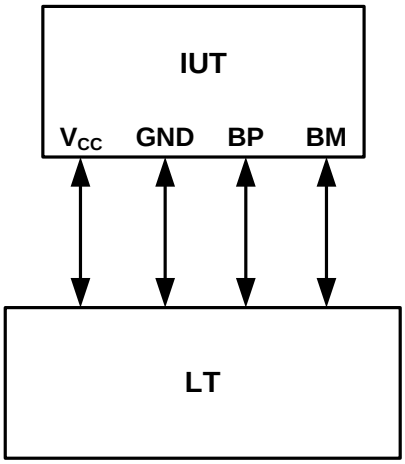
— Observe and acquire the received data stream

— Provide IUT functions to the supervisor

— Provide test system functionality to the IUT

6.2.3 Lower Tester

The Lower Tester has to provide data and observe the IUT at its lower interface – the supply and bus interface of the IUT. Figure 4 shows an overview of the Lower Tester.



Components		Connections and supplies	
IUT	Implementation Under Test	BM	Bus minus
LT	Lower Tester	BP	Bus plus
		GND	Ground connection
		V_{CC}	Supply voltage for digital signals

Figure 4 — Lower Tester

The tasks of the Lower Tester are:

— Generate and control bus failures

— Generate ground shift

— Control the supply voltages

— Provide IUT functions to the supervisor

— Provide test system functionality to the IUT

6.2.4 Supervisor

The SV has to control and observe the whole test system and communicates with the IUT via the LT and UT.

The tasks of the SV are:

— Control the LT and UT

— Observe and acquire the LT and UT

— Control and observe optional measurement devices

— Execute and coordinate test procedures

— Create the test report

6.3 Test environment

The following parameters are constants within the conformance test and used in the *standard environment*:

— Temperature: ambient

— Moisture: ambient

— Test topology: as described in 6.4

— Termination: as described in the test topology; differences are specified in the used test case

— Amount of nodes: as described in the test topology

— Amount of Stars: as described in the test topology

— Baud rate: 10 Mbit/s (gdBit = 100 ns) as part of the harmonized baud rates in the FlexRay consortium

— Common mode choke: as specified in 6.4.6

6.4 Test topology

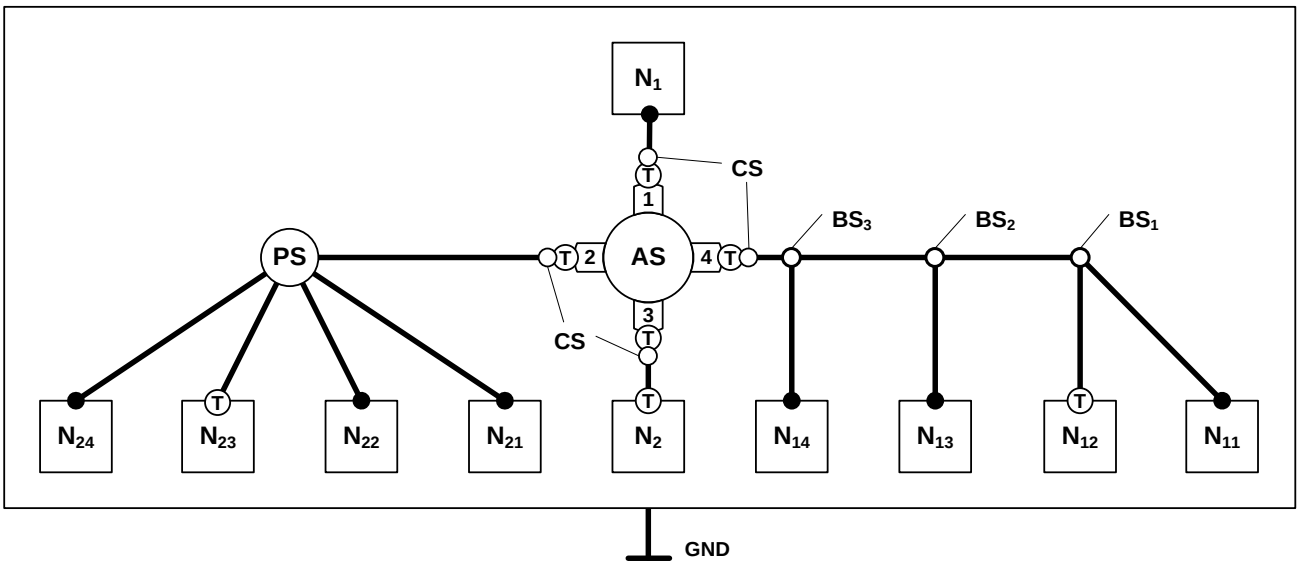
6.4.1 General

The purpose is to test the expected worst case of a possible topology with the maximum number of cascaded Active Stars, one passive star and one passive bus.

It is sufficient to test only with one physical channel, because the behaviour of the physical layer is independent from the number of used channels in a communication network.

The used test topology is described in the following subclauses and shown in Figure 5.

Figure 5 depicts the conformance test topology.



Components

AS	Active Star
BS_x	Bus splice x
CS	Cable shield connection
N_X	FlexRay node x
PS	Passive Star
T	Bus termination

Connections and supplies

GND	System ground

NOTE 1 V_{ANY} is not a supply voltage. It is a voltage used as stress condition where BP and BM are short-circuit to this voltage. V_{ANY} is product-specific and varies from the implementation of supply voltages of the IUT and the ground shift.

NOTE 2 Further details of the cable lengths used in the test topology are given in Table 2.

Figure 5 — Conformance test topology

Description of the test topology:

— For detailed description of the AS hardware see 6.4.7.

— A detailed description of the passive star hardware is given in 6.4.8.

— A detailed description of the passive bus hardware is given in 6.4.9.

— Nodes without ground shift stress shall be connected with their negative terminal to one of the ground splices that are mounted on the stainless steel chassis.

— The four ground splices shall be mounted near the nodes and the AS to consider the length of the GND cables of the nodes and the AS. The following nodes are connected to one of the GND splices:
GND splice 1: Nodes 11, 12, 13 and 14
GND splice 2: Nodes 21, 22, 23 and 24
GND splice 3: Nodes 1, 2 and the AS
GND splice 4: negative terminal of all supplies

— Nodes that are stressed with ground shift are connected to a switch[1)] that guarantees that these nodes could be connected directly to ground or are stressed by ground shift. This switch shall be controllable by the SV. The attenuation of the used switches shall be as small as possible. The switch shall be on the nodes and the AS. The connections from the switch to the terminals shall be as short as possible.

— The ground shift terminal of the nodes and the AS are connected to the positive terminal of the ground shift generator. The length of this cable is 1 m.

— The negative terminal of the ground shift generator is connected to the GND splice of the test system (chassis). The length of this cable is 1 m.

— All nodes shall be connected to the V_{BAT} splice (+) that is mounted on the chassis. The V_{BAT} splice is a separate board on which the splices for the supply voltages are placed.

— The AS shall be connected to the V_{BAT} splice (+) for the AS that is mounted on the chassis.

— The AS shall be connected to the V_{CC} splice (+) for the AS that is mounted on the chassis.

— The AS shall be connected to the V_{IO} splice (+) for the AS that is mounted on the chassis.

— The AS shall be connected to the V_{ANY} splice with a cable length of 3 m.

— Node 24 shall be connected to the V_{BAT} splice (+) for the node that is mounted on the chassis.

— Node 24 shall be connected to the V_{CC} splice (+) for the node that is mounted on the chassis.

— Node 24 shall be connected to the V_{IO} splice (+) for the node that is mounted on the chassis.

— Node 24 shall be connected to the V_{ANY} splice with a cable length of 3 m.

— Node 23 shall be connected to the V_{CC} splice (+) for the node that is mounted on the chassis.

— Node 23 shall be connected to the V_{IO} splice (+) for the node that is mounted on the chassis.

— Node 21 shall be connected to the V_{CC} splice (+) for the node that is mounted on the chassis.

— Node 21 shall be connected to the V_{IO} splice (+) for the node that is mounted on the chassis.

— The chassis shall be a steel plate for the ground connections of the IUTs and the power supply.

— The chassis is connected to the negative terminal of the power supply (clamp 31).

— The V_{BAT} splice is connected to the positive terminal of the power supply (clamp 30).

— The V_{BAT} splice for the nodes is connected to the positive terminal of the nodes V_{BAT} power supply.

— The V_{BAT} splice for the AS is connected to the positive terminal of the AS V_{BAT} power supply.

— The V_{CC} splice for the AS is connected to the positive terminal of the first +5 V power supply.

— The V_{BAT} splice for the node 24 is connected to the positive terminal of the V_{BAT} power supply for node 24.

1) The switch shall be on the nodes and the AS. The connections from the switch to the terminals shall be as short as possible.

— The V_{CC} splice for the node 24 is connected to the positive terminal of the second +5 V power supply.

— The V_{IO} splice for the node 24 is connected to the positive terminal of the V_{IO} reference voltage.

— All communication channels shall be terminated regarding ISO 17458-4.

— The shield of every link shall be terminated regarding ISO 17458-4.

— The bus cables shall meet the requirements of ISO 17458-4; see also 6.4.10.1. All bus cables are shielded. The shield is only connected at the AS (see also 6.4.3).

— The supply cables shall meet the requirements specified in 6.4.10.2.

The following topics are part of the implementation of the conformance test, but have to meet ISO 17458-4:

— the type of mounting of the IUTs on the chassis

— the type and manufacturer of the cables

— the type and manufacturer of the connectors

— the type of the splices

— the wiring of the IUT

6.4.2 Cable overview of the test topology

Table 2 gives a full overview of the cables of the test topology

Table 2 — Cable overview of test topology

No.	Type	From	To	Length m	Termination	Remarks
1	Bus wire	Node 1	Active Star	1	Both ends	—
2	Ground wire	Node 1	GND splice 3	0,5	—	—
3	Supply wire	Node 1	V_{BAT} splice	2	—	—
4	Bus wire	Node 2	Active Star	3,5	Both ends	—
5	Ground wire	Node 2	GND splice 3	5	—	This node emulates an ECU in a roof of a vehicle where no ground splice in the roof is available.
6	Supply wire	Node 2	V_{BAT} splice	6	—	—
7	Bus wire	Node 11	Bus splice 1	0,3	No termination	Part of the passive bus
8	Ground wire	Node 11	GND splice 1	0,5	—	—
9	Supply wire	Node 11	V_{BAT} splice	6	—	—
10	Bus wire	Node 12	Bus splice 1	0,3	Only at node 12	Part of the passive bus

No.	Type	From	To	Length m	Termination	Remarks
11	Ground wire	Node 12	GND splice 1	0,5	—	—
12	Supply wire	Node 12	V_{BAT} splice	8	—	—
13	Bus wire	Node 13	Bus splice 2	0,3	No termination	Part of the passive bus
14	Ground wire	Node 13	GND splice 1	0,5	—	—
15	Supply wire	Node 13	V_{BAT} splice	9	—	—
16	Bus wire	Node 14	Bus splice 3	0,3	No termination	Part of the passive bus
17	Ground wire	Node 14	GND splice 1	0,5	—	—
18	Supply wire	Node 14	V_{BAT} splice	10	—	—
19	Bus wire	Node 21	Passive star	0,25	No termination	Connected to the passive star
20	Ground wire	Node 21	GND splice 2	0,5	—	—
21	Supply wire	Node 21	V_{BAT} splice	4	—	—
22	Bus wire	Node 22	Passive star	0,25	No termination	Connected to the passive star
23	Ground wire	Node 22	GND splice 2	0,5	—	—
24	Supply wire	Node 22	V_{BAT} splice	3	—	—
25	Bus wire	Node 23	Passive star	1	Only at node 23	Connected to the passive star
26	Ground wire	Node 23	GND splice 2	0,5	—	—
27	Supply wire	Node 23	V_{BAT} splice	5	—	—
28	Ground shift wire [a]	V_{GS} supply	Node 23	2	—	Connected to positive terminal
29	Ground shift wire [b]	V_{GS} supply	GND splice 4	1	—	Connected to negative terminal (ground wire of node 23)
30	Bus wire	Node 24	Passive star	0,25	No termination	Connected to the passive star
31	Ground wire	Node 24	GND splice 2	0,5	—	—
32	Supply wire	Node 24	V_{BAT} splice	4	—	—
33	Ground shift wire [a]	V_{GS} supply	Node 24	2	—	Connected to positive terminal
34	Ground shift wire [b]	V_{GS} supply	GND splice 4	1	—	Connected to negative terminal (ground wire of node 24)

No.	Type	From	To	Length m	Termination	Remarks
35	Ground wire	Active Star	GND splice 2	0,5	—	—
36	Supply wire	Active Star	V_{BAT} splice	4	—	—
37	Supply wire	Active Star	V_{CC} splice	4	—	—
38	Bus wire	Active Star	Passive star	11	Only at Active Star	—
39	Bus Wire	Active Star	Bus splice 3	1,5	Only at Active Star	—
40	Ground shift wire [a]	V_{GS} supply	Active Star	2	—	Connected to positive terminal
41	Ground shift wire [b]	V_{GS} supply	GND splice 4	1	—	Connected to negative terminal (ground wire of AS)
42	Bus wire	Bus splice 1	Bus splice 2	10	No termination	Part of the passive bus
43	Bus wire	Bus splice 2	Bus splice 3	0,15	No termination	Part of the passive bus
44	Supply wire	Battery	V_{BAT} splice	3	—	V_{BAT} supply for nodes
45	Ground wire	Battery	GND splice 4	1,5	—	V_{BAT} supply for nodes
46	Supply wire	Battery	V_{BAT} splice	3	—	V_{BAT} supply for AS
47	Ground wire	Battery	GND splice 4	1,5	—	V_{BAT} supply for AS
48	Supply wire	V_{CC} Supply	V_{CC} splice	3	—	V_{CC} supply for AS
49	Ground wire	V_{CC} Supply	GND splice 4	1,5	—	V_{CC} supply for AS
50	Supply wire	V_{IO} Supply	V_{CC} splice	4	—	V_{IO} supply for AS
51	Ground wire	V_{IO} Supply	GND splice 4	1,5	—	V_{IO} supply for AS
52	Supply wire	Battery	V_{BAT} splice	4	—	V_{BAT} supply for node 24
53	Ground wire	Battery	GND splice 4	1,5	—	V_{BAT} supply for node 24
54	Supply wire	V_{CC} Supply	V_{CC} splice	4	—	V_{CC} supply for node 21, 23 & 24
55	Ground wire	V_{CC} Supply	GND splice 4	1,5	—	V_{CC} supply for node 21, 23 & 24
56	Supply wire	V_{IO} Supply	V_{IO}splice	4	—	V_{IO} supply for node 21, 23 & 24
57	Ground wire	V_{IO} Supply	GND splice 4	1,5	—	V_{IO} supply for node 21, 23 & 24
58	Ground wire	Passive star	GND splice 2	0,3	—	Ground connection of PS

No.	Type	From	To	Length m	Termination	Remarks
59	Stress wire	V_{any} supply	Node 24	3	—	Stress voltage for node 24
60	Stress wire	V_{any} supply	Active Star	3	—	Stress voltage for AS
61	Bus wire	Node 1	Active Star	1	Both ends	—
62	Ground wire	Node 1	GND splice 3	0,5	—	—
63	Supply wire	Node 1	Battery splice	2	—	—
64	Bus wire	Node 2	Active Star	3,5	Both ends	—
65	Ground wire	Node 2	GND splice 3	5	—	—
66	Supply wire	Node 2	Battery splice	6	—	—
67	Bus wire	Node 11	Bus splice 1	0,3	No termination	Part of the passive bus
68	Ground wire	Node 11	GND splice 1	0,5	—	—
69	Supply wire	Node 11	Battery splice	6	—	—
70	Bus wire	Node 12	Bus splice 1	0,3	Only at node 12	Part of the passive bus
71	Ground wire	Node 12	GND splice 1	0,5	—	—
72	Supply wire	Node 12	Battery splice	8	—	—
73	Bus wire	Node 13	Bus splice 2	0,3	No termination	Part of the passive bus
74	Ground wire	Node 13	GND splice 1	0,5	—	—
75	Supply wire	Node 13	Battery splice	9	—	—
76	Bus wire	Node 14	Bus splice 3	0,3	No termination	Part of the passive bus
77	Ground wire	Node 14	GND splice 1	0,5	—	—
78	Supply wire	Node 14	Battery splice	10	—	—
79	Bus wire	Node 21	Passive star	0,25	No termination	Connected to the passive star
80	Ground wire	Node 21	GND splice 2	0,5	—	—
81	Supply wire	Node 21	Battery splice	4	—	—

No.	Type	From	To	Length m	Termination	Remarks
82	Bus wire	Node 22	Passive star	0,25	No termination	Connected to the passive star
83	Ground wire	Node 22	GND splice 2	0,5	—	—
84	Supply wire	Node 22	Battery splice	3	—	—
85	Bus wire	Node 23	Passive star	1	Only at node 23	Connected to the passive star
86	Ground wire	Node 23	GND splice 2	0,5	—	—
87	Supply wire	Node 23	Battery splice	5	—	—
88	Ground shift wire [a]	V_{GS} supply	Node 23	2	—	Connected to positive terminal
89	Ground shift wire [b]	V_{GS} supply	GND splice 4	1	—	Connected to negative terminal (ground wire of node 23)
90	Bus wire	Node 24	Passive star	0,25	No termination	Connected to the passive star
91	Ground wire	Node 24	GND splice 2	0,5	—	—
92	Supply wire	Node 24	Battery splice	4	—	—
93	Ground shift wire [a]	V_{GS} supply	Node 24	2	—	Connected to positive terminal
94	Ground shift wire [b]	V_{GS} supply	GND splice 4	1	—	Connected to negative terminal (ground wire of node 24)
95	Ground wire	Active Star	GND splice 2	0,5	—	—
96	Supply wire	Active Star	V_{BAT} splice	4	—	—
97	Supply wire	Active Star	V_{CC} splice	4	—	—
98	Bus wire	Active Star	Passive star	11	Only at Active Star	—
99	Bus Wire	Active Star	Bus splice 3	1,5	Only at Active Star	—
100	Ground shift wire [a]	V_{GS} supply	Active Star	2	—	Connected to positive terminal
101	Ground shift wire [b]	V_{GS} supply	GND splice 4	1	—	Connected to negative terminal (ground wire of AS)
102	Bus wire	Bus splice 1	Bus splice 2	10	No termination	Part of the passive bus
103	Bus wire	Bus splice 2	Bus splice 3	0,15	No termination	Part of the passive bus
104	Supply wire	Battery	Battery splice	3	—	V_{BAT} supply for nodes

No.	Type	From	To	Length m	Termination	Remarks
105	Ground wire	Battery	GND splice 4	1,5	—	V_{BAT} supply for nodes
106	Supply wire	Battery	Battery splice	3	—	V_{BAT} supply for AS
107	Ground wire	Battery	GND splice 4	1,5	—	V_{BAT} supply for AS
108	Supply wire	V_{CC} Supply	V_{CC} splice	3	—	V_{CC} supply for AS
109	Ground wire	V_{CC} Supply	GND splice 4	1,5	—	V_{CC} supply for AS
110	Supply wire	V_{IO} Supply	V_{CC} splice	4	—	V_{IO} supply for AS
111	Ground wire	V_{IO} Supply	GND splice 4	1,5	—	V_{IO} supply for AS
112	Supply wire	Battery	Battery splice	4	—	V_{BAT} supply for node 24
113	Ground wire	Battery	GND splice 4	1,5	—	V_{BAT} supply for node 24
114	Supply wire	V_{CC} Supply	V_{CC} splice	4	—	V_{CC} supply for node 21 & 24
115	Ground wire	V_{CC} Supply	GND splice 4	1,5	—	V_{CC} supply for node 21 & 24
116	Supply wire	V_{IO} Supply	V_{IO}splice	4	—	V_{IO} supply for node 21 & 24
117	Ground wire	V_{IO} Supply	GND splice 4	1,5	—	V_{IO} supply for node 21 & 24
118	Ground wire	Passive star	GND splice 2	0,3	—	Ground connection of PS
119	Stress wire	V_{any} supply	Node 24	3	—	Stress voltage for node 24
120	Stress wire	V_{any} supply	Active Star	3	—	Stress voltage for AS

[a] Positive terminal of the Ground Shift Generator

[b] Negative terminal of the Ground Shift Generator

6.4.3 Shield

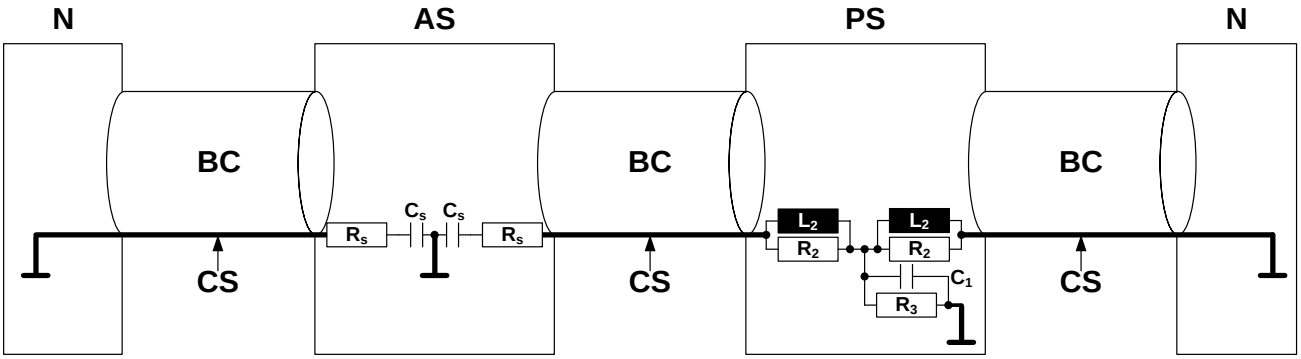
Each communication link shall have one cable shield connection. The conformance test uses one Active Star, that is the central point of shield connection in the topology.

Table 3 defines the specified shield connection with bus cable, connectors, Active Star and node:

Table 3 — Shield connection components

Name	Description	Typ	Unit
R_S	Damping resistance	1 000	Ω
	Tolerance	1	%
C_S	Capacitance	470	nF
	Tolerance	10	%
L_2, R_2, R_3 and C_1	Components of the passive star, see 6.4.8.		

Figure 6 depicts the cable shield connection.



Components

AS	Active Star
BC	Bus cable
CS	Cable shield
C_1	Capacitor of the Passive Star (see Table 3)
C_S	Capacitor of the Active Star (see Table 3)
L_2	Inductor of the Passive Star
N	FlexRay node
PS	Passive Star
R_1	Resistor of the Passive Star (see Table 3)
R_2	Resistor of the Passive Star (see Table 3)
R_3	Resistor of the Passive Star (see Table 3)
R_S	Resistor of the Active Star (see Table 3)

Figure 6 — Cable shield connection

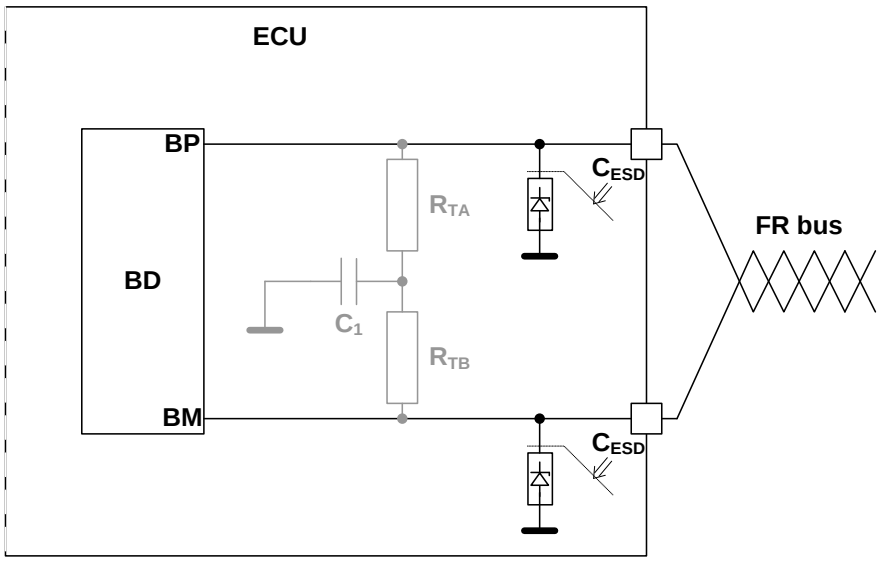
The cable shield of each branch at the PS is connected via L_2 and R_2 to C_1 and R_3 to the local ground of the PS, see 6.4.8.

The shield shall be interrupted between the housings of the Active Star, N23 and N24 due to ground shift condition at those nodes.

The shield shall not be interrupted between the housings of N1, N2, N11-14, N21 and N22, because those nodes have no ground shift condition.

6.4.4 ESD protection

An ESD protection element shall be connected to each BD and each connected branch of AS in order to increase ESD protection capabilities. The implemented protection device shall not exceed the maximum rating (see Figure 7).



Components

BD	Bus Driver
C_1	Termination capacitor
C_{ESD}	Capacitor between BP/BM and GND
ECU	Electronic Control Unit
R_{TA}	Termination resistor towards BP
R_{TB}	Termination resistor towards BM

Connections and supplies

BM	Bus minus
BP	Bus plus

Figure 7 — ESD load circuit

Table 4 defines the ESD load circuit.

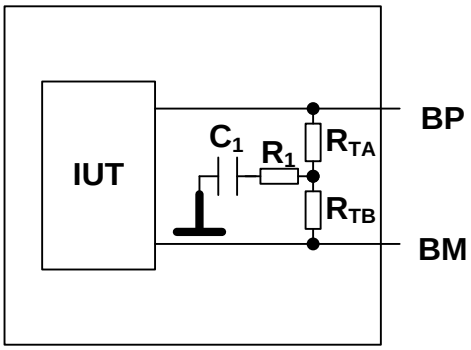
Table 4 — ESD load circuit

Name	Description	Max	Unit
C_{ESD}	Capacitance of BP/BM to GND	20	pF
	Tolerance; NP0 dielectric	1	%

As described in Figure 7 the ESD load circuit is placed on the board between the termination and the bus terminals. If no termination exist the ESD load circuit is placed between the CMC and the bus terminals.

6.4.5 Termination

Each terminated node and star as described in the test topology shall have a split termination as shown in Figure 8. Node 2 is an example of a terminated node (see Figure 5).



Components

C_1	Termination capacitor
IUT	Implementation Under Test
R_1	Termination resistor
R_{TA}	Termination resistor towards BP
R_{TB}	Termination resistor towards BM

Connections and supplies

BP	Bus plus
BM	Bus minus

Figure 8 — Terminated node

The *RDCLoad* is specified in ISO 17458-4. For the nominal (default) *RDCLoad* the termination resistor, as specified in ISO 17458-4, is defined as follows:

$$R_T = R_{TA} + R_{TB}$$

where

R_T is the resulting termination resistor

R_{TA} is the termination resistor connected to BP

R_{TA} is the termination resistor connected to BM

Table 5 lists the values of the split termination components.

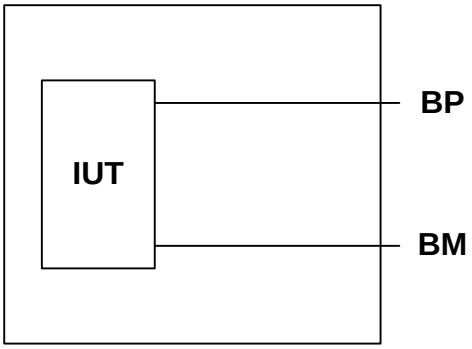
Table 5 — Split termination components

Name	Description	Typ	Unit
R_{TA}	Resistor of split termination	$\frac{Z_0}{2}$ [a]	Ω
	Tolerance	1	%
R_{TB}	Resistor of split termination	$\frac{Z_0}{2}$ [a]	Ω
	Tolerance	1	%
R_1	Resistor	5	Ω
	Tolerance	1	%
C_1	Ceramic capacitor	4,7	nF
	Tolerance	10	%
[a] Z_0: characteristic impedance of the used cable. See also 6.4.10.1.			

The value of Z_0 depends on the used bus cable. This cable is defined in 6.4.10.1.

Some nodes in the test topology have no termination. Node 14 is an example of an unterminated node (see Figure 5).

Figure 9 shows the bus connection of an unterminated node.



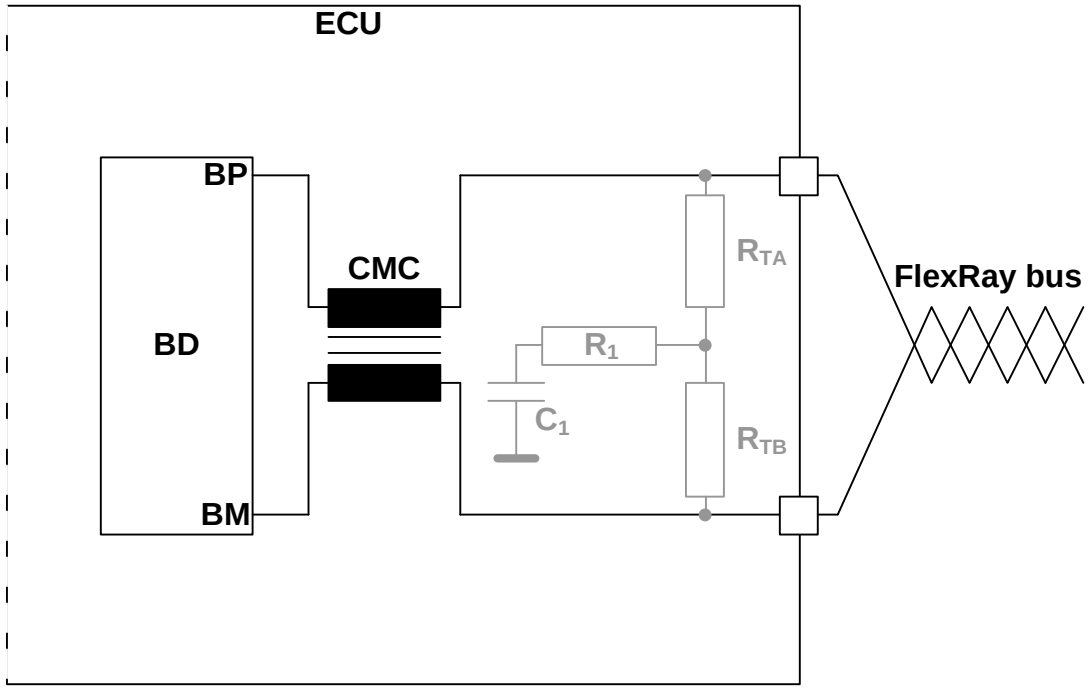
Components		**Connections and supplies**	
IUT	Implementation Under Test	BM	Bus minus
		BP	Bus plus

Figure 9 — Unterminated node

NOTE According to [12], all non-terminated nodes should have a high-ohmic split termination (e.g. 2 x 1 300 Ω + 4,7 nF).

6.4.6 Common mode chokes

Common mode chokes shall be used within the conformance testing of Bus Drivers as depicted in Figure 10.



Components		Connections and supplies	
BD	Bus Driver	BM	Bus minus
ECU	Electronic Control Unit	BP	Bus plus
R_1	Termination resistor	CMC	Common Mode Choke
R_{TA}	Termination resistor towards BP	C_1	Termination capacitor
R_{TB}	Termination resistor towards BM		

Figure 10 — Common mode choke implementation

As described in Figure 10, the CMC is placed on the board between the IUT and the termination. If no termination exist the CMC is placed between the IUT and the ESD protection circuit.

— The manufacturer[2)] of the CMC is: Epcos

— The type of the CMC is: B82789C0104N002 (bifilar winding)

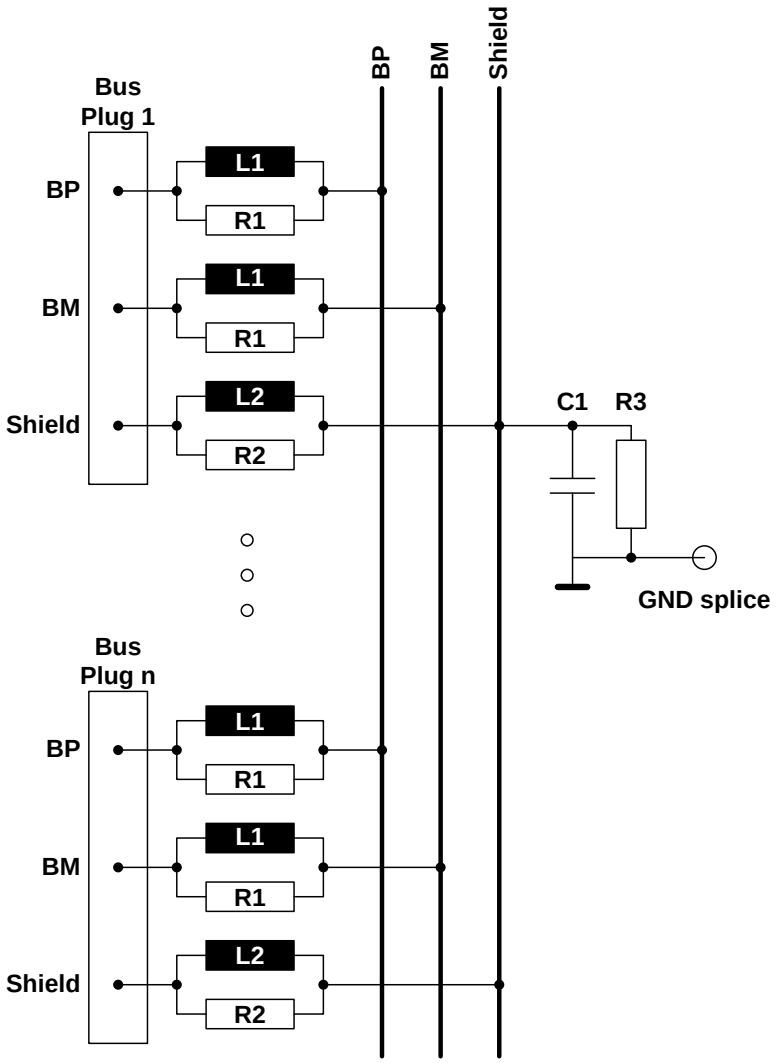
6.4.7 Active Star

The conformance test specification does not prescribe a certain implementation of the AS. This depends on the device specification of the IUT.

2) The suggested CMC is supplied by Epcos. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

6.4.8 Passive star

The passive star shall be implemented as depicted in Figure 11.



Components

C1	(see Table 6)
L1	(see Table 6)
L2	(see Table 6)
R1	(see Table 6)
R2	(see Table 6)
R3	(see Table 6)

Connections and supplies

BM	Bus minus
BP	Bus plus
Bus plug [1..n]	Generic node connector
GND splice	Connection to system ground
Shield	Cable shield

Figure 11 — Passive star implementation

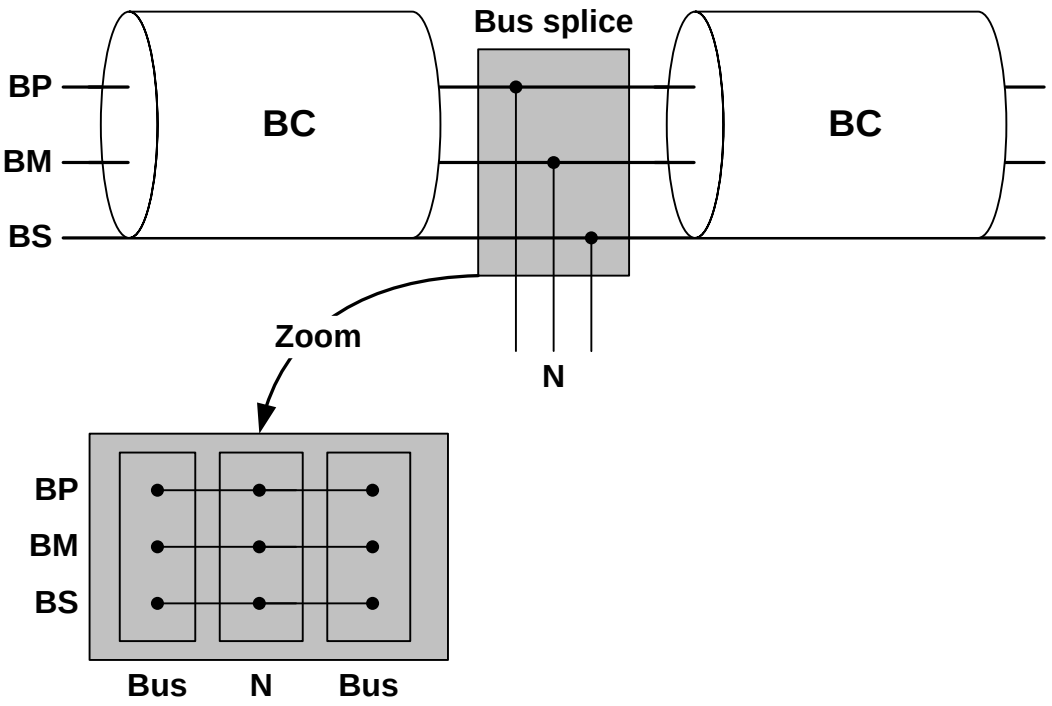
Table 6 lists the parameters of the passive star implementation.

Table 6 — Passive star implementation

Name	Description	Value	Unit
R_1	Series resistance on signal wire	22	Ω
	Tolerance	1	%
L_1	Series inductance on signal wire	220	nH
	Tolerance	10	%
R_2	Series resistance on signal wire	100	Ω
	Tolerance	1	%
L_2	Series inductance on signal wire	220	nH
	Tolerance	10	%
R_3	Inductance of shield to system ground	1	MΩ
	Tolerance	1	%
C_1	Capacitance to system ground	100	nF
	Tolerance	10	%
NOTE The ground of the passive star is connected to GND splice 2 with a ground wire of 0,1 m length.			

6.4.9 Passive bus

The passive bus shall be implemented as depicted in Figure 12.



Components

BC	Bus cable
BS	Bus shield

Connections and supplies

BM	Bus minus
BP	Bus plus
N	FlexRay node connection

Figure 12 — Passive bus implementation

The plugs shall be realized with 9 pin Sub-D connectors mounted on a small board. The wires between the connectors shall be as short as possible.

6.4.10 Cables

6.4.10.1 Bus Cables

The used bus cables in the conformance test shall have a shield and require the conditions listed in Table 7.

Table 7 — Bus cable impedance

Name	Description	Value	Tolerance	Unit
Z_0	Differential mode impedance at 10 MHz	90	± 2 %	Ω

Table 8 — Bus cable characteristics

Name	Description	Min	Max	Unit
T'_0	Specific line delay	—	10	ns/m
$\alpha_{5\ MHz}$	Cable attenuation at 5 MHz	—	82	dB/km
$lStubDistance_{M,N}$	Distance between two network splices	150	—	mm

See further recommendations about bus cables in the application notes of ISO 17458-4.

EXAMPLE bus cable:

— Cable manufacturer[3]: Gebauer & Griller

— Cable type: xF8FF_2_B56_FIM02YHBY

6.4.10.2 Power supply cables

The used cables in the conformance test shall require the following conditions:

Table 9 — Supply cable characteristics

Name	Description	Min	Max	Unit
$A_{Cross\ section}$	Cross section of GND and power supply wires	1,5	—	mm^2

EXAMPLE supply cable:

— Supply cable manufacturer[4]: Coroplast

— Supply cable type: FLRY-A 2,5

6.4.11 Connectors

The used connectors in the conformance test shall require the conditions listed in Table 10.

3) The suggested bus cables are supplied by Gebauer & Griller. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

4) The suggested power supply cables are supplied by Coroplast. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

Table 10 — Connectors characteristics

Name	Description	Min	Max	Unit
$R_{DCContact}$	Contact resistance (including crimps)	—	50	mΩ
$Z_{Connector}$	Impedance of connector	70	200	Ω
$l_{Coupling}$	Length coupling connection[a]	—	150	mm
$d_{ContactInterruption}$	Contact interruption; $R_{DCContact} > 1\Omega$ [b]	—	100	ns
[a] To be measured from end to end of untwisted area in the connected cables				
[b] The time limit reflects the state of the art measurements techniques and potentially needs to be lower				

See further recommendations about connectors in the application notes of ISO 17458-4.

An example for a connector is:

— Connector manufacturer[5]: Erni

— Connector type: Sub-D 9 pin

6.5 Test equipment

6.5.1 General

In every test case the accuracy and the resolution of each generator and measurement device shall be taken into account.

INH1 is floating while the IUT is in sleep mode and is pulled to V_{BAT} level while the IUT is not in a sleep mode. A pull down resistor shall be used to force a floating INH1 output to ground.

The logical level of the optional signal INH1 shall be interpreted as:

— Logical High: $uINH1 > uV_{BAT} - 1$ V while $uV_{BAT} \geq 5{,}5$ V

— Logical Low: $uINH1 < uV_{BAT} - 1$ V while $uV_{BAT} \geq 5{,}5$ V

6.5.2 Power supply V_{BAT}

The power supply shall be connected with the negative terminal to the chassis of the test system (that is connected to the ground pin) and with the positive terminal to the V_{BAT} splice of the communication network. This supply simulates a battery in an automotive environment.

The default voltage of V_{BAT} is the maximal battery operational range defined in the data sheet of the IUT up to +42 V.

Alternatively, for some test cases, the IUT is powered by a low battery generator as defined in 6.5.6 instead.

5) The suggested connectors are supplied by Erni. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

Table 11 lists the power supply characteristics for V_{BAT}.

Table 11 — V_{BAT} power supply characteristics

Output	Description	Min	Max	Unit
V_{BAT}	Supply voltage DC	0	+50	V
	I_{min}	5	—	A

EXAMPLE

— Supply manufacturer[6]: Toellner

— Supply type: 8805-64

Used voltages of V_{BAT}: $V_{BATUndervoltage}$, +5,5 V…+42 V

All nodes shall support to be supplied independently by extra V_{BAT} power supplies.

Nodes 21, 23 and 24 shall support to be supplied independently by extra V_{CC} and V_{IO} power supplies.

The Active Star shall support to be supplied independently by extra V_{BAT}, V_{CC} and V_{IO} power supplies.

6.5.3 Power supply V_{CC}

The power supply shall be connected with the negative terminal to the chassis of the test system (that is connected to the ground pin) and with the positive terminal to the V_{CC} splice of the communication network. This supply simulates the voltage regulator inside an Active Star or a node in an automotive environment.

The default voltage of V_{CC} is +5,0 V. Table 12 lists the power supply characteristics of V_{CC}.

Table 12 — V_{CC} power supply characteristics

Output	Description	Min	Max	Unit
V_{CC}	Supply voltage DC	0	+5,05	V
	I_{min}	0,7	—	A

EXAMPLE

— Supply manufacturer[7]: Toellner

— Supply type: 8842-32

The V_{CC} on the nodes shall be generated by local voltage regulators and are not independent from V_{BAT}.

Used voltages of V_{CC}: +5,0 V (normal), $V_{CCUndervoltage}$.

6) The suggested power supplies are supplied by Toellner. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

7) The suggested power supplies are supplied by Toellner. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

Node 21, 23, Node 24 and the AS shall be supplied independently by an extra V_{CC} power supply.

6.5.4 Reference voltage V_{IO}

The reference voltage supply shall be connected with the negative terminal to the chassis of the test system (that is connected to the ground pin) and with the positive terminal to the V_{IO} splice of the communication network. This reference voltage supply simulates the voltage regulator inside a node in an automotive environment.

The default voltage of V_{IO} depends on the I/O voltage of the devices counterpart, i.e. the host. Table 13 lists the reference voltage characteristics of V_{IO}.

Table 13 — V_{IO} reference voltage characteristics

Output	Description	Min	Max	Unit
V_{IO}	Supply voltage DC	0	+5,05	V
	I_{min}	0,7	—	A

EXAMPLE

— Supply manufacturer[8]: Toellner

— Supply type: TOE 8840

The V_{IO} on the nodes shall be generated by local voltage regulators and are not independent from V_{BAT}.

Standard voltage of V_{IO}: depends on implementation.

Undervoltage of V_{IO}: $V_{IOUndervoltage}$.

Node 21, 23, 24 and the Active Star shall be supplied independently by an extra V_{IO} reference voltage.

The logical high level of the digital signal is specified in ISO 17458-4.

6.5.5 Ground shift generator

This generator is used to simulate ground shift between selected nodes and stars of a communication network. It is connected between the predefined ground pin of the node or star and the chassis of the test system (ground connection of the power supply).

Table 14 lists the characteristics of the ground shift generator.

Table 14 — Ground shift generator characteristics

Output	Description	Min	Max	Unit
U_{GS}	Ground shift voltage DC	-5	+5	V
	I_{min}	0,8	—	A

8) The suggested power supplies are supplied by Toellner. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

EXAMPLE

— Supply manufacturer[9]: Kepco

— Supply type: BOP 20-10 M

For the ground shift generator, a sink shall be implemented, e.g. in kind of a two-quadrant power supply.

6.5.6 Low battery generator

This generator is used to simulate a low battery voltage that appears when turning on the starter circuit. The power supply shall be connected with the negative terminal to the chassis (that is connected to the ground pin) and with the positive terminal to the V_{BAT} splice of the communication network. This supply may be the same as specified in 6.5.2 and depends on the test case.

The IUTs are supplied by either this low battery generator or a battery power supply as defined in 6.5.2.

The test signal is defined in ISO 7637-1:2002.

Table 15 lists the characteristics of the low battery generator.

Table 15 — Low battery generator characteristics

Output	Description	Min	Max	Unit
V_{BAT}	Low battery voltage DC	0	+50	V
	Imin	5	—	A

EXAMPLE

— Supply manufacturer[10]: Toellner

— Supply type: 8842-64

6.5.7 Signal generator

The signal generator is connected to TxD, TxEN and BGE[11] of the Bus Driver and its ground pin. The generator is used to provide various test patterns, that are described in the test case clauses below.

Table 16 lists the characteristics of the signal generator.

9) The suggested ground shift generator is supplied by Kepco. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

10) The suggested low battery generator is supplied by Toellner. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

11) Only if this signal is available.

Table 16 — Signal generator characteristics

Output	Description	Min	Max	Unit
U_{TxD}	Bit time in test pattern	70	—	ns
	Voltage level of test pattern for digital input	0	5	V
	I_{min}	10	—	mA
	Sum of rise and fall time of signal at digital input of IUT with a 25 nF load	—	9	ns

EXAMPLE generator

Generator manufacturer[12]: Agilent

Generator type: 16720A

6.5.8 Analog signal measurement

The characteristics of the measurement device are described in this subclause. This may be an oscilloscope or equivalent device.

Table 17 lists the characteristics of the analog measurement device.

Table 17 — Analog measurement device characteristics

Input	Description	Min	Max	Unit
U_x	Voltage level of analog test signals	0	14	V
C_x	Input capacitance of probe	—	10	pF
R_x	Input resistance	1	—	MΩ
	Sample Rate	800	—	MSa/s
	Bandwidth	200	—	MHz

EXAMPLE oscilloscope

— Oscilloscope manufacturer[13]: LeCroy

— Oscilloscope type: Waverunner 6050

6.5.9 Digital signal measurement

The characteristics of the measurement device are described in this subclause. This shall be a logic analyzer or equivalent device.

12) The suggested signal generator is supplied by Agilent. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

13) The suggested oscilloscope is supplied by LeCroy. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

Table 18 lists the characteristics of the digital measurement device.

Table 18 — Digital measurement device characteristics

Input	Description	Min	Max	Unit
U_x	Voltage level of digital test signals	-5	5	V
	Bandwidth	2	—	GHz
C_x	Capacitance load	—	10	pF
R_x	Resistive load	0,1	—	MΩ
	Number of channels	96	—	—
	Timing sample rate (full channel mode)	2	—	ns
	Threshold	—	50 % of U_x	—

EXAMPLE logic analyzer

— Logic analyzer manufacturer[14]: Agilent

— Logic analyzer type: 16911A

6.5.10 Data acquisition unit

The characteristics of the measurement device are described in this subclause. This shall be a unit for measuring voltages or currents.

Table 19 lists the characteristics of the data acquisition unit.

Table 19 — Data acquisition unit

Input	Description	Min	Max	Unit
Ux	Absolute input voltage	-5	5	V
Ix	Absolute input current	-1	1	A
	Number of channels	2	—	—
	Timing sample rate (full channel mode)	600	—	S/s

EXAMPLE data acquisition unit

— Data acquisition unit manufacturer[15]: Agilent

— Data acquisition unit type: 34970A

14) The suggested logic analyzer is supplied by Agilent. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

15) The suggested data acquisition unit is supplied by Agilent. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

6.5.11 Broadband amplifier

The characteristics of this generator are described in this subclause. This device is necessary for dynamic ground shift.

Table 20 lists the characteristics of the broadband amplifier.

Table 20 — Broadband amplifier

Output	Description	Min	Max	Unit
U_x	Absolute output voltage	0	10	V
	Gain	—	13	dB
	I_{min}	1	—	A

EXAMPLE broadband amplifier

— Broadband amplifier manufacturer[16]: Toellner

— Broadband amplifier type: 7608

The used broadband amplifier shall support at least 2 quadrants.

6.5.12 Arbitrary function generator

The characteristics of this generator are described in this subclause. This device is necessary for dynamic ground shift.

Table 21 lists the characteristics of the arbitrary function generator.

Table 21 — Arbitrary function generator

Output	Description	Min	Max	Unit
U_x	Voltage level of digital test signals	0	2	V
	Frequency range (-3dB)	0	500	kHz
	Sample rate	50	—	MS/s

EXAMPLE arbitrary function generator

— Arbitrary function generator manufacturer[17]: Agilent

— Arbitrary function generator type: 33250A

16) The suggested broadband amplifier is supplied by Toellner. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

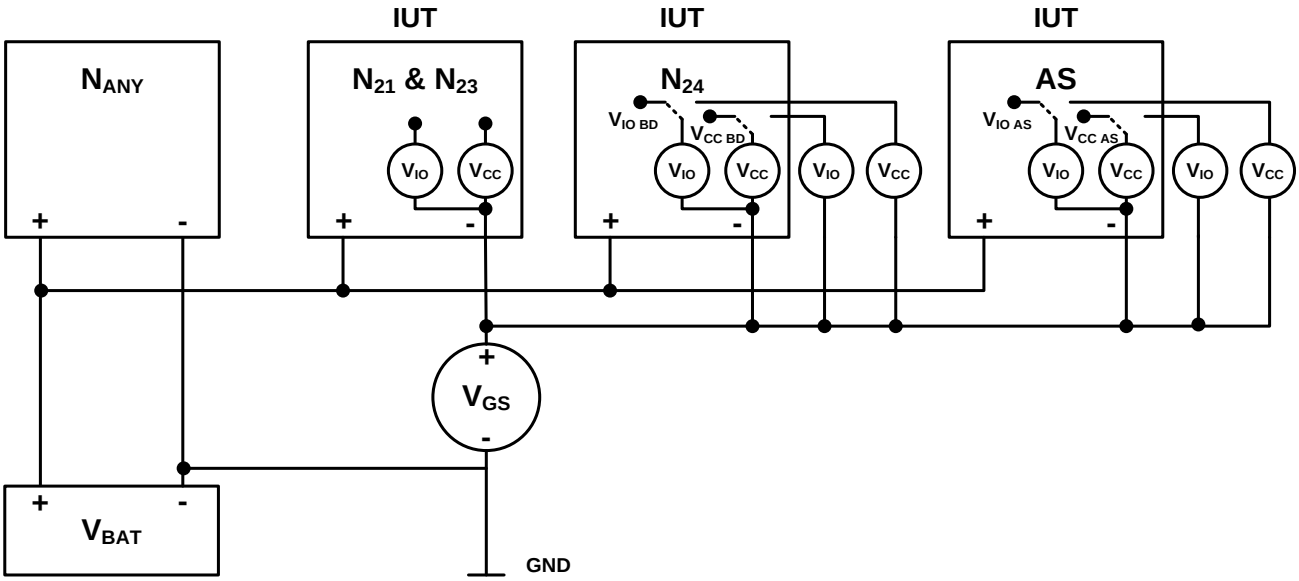
17) The suggested arbitrary function generator is supplied by Agilent. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO of the product named. Equivalent products may be used if they can be shown to lead to the same results.

7 Stress Conditions

7.1 Ground shift

The ground shift is located between the chassis and the predefined ground connection of the used IUTs. In every test case separate information are given about the usage of the ground shift and the IUT affected.

Figure 13 depicts the usage of ground shift.



Components

AS	Active Star
IUT	Nodes that are used as Implementation Under Test
N_X	FlexRay node x
V_{BAT}	Battery voltage
V_{CC}	Node supply voltage
$V_{CC\ BD}$	Supply voltage of the Bus Driver
$V_{CC\ AS}$	Supply voltage of the Active Star
V_{GS}	Ground shift voltage
V_{IO}	Input/output voltage
$V_{IO\ AS}$	Input/output voltage of the Active Star
$V_{IO\ BD}$	Input/output voltage of the Bus Driver

Connections and supplies

GND	System ground

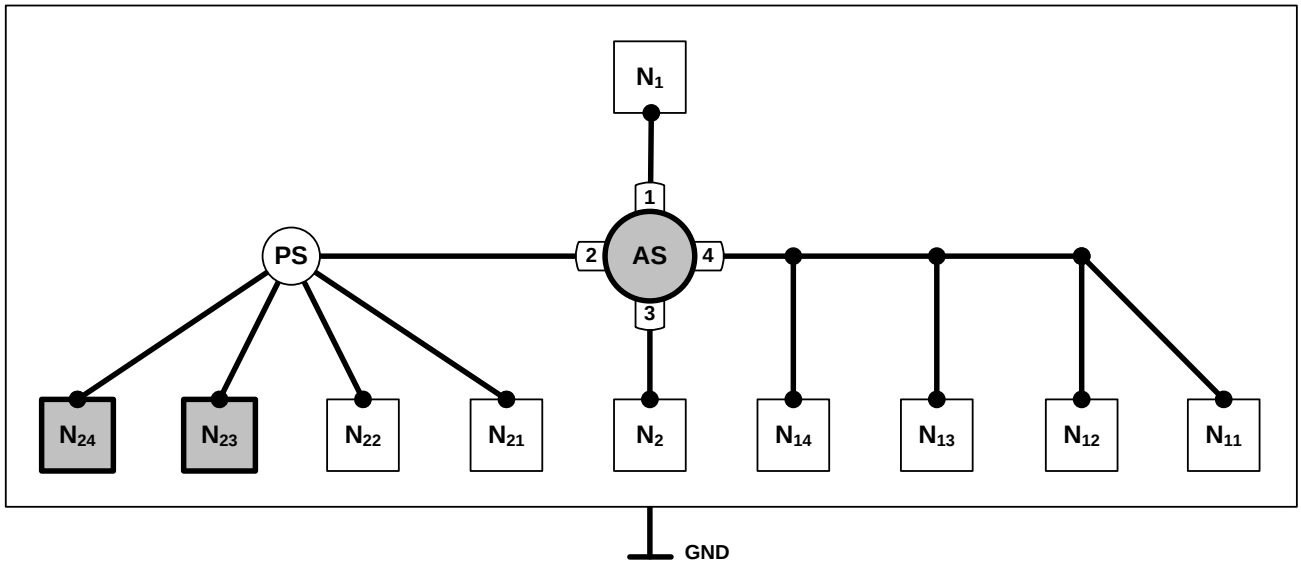
Figure 13 — Usage of ground shift

Table 14 depicts the ground shift.

Table 22 — Ground shift

Signal	Description	Min	Max
U_{GS}	Static ground shift voltage	—	+5,0 V

Figure 14 depicts the location of ground shift in the test topology. The ground shift is injected in the emphasided nodes (N_{23}, N_{24}, AS).



Components

AS	Active Star
N_x	FlexRay node x
PS	Passive Star

Connections and supplies

GND	System ground

Figure 14 — Location of ground shift

7.2 Low battery voltage inside operational range

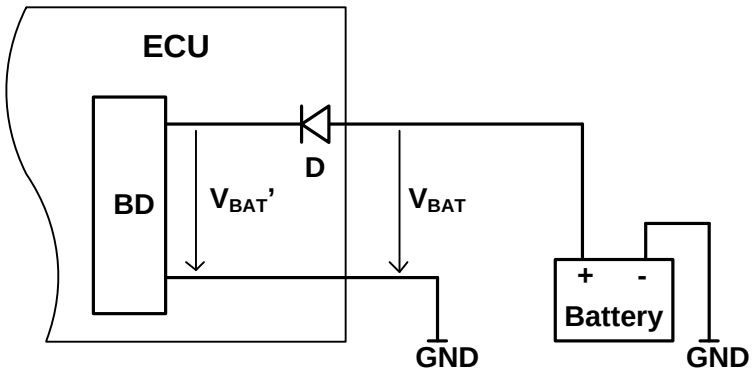
The test condition in case of a heavily discharged battery inside the operational range (with respect to the supply voltage boundaries specified in ISO 17458-4) is called low battery voltage inside operational range. The behaviour of the IUT during this stress condition is very important regarding the low power operation modes and the wakeup mechanism.

Since the kind of reverse connection protection (e.g. Schottky diode) inside the ECU varies from application to application V_{BAT}' is the stress voltage instead of V_{BAT}. The difference between V_{BAT} (supply voltage at the ECU) and V_{BAT}' (the voltage at the Bus Driver pin), is described in Figure 15.

Requirements:

All nodes including the IUTs and hosts of the topology (in Bus Driver test cases) / the Active Star (in Active Star test cases) shall be supplied by this low battery voltage.

Figure 15 depicts the description of V_{BAT} and V_{BAT}'.



Components		Connections and supplies	
BD	Bus Driver	GND	System ground
D	Diode	V_{BAT}	Battery voltage outside the ECU
ECU	Electronic control unit (FlexRay node or Active Star)	V_{BAT}'	Battery voltage inside the ECU (after the diode)

Figure 15 — Description of V_{BAT} and V_{BAT}'

Table 23 lists the stress conditions of static low battery voltage inside the operational range.

Table 23 — Stress condition static low battery voltage inside operational range

Signal	Description	Min	Max	Unit
$uV1_{BATlow}$	Low battery voltage for evaluation of wakeup detection if V_{CC} is not implemented and non wakeup test cases are applied.	—	+5,5	V
$uV2_{BATlow}$	Low battery voltage for evaluation of wakeup detection if V_{CC} is implemented.	—	+7,0	V

7.3 Undervoltage

The behaviour of the IUT during this stress condition is very important regarding the low power operation modes and the wakeup mechanism, especially for the recovery functionality of the IUT. According to ISO 17458-4, the minimum allowed undervoltage detection thresholds are the following:

— In case of presence of a V_{BAT} pin: $V_{BATUndervoltage}$= +4,0 V.

— In case of presence of a V_{CC} pin: $V_{CCUndervoltage}$= +4,0 V.

— In case of presence of a V_{IO} pin: $V_{IOUndervoltage}$ = +2,0 V.

In case the implemented minimum undervoltage detection threshold of the IUT for V_{BAT}, V_{CC} of V_{IO} is higher than specified in ISO 17458-4 then the undervoltage value in the conformance test shall be the specified minimum undervoltage value as given in the data sheet of the IUT.

EXAMPLE 1 for UV_V_{BAT}:

The undervoltage value of V_{BAT} is specified in ISO 17458-4 as +4,0 V.

If the minimum undervoltage threshold of V_{BAT} of the IUT in the data sheet is +4,5 V, then the undervoltage value for V_{BAT} in the conformance test shall be +4,5 V.

EXAMPLE 2 for UV_V_{CC}:

The undervoltage value of V_{CC} is specified in ISO 17458-4 as +4,0 V.

If the minimum undervoltage threshold of V_{CC} of the IUT in the data sheet is +4,2 V, then the undervoltage value for V_{CC} in the conformance test shall be +4,2 V.

EXAMPLE 3 for UV_V_{IO}:

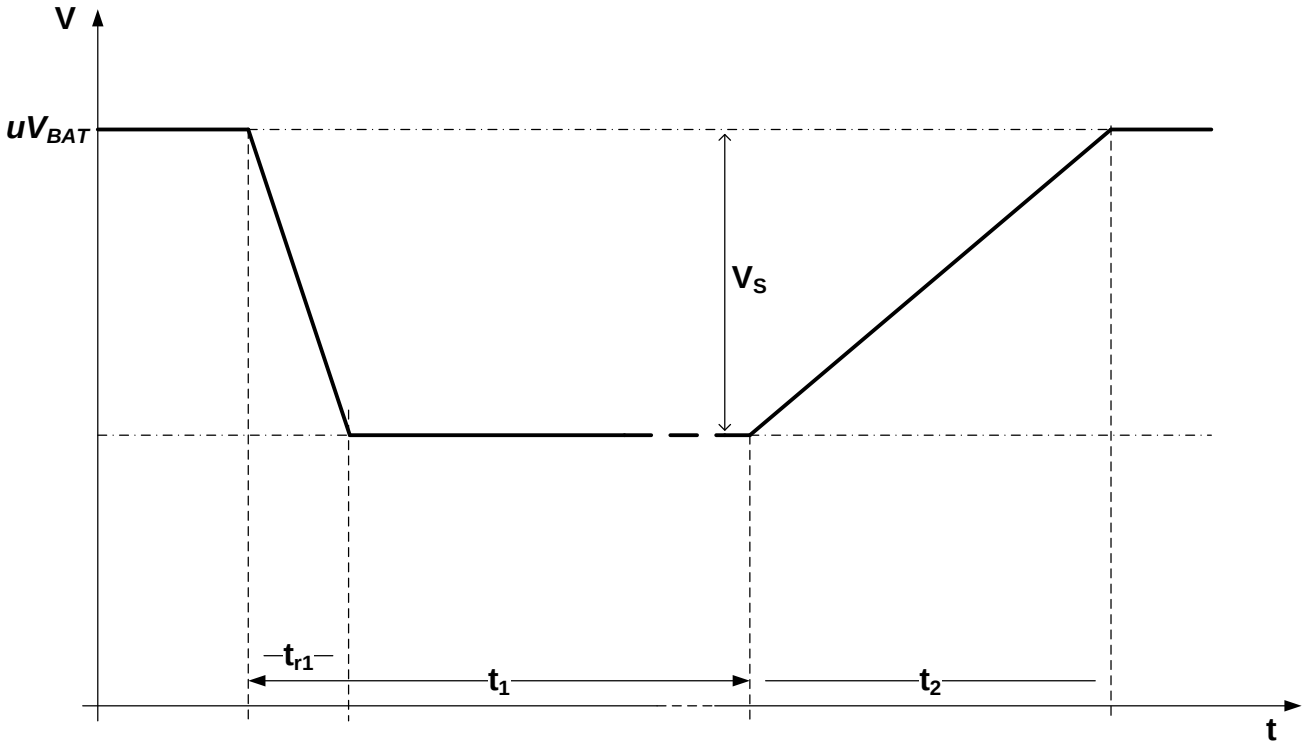
The undervoltage value of V_{IO} is specified in ISO 17458-4 as +2,0 V.

If the minimum undervoltage threshold of V_{IO} of the IUT in the data sheet is +2,5 V, then the undervoltage value for V_{IO} in the conformance test shall be +2,5 V.

7.4 Dynamic low battery voltage

The IUT will also be affected by a test signal that emulates a low battery voltage that appears when turning on the starter circuit, so the generator is connected to V_{BAT} of the IUT.

Figure 16 depicts the stress signal of DynamicLowBattery.



NOTE The components are described in Table 24.

Figure 16 — Stress signal DynamicLowBattery

Table 24 defines the stress signal DynamicLowBattery.

Table 24 — Stress signal DynamicLowBattery

Signal	Description	Value	Unit
V_S	Battery voltage difference after t_r at the IUT	6,1	V
uV_{BAT}	Nominal battery voltage at the IUT	11,6	V
t_{r1}	Fall time of battery voltage	70	ms
t_1	Time of low battery voltage without t_2	10 000	ms
t_2	Rise time of battery voltage	100	ms
NOTE The slew rate of V_S/t_{r1} simulates a small capacitance in an ECU.			

7.5 Dynamic low supply voltage

In case the supply voltages V_{BAT} and V_{CC} of a BD ramp down to undervoltage thresholds and up again, the BD shall react on undervoltage conditions but do not enter *BD_Off* or hang up when V_{IO} is constantly supplied with the product specific minimum operating voltage according to the BD datasheet.

Four different cases have to be considered in case both V_{BAT} and V_{CC} supply inputs are implemented:

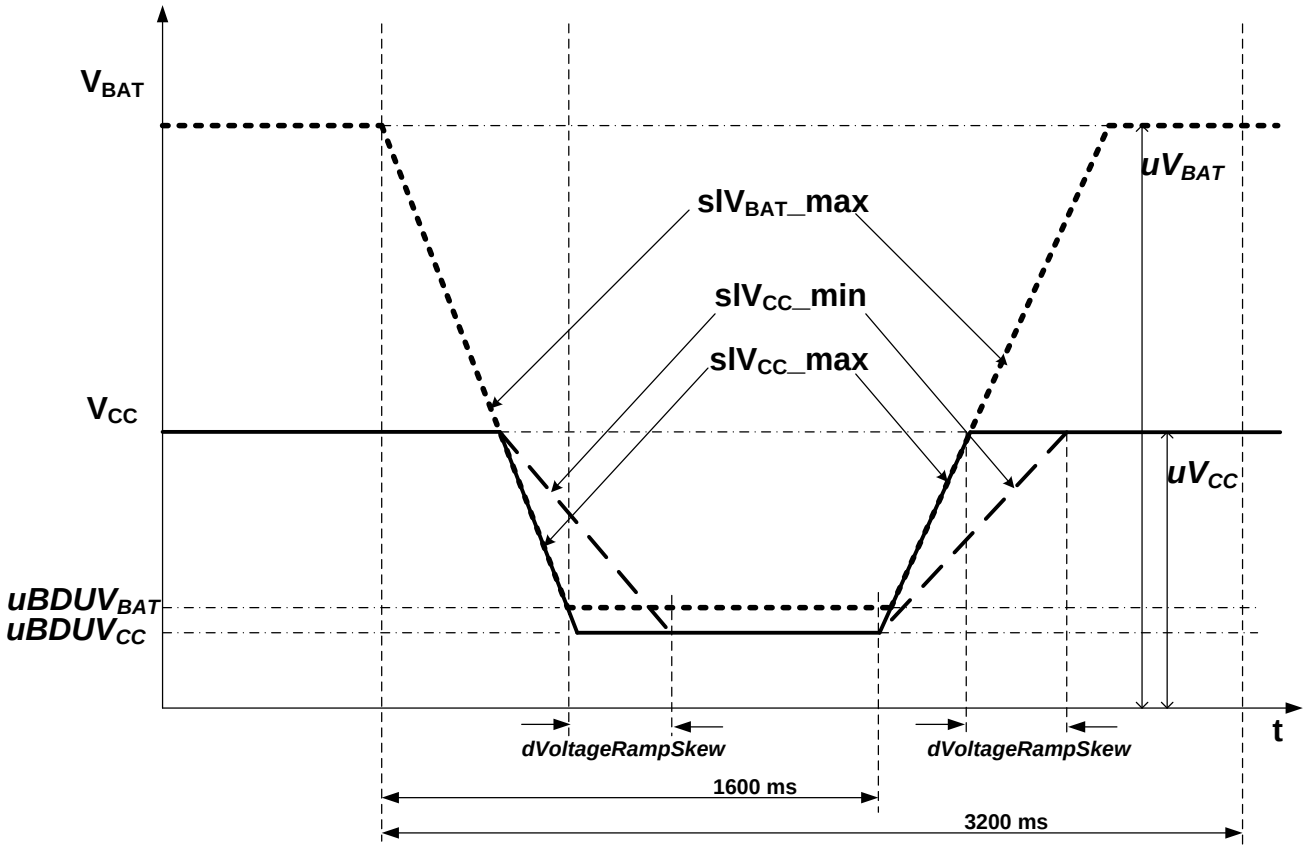
— Case1,1: Fast V_{BAT} voltage drop with slV_{BAT}_max=7,6 V/5 ms, and the same voltage drop on V_{CC} (slV_{CC}_max=slV_{BAT}_max) see Figure 17.

— Case1,2: Fast V_{BAT} voltage drop with slV_{BAT}_max=7,6 V/5 ms, combined with slower voltage drop on V_{CC} than V_{BAT} with slV_{CC}_min=6,1 V/(5 ms+65 ms) see Figure 17.

— Case2,1: Slow V_{BAT} voltage drop with slV_{BAT}_min=6,1 V/300 ms, and the same voltage drop on V_{CC} (slV_{CC}_max=slV_{BAT}_min) see Figure 18.

— Case2,2: Slow V_{BAT} voltage drop with slV_{BAT}_min=6,1 V/300 ms, combined with slower voltage drop on V_{CC} than V_{BAT} with slV_{CC}_min=6,1 V/(300 ms+65 ms) see Figure 18.

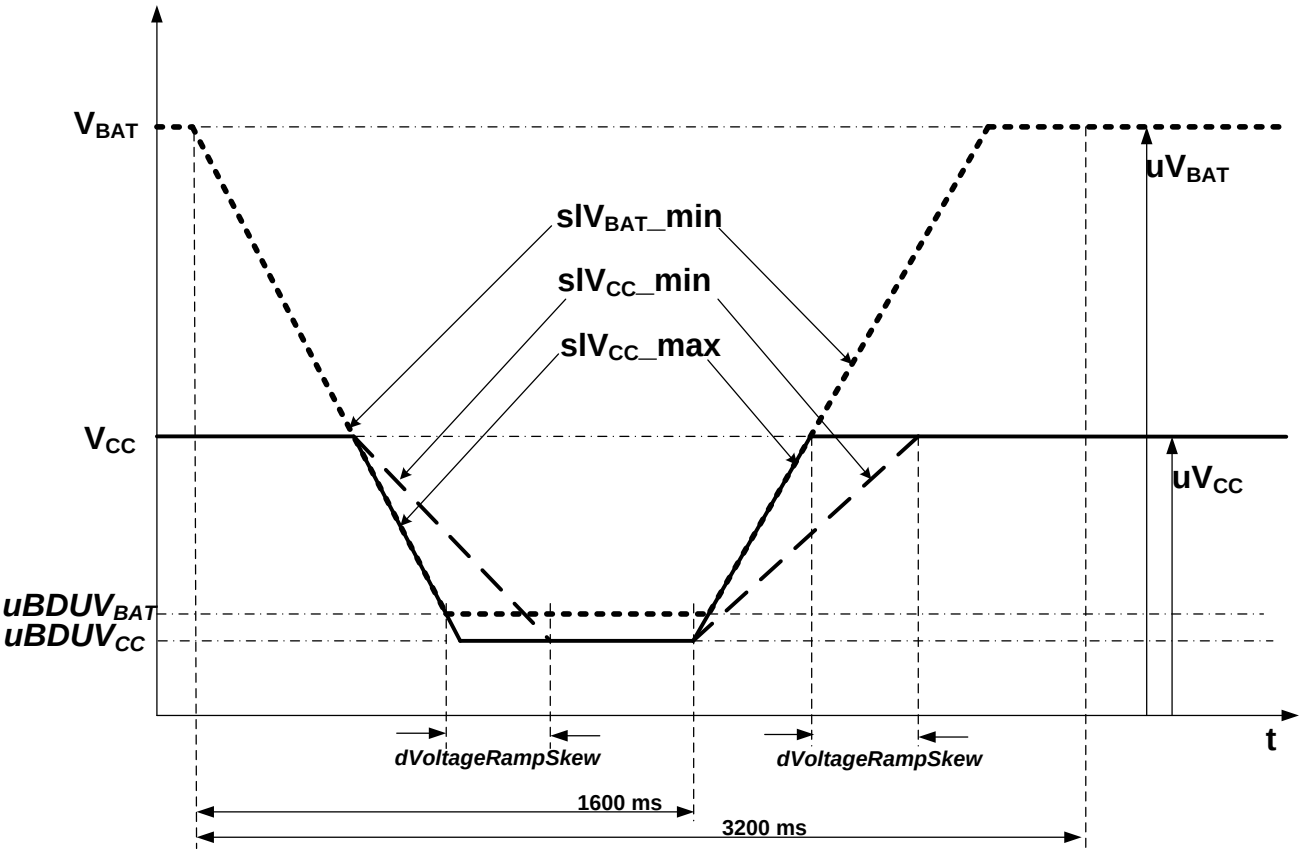
Figure 17 depicts the stress signal of the dynamic low supply case 1.



NOTE The components are described in Table 25.

Figure 17 — Stress signal dynamic low supply (case 1)

Figure 18 depicts the stress signal dynamic low supply case 2.



NOTE The components are described in Table 25.

Figure 18 — Stress signal dynamic low supply (case 2)

Table 25 lists the values of the dynamic low supply stress signal.

Table 25 — Stress signal dynamic low supply

Signal	Description	Min	Typ	Max	Unit
uV_{BAT}	Voltage value of V_{BAT} voltage supply at the IUT	—	11,6	—	V
uV_{CC}	Voltage value of V_{CC} voltage supply at the IUT	—	5	—	V
slV_{BAT}	Absolute slope of V_{BAT} voltage	0,02	—	1,52	V/ms
slV_{CC}	Absolute slope of V_{CC} voltage	see b	—	slV_{BAT}	V/ms
$uBDUV_{BAT}$	Undervoltage detection threshold on V_{BAT}	4 [a]	—	5,5 [a]	V
$uBDUV_{CC}$	Undervoltage detection threshold on V_{CC}	4 [a]	—	— [a]	V
dVoltageRamp Skew	*Time skew in reaching end of dynamic low supply voltage slope*	0	—	65	ms

[a] See also 7,3.

[b] Minimum value results from slVbat and dVoltageRamp, as depicted in Figure 18.

7.6 Failures

This stress parameter shall examine the behaviour of the IUT in case of failures onboard. A faulty link might be a faulty connection between the power lines or the digital signals.

Requirements:

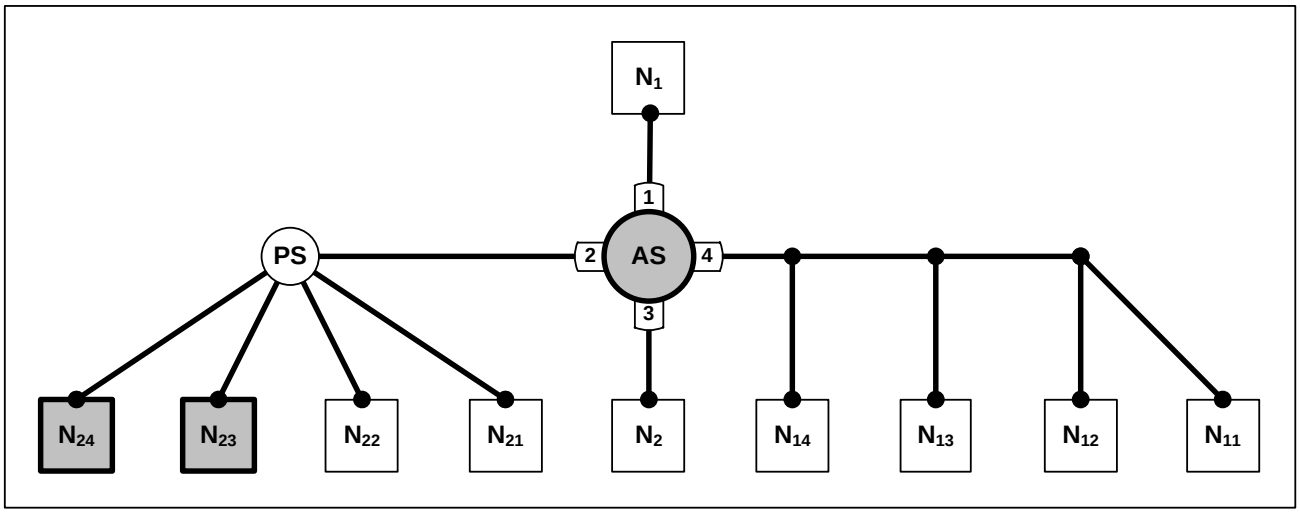
— The test nodes shall be supplied as specified in the test case.

— The behaviour of the IUT shall be checked while stressed.

— The recovery of the IUT shall be checked after removal of stress.

NOTE S/C (short-circuit) means a RDC < 1 Ω

Figure 19 depicts the location of the onboard failures. The onboard failures are injected in the emphasided nodes (N_{23}, N_{24}, AS).



Components

AS Active Star

N_x FlexRay node x

PS Passive Star

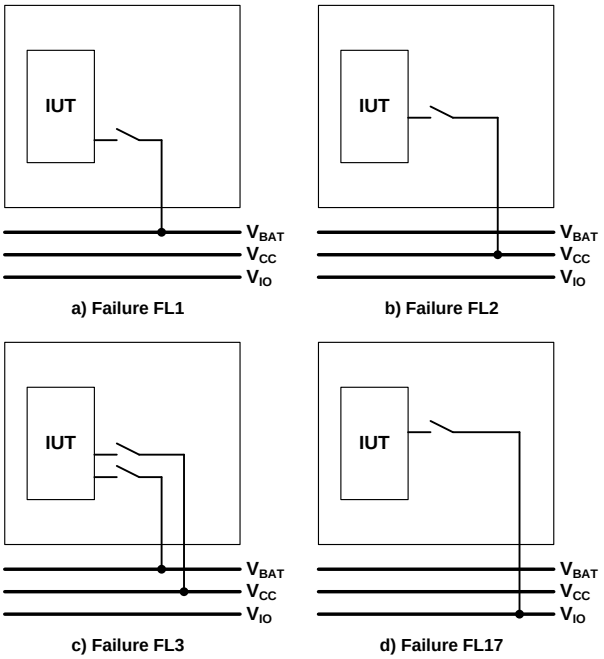
Figure 19 — Location of the onboard failures

Table 26 gives an overview of all faulty lines test parameters.

Table 26 — Faulty lines test parameters

Failure	Condition	Description
FL1	I/R V_{BAT}	Interruption of supply line V_{BAT} of the IUT
FL2	I/R V_{CC}	Interruption of supply line V_{CC} of the IUT
FL3	I/R V_{BAT} and V_{CC}	Interruption of supply lines V_{BAT} and V_{CC} of the IUT
FL4	S/C TxEN → GND	Short-circuit between TxEN and ground
FL5	I/R TxEN	Floating of TxEN
FL6	I/R TxD	Floating of TxD
FL7	*Minimum* R_{DCLoad}	Minimum allowed bus load (40 Ω) in node 23, see ISO 17458-4 See also Figure 8.
FL8	Maximum *RDCLoad*	Maximum allowed bus load (55 Ω) in node 23, see ISO 17458-4. See also Figure 8.
FL9	I/R STBN	Floating of STBN
FL10	I/R BGE	Floating of BGE
FL11	S/C BP → GND	Short-circuit between BP and GND
FL12	S/C BM → GND	Short-circuit between BM and GND
FL13	S/C BP → +48 V	Short-circuit between BP and +48 V [a] V_{ANY}
FL14	S/C BM → +48 V	Short-circuit between BM and +48 V [a] V_{ANY}
FL17	I/R V_{IO}	Interruption of supply line V_{IO} of the IUT
FL18	I/R EN	Floating of EN
FL19	S/C BP → -5 V	Short-circuit between BP and -5 V
FL20	S/C BM → -5 V	Short-circuit between BM and -5 V
FL21	S/C BP → BM	Short-circuit between BP and BM
FL25	I/R BP and I/R BM	BD looses connection to channel (BP and BM interrupted)
[a] In case the IUT is able to operate with 42 V, otherwise the short-circuit voltage is +27 V		

Figure 20 depicts various failures, loss of supply voltage.



Components

IUT Implementation Under Test

Connections and supplies

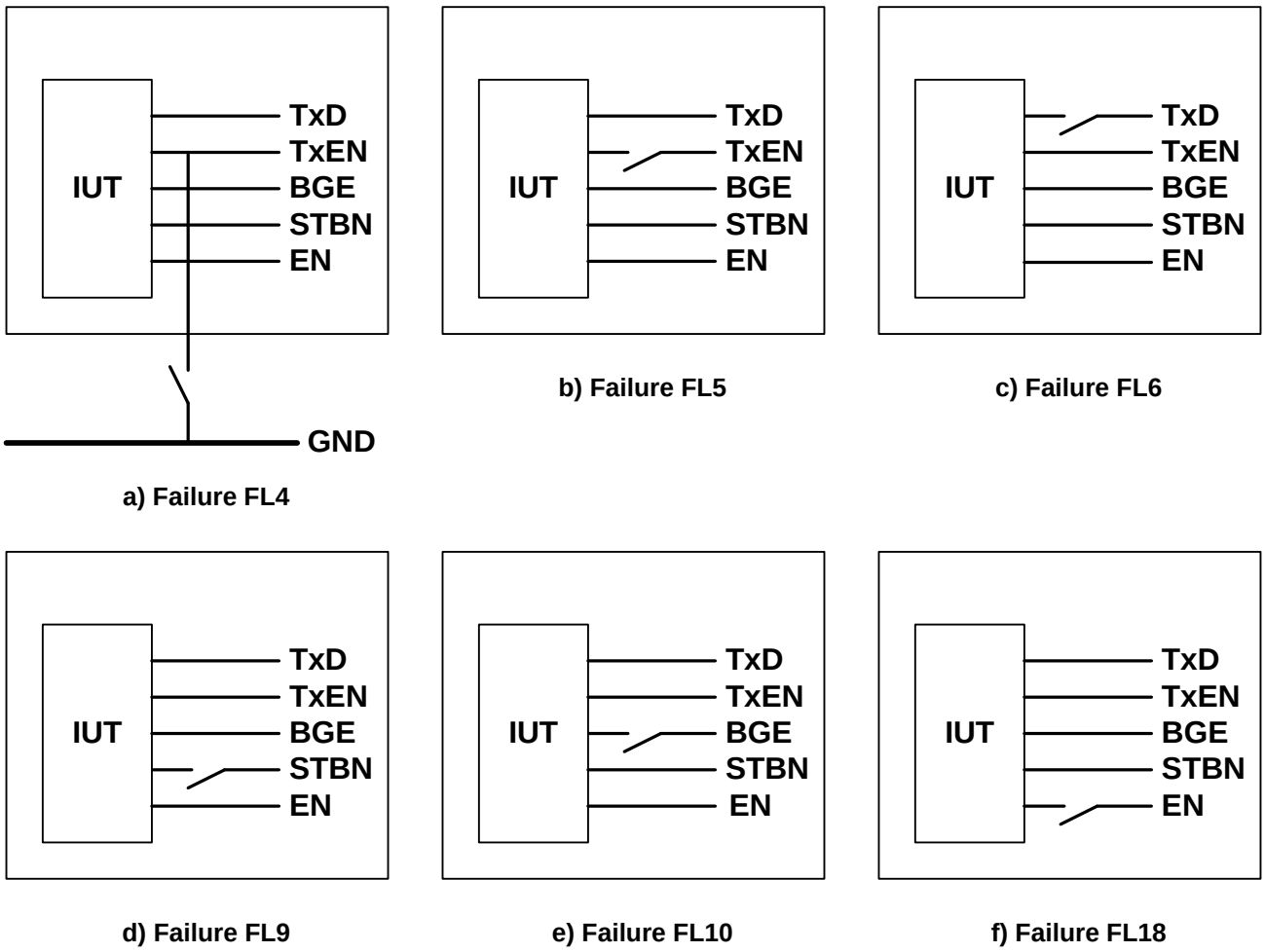
V_{BAT} Battery supply voltage

V_{CC} Supply voltage to drive bus signals

V_{IO} Reference voltage of the digital interface

Figure 20 — Failure, loss of supplies

Figure 21 depicts various failures of digital signals.



Components

IUT Implementation Under Test

Connections and supplies

BGE Bus guardian enable

EN Enable

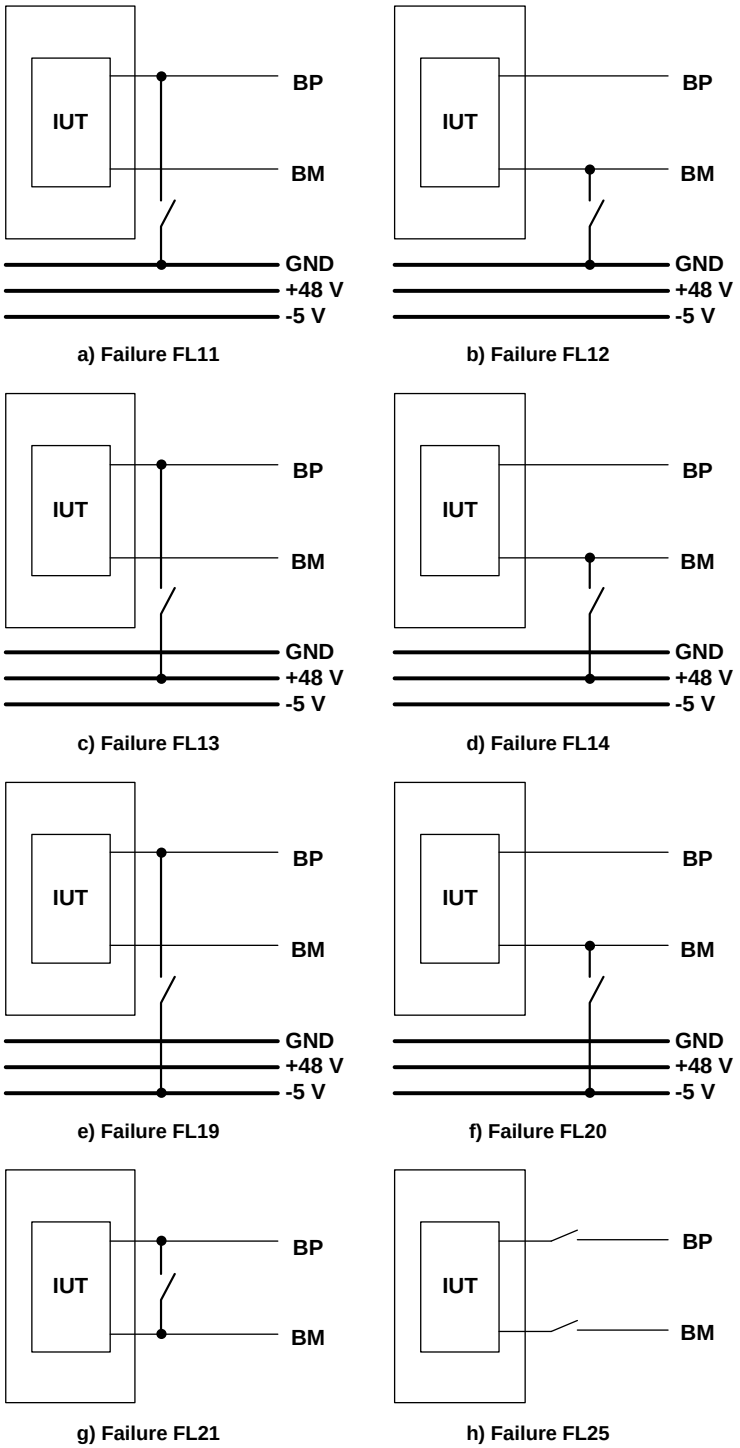
STBN Standby not

TxD Transmit data

TxEN Transmit enable not

Figure 21 — Failures of digital signals TxEN, TxD, BGE, STBN and EN

Figure 22 depicts failures of bus wires BP and BM (FL11 to FL14).



Components

IUT Implementation Under Test

Connections and supplies

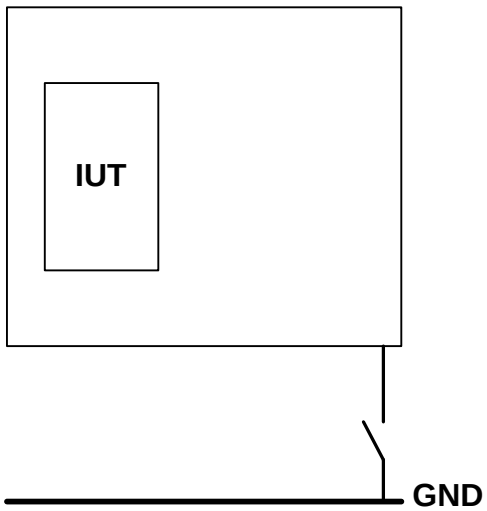
BM Bus minus

BP Bus plus

GND Ground connection

Figure 22 — Failures of bus wires BP and BM (FL11 to FL14)

Figure 23 depicts the failures of bus wires BP and BM (FL19 to FL25).



Components

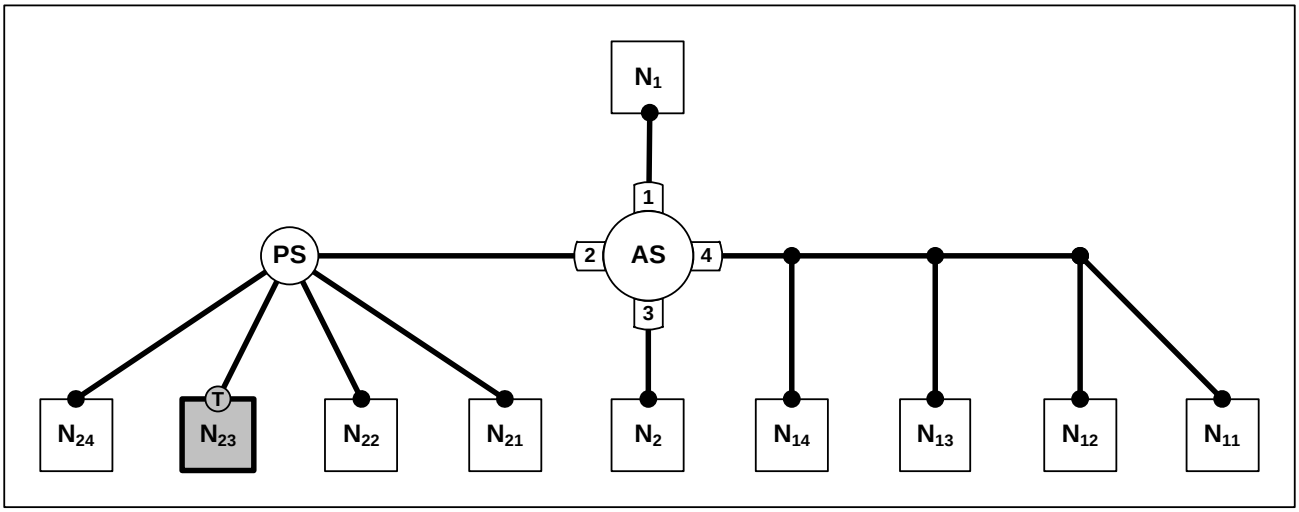
IUT Implementation Under Test

Connections and supplies

GND Ground connection

Figure 23 — Failures of bus wires BP and BM (FL19 to FL25)

Figure 24 depicts the location of termination changes inside a node. The affected nodes are emphasized (N_{23}).



Components

AS Active Star

N_X FlexRay node x

PS Passive Star

T Bus termination

Figure 24 — Location of termination changes inside a node

7.7 Babbling idiot

The AS shall recognize a babbling idiot at a branch in order to prevent the communication of the other nodes from a faulty node. This is also described in ISO 17458-4.

Requirements:

— The test signal shall stimulate the TxD pin of the babbling idiot(s).

— The TxEN shall be active while sending data (the IUTs are enabled to transmit data from their CCs/hosts).

— An optional BGE signal shall be active (the IUTs shall be enabled to transmit data from their CCs/hosts).

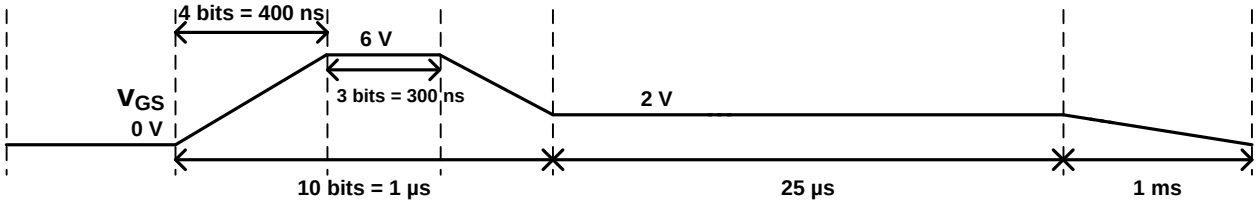
— Optional mode control signals shall be set to normal mode of the IUTs.

The test signal is specified in 10.2.3.1.

7.8 Dynamic ground shift

The IUT shall also be affected by a dynamic ground shift. The connection and usage are described in 7.1.

Figure 25 depicts the dynamic ground shift curve for input.



Key

V_{GS} Ground shift voltage

Figure 25 — Dynamic ground shift curve for input

Due to internal filters and the speed of a broad band amplifier the output (*uGS_dyn*) may look like upper curve in Figure 26 (the lower curve is the input signal).

Figure 26 depicts the dynamic ground shift curve for possible output.

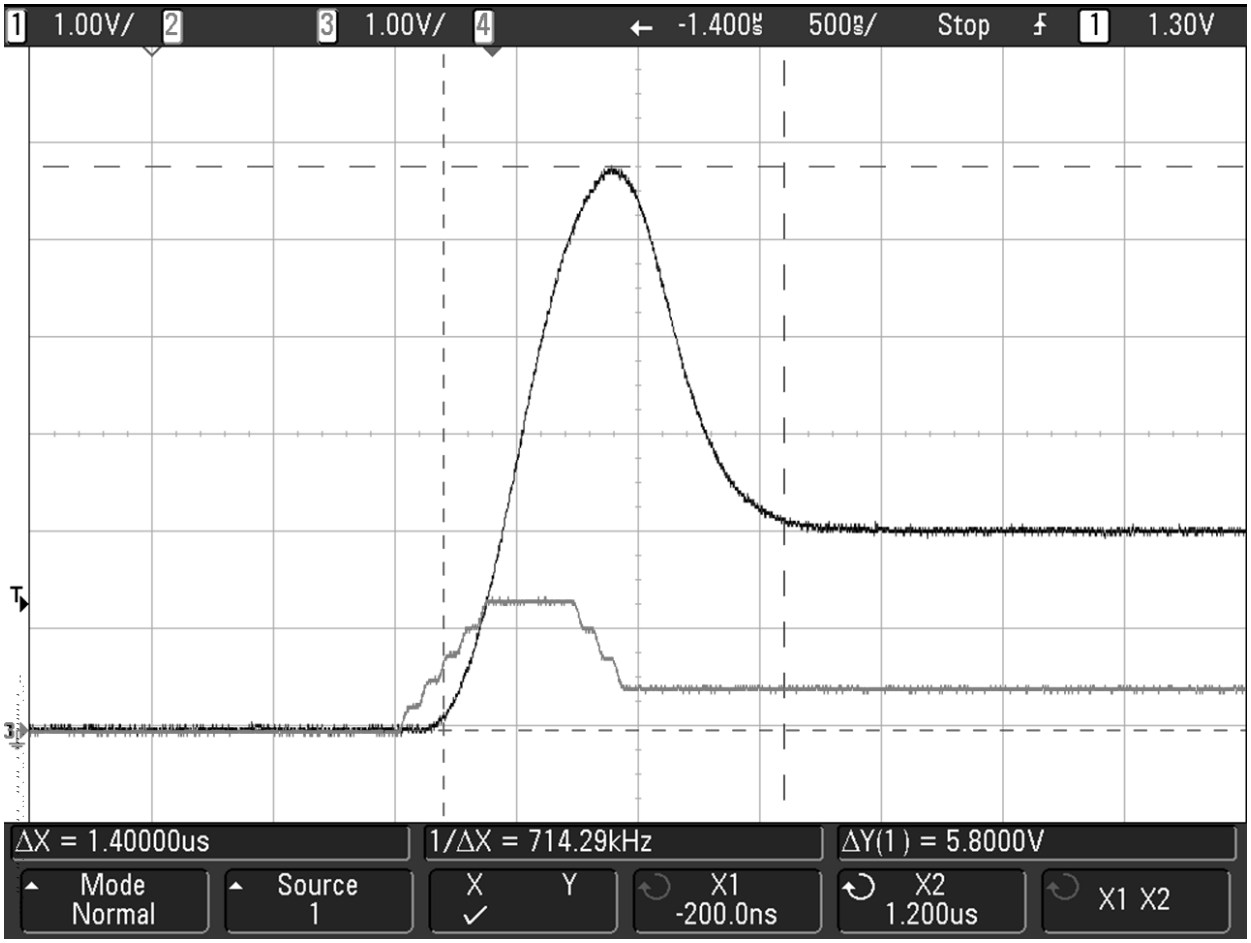


Figure 26 — Dynamic ground shift curve for possible output

7.9 EMC

This conformance test specification does not support EMC stress conditions. This is part of a separate specification that is part of the FlexRay consortium in the corresponding working group.

7.10 ESD

This international standard does not support EMC stress conditions. This is part of ISO 17458-4.

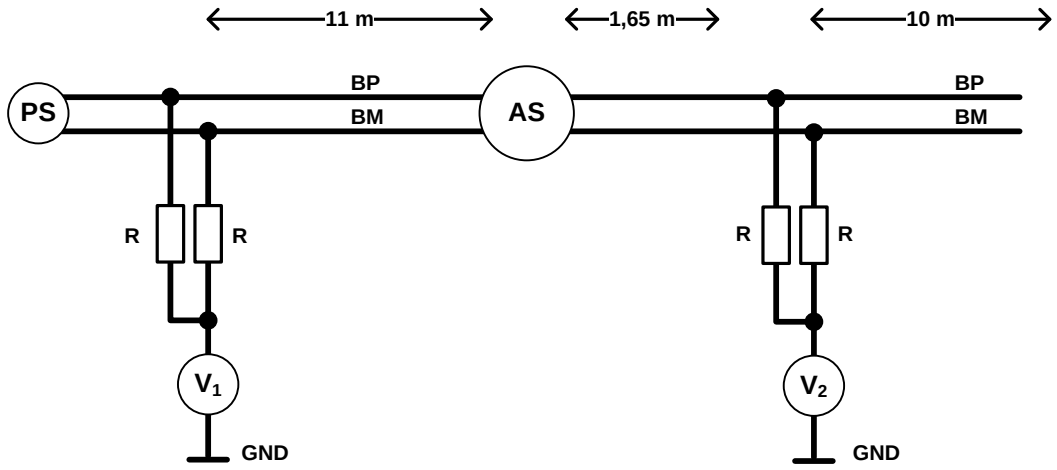
7.11 Temperature tests

This conformance test specification does not support temperature tests as a stress condition. This is part of the semiconductor manufacturer and included in the data sheet of the corresponding physical layer device.

7.12 Common mode offset

To estimate the behavior of the Bus Drivers (see 9.3.22) and the Active Star (see 10.4.20) an additional common mode offset is applied at the bus lines BM and BP according Figure 27.

Figure 27 depicts additional components for common mode offset feeding.



Components

AS	Active Star
PS	Passive Star
R	Pull-up resistor R = 10 kΩ
V_1	Offset voltage applied on the Passive Star side
V_2	Offset voltage applied on the Active Star side

Connections and supplies

BM	Bus minus
BP	Bus plus
GND	System ground

Figure 27 — Additional components for common mode offset feeding

The offset is applied with a positive value of +12,5 V and negative value of -12,5 V. It is applied either at the passive star (V_1) or at the passive bus (V_2) or at both.

8 Parameter List

8.1 General

The parameter list is organized by a tree and structured by the system operating variable space (SOVS). The SOVS approach is a specific method to derive test cases by combining basic system *variables* with each other.

The system operating conditions are given from experience from existing communication systems. In order to have an easier way of reproducibility the test parameters are grouped into the following variables:

— Static test cases

— Communication

— Host interface

— Mode

— Power supply

— Environment

- Dynamic low battery voltage
- Ground shift
- Failure
- Functional class
- Simulation

All combinations of these variables represent all theoretical possible test cases. This results in a very large number of test cases. The number of combinations can be reduced dramatically by defining variables as *constant* (e.g. environment) or by selecting just a few representative (i.e. concerted) values for each variable. So the relevant test cases are selected in the test cases beginning from Clause 9.

8.2 Static test cases

These tests shall be done manually and contain the comparison of the data sheet of the IUT with the required parameters. There is no automatic test with hard and/or software necessary.

8.3 Communication

8.3.1 General

This vector contains the test parameters that affect the data communication of the test system in normal operational mode. It is divided in some more sub items as follows:

- Communication
  - Delay
  - Signal shape
  - Threshold
  - Timing
    - Bus Driver
    - Active Star
  - Truncation
  - Transmitter activation

8.3.2 Communication.Delay

The sub item delay contains all relevant tests with the focus on delay in the data communication. This item is divided into more sub items as follows:

- Delay
  - *dStarDelay10*
  - *dStarDelay01*
  - *dStarAsym*

- *dStarAsym2*
- *dStarSetUpDelay*
- *dBDTx01*
- *dBDTx10*
- *dBDTxAsym*
- *dBDRx01*
- *dBDRx10*
- *dBDRxAsym*
- *dStarTxAsym*
- *dStarTx01*
- *dStarTx10*
- *dStarRxAsym*
- *dStarRx01*
- *dStarRx10*
- *dBDTxDM*

8.3.3 Communication.Signal shape

The sub item signal shape contains all relevant tests with the focus on the signal form. This item is divided into more sub items as follows:

- Signal shape
  - *dBusTxai*
  - *dBusTxia*
  - $uBDTx_{active}$
  - $uBDTx_{idle}$
  - $uStarTx_{active}$
  - $uStarTx_{idle}$
  - uRx_{Data}
  - *dBusTx01*
  - *dBusTx10*

— *dBusTxDif*

8.3.4 Communication.Threshold

Threshold test cases are static test cases and specified in the subclauses 9.2, 10.3, 11.2, and 12.2. They are grouped into sub items as follows:

— Threshold

  — $uV_{DIG\text{-}OUT\text{-}HIGH}$

  — $uV_{DIG\text{-}OUT\text{-}LOW}$

  — $uV_{DIG\text{-}IN\text{-}HIGH}$

  — $uV_{DIG\text{-}IN\text{-}LOW}$

  — $uV_{DIG\text{-}OUT\text{-}OFF}$

  — $uV_{DIG\text{-}OUT\text{-}UV}$

  — *uData0*

  — *uData1*

  — *uData1*-|*uData0*|

  — *uBDLogic_1*

  — *uBDLogic_0*

  — *uStarLogic_1*

  — *uStarLogic_0*

  — $uINH1_{Not\_Sleep}$

  — *uData0_LP*

8.3.5 Communication.Timing

8.3.5.1 General

The sub item timing contains all relevant tests with the focus on the timing of the transmitted signal. This item is divided into more sub items as follows:

— Timing

  — Bus Driver

  — Active Star

8.3.5.2 Communication.Timing.Bus Driver

This sub item defines the timing parameters for Bus Drivers. It is divided into more sub items as follows:

— Bus Driver

- *dBDTxai*
- *DBDTxia*
- *dBDRxai*
- *dBDRxia*
- *dBDActivityDetection*
- *dBDIdleDetection*
- $dBDRxD_{R25} + dBDRxD_{F25}$
- $|dBDRxD_{R25} - dBDRxD_{F25}|$
- *dBDTxActiveMax*
- $dBDRxD_{R15} + dBDRxD_{F15}$
- $|dBDRxD_{R15} - dBDRxD_{F15}|$
- *dBDTxRxai*

8.3.5.3 Communication.Timing.Active Star

This sub item defines the timing parameters for Active Stars. It is divided into more sub items as follows:

- Active Star
  - *dBranchRxActiveMax*
  - *dStarTxai*
  - *dStarTxia*
  - *dStarRxai*
  - *dStarRxia*
  - $dStarRxD_{R15} + dStarRxD_{F15}$
  - $|dStarRxD_{R15} - dStarRxD_{F15}|$
  - *dStarTxRxai*
  - *dStarActivityDetection*
  - *dStarIdleDetection*
  - *dStarTxActiveMax*
  - $dStarTx_{reaction}$

8.3.6 Communication.Truncation

The sub item truncation contains all relevant tests with the focus on the star truncation. This item is divided into more sub items as follows:

- Truncation
  - *dStarTSSLengthChange*
  - *dStarFES1LengthChange*
  - *dStarSymbolLengthChange_TxD_Bus*
  - *dStarFES1LengthChange_TxD_Bus*
  - *dStarSymbolLengthChange_TxD_Bus*
  - *dStarTSSLengthChange_Bus_RxD*
  - *dStarFES1LengthChange_Bus_RxD*
  - *dStarSymbolLengthChange_Bus_RxD*
  - *dFrameTSSLengthChange*$_{M,N}$
  - *dStarSymbolEndLengthChange*

8.4 Host Interface

The sub item Host Interface contains all relevant tests with the focus on the host interface of the Active Star and the Bus Driver. This item is divided into more sub groups and parameters as follows:

- Host interface
  - Active Star
    - SPI
      - *dStarModeChange*$_{SPI}$
      - *dStarReactionTimer*$_{SPI}$
  - Bus Driver
    - SPI
      - *dBDModeChange*$_{SPI}$
      - *dBDReactionTime*$_{SPI}$
    - Hard wired signals
      - *dBDModeChange*
      - *dBDERRN*$_{Stable}$
      - *dReactionTime*$_{ERRN}$

8.5 Mode

8.5.1 General

This vector contains the test parameters that contain the mode transitions and especially the low power operation modes of the physical layer in node and Active Star application. It is divided into more sub groups and parameters as follows:

- Mode
  - Active Star
    - Branch
      - Receive.Transmit
      - Idle
      - FailSilent
      - Disabled
      - TxOnly
    - Low power
      - Standby
        - Wakeup
      - Sleep (optional)
        - Wakeup
    - Normal
      - GoToSleep
      - GoToSleep_Fail
    - Off
  - Bus Driver
    - Low power
      - Standby
      - Sleep (optional)
        - Wakeup
    - Normal
    - ReceiveOnly

- DynamicLowSupply voltage

8.5.2 Mode.Active Star

8.5.2.1 General

This sub vector contains all relevant test parameters regarding the Bus Driver equipped in an Active Star. It is divided in several sub items:

- Active Star
  - Branch
    - Receive.Transmit
    - Idle
    - FailSilent
    - Disabled
    - TxOnly
  - Low power
    - Standby
      - Wakeup
    - Sleep (optional)
      - Wakeup
  - Normal
    - GoToSleep
    - GoToSleep_Fail
  - Off

8.5.2.2 Mode.Active Star.Branch

Tests regarding the behaviour of branches are:

- Branch
  - Active
  - Idle
  - FailSilent
    - *dBranchRxActiveMax*

8.5.2.3 Mode.Active Star.Low power

Tests regarding the low power operation modes are:

— Low power

  — Sleep (optional)

    — Wakeup

      — *dStarWakeupReactionTime*

      — *dStarWakePulseFilter*

      — $dWU_{0Detect}$

      — $dWU_{IdleDetect}$

      — $dWU_{Timeout}$

      — $dWU_{Interrupt}$

      — $dStarWakeupReaction_{local}$

  — Standby

    — Wakeup

      — *dStarWakeupReactionTime*

      — *dStarWakePulseFilter*

      — $dWU_{0Detect}$

      — $dWU_{IdleDetect}$

      — $dWU_{Timeout}$

      — $dWU_{Interrupt}$

      — $dStarWakeupReaction_{local}$

  — *dStarGoToSleep*

  — *uBias* – Low power

  — $iINH1_{Leak}$

8.5.2.4 Mode.Active Star.Normal

Tests regarding the normal mode and its behaviour are:

— Normal

  — GoToSleep

— GoToSleep_Fail

8.5.2.5 Mode.Active Star.Off

Tests regarding the off mode and its behaviour are:

— Off

— iBP_{Leak}

— iBM_{Leak}

— *uBias* – Low power

8.5.3 Mode.Bus Driver

8.5.3.1 General

This sub vector contains all relevant test parameters regarding the Bus Driver equipped in a node. It is also divided into three sub items as follows:

— Bus Driver

— Low power

— Standby

— Sleep (optional)

— Wakeup

— Normal

— ReceiveOnly

8.5.3.2 Mode.Bus Driver.Low power

Tests regarding the low power operation mode and its behaviour are:

— Low Power

— *uBias* – Low power

— $iINH1_{Leak}$

— Wakeup

— *dBDWakePulseFilter*

— $dWU_{0Detect}$

— $dWU_{IdleDetect}$

— $dWU_{Timeout}$

— $dWU_{Interrupt}$

- *dBDWakeupReaction$_{local}$*
- *dBDWakeupReaction$_{remote}$*

8.5.3.3 Mode.Bus Driver.Normal

Tests regarding the normal mode and its behaviour are:

- Normal
  - *uBias – BD_Normal*

8.5.3.4 Mode.Bus Driver.ReceiveOnly

Tests regarding the operation mode *BD_ReceiveOnly* and its behaviour. It is not divided into any sub items.

8.5.3.5 Mode.Bus Driver.Off

Tests regarding the off mode and its behaviour are:

- Off
  - *iBP$_{Leak}$*
  - *iBM$_{Leak}$*

8.6 Power supply

8.6.1 General

This vector stresses the physical layer at its given pins, e.g. undervoltage. It is divided into several sub items as follows:

- Power supply
  - Bus Driver
    - Undervoltage V_{BAT}
    - Undervoltage V_{CC}
    - Undervoltage V_{IO}
  - Active Star
    - Undervoltage V_{BAT}
    - Undervoltage V_{CC}
    - Undervoltage V_{IO}
    - Undervoltage $V_{StarSupply}$
  - *uV$_{BAT-Wake}$*

- Undervoltage recovery
- Wakeup detection
  - Undervoltage detection timeout

8.6.2 Power supply.Bus Driver

This vector stresses the physical layer of a Bus Driver at its given pins, e.g. undervoltage. It is divided into several sub items as follows:

- Bus Driver
  - Undervoltage V_{BAT}
    - *uBDUVV*$_{BAT}$
    - *dBDUVV*$_{BAT}$
    - *dBDRV*$_{BAT}$
  - Undervoltage V_{CC}
    - *uBDUVV*$_{CC}$
    - *dBDUVV*$_{CC}$
    - *dBDRV*$_{CC}$
  - Undervoltage V_{IO}
    - *uUV*$_{IO}$
    - *dBDUVV*$_{IO}$
    - *dBDRV*$_{IO}$

8.6.3 Power supply.Active Star

This vector stresses the physical layer of an Active Star at its given pins, e.g. undervoltage. It is divided into several sub items as follows:

- Active Star
  - Undervoltage V_{BAT}
    - *uStarUVV*$_{BAT}$
    - *dStarUV*$_{BAT}$
    - *dStarRV*$_{BAT}$
  - Undervoltage V_{CC}
    - *uStarUVV*$_{CC}$
    - *dStarUV*$_{CC}$

- — *dStarRV$_{CC}$*
- — Undervoltage V_{IO}
  - — *uStarUVV$_{IO}$*
  - — *dStarUV$_{IO}$*
  - — *dStarRV$_{IO}$*
- — Undervoltage $V_{StarSupply}$
  - — *uStarUVV$_{Supply}$*
  - — *dStarUV$_{Supply}$*
  - — *dStarRV$_{Supply}$*

8.7 Environment

8.7.1 General

The environment of the IUT is tested by this vector. It is divided into several sub items as follows:

- — Environment
  - — *RCM1*
  - — *RCM2*
  - — Common mode voltages
    - — *uCM*
  - — Ground shift
    - — *uCM*
    - — Dynamic ground shift
  - — *T$_{AMB_Class0}$*
  - — *T$_{AMB_Class1}$*
  - — *T$_{AMB_Class2}$*
  - — *T$_{AMB_Class3}$*
  - — *uESD$_{EXT}$*
  - — *uESD$_{INT}$*
  - — *uESD$_{IEC}$*
  - — *C_BDTxD*

— *C_StarTxD*

8.7.2 Environment.Ground shift

This vector stresses the physical layer with a specified ground shift as described in 7.1. The ground shift generator requirements are described in 6.5.5.

This vector is divided as follows:

— Ground shift

  — *uCM*

  — Dynamic ground shift

8.8 Dynamic low battery voltage

This vector emulates the start of an engine with a dynamic low battery voltage. The supply voltage is specified in 7.4. This SOVS parameter does not have sub items.

8.9 Dynamic low supply voltage

This vector emulates that the supply voltages (if implemented) synchronously ramp up and down slowly. The supply voltage is specified in 7.5. This SOVS parameter does not have sub items.

8.10 Failure

8.10.1 General

This vector stresses the physical layer with predefined failures of the links, power supplies and termination. The failures are described in 7.6. They are divided into several sub items as follows:

— Failure

  — Babbling idiots

  — Loss

    — Power

      — V_{BAT}

      — V_{CC}

      — V_{IO}

    — TxD

    — TxEN

    — GND

      — IUT
        — $iBP_{LeakGND}$
        — $iBM_{LeakGND}$

- EN
- STBN
- BGE

- Short circuit
  - BM
  - BP
  - TxEN

- Termination
  - Minimum R_{DCLoad}
  - Maximum R_{DCLoad}
  - Nominal R_{DCLoad}

- Error indication

8.10.2 Failure.Babbling idiot

This vector contains the test parameter regarding the detection and signaling of a babbling idiot. It is not divided into any sub items.

8.10.3 Failure.Loss

This vector describes the possible loss of supply lines and digital signals at the Bus Driver. It is divided into several sub items as follows:

- Loss
  - Power
    - V_{BAT}
    - V_{CC}
    - V_{IO}
  - TxD
  - TxEN
  - GND
    - IUT
      - $iBP_{LeakGND}$
      - $iBM_{LeakGND}$

- EN
- STBN
- BGE

8.10.4 Failure.Short-circuit

This vector describes the possibility of short-circuit of digital signals and the bus wires and the behaviour of the Bus Driver. It is divided into several sub items as follows:

- Short circuit
  - BM
    - $iBM_{GNDShortMax}$
    - $iBM_{BAT27ShortMax}$
    - $iBM_{BAT48ShortMax}$
    - $iBM_{BAT60ShortMax}$
    - $iBM_{-5VShortMax}$
    - $iBM_{BPShortMax}$
  - BP
    - $iBM_{GNDShortMax}$
    - $iBM_{BAT27ShortMax}$
    - $iBM_{BAT48ShortMax}$
    - $iBM_{BAT60ShortMax}$
    - $iBM_{-5VShortMax}$
    - $iBM_{BPShortMax}$
  - TxEN

8.10.5 Failure.Termination

This vector contains test parameters regarding different termination values. It is divided into several sub items as follows:

- Termination
  - Minimum R_{DCLoad}
  - Maximum R_{DCLoad}
  - Nominal R_{DCLoad}

8.11 Functional class

This vector contains functional classes of the IUT. It is divided into several sub items as follows:

- Functional class
  - Bus Driver voltage control
    - Bus Driver remote wakeup
  - Bus Driver – bus guardian interface
  - Bus Driver internal voltage regulator
    - Bus Driver remote wakeup (optional)
    - Bus Driver logic level adaption (optional)
  - Bus Driver logic level adaption
  - Bus Driver remote wakeup
  - Active Star – communication controller interface
  - Active Star – bus guardian interface
  - Active Star – voltage regulator control
  - Active Star – internal voltage regulator
  - Active Star – logic level adaption
  - Active Star – host interface
  - Active Star Increased voltage amplitude transmitter

8.12 Simulation

This vector contains test constraints regarding the simulation of some electrical behaviours. It is divided into several sub items as follows:

- Simulation
  - RxD signal sum of rise and fall time at TP4_CC
  - RxD signal difference of rise and fall time at TP4_CC
  - $R_{BDTransmitter}$
  - $R_{StarTransmitter}$

9 Test Cases for Bus Drivers

9.1 Configuration

9.1.1 Topology

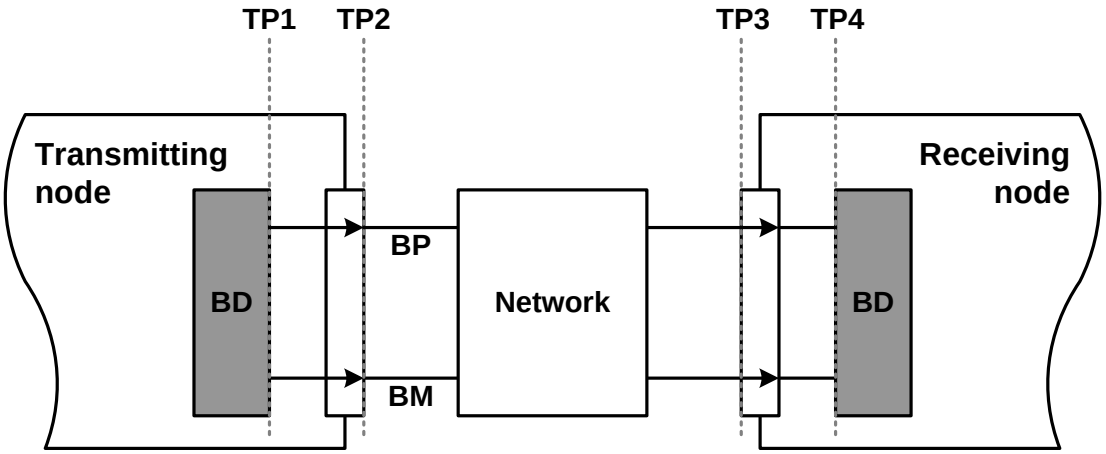
As specified in subclause, 6.4, all IUTs shall be of the same type and manufacturer.

9.1.2 Test planes

9.1.2.1 Analog signals

The test planes at the FlexRay node for analog signals (FlexRay bus) shall be the same as specified in ISO 17458-4.

Figure 28 depicts the planes at the nodes (analog signals).



Components

BD Bus Driver

Connections and supplies

BM Bus minus

BP Bus plus

TPx Test plane x (see Table 27)

Figure 28 — Planes at the nodes (analog signals)

Table 27 depicts the test planes at the nodes (analog signals).

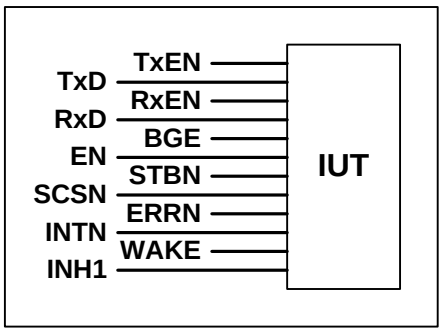
Table 27 — Test planes at the nodes (analog signals)

TP Name	Signals	Description
TP1	*uBP* / *uBM*	Bus signals of the transmitter as close as possible to the chip
TP2	*uBP* / *uBM*	Bus signals of the transmitter at the connector near to the network
TP3	*uBP* / *uBM*	Bus signals of the receiver at the connector near to the network
TP4	*uBP* / *uBM*	Bus signals of the receiver as close as possible to the chip

9.1.2.2 Digital signals

The test planes at the FlexRay node for digital signals (observed by the logic analyzer) are specified as:

Figure 29 depicts the test planes at the nodes (digital signals).



Components | **Connections and supplies**

IUT Implementation Under Test | (see Table 28)

Figure 29 — Test planes at the nodes (digital signals)

Table 28 depicts the test planes at the nodes (digital signals).

Table 28 — Test planes at the nodes (digital signals)

TP Name	Signals	Basis	Description
TP_Nx_TxEN	TxEN	V_{IO}/V_{CC}	Transmit Data Enable Not input signal of the IUT
TP_Nx_TxD	TxD	V_{IO}/V_{CC}	Transmit Data input signal of the IUT
TP_Nx_RxD	RxD	V_{IO}/V_{CC}	Receive Data output signal of the IUT
TP_Nx_ERRN	ERRN	V_{IO}/V_{CC}	Error Not output signal of the IUT (only if host interface A is implemented)
TP_Nx_STBN	STBN	V_{IO}/V_{CC}	Standby Not input signal of the IUT (only if host interface A is implemented)
TP_Nx_INTN	INTN	V_{IO}/V_{CC}	Interrupt Not output signal of the IUT (only if host interface B is implemented)
TP_Nx_SCSN	SCSN	V_{IO}/V_{CC}	The SCSN input signal of the SPI of the IUT (only if host interface B is implemented)
TP_Nx_EN	EN	V_{IO}/V_{CC}	Mode control input signal of the IUT (only if host interface A is implemented AND Functional Class "BD voltage regulator control" is implemented or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” are implemented)
TP_Nx_WAKE	WAKE	V_{BAT}	Local wakeup input signal input of the IUT (only if Functional Class "BD voltage regulator control" is implemented or Functional class “Bus driver internal voltage regulator” is implemented)
TP_Nx_INH1	INH1	V_{BAT}	INH1 output signal of the IUT (only if Functional Class "BD voltage regulator control" is implemented or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented)
TP_Nx_BGE	BGE	V_{IO}/V_{CC}	BG Enable input signal (only if Functional Class "Bus Driver - Bus Guardian control interface" is implemented)
TP_Nx_RxEN	RxEN	V_{IO}/V_{CC}	Receive Data Enable Not output signal of the IUT (only if Functional Class "Bus Driver - Bus Guardian control interface" is implemented)

9.1.2.3 Naming convention

The test planes used in this specification are divided in three parts for digital signals and two parts for analog signals. The naming convention is defined as:

— *TPy_Nx* for analog signals
y describes the location of the test plane
x represents the number of the node, see topology in 6.4

— *TP_Nx_YYY* for digital signals
x represents the number of the node, see topology in 6.4
YYY stands for the digital signal

— The analog test planes of the FlexRay bus are differential signals: *uBus* = *uBP* – *uBM*.

— The digital test planes of the digital signals are single ended signals: *uRxD*, *uTxD* and *uTxEN*.

EXAMPLE 1

TP_N1_RxD represents the test plane for the single ended signal RxD at node 1.

EXAMPLE 2

TP4_N23 represents the test plane for the differential analog bus signal of the receiver at node 23.

9.1.2.4 Test planes for the oscilloscope

The oscilloscope observes the following test planes:

— *TP_N23_RxD*

— *TP_N23_TxEN*

— *TP_N23_TxD*

— *TP1_N23* (if the node is a transmitter)

— *TP4_N23* (if the node is a receiver)

— *TP4_N2*

— *TP4_N12*

— *TP_N12_RxD*

— *TP_N24_TxD*

— *TP_N24_TxEN*

— *TP_N24_RxD*

— *TP_N24_BP*

— *TP_N24_BM*

— *Eye_TPAS4_B3*

— *TP_N23_UGS* (dynamic ground shift voltage)

9.1.2.5 Test planes for the logic analyzer

The logic analyzer shall observe the following test planes[18)]

— *TP_Nx_RxD*

— *TP_Nx_RxEN*

— *TP_Nx_TxD*

— *TP_Nx_TxEN*

— *TP_Nx_STBN*

— *TP_Nx_ERRN*

— *TP_Nx_INH1*

— *TP_Nx_WAKE*

— *TP_Nx_BGE*

— *TP_Nx_EN*

— *TP_Nx_INTN*

— *TP_Nx_SCSN*

9.1.2.6 Test planes for the pattern generator

The pattern generator shall stimulate the following test planes[19)]

— *TP_Nx_TxD*

— *TP_Nx_TxEN*

— *TP_Nx_BGE*

— *TP_N24_WAKE*

9.1.2.7 Test planes for current measurement

A shunt shall be implemented in order to measure the current of the bus wires[20)]

— $TP\_Nx\_R_{iBP}$

— $TP\_Nx\_R_{iBM}$

18) The node number depends on the test case

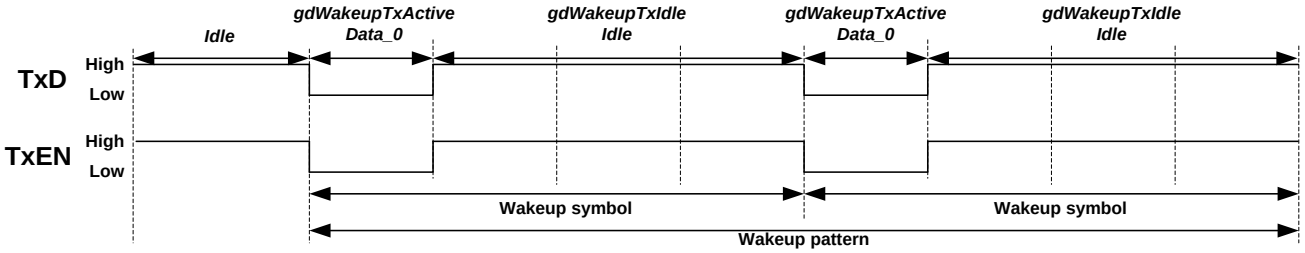
19) The node number depends on the test case

20) The node number depends on the test case

9.1.3 Test patterns

9.1.3.1 Wakeup

The wakeup signal is specified in ISO 17458-2 and shown in Figure 30.



Key

TxD	Transmit data
TxEN	Transmit enable not

Figure 30 — Wakeup test pattern

The length of *gdWakeupTxActive* and *gdWakeupTxIdle* shall be independent of the bus speed. The wakeup pattern shall be repeated *pWakeupPattern* times.

Length of *gdWakeupTxActive*: 60 *gdBit*

Length of *gdWakeupTxIdle*: 180 *gdBit*

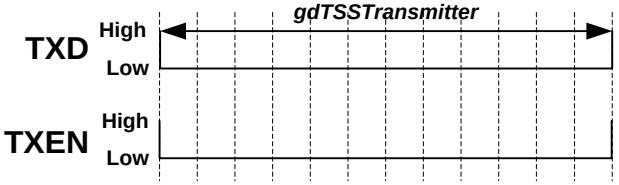
Number of repetitions of a wakeup symbol (*pWakeupPattern*): 2..24

When transmitting two wakeup symbols, a reaction of the **Bus Driver** on the wakeup is expected between 31 µs (6 µs + 18 µs + 6 µs + 1 µs = 31 µs) and 134 µs (6 µs + 18 µs + 6 µs + 4 µs + 100 µs = 134 µs) after the beginning of the stimulation.

When transmitting two wakeup symbols, a reaction of the **Active Star** on the wakeup is expected between 31 µs (6 µs + 18 µs + 6 µs + 1 µs = 31 µs) and 104 µs (6 µs + 18 µs + 6 µs + 4 µs + 70 µs = 104 µs) after the beginning of the stimulation.

9.1.3.2 TSS

The TSS symbol is specified in ISO 17458-2 and shown in Figure 31:



Key

TxD	Transmit data
TxEN	Transmit enable not

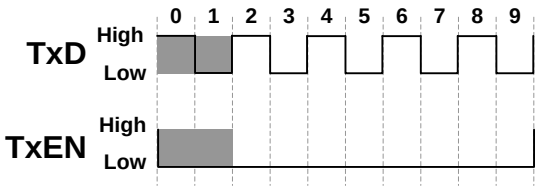
Figure 31 — Test pattern for the TSS symbol

The length of the TSS depends on *gdTSSTransmitter* (1..15 gdBit) and the bus speed (see ISO 17458-2) and is specified in Annex A.

The pattern of *gdTSSTransmitter* is sent in each test case once with a length of 11 bit, i.e. 1 100 ns.

9.1.3.3 Data signal 50/50

This test signal has a duty cycle of 50 % (including the BSS) as shown in Figure 32.



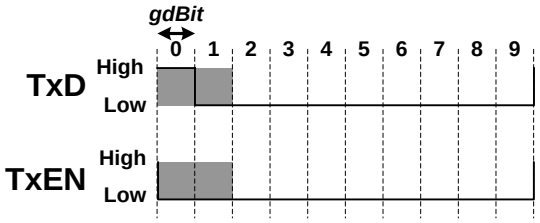
Key

TxD	Transmit data
TxEN	Transmit enable not

Figure 32 — Test pattern for data signal 50-50

9.1.3.4 Data signal 10/90

This test signal has a duty cycle of 10/90, that means that 1 bit has high and 9 bit have low level (including the BSS) as shown in Figure 33.



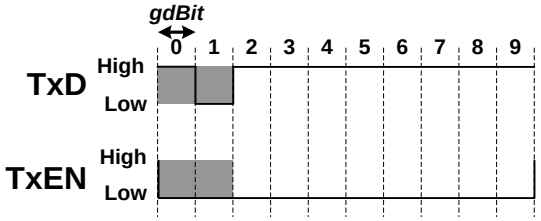
Key

TxD	Transmit data
TxEN	Transmit enable not

Figure 33 — Test pattern for data signal 10-90

9.1.3.5 Data signal 90/10

This test signal has a duty cycle of 90/10, that means that 9 bit have high and 1 bit has low level (including the BSS) an shown in Figure 34.



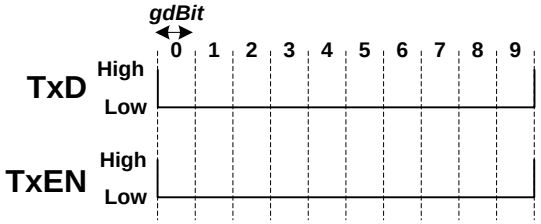
Key

TxD	Transmit data
TxEN	Transmit enable not

Figure 34 — Test pattern for data signal 90-10

9.1.3.6 Data signal 10Bit Low

The IUT shall signal *Data_0* on the bus with this test signal as shown in Figure 35.



Key

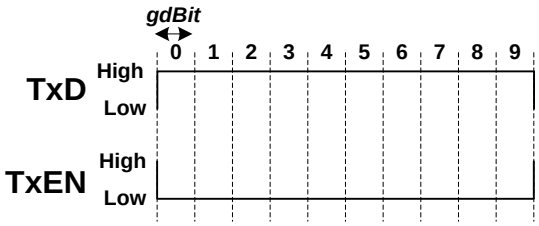
TxD	Transmit data
TxEN	Transmit enable not

Figure 35 — Test pattern 10 bit low

9.1.3.7 Data signal 10Bit High

This test signal is necessary to verify the *BD_Standby* state of the IUT. TxD shall stay in logical HIGH state.

Figure 36 depicts the test pattern 10 bit high.



Key

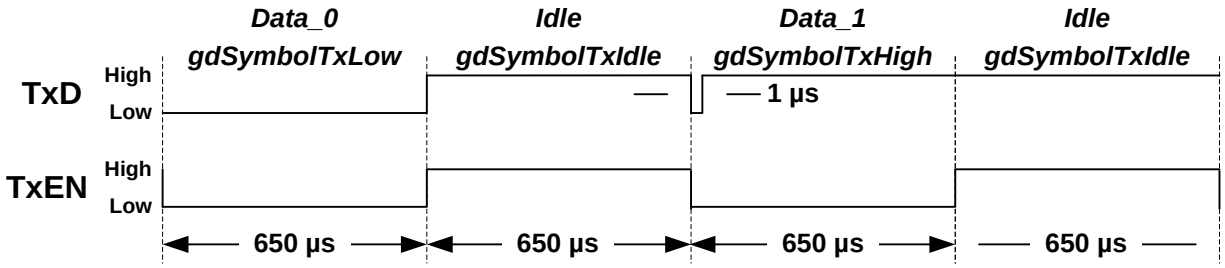
TxD Transmit data

TxEN Transmit enable not

Figure 36 — Test pattern 10 bit high

9.1.3.8 Current measurement

This test pattern shall be used to measure the current flowing from the BD into the bus wires. Figure 37 depicts the pattern for current measurement of bus wires.



Key

TxD Transmit data

TxEN Transmit enable not

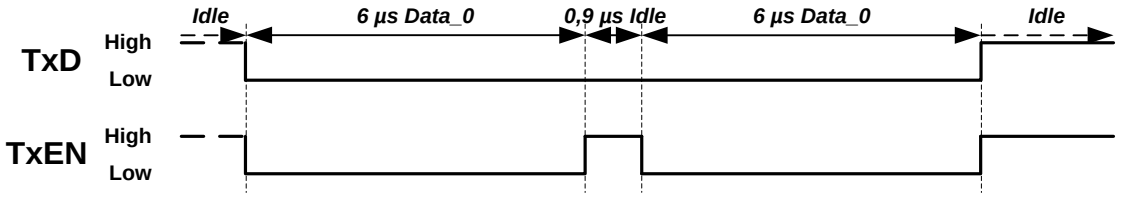
Figure 37 — Pattern for current measurement of bus wires

To avoid that the communication starts with *Data_1* a short *Data_0* phase is inserted. For the length of the Data_0 and Data_1 phases the minimum values of *dBDTxActiveMax* and *dBranchRxActiveMax* are used.

9.1.3.9 Non wakeup short idle phase

This test pattern shall be used to check the robustness of the IUT not to wakeup in case of a non suitable wakeup pattern due to a shorter idle phase.

Figure 38 depicts the test pattern for non suitable wakeup short idle phase.



Key

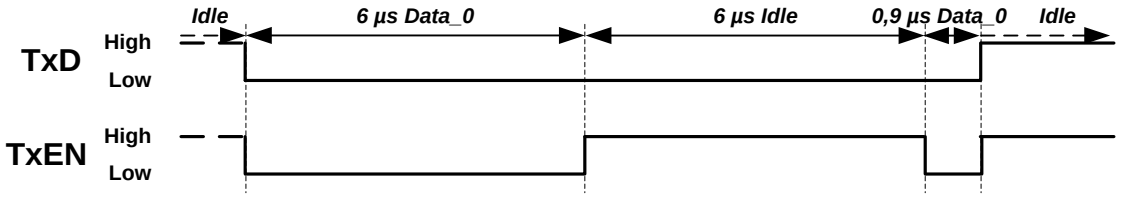
TxD	Transmit data
TxEN	Transmit enable not

Figure 38 — Test pattern for non suitable wakeup short idle phase

9.1.3.10 Non wakeup short low phase

This test pattern shall be used to check the robustness of the IUT not to wakeup in case of a non-suitable wakeup pattern due to a shorter low phase.

Figure 39 depicts the test pattern for non-suitable wakeup short low phase.



Key

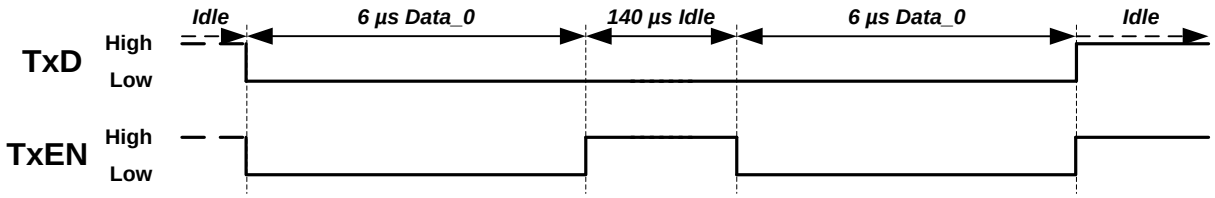
TxD	Transmit data
TxEN	Transmit enable not

Figure 39 — Test pattern for non-suitable wakeup short low phase

9.1.3.11 Non wakeup prolonged pattern

This test pattern shall be used to check the robustness of the IUT not to wakeup in case of a non suitable wakeup pattern due to a prolonged pattern.

Figure 40 depicts the test pattern for non suitable wakeup prolonged pattern.



Key

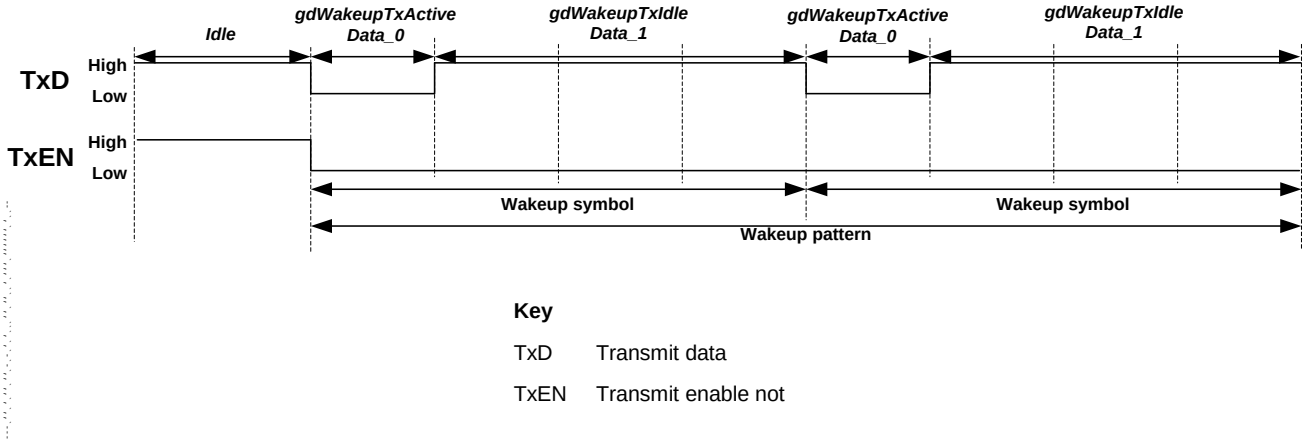
TxD	Transmit data
TxEN	Transmit enable not

Figure 40 — Test pattern for non suitable wakeup prolonged pattern

9.1.3.12 Alternative wakeup pattern

The alternative wakeup test pattern shall be used to wakeup the IUT with *Data_1* instead of *Idle* during the *gdWakeupTxIdle* phase.

Figure 41 depicts the alternative wakeup test pattern.



Key

TxD	Transmit data
TxEN	Transmit enable not

Figure 41 — Alternative wakeup test pattern

The length of *gdWakeupTxActive* (*Data_0*) and *gdWakeupTxIdle* (*Data_1*) shall be independent of the bus speed. The wakeup pattern shall be repeated *pWakeupPattern* times with the following parameters:

— Length of *gdWakeupTxActive*: 60 *gdBit*

— Length of *gdWakeupTxIdle*: 180 *gdBit*

— Number of repetitions of wakeup symbols (*pWakeupPattern*): 2

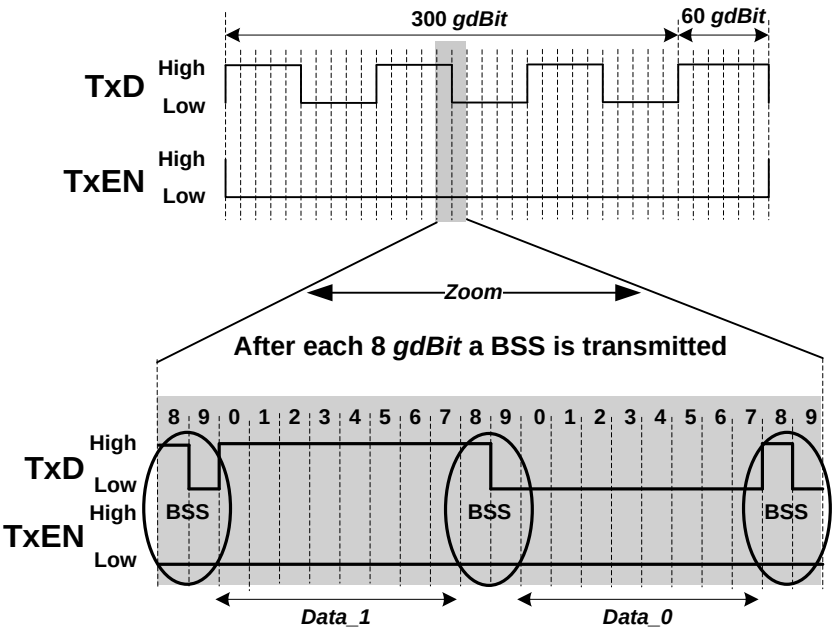
When transmitting one alternative wakeup pattern, a reaction of the **Bus Driver** on the wakeup is expected between 31 µs (6 µs + 18 µs + 6 µs + 1 µs = 31 µs) and
134 µs (6 µs + 18 µs + 6 µs + 4 µs + 100 µs = 134 µs) after the beginning of the stimulation.

When transmitting one alternative wakeup pattern, a reaction of the **Active Star** on the wakeup is expected between 31 µs (6 µs + 18 µs + 6 µs + 1 µs = 31 µs) and 104 µs (6 µs + 18 µs + 6 µs + 4 µs + 70 µs = 104 µs) after the beginning of the stimulation.

9.1.3.13 Wakeup frame payload

The wakeup frame shall be used to wake up the IUT with a 36 byte payload content to test the wakeup ability with frames in 10 Mbit/s systems. The payload consists of three alternating *Data_1* and *Data_0* plus one elongated *Data_1* phase at the end of the payload, i.e. seven phases as described in ISO 17458-4.

Before each byte, a byte start sequence (BSS) is transmitted, which consists of one bit HIGH, followed by one bit LOW as shown in Figure 42.



Key

TxD	Transmit data
TxEN	Transmit enable not

Figure 42 — Wakeup frame payload test pattern

— The wakeup pattern shall be transmitted *pWakeupPattern* times.

— Length of each *Data_0* phase (incl. BSS): 50 *gdBit*

— Length of each *Data_1* phase except the fourth (incl. BSS): 50 *gdBit*

— Length of the fourth *Data_1* phase (incl. BSS): 60 *gdBit*

— Number of repetitions (*pWakeupPattern*): 1

When receiving a wakeup frame, the reaction of the **Bus Driver** is expected latest 100 µs after the positive edge on TxEN signal at the transmitter node, i.e. after the end of the wakeup frame.

When receiving a wakeup frame, the reaction of the **Active Star** expected 70 µs after the positive edge on TxEN signal at the transmitter node, i.e. after the end of the wakeup frame.

9.1.3.14 Shorted Wakeup

This wakeup pattern is implemented for testing the reception of shorted remote wakeups which contain minimum *Data_0* and *Idle* phases as specified in ISO 17458-2. This pattern is almost the same as the wakeup

pattern described in 9.1.3.1 with the difference that shorter values for the *gdWakeupTxActive* and *gdWakeupTxIdle* phases are used:

— Length of *gdWakeupTxActive*: 41 *gdBit*

— Length of *gdWakeupTxIdle*: 41 *gdBit*

— Number of repetitions of a wakeup symbol (*pWakeupPattern*): 2

The length of *gdWakeupTxActive* and *gdWakeupTxIdle* shall be independent of the bus speed. The wakeup pattern shall be repeated *pWakeupPattern* times.

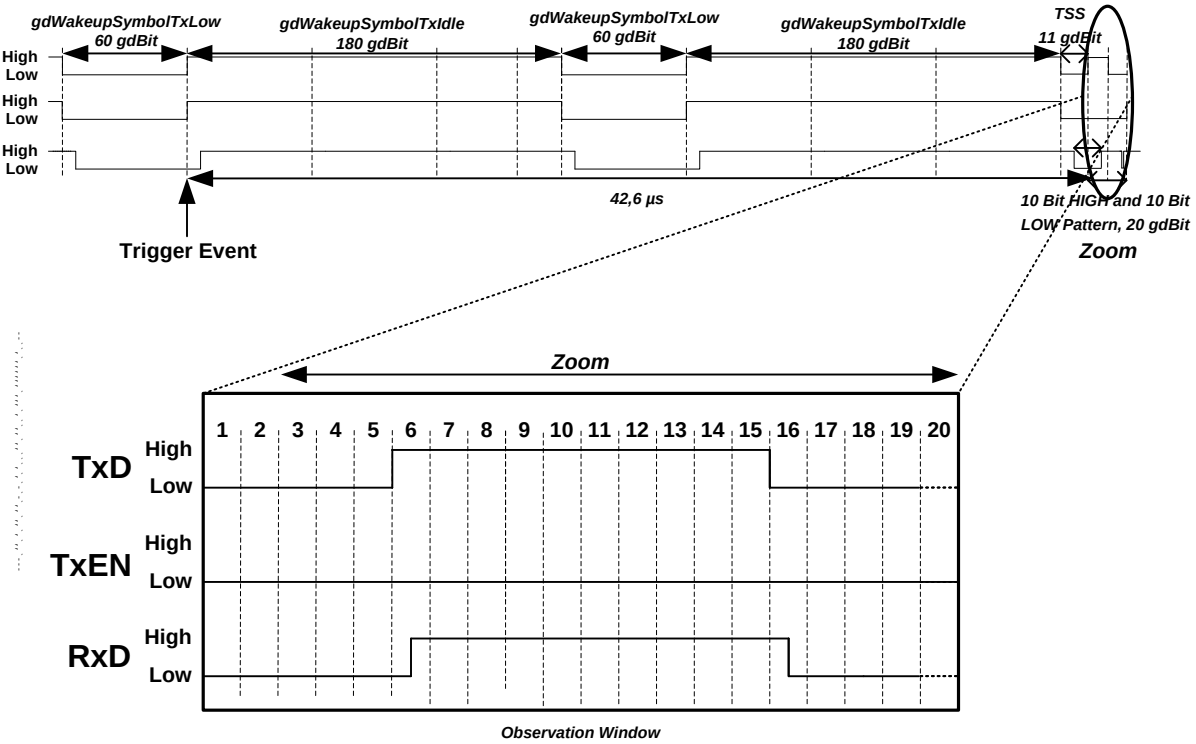
When receiving two short wakeup symbols, a reaction of the **Bus Driver** on the wakeup is expected between 13,3µs (4,1µs + 4,1µs + 4,1µs + 1µs = 13,3µs) and 116,3 µs (4,1 µs + 4,1 µs + 4,1 µs + 4 µs + 70 µs = 116,3 µs).

When receiving two short wakeup symbols, a reaction of the **Active Star** on the wakeup is expected between 13,3 µs (4,1 µs + 4,1 µs + 4,1 µs + 1 µs = 13,3 µs) and 86,3 µs (4,1 µs + 4,1 µs + 4,1 µs + 4 µs + 70 µs = 86,3 µs).

9.1.4 Observation windows

9.1.4.1 Parameters *dBDTx10*, *dBDTx01*, *dBDRx10* and *dBDRx01*

Figure 43 depicts the observation point for the analysis of the timing characteristics.



Key

TxD Transmit data

TxEN Transmit enable not

NOTE The measurement descriptions of the parameters [*dBDRx10*, *dBDRx01*] and [*dBDTx10*, *dBDTx01*] are shown in ISO 17458-4.

Figure 43 — Observation point for the analysis of the timing characteristics

— Trigger event: first positive edge of TxD or RxD signal (inside WUP).

— Trigger level: 70 % of V_{IO} (if implemented, otherwise V_{CC}) level

— Start acquisition point: 42,6 µs after the trigger event.

— Observation Window: 2,0 µs

9.1.4.2 Verification of bus in idle state (short)

The bus is verified to be in *Idle* or *Idle_LP* state at TP1/4 of node 23, node 24 or branch 4 of the Active Star:

— *Trigger event:* first negative edge of external trigger signal.

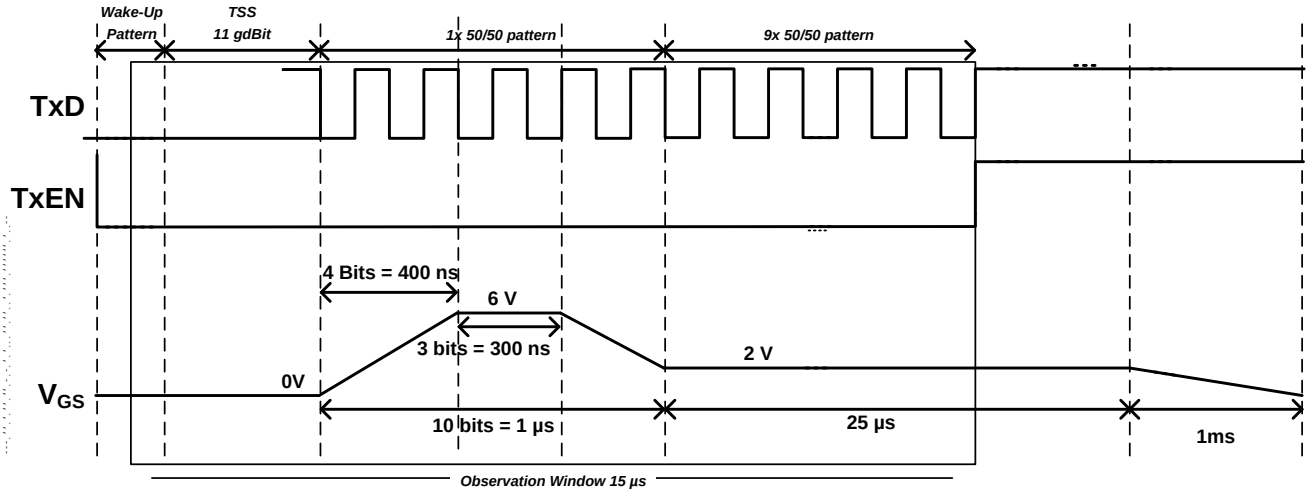
— *Start acquisition point:* 0 µs after the trigger event.

— Observation Window: 5,0 µs.

The absolute differential voltage |*uBus*| shall not exceed 30 mV (*uBDTxidle*).

9.1.4.3 Dynamic ground shift

Figure 44 depicts the observation point for dynamic ground shift.



Key

TxD	Transmit data
TxEN	Transmit enable not
V_{GS}	Ground shift voltage

Figure 44 — Observation point for dynamic ground shift

— *Trigger event:* first falling edge of TxD (within the first wakeup low phase), trigger level +2,0 V.

— *Start acquisition point:* 47 µs after the trigger event.

— Observation Window: 15 µs.

9.1.4.4 Verification of bus in idle state (long)

The bus is verified to be in *Idle* or *Idle_LP* state at TP1/4 of node 23 or at the Active Star.

— *Trigger event:* first negative edge of external trigger signal.

— *Start acquisition point:* 0 µs after the trigger event.

— Observation Window: 1,2 s.

The absolute differential voltage |*uBus*| shall not exceed 30 mV (*uBDTxidle*).

9.1.5 Operation modes of the Bus Driver

The IUT is expected to have the following operation modes:

— *BD_Normal*: receive/transmit possible.

— *BD_Standby*: receive/transmit NOT possible.

— *BD_Sleep*: optional: receive/transmit NOT possible.

— *BD_ReceiveOnly*: optional: receive possible, transmit NOT possible.

Table 29 defines the operation modes of the Bus Driver.

Table 29 — Operation modes of the Bus Driver

Operation mode	Hard Wired Signals	SPI
BD_Normal	STBN = High EN (optional [b]) = High	Product specific. Part of the implementation.
BD_Standby	STBN = Low EN (optional [b]) = Low	Product specific. Part of the implementation.
BD_Sleep	STBN = Low EN (optional [b]) = High	Product specific. Part of the implementation.
BD_ReceiveOnly [a]	STBN = High EN (optional [b]) = Low	Product specific. Part of the implementation.
[a] The number of the node depends on the test case.		
[b] Only available if functional class "BD voltage regulator control" is implemented		

9.1.6 Power supplies

9.1.6.1 The used power supplies of the nodes

— In case of a V_{BAT} pin the V_{BAT} supply is connected to the IUT with different voltages.
V_{BAT}= $V_{BATUndervoltage}$, +5,5 V, +7,0 V, default[21)]

— In case of a V_{CC} pin the V_{CC} supply is connected to the IUT with different voltages.
V_{CC}= $V_{CCUndervoltage}$, +5,0 V.

All other supplies are optional and part of the implementation.

9.1.6.2 The used power supplies of the Active Star

The Active Star shall be supplied as follows:

— The $V_{StarSupply}$ is the power supply of the Active Star. The datasheet of the IUT shall state what supply is. It may depend on V_{BAT}, V_{CC} or on both.

— In case that V_{CC} is implemented:
V_{CC} power supply of Active Star: +5,0 V.

— In case that V_{BAT} is implemented:
V_{BAT} power supply of Active Star: default[22)]

21) The default voltage of V_{BAT} is the maximal battery operational range defined in the data sheet of the IUT up to +42 V, see 6.5.2.

22) The default voltage of V_{BAT} is the maximal battery operational range defined in the data sheet of the IUT up to +42 V, see 6.5.2.

— In case that V_{IO} is implemented:

  — V_{IO} reference voltage of Active Star: depends on implementation (see 6.5.4).

9.1.7 Stress

— The ground shift is located as shown in Figure 14 in 7.1.

— The low battery is a global stress parameter and affects all nodes of the topology.

NOTE The Active Star is not stressed at all in Bus Driver test cases. The Active Star is always supplied with all implemented supply voltages and not stressed by low battery or ground shift.

9.1.8 Failures

The failures are located as shown in Figure 19 in 7.6.

9.1.9 Optional features

The following features are optional as specified in ISO 17458-4 and shall be tested in the test cases if available in the IUT:

— BD mode *BD_Sleep*

— BD mode *BD_ReceiveOnly*

— Signal BGE

— Signal INH1

— Signal RxEN

— Signal WAKE

— Signal EN

— Power supply input V_{IO}

— Power supply input V_{CC}

— Power supply input V_{BAT}

9.1.9.1 Functional class “Bus Driver voltage regulator control”

This functional class requires the following optional features to be implemented in coexistence:

— Power supply input V_{BAT}

— Power supply input V_{CC}

— Signal WAKE (optional within this functional class)

— Signal INH1

— BD mode *BD_Sleep*

— Signal EN (in case the host interface is not a SPI)

— Implementation of the functional class “Bus Driver remote wakeup” (see 9.1.9.5)

9.1.9.2 Functional class “Bus Driver – bus guardian interface”

This functional class requires the following optional features to be implemented in coexistence:

— Signal BGE

— Signal RxEN (optional within this functional class)

9.1.9.3 Functional class “Bus Driver internal voltage regulator”

This functional class requires the following optional features to be implemented in coexistence:

— Power supply input V_{BAT}

— Signal WAKE (optional within this functional class)

— Optionally, the subgroup BDControl may be implemented within this functional class, including the following features:

  — Signal INH1

  — BD mode *BD_Sleep*

  — Signal EN

— Implementation of the functional class “Bus Driver logic level adaptation” (see 9.1.9.4) optional within this functional class

— Implementation of the functional class “Bus Driver remote wakeup” (see 9.1.9.5) optional within this functional class

— No V_{CC} supply input is present

9.1.9.4 Functional class “Bus Driver logic level adaptation”

This functional class comprises the implementation of a “V_{IO}” power supply input and requires that the thresholds of all digital inputs can be controlled by this voltage as well as all digital outputs are related to this voltage level.

9.1.9.5 Functional class “Bus Driver remote wakeup”

This functional class comprises the implementation of the option “Remote Wakeup event detector”.

9.1.9.6 Functional class “Bus Driver increased voltage amplitude transmitter”

This functional class requires that the minimum *uBDTxActive* shall be 900 mV.

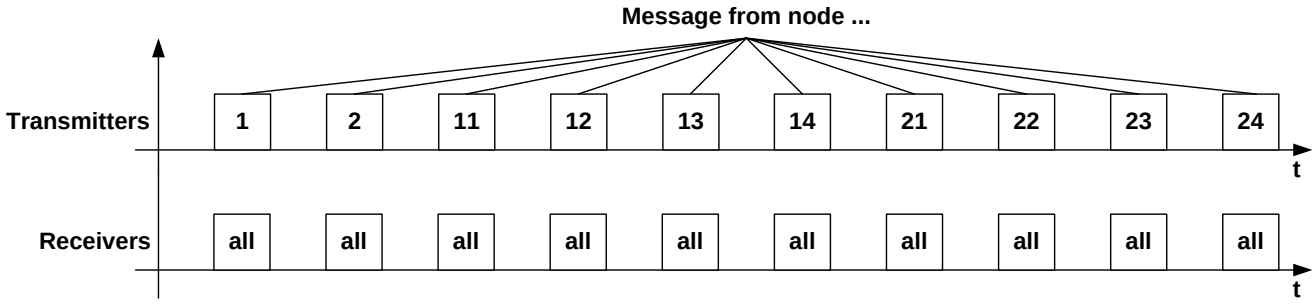
9.1.10 Definition of communication and control

9.1.10.1 Communication

Matrix A (round robin test):

In some test cases it is necessary that every node within the specified topology is the transmitter, i.e. the test case starts with node 1 as transmitter and the other nodes transmit one after another (all other nodes are receivers). This matrix is used for observation of digital signals.

Figure 45 depicts the communication matrix A.



NOTE The transmitting node is not part of the receiving nodes, i.e. the receivers are all nodes except the transmitter.

Figure 45 — Communication matrix A

Pause between the messages[23)] : 20 µs.

Node 11 as transmitter:

In some test instances node 11 is the transmitter and node 12 that is observed by the oscilloscope is the receiver.

Figure 46 depicts the communication with node 11 as transmitter (time diagram).

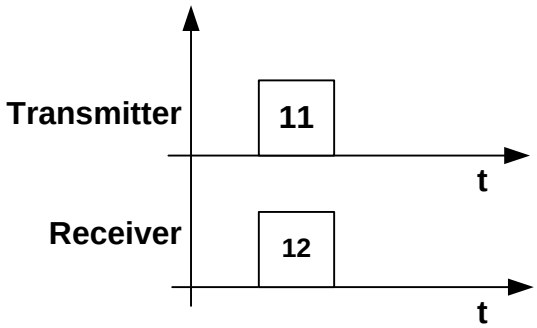


Figure 46 — Communication with node 11 as transmitter (time diagram)

Node 12 as transmitter:

23) A message is the whole test pattern (wakeup, TSS and data signal) which is sent by the transmitter and received by the receivers, see also 9.1.2.7.

In some test instances node 12 is the transmitter and node 23 that is observed by the oscilloscope is the receiver.

Figure 47 depicts the communication with node 12 as transmitter (time diagram).

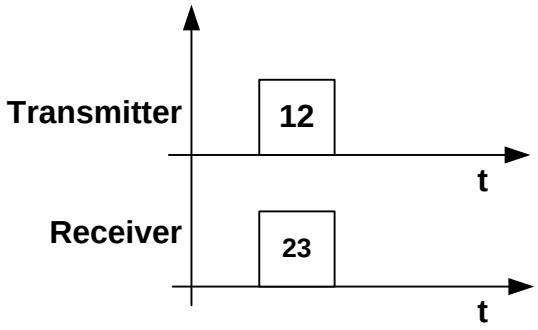


Figure 47 — Communication with node 12 as transmitter (time diagram)

Node 1 as transmitter:

In some test instances node 1 is the transmitter and node 2 that is observed by the oscilloscope is the receiver.

Figure 48 depicts the communication with node 1 as transmitter (time diagram).

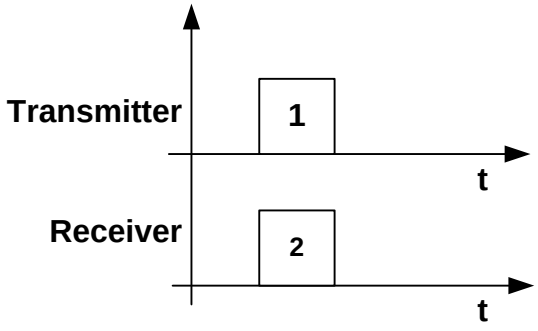


Figure 48 — Communication with node 1 as transmitter (time diagram)

Node 23 as transmitter:

In this communication node 23 is the transmitter and observed by the oscilloscope.

Figure 49 depicts the communication with node 23 as transmitter (time diagram).

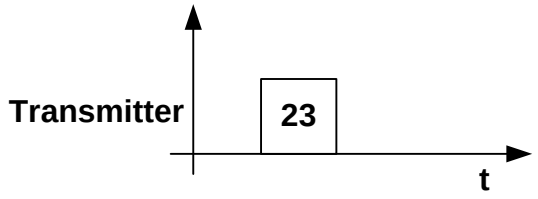


Figure 49 — Communication with node 23 as transmitter (time diagram)

Node 24 as transmitter:

In this communication node 24 is the transmitter and node 23 is observed by the oscilloscope.

Figure 50 depicts the communication with node 24 as transmitter (time diagram).

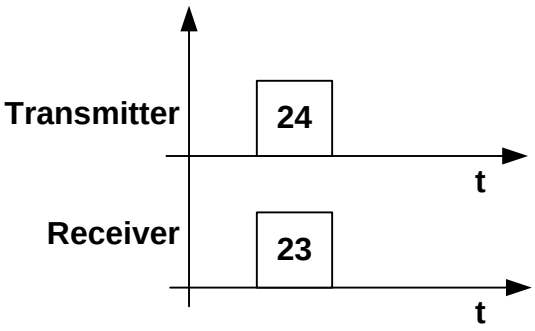


Figure 50 — Communication with node 24 as transmitter (time diagram)

Node 23 and 24 as transmitter:

In this communication node 23 and 24 are the transmitters with scope observation of the bus at node 23 and logic analyzer observation of both nodes.

Figure 51 depicts the communication with node 24 as observed transmitter (time diagram).

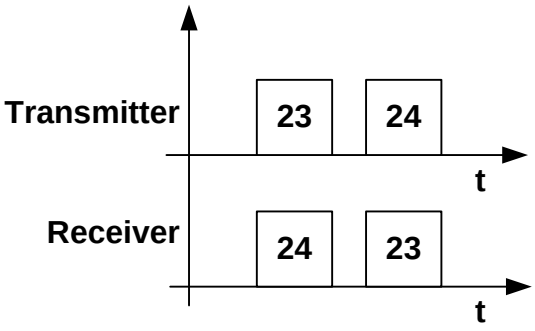


Figure 51 — Communication with node 23 and 24 as transmitter (time diagram)

Node 24 and node 23 as transmitter:

In this communication node 24 and 23 are the transmitters with scope observation of the bus at node 23 and logic analyzer observation of both nodes.

Figure 51 depicts the communication with node 24 as observed transmitter (time diagram).

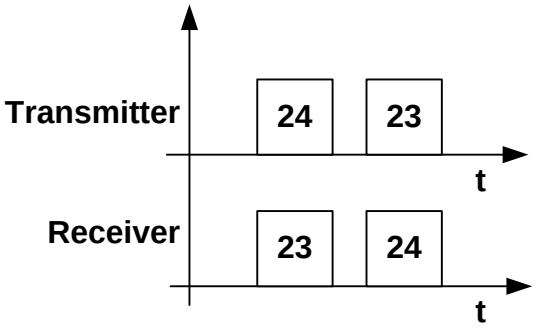


Figure 52 — Communication with node 24 and 23 as transmitter (time diagram)

Node 24 and 1 as transmitter:

In this communication node 24 and node 1 are the transmitters and all IUTs are observed by the logic analyzer.

Figure 53 depicts the communication with node 24 and 1 as transmitter (time diagram).

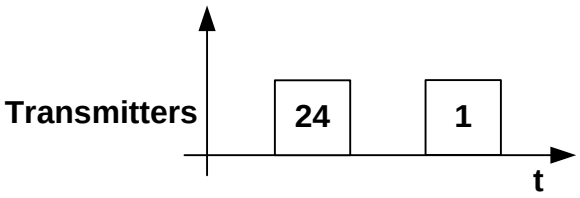


Figure 53 — Communication with node 24 and 1 as transmitter (time diagram)

9.1.10.2 Control

Host command:

Wait 100 µs (if hard wired host interface, i.e. option A is implemented) or 100 µs (if SPI, i.e. option B is implemented) after a host command to the IUT before performing the next step in the test execution. In that case the IUT is able to switch from one mode to the other.

The commanded nodes and the observed nodes are specified in the test cases.

9.1.11 Standard preamble

The standard preamble consists of the following configuration steps:

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure condition.

e) TxEN and TxD shall be in logical HIGH (idle) state.

f) In case of a BGE signal this signal shall be in logical HIGH state.

g) In case of a V_{IO} input this voltage shall be supplied by the voltage used in the implementation of the conformance test.

h) In case of a WAKE pin this signal shall be in logical HIGH state.

i) Stimulate all IUTs via the host interface to enter *BD_Normal*.

j) Wait 100 µs for the IUTs to enter *BD_Normal*.

k) Make sure that the Active Star is in *AS_Normal* mode when this preamble is left and the test execution is entered, e.g. by switching on the power supply of the Active Star just before the end of the preamble.

9.1.12 Standby preamble

The standby preamble consists of the following configuration steps:

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure condition.

e) TxEN and TxD shall be in logical HIGH (idle) state.

f) In case of a BGE signal this signal shall be in logical HIGH state.

g) In case of a V_{IO} input this voltage shall be supplied by the voltage used in the implementation of the conformance test.

h) In case of a WAKE pin this signal shall be in logical HIGH state.

i) Stimulate all IUTs via the host interface to enter *BD_Standby*.

j) Wait 100 µs for the IUTs to enter *BD_Standby*.

k) Make sure that the Active Star is in *AS_Normal* mode when this preamble is left and the test execution is entered, e.g. by switching on the power supply of the Active Star just before the end of the preamble.

9.1.13 Sleep preamble

The sleep preamble will only be used if the IUT has the functional class “BD voltage regulator control” (*BD_Sleep* mode) or the subgroup BDControl within the functional class “Bus Driver internal voltage regulator” (see 9.1.9.3) implemented. The needed host command will be product specific.

The sleep preamble consists of the following configuration steps:

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure condition.

e) TxEN and TxD shall be in logical HIGH (idle) state.

f) In case of a BGE signal this signal shall be in logical HIGH state.

g) In case of a V_{IO} input this voltage shall be supplied by the voltage used in the implementation of the conformance test.

h) In case of a WAKE pin this signal shall be in logical HIGH state.

i) Stimulate all IUTs via the host interface to enter *BD_Sleep*.

j) Wait 100 µs for the IUTs to enter *BD_Sleep*.

k) In case that hard wired signals as host interface are implemented, set the EN signal to logical LOW state.

l) Make sure that the Active Star is in *AS_Normal* mode when this preamble is left and the test execution is entered, e.g. by switching on the power supply of the Active Star just before the end of the preamble.

9.1.14 ReceiveOnly preamble

The ReceiveOnly preamble will only be used if the IUT has the *BD_ReceiveOnly* mode implemented. The needed host command will be product specific.

The ReceiveOnly preamble consists of the following configuration steps:

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure condition.

e) TxEN and TxD shall be in logical HIGH (idle) state.

f) In case of a BGE signal this signal shall be in logical HIGH state.

g) In case of a V_{IO} input this voltage shall be supplied by the voltage used in the implementation of the conformance test.

h) In case of a WAKE pin this signal shall be in logical HIGH state.

i) Stimulate all IUTs via the host interface to enter *BD_ReceiveOnly*.

j) Wait 100 µs for the IUTs to enter *BD_ReceiveOnly*.

k) Make sure that the Active Star is in *AS_Normal* mode when this preamble is left and the test execution is entered, e.g. by switching on the power supply of the Active Star just before the end of the preamble.

9.1.15 Standard postamble

The standard postamble consists of the following steps:

a) Set ground shift to 0 V.

b) Set to faultless configuration (reset failures).

c) Switch off power supplies.

9.1.16 Receiver masks

The path asymmetry is a very important parameter for the decoding of FlexRay signals. Each component in the physical layer may cause asymmetries, transmitters, Active Stars, receivers, but also passive network segments as passive busses or stars, connectors, ESD protection, etc. As a consequence, it is not enough to just sum up the allowed asymmetries for transmitters, receivers and Active Stars. These parameters are verified separately. The complete physical layer including the whole signal path may cause a path asymmetry as defined in ISO 17458-4.

Table 30 defines the allowed path asymmetry for a sequence of 10 bit logical LOW.

Table 30 — Allowed path asymmetry for a sequence of 10 bit logical LOW

FlexRay Parameter	Description	Min	Max	Unit
dCCRxAsymAccept15	*Acceptance of asymmetry at receiving CC*	-31,5	+44,0	ns

The accuracy/resolution of the logic analyzer as described in 6.5.9 shall be taken into account. The sequence of 10 bit logical LOW shall be enclosed by logical HIGH sequences, i.e. the bus shall change from *Data_1* to 10 bit times *Data_0* and back to *Data_1*.

The asymmetric channel delays shall be independent from the propagation delay.

9.2 Static test cases

The motivation of static test cases is to check the availability and the boundaries in the data sheet of the IUT (topology independent). Every parameter shall be part of the data sheet and fulfil the specified boundaries. If at least one parameter does not pass this test, the result of the whole conformance test is failed.

Table 31 defines the static test cases for Bus Drivers.

Table 31 — Static test cases for Bus Drivers

No.	Parameter	SOVS Brace	Description	Min	Max	Unit
1.	*dBDRxAsym*	Communication. Delay	Receiver delay mismatch[a b c]	—	5	ns
2.	*dBDRx10*	Communication. Delay	Receiver delay, negative edge [a b]	—	75	ns
3.	*dBDRx01*	Communication. Delay	Receiver delay, positive edge [a b]	—	75	ns

No.	Parameter	SOVS Brace	Description	Min	Max	Unit
4.	*dBDRxai*	Communication. Timing	Idle reaction time [d]	50	275	ns
5.	*dBDRxia*	Communication. Bus Driver.Timing	Activity reaction time [d]	100	325	ns
6.	*dBDTxAsym*	Communication. Delay	Transmitter delay mismatch [c e f]	—	4	ns
7.	*dBDTx10*	Communication. Delay	Transmitter delay, negative edge [e f g]	—	75	ns
8.	*dBDTx01*	Communication. Delay	Transmitter delay, positive edge [e f g]	—	75	ns
9.	*dBDTxai*	Communication. Bus Driver.Timing	Propagation delay active→idle [g]	—	75	ns
10.	*dBDTxia*	Communication. Timing.Bus Driver	Propagation delay idle→active [g]	—	75	ns
11.	*dBusTxai*	Communication. Signal Shape	Transition time active→idle [g]	—	30	ns
12.	*dBusTxia*	Communication. Signal Shape	Transition time idle→active [g]	—	30	ns
13.	*dBusTx01*	Communication. Signal Shape	Rise time differential voltage 20 %→80 % [f g]	6	18,75	ns
14.	*dBusTx10*	Communication. Signal Shape	Fall time differential voltage (80 % → 20 %) [f g]	6	18,75	ns
15.	$uBDTx_{active}$	Communication. Signal Shape	Absolute differential voltage while sending [f h i]	600	2000	mV
16.	$uBDTx_{idle}$	Communication. Signal Shape	Absolute differential voltage while *Idle* [f h j]	0	30	mV
17.	$uV_{DIG\text{-}OUT\text{-}HIGH}$	Communication. Threshold	Output voltage on a digital output, when in logical high state [k l m n]	80	100	%
18.	$uV_{DIG\text{-}OUT\text{-}LOW}$	Communication. Threshold	Output voltage on a digital output, when in logical low state [k l m n]	—	20	%
19.	$uV_{DIG\text{-}IN\text{-}HIGH}$	Communication. Threshold	Threshold for detecting a digital input as on logical high [l m]	—	70	%
20.	$uV_{DIG\text{-}IN\text{-}LOW}$	Communication. Threshold	Threshold for detecting a digital input as on logical low [l m]	30	—	%
21.	*uData0*	Communication. Threshold	Receiver threshold for detecting *Data_0* [o]	-300	-150	mV
22.	*uData1*	Communication. Threshold	Receiver threshold for detecting *Data_1* [o]	150	300	mV
23.	*uData1*-|*uData0*|	Communication. Threshold	Mismatch of receiver thresholds [p]	-30	+30	mV
24.	*dBDActivity Detection*	Communication. Timing.Bus Driver	Bus Driver filter time for activity detection	100	250	ns
25.	*dBDIdle Detection*	Communication. Timing.Bus Driver	Bus Driver filter time for *Idle* detection	50	200	ns

No.	Parameter	SOVS Brace	Description	Min	Max	Unit
26.	R_{CM1}, R_{CM2}	Environment	Receiver common mode input resistance [q]	10	40	kΩ
27.	*uCM*	Environment. Common Mode Voltages	Common mode voltage range that does not disturb the receive function [r s]	-10	+15	V
28.	*SPI* [t]	Host Interface. Bus Driver	Characteristics of the optional SPI Bus Driver to host interface [s]	0,01	1	Mbit /s
29.	$iBM_{GNDShortMax}$	Failure. Short-circuit.BM	Maximum output current when shorted to GND	—	60	mA
30.	$iBP_{GNDShortMax}$	Failure. Short-circuit.BP	Maximum output current when shorted to GND	—	60	mA
31.	$iBP_{BAT48ShortMax}$	Failure. Short-circuit.BP	Maximum output current when shorted to V_{BAT} = 48 V [u]	—	72	mA
32.	$iBM_{BAT48ShortMax}$	Failure. Short-circuit.BM	Maximum output current when shorted to V_{BAT} = 48 V [u]	—	72	mA
33.	$iBM_{BAT27ShortMax}$	Failure. Short-circuit.BM	Maximum output current when ocnnected to V_{BAT} = +27 V	—	60	mA
34.	$iBP_{BAT27ShortMax}$	Failure. Short-circuit.BP	Maximum output current when shorted to V_{BAT} = +27 V	—	60	mA
35.	*uBias – Non-Low Power*	Mode. Bus Driver. Normal	Voltage at BP & BM during bus state *Idle* [q v]	1 800	3 200	mV
36.	*uBias – Low Power*	Mode. Bus Driver. Low Power	Voltage at BP & BM during bus state *Idle_LP* [q v]	-200	+200	mV
37.	*dBDWake PulseFilter*	Mode. Bus Driver. Low Power. Wakeup	Duration of a valid wake pulse at local WAKE pin	1	500	µs
38.	$dWU_{0Detect}$	Mode. Bus Driver. Low Power. Wakeup	Time for detection of a *Data_0* phase in WU pattern	1	4	µs
39.	$dWU_{IdleDetect}$	Mode. Bus Driver. Low Power. Wakeup	Time for detection of an *Idle* phase in WU pattern	1	4	µs
40.	$dWU_{Timeout}$	Mode. Bus Driver. Low Power. Wakeup	Acceptance timeout for WU pattern recognition	48	140	µs
41.	$uV_{BAT\text{-}WAKE}$	Power Supply	Minimum battery voltage required for wakeup detector (local and remote) operation in case that V_{CC} is implemented	—	7	V
42.	*uBDUVVBAT*	Power Supply. Bus Driver. Undervoltage V_{BAT}	Undervoltage detection threshold for Bus Driver with undervoltage on V_{BAT}	4	5,5	V

No.	Parameter	SOVS Brace	Description	Min	Max	Unit
43.	*uBDUVVCC*	Power Supply. Bus Driver. Undervoltage V_{CC}	Undervoltage detection threshold for Bus Driver with undervoltage on V_{CC}	4	—	V
44.	*dBDUVV$_{CC}$*	Power Supply. Bus Driver. Undervoltage V_{CC}	Reaction time for V_{CC} undervoltage detection	—	1 000	ms
45.	*iBP$_{Leak}$*	Mode. Bus Driver. Off	Absolute leakage current when in *BD_Off* [w]	—	25	µA
46.	*iBM$_{Leak}$*	Mode. Bus Driver. Off	Absolute leakage current when in *BD_Off* [w]	—	25	µA
47.	Functional Class ”BD voltage regulator control”	Functional Class	Checks the complete implementation of all specified options	—	—	-
48.	Functional Class ”Bus Driver internal voltage regulator”	Functional Class	Checks the complete implementation of all specified options	—	—	-
49.	Functional Class ”Bus Driver logic level adaptation”	Functional Class	Checks the complete implementation of all specified options	—	—	-
50.	Functional Class ”Bus Driver – Bus guardian interface”	Functional Class	Checks the complete implementation of all specified options	—	—	
51.	Device qualification according to [13]		Checks the existence of this qualification in the datasheet			
52. [T]	T_{AMB_Class0}	Environment	Ambient temperature for class 0 [s x]	-40	+150	°C
53.	T_{AMB_Class1}	Environment	Ambient temperature for class 1 [s x]	-40	+125	°C
54.	T_{AMB_Class2}	Environment	Ambient temperature for class 2 [s x]	-40	+105	°C
55.	T_{AMB_Class3}	Environment	Ambient temperature for class 3 [s x]	-40	+85	°C
56.	*dBDTxDM*	Communication. Delay	Idle-active transmitter delay mismatch |*dBDTxia-dBDTxai*| [g]	-50	50	ns
57.	*iBM$_{-5VshortMax}$*	Failure. Short-circuit.BM	Maximum output current when shorted to V_{BAT} = -5 V	—	60	mA
58.	*iBP$_{-5VshortMax}$*	Failure. Short-circuit.BP	Maximum output current when shorted to V_{BAT} = -5 V	—	60	mA
59.	*iBM$_{BPShortMax}$*	Failure. Short-circuit.BM	Maximum output current when BM is shorted to BP	—	60	mA
60.	*iBP$_{BMShortMax}$*	Failure. Short-circuit.BP	Maximum output current when BP is shorted to BM	—	60	mA
61.	*iBM$_{BAT60ShortMax}$*	Failure. Short-circuit.BM	Maximum output current when shorted to V_{BAT} = +60 V	—	90	mA

No.	Parameter	SOVS Brace	Description	Min	Max	Unit
62.	*iBP*$_{BAT60ShortMax}$	Failure. Short-circuit.BP	Maximum output current when shorted to V_{BAT} =+60 V [u y]	—	90	mA
63.	*dBDUVV*$_{BAT}$	Power Supply. Bus Driver. Undervoltage V_{BAT}	Reaction time for V_{BAT} undervoltage detection	—	1 000	ms
64.	*uUV*$_{IO}$	Power Supply. Bus Driver. Undervoltage V_{IO}	Undervoltage detection threshold for Bus Driver with undervoltage on V_{IO}	2	—	V
65.	*dBDUVV*$_{IO}$	Power Supply. Bus Driver. Undervoltage V_{IO}	Reaction time for V_{IO} undervoltage detection	—	1 000	ms
66.	*dBDWakeup Reaction*$_{local}$	Mode. Bus Driver. Low Power. Wakeup	Bus Driver reaction time on a local wakeup event	—	100	µs
67.	*dBDWakeup Reaction*$_{remote}$	Mode. Bus Driver. Low Power. Wakeup	Bus Driver reaction time on a remote wakeup event	—	100	µs
68.	*dBDTxActive Max*	Communication.Bus Driver. Timing	Maximum length of transmitter activation	650	2 600	µs
69.	*dBDMode Change*	Host Interface. Bus Driver. hard wired signals	Mode transition time after (hard-wired) host command	—	100	µs
70.	*dBD ERRN*$_{Stable}$	Host Interface. Bus Driver. hard wired signals	Error signaling time on ERRN pin	1	10	µs
71.	*dReaction Time*$_{ERRN}$	Host Interface. Bus Driver. hard wired signals	*Reaction time on ERRN pin*	—	100	µs
72.	*dBDMode Change*$_{SPI}$	Host Interface. Bus Driver. SPI	Mode transition time after (SPI) host command	—	100	µs
73.	*dBDReaction Time*$_{SPI}$	Host Interface. Bus Driver. SPI	Time from detection of an event to falling edge of INTN	—	200	µs
74.	*uINH1*$_{Not\_Sleep}$	Communication. Threshold	Voltage on inhibit pin, when signaling *Not_Sleep* at 200 µA load, *uVBAT* > 5,5 V	*uVBAT* – 1 V	—	V
75.	*iINH1Leak*	Mode. Bus Driver. Low Power	Absolute leakage current while signaling *Sleep*	—	10	µA
76.	*uData0_LP*	Communication. Threshold	Low power receiver threshold for detecting *Data_0* [z]	-400	-100	mV
77.	*dWU*$_{Interrupt}$	Mode. Bus Driver. Low Power. Wakeup	*Acceptance timeout for interruptions*	0,13 [aa]	1	µs

No.	Parameter	SOVS Brace	Description	Min	Max	Unit
78.	*uBDLogic_1*	Communication. Threshold	*Threshold for detecting logical high*	—	60	%
79.	*uBDLogic_0*	Communication. Threshold	*Threshold for detecting logical low*	40	—	%
80.	$dBDRV_{CC}$	Power Supply. Bus Driver. Undervoltage V_{CC}	V_{CC} Undervoltage recovery time for Bus Drivers	—	10	ms
81.	$dBDRV_{BAT}$	Power Supply. Bus Driver. Undervoltage V_{BAT}	V_{BAT} Undervoltage recovery time for Bus Drivers	—	10	ms
82.	$dBDRV_{IO}$	Power Supply. Bus Driver. Undervoltage V_{IO}	V_{IO} Undervoltage recovery time for Bus Drivers	—	10	ms
83.	$iBP_{LeakGND}$	Failure. Loss.GND.IUT	Absolute leakage current in case of loss of GND [bb]	—	1 600	µA
84.	$iBM_{LeakGND}$	Failure. Loss.GND.IUT	Absolute leakage current in case of loss of GND [bb]	—	1 600	µA
85.	Functional Class ”Bus Driver Remote Wakeup”	Functional Class	Checks the complete implementation of all specified options	—	—	—
86.	Functional Class ”Increased Voltage Amplitude Transmitter”	Functional Class	Checks the complete implementation of all specified options	—	—	—
87.	$uESD_{EXT}$	Environment	ESD protection on pins that lead to ECU terminals [cc]	6	—	kV
88.	$uESD_{INT}$	Environment	ESD on all other pins	2	—	kV
89.	$uESD_{IEC}$	Environment	ESD protection on BP and BM	6	—	kV
90.	$dBDRxD_{R15}$ + $dBDRxD_{F15}$	Communication. Timing. Bus Driver	Sum of rise and fall time at 15 pF load [dd]	—	13	ns
91.	$\lvert dBDRxD_{R15} - dBDRxD_{F15} \rvert$	Communication. Timing. Bus Driver	Difference of rise and fall time at 15 pF load	—	5	ns
92.	C_*BDTxD*	Environment	Input capacitance on TxD pin	—	10	pF
93.	*dBDTxRxai*	Communication. Timing. Bus Driver	Idle-Loop delay	—	325	ns
94.	$uV_{DIG\text{-}OUT\text{-}UV}$	Communication. Threshold	*Output voltage on a digital output at 100 k*Ω load, when V_{DIG} in undervoltage [ee]	—	500	mV
95.	Operation modes in case of $V_{BAT} \geq 5{,}5$ V and V_{CC} = nominal (if implemented)	—	The Bus Driver shall be able to operate in all operation modes (in case that V_{CC} is implemented, wakeup detection is not mandatory)	—	—	—

No.	Parameter	SOVS Brace	Description	Min	Max	Unit
96.	Operation modes in case of $V_{BAT} \geq 7$ V and V_{CC} = nominal	—	The Bus Driver shall be able to operate in all operation modes (wakeup detection mandatory)	—	—	—
97.	*$uV_{DIG\text{-}OUT\text{-}OFF}$*	Communication. Threshold	Output voltage on a digital output at 100 kΩ load, when unsupplied [ff] Checks the existence of this parameter in the datasheet	product specific	product specific	
98.	*$R_{BDTransmitter}$*	Simulation	Bus Driver – Bus interface simulation resistor	product specific	product specific	
99.	*RxD signal sum of rise and fall time at TP4_CC*	Simulation	Between 20 % and 80 % V_{DIG} at 10 pF load at the end of a 50 Ω, 1 ns microstripline	—	16,5	ns
100.	*$uV_{BAT\text{-}WAKE}$*	Power Supply	Minimum battery voltage required for wakeup detector (local and remote) operation in case that V_{CC} is not implemented	—	5,5	V
101.	*$dBDRxD_{R25}$* + *$dBDRxD_{F25}$*	Communication.Timing. Bus Driver	Sum of rise and fall time at 25 pF load [gg]	—	16,5	ns
102.	| *$dBDRxD_{R25}$* - *$dBDRxD_{F25}$* |	Communication.Bus Driver. Timing	Difference of rise and fall time at 25 pF load	—	5	ns
103.	*dBusTxDif*	Communication. Signal Shape	Difference between differential rise and all time | dBusTx10 - dBusTx01 |	—	3	ns
104.	Behaviour in case of SCK unconnected	Simulation	SCK (if implemented) shall have pull-down behaviour in case it is unconnected	—	—	—
105.	*RxD signal difference of rise and fall time at TP4_CC*	Simulation	Between 20 % and 80 % V_{DIG} at 10 pF load at the end of a 50 Ω, 1 ns microstripline	—	5	ns

[a] Load on RxD: 25 pF

[b] To be tested with a signal according to the definitions of ISO 17458-4

[c] Shall be guaranteed for +/-300 mV as well as for +/-150 mV level of *uBus*

[d] To be tested with a signal according to the definitions of ISO 17458-4

[e] For all TxD signals with a sum of rise and fall time (20 % to 80 % V_{DIG}) of up to 9 ns.

[f] The values shall be guaranteed, when the TxD signal is constant for 100 ns to 4 400 ns before the first edge and also in case the test is performed with the opposite polarity (see ISO 17458-4).

[g] Load on BP / BM: 40 Ω || 100 pF

[h] Load on BP / BM: (40 .. 55) Ω || 100 pF

[i] In case the functional class “Bus Driver increased voltage amplitude transmitter” or the functional class “Active Star increased voltage amplitude transmitter” is implemented, the minimum of *uBDTxActive* or *uStarTxAcive* shall be shifted to 900 mV.

[j] *uBus* shall be measured with a limited bandwidth not lower than 20 MHz before comparing with the limit of

No.	Parameter	SOVS Brace	Description	Min	Max	Unit

uBDTxidle.

k Load conditions are product specific and documented in the product datasheet.

l In case a reference voltage for digital IO is available via a V_{IO} pin, then $uV_{DIG} = uV_{IO}$, otherwise $uV_{DIG} = uV_{CC}$.

m Relative to V_{DIG}

n The values shall be guaranteed, when the TxD signal is constant for (100 .. 4 400) ns before the first edge and also in case the test is performed with the opposite polarity (see also ISO 17458-4)

o Prerequisite for detecting *Data_0* or *Data_1* is detection of activity previously. *Data_0* and *Data_1* shall be reliably detected with uBus in the range of up to ±3 000 mV.

p Test with (*uBP* + *uBM*) / 2 = *uCM* = 2,5 V

q Prerequisite is that BD is connected to GND and uV_{CC} = 5 V (if applicable) and $uV_{BAT} \geq 7$ V (if applicable)

r *uCM* = (*uBP* + *uBM*) / 2. To be tested on a receiving Bus Driver with a sending Bus Driver that has a ground offset voltage in the range of [-12,5 V .. +12,5 V] and sends a 50 / 50 pattern.

s The device shall be in the range given in ISO 17458-4.

t The values represent the range of the transfer speed which shall be guaranteed by the IUT.

u These limitations are only valid for devices that are meant to be used in 42 V board net systems.

v Load on BP/BM: (40 .. 55) Ω || 100 pF. Nominal voltage of *uBias* is 2 500 mV in normal mode and 0 mV in low power modes.

w Test conditions: *uBP* = *uBM* = 5 V, all other pins connected to GND. GND pin connected directly to 0 V.

x At least one of the classes shall be implemented.

y 400 ms originated from load dump conditions.

z Given the prerequisite that $uV_{BAT} \geq 7$ V (if applicable, otherwise uV_{CC} = 5 V)

aa The minimum value is only guaranteed, when the phase that is interrupted was continuously present for at least 870 ns.

bb Test conditions: *uBP* = *uBM* = 0 V, all other pins connected via 0 Ω to 16 V.

cc Typically: BM, BP, WAKE and V_{BAT}

dd 20 % to 80 % of V_{DIG}. A datasheet for the BD/CC/AS shall state maximum rise and fall time on RxD/TxD separately.

ee Condition: V_{CC} or V_{BAT} supplied, depending on the product specific supply thresholds below undervoltage thresholds, e.g. in *BD_Off* or *AS_Off* mode.

ff Product specific supply thresholds below undervoltage thresholds, e.g. in *BD_Off* or *AS_Off* mode.

gg 20 % – 80 % V_{DIG}, a datasheet for the BD/CC/AS shall state maximum rise and fall time on RxD/TxD separately.

9.3 Test cases

9.3.1 Communication.Delay.*dBDTx01*

9.3.1.1 Transmitter delay *dBDTx01*

Table 32 defines the test case for the transmitter delay dBDTx01.

Table 32 — Test case for the transmitter delay *dBDTx01*

Name	Transmitter delay *dBDTx01*
Test purpose	This test checks the transmitter delay *dBDTx01* from *low* to *high* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} supply input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23 according to the observation window described in 9.1.4.1. b) Observe and acquire *uBus* at *TP1_N23* of node 23 according to the observation window described in 9.1.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N23_INH1* of node 23. d) Stimulate the IUT of node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 10Bit High pattern, followed by one 10Bit Low pattern.
Postamble	Standard postamble.
Pass criteria	— *dBDTx01* ≤ 75 ns.

Name	Transmitter delay *dBDTx01*
	— in case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 33 defines the test instances for transmitter delay *dBDTx01* test case defined in Table 32.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 33 — Test instances for transmitter delay *dBDTx01*

Instance		**1**	**2**	**3**	**4**	**5**	**6**
Purpose	**Stress**	none	ground shift at transmitter	ground shift at receiver	low battery	min. bus load	max. bus load
	Precondition	—	—	—	BD_VRCor BD_IVR impl.	—	—
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V	—	—
	Ground shift	—	+5,0 V at N23	+5,0 V at N24	—	—	—
	Failure	—	—	—	—	FL7 at N23	FL8 at N23
Preamble		—	—	—	—	—	—
Test execution		—	—	—	—	—	—
Pass criteria		—	—	—	—	—	—

9.3.2 Communication.Delay.*dBDTx10*

9.3.2.1 Transmitter delay *dBDTx10*

Table 34 defines the test case for transmitter delay dBDTx10.

Table 34 — Test case for transmitter delay *dBDTx10*

Name	Transmitter delay *dBDTx10*
Test purpose	This test checks the transmitter delay *dBDTx10* from *high* to *low* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23 according to the observation window described in 9.1.4.1. b) Observe and acquire *uBus* at *TP1_N23* of node 23 according to the observation window described in 9.1.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N23_INH1* of node 23. d) Stimulate the IUT of node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 10Bit High pattern, followed by one 10Bit Low pattern.
Postamble	Standard postamble.
Pass criteria	— *dBDTx10* ≤ 75ns. — in case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 35 defines the test instances for transmitter delay dBDTx10 test case defined in Table 34.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 35 — Test instances for transmitter delay *dBDTx10*

Instance		1	2	3	4	5	6
Purpose	**Stress**	none	ground shift at transmitter	ground shift at receiver	low battery	min. bus load	max. bus load
	Precondition	—	—	—	BD_VRCor BD_IVR impl.	—	—
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V	—	—
	Ground shift	—	+5,0 V at N23	+5,0 V at N24	—	—	—
	Failure	—	—	—	—	FL7 at N23	FL8 at N23
Preamble		—	—	—	—	—	—
Test execution		—	—	—	—	—	—
Pass criteria		—	—	—	—	—	—

9.3.3 Communication.Delay.*dBDRx01*

9.3.3.1 Receiver delay *dBDRx01*

Table 36 defines the test case for receiver delay dBDRx01.

Table 36 — Test case for receiver delay *dBDRx01*

Name	Receiver delay *dBDRx01*
Test purpose	This test checks the receiver delay *dBDRx01* from *low* to *high* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 12 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uRxD* at *TP_N23_RxD* of node 23 according to the observation window described in 9.1.4.1. b) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N23_INH1* of node 23. d) In case node 12 is the transmitter, stimulate the IUT of node 12 at *TP_N12_TxD* and *TP_N12_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 10Bit High pattern, followed by one 10Bit Low pattern. In case node 24 is the transmitter, stimulate the same pattern sequence at *TP_N24_TxD* and *TP_N24_TxEN*
Postamble	Standard postamble.
Pass criteria	— *dBDRx01* ≤ 75 ns. — in case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 37 defines the test instances for receiver delay dBDRx01 test case defined in Table 36.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 37 — Test instances for receiver delay *dBDRx01*

Instance		**1**	**2**	**3**	**4**	**5**	**6**
Purpose	**Stress**	none	ground shift at transmitter	ground shift at receiver	low battery	min. bus load	max. bus load
	Precondition	—	—	—	BD_VRCor BD_IVR impl.	—	—
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V	—	—
	Ground shift	—	+5,0 V at N24	+5,0 V at N23	—	—	—
	Failure	—	—	—	—	FL7 at N23	FL8 at N23
Preamble		—	—	—	—	—	—
Test execution		—	N24 as transmitter	—	—	—	—
Pass criteria		—	—	—	—	—	—

9.3.4 Communication.Delay.*dBDRx10*

9.3.4.1 Receiver delay *dBDRx10*

Table 38 defines the test case for receiver delay dBDRx10.

Table 38 — Test case for receiver delay *dBDRx10*

Name	Receiver delay *dBDRx10*
Test purpose	This test checks the receiver delay *dBDRx10* from *high* to *low* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 12 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uRxD* at *TP_N23_RxD* of node 23 according to the observation window described in 9.1.4.1. b) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N23_INH1* of node 23. d) In case node 12 is the transmitter, stimulate the IUT of node 12 at TP_N12_TxD and TP_N12_TxEN by one wakeup pattern, followed by one TSS pattern, followed by one 10Bit High pattern, followed by one 10Bit Low pattern. In case node 24 is the transmitter, stimulate the same pattern sequence at TP_N24_TxD and TP_N24_TxEN
Postamble	Standard postamble.
Pass criteria	— *dBDRx10* ≤ 75 ns. — in case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 39 defines the test instances for receiver delay dBDRx10 test case defined in Table 38.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 39 — Test instances for receiver delay *dBDRx10*

Instance		**1**	**2**	**3**	**4**	**5**	**6**
Purpose	**Stress**	none	ground shift at transmitter	ground shift at receiver	low battery	min. bus load	max. bus load
	Precondition	—	—	—	BD_VRC or BD_IVR impl.	—	—
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V	—	—
	Ground shift	—	+5,0 V at N24	+5,0 V at N23	—	—	—
	Failure	—	—	—	—	FL7 at N23	FL8 at N23
Preamble		—	—	—	—	—	—
Test execution		—	N24 as transmitter	—	—	—	—
Pass criteria		—	—	—	—	—	—

9.3.5 Mode.Bus Driver.Low Power.Standby

9.3.5.1 Operation mode change from *BD_Normal* to *BD_Standby* due to host command

Table 40 defines the test case for operation mode change from BD_Normal to BD_Standby due to host command.

Table 40 — Test case for operation mode change from *BD_Normal* to *BD_Standby* due to host command

Name	Operation mode change from *BD_Normal* to *BD_Standby* due to host command
Test purpose	This test checks the ability of the IUT to change from *BD_Normal* mode to *BD_Standby* due to host command according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. b) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. c) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. d) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. e) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. f) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. g) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of

Name	Operation mode change from *BD_Normal* to *BD_Standby* due to host command
	node 24.c i) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. j) Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. k) Wait 100 µs (the IUT shall change to *BD_Standby*). l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. m) Trigger the scope to start the observation synchronously with the stimuli at node 24. n) Wait until end of the scope observation window, i.e. 5,0 µs. o) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	— *uBus* at \ of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of TxEN of node 24. The absolute bus voltage shall not exceed 30 mV (*uBDTxidle*). — *uRxD* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution.

Table 41 defines the test instances for operation mode change from *BD_Normal* to *BD_Standby* due to host command test case defined in Table 40.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 41 — Test instances for operation mode change from *BD_Normal* to *BD_Standby* due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.2 Operation mode change from *BD_Sleep* to *BD_Standby* due to remote wakeup

Table 42 defines the test case for operation mode change from BD_Sleep to BD_Standby due to remote wakeup.

Table 42 — Test case for operation mode change from *BD_Sleep* to *BD_Standby* due to remote wakeup

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to remote wakeup
Test purpose	This test checks the ability of the IUT to change from *BD_Sleep* mode to *BD_Standby* due to a remote wakeup according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — neither the Functional class “Bus Driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus Driver internal voltage regulator” is implemented — the Functional class “Bus Driver remote wakeup” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes except node 24. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 24. e) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of all nodes. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 24. g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one wakeup

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to remote wakeup
	pattern as described in 9.1.3.1.
Postamble	Standard postamble.
Pass criteria	— *uINH1* of all observed nodes shall be in logical LOW state (*Sleep*) at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uINH1* of all observed nodes shall be in logical HIGH state (*Not_Sleep*), i.e. the IUTs are in *BD_Standby* mode. — *uRxD* of all observed nodes shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uRxD* of all observed nodes shall be in logical LOW state. — In case of an available RxEN signal *uRxEN* all observed nodes shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uRxEN* of all observed nodes shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal shall be LOW at the host interface of all observed nodes except node 24 after the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 100 µs after the beginning of the wakeup pattern). — In case that SPI as host interface is implemented: The error signal shall be LOW at the host interface of all observed nodes except node 24 after the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 200 µs after the beginning of the wakeup pattern). — The error signal shall be HIGH at the host interface of node 24 during the test execution.

Table 43 defines the test instances for operation mode change from *BD_Sleep* to *BD_Standby* due to remote wakeup test case defined in Table 42.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 43 — Test instances for operation mode change from *BD_Sleep* to *BD_Standby* due to remote wakeup

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.3 Operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (negative pulse)

Table 44 defines the test case for operation mode change from BD_Sleep to BD_Standby due to local wakeup (negative pulse).

Table 44 — Test case for operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (negative pulse)

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (negative pulse)
Test purpose	This test checks the ability of the IUT to change from *BD_Sleep* mode to *BD_Standby* due to a local wakeup (LWU) event according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — neither the Functional class “Bus Driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus Driver internal voltage regulator” is implemented — the local wakeup is not implemented
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	Sleep preamble.
Test execution	a) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. b) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire the error signal of the host interface (TP_N24_ERRN or TP_N24_INTN) of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Apply a negative wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4.

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (negative pulse)
Postamble	Standard postamble.
Pass criteria	— *uINH1* shall be in logical LOW state (*Sleep*) while the IUT of node 24 is in *BD_Sleep* mode, at least until 1 µs after the falling edge of *uWAKE.* After the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs after the beginning of the local wakeup event), *uINH1* shall be in logical HIGH state (*BD_Standby*: *Not_Sleep*). — *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE.* After the wakeup event is detected (latest 100 µs + 500 µs after the falling edge of *uWAKE*), *uRxD* of node 24 shall be in logical LOW state. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE.* After the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs after the beginning of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal shall be LOW at the host interface of node 24 after the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs + 100 µs after the beginning of the local wakeup event). — In case that SPI as host interface is implemented: The error signal shall be LOW at the host interface of node 24 after the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs + 200 µs after the beginning of the local wakeup event).

Table 45 defines the test instances for Test case for operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (negative pulse) test case defined in Table 44.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 45 — Test instances for Test case for operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (negative pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.4 Operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (positive pulse)

Table 46 defines the test case for operation mode change from BD_Sleep to BD_Standby due to local wakeup (positive pulse).

Table 46 — Test case for operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (positive pulse)

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (positive pulse)
Test purpose	This test checks the ability of the IUT to change from *BD_Sleep* mode to *BD_Standby* due to a local wakeup (LWU) event according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the local wakeup (positive pulse) is not implemented — neither the Functional class “Bus Driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus Driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Sleep preamble. — Set *uWAKE* to logical LOW before the IUT is set to *BD_Sleep*.
Test execution	a) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. b) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Apply a positive wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE*

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (positive pulse)
	according to *dBDWakePulseFilter* in ISO 17458-4.
Postamble	Standard postamble.
Pass criteria	— *uINH1* shall be in logical LOW state (*Sleep*) while the IUT of node 24 is in *BD_Sleep* mode, at least until 1 µs after the rising edge of *uWAKE.* After the wakeup event is detected between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs after the beginning of the local wakeup event), *uINH1* shall be in logical HIGH state (*BD_Standby*: *Not_Sleep*). — *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of uWAKE. After the wakeup event is detected between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs after the beginning of the local wakeup event), uRxD of node 24 shall be in logical LOW state. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE.* After the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs after the beginning of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal shall be LOW at the host interface of node 24 after the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs + 100 µs after the beginning of the local wakeup event). — In case that SPI as host interface is implemented: The error signal shall be LOW at the host interface of node 24 after the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs + 200 µs after the beginning of the local wakeup event).

Table 47 defines the test instances for operation mode change from BD_Sleep to BD_Standby due to local wakeup (positive pulse) test case defined in Table 46.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 47 — Test instances for operation mode change from *BD_Sleep* to *BD_Standby* due to local wakeup (positive pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.5 Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to host command

Table 48 defines the test case for operation mode change from BD_ReceiveOnly to BD_Standby due to host command.

Table 48 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to host command

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to host command
Test purpose	This test checks the ability of the IUT to change from *BD_ReceiveOnly* mode to *BD_Standby* due to host command according to ISO 17458-4 while no other stress condition is present. This test case is skipped if the BD_ReceiveOnly mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 24. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes except node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 24. f) Stimulate the IUTs of all nodes except node 24 via the host interface to enter *BD_Standby*.

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to host command
	g) Wait 100 µs (the IUTs shall change to *BD_Standby*). h) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 50/50 pattern.
Postamble	Stansdard postamble.
Pass criteria	All observed nodes shall not receive the transmission of node 24, but they should detect the transmitted wakeup pattern and bus activity as remote wakeup event. Thus, *uRxD* and *uRxEN* should change from logical HIGH state to logical LOW state during the test execution. — *uRxD* of all observed nodes shall not contain more than one falling edge (remote wakeup detection), i.e. the observed nodes shall not receive the patterns applied to *uTxD* and *uTxEN* of node 24. — In case of an available INH1 signal *uINH1* of all observed nodes shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of all observed nodes shall not contain more than one falling edge (remote wakeup detection).

Table 49 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Standby due to host command test case defined in Table 48.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 49 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.6 Operation mode change from *BD_Standby* to *BD_Standby* due to remote wakeup

Table 50 defines the test case for operation mode change from BD_Standby to BD_Standby due to remote wakeup.

Table 50 — Test case for operation mode change from *BD_Standby* to *BD_Standby* due to remote wakeup

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to remote wakeup
Test purpose	This test checks the ability of the IUT to change from *BD_Standby* mode to *BD_Standby* due to a remote wakeup according to ISO 17458-4 while no other stress condition is present. This test case is skipped if the Functional class “Bus Driver remote wakeup” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 24. d) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of all nodes. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes except node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 24. g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one wakeup

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to remote wakeup
	pattern as described in 9.1.3.1.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all observed nodes shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected *(*between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uRxD* of all observed nodes shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal shall be LOW at the host interface of all observed nodes except node 24 after the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 100 µs after the beginning of the wakeup pattern). — In case that SPI as host interface is implemented: The error signal shall be LOW at the host interface of all observed nodes except node 24 after the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 200 µs after the beginning of the wakeup pattern). — The error signal shall be HIGH at the host interface of node 24 during the test execution. — In case of an available INH1 signal *uINH1* of all observed nodes shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* all observed nodes shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected *(*between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uRxEN* of all observed nodes shall be in logical LOW state.

Table 51 defines the test instances for operation mode change from BD_Standby to BD_Standby due to remote wakeup test case defined in Table 50.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 51 — Test instances for operation mode change from *BD_Standby* to *BD_Standby* due to remote wakeup

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.7 Operation mode change from *BD_Standby* to *BD_Standby* due to local wakeup (negative pulse)

Table 52 defines the test case for operation mode change from BD_Standby to BD_Standby due to local wakeup (negative pulse).

Table 52 — Test case for operation mode change from *BD_Standby* to *BD_Standby* due to local wakeup (negative pulse)

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to local wakeup (negative pulse)
Test purpose	This test checks the ability of the IUT to change from *BD_Standby* mode to *BD_Standby* due to a local wakeup event according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — neither the Functional class "Bus Driver voltage regulator control" nor the Functional class "Bus Driver internal voltage regulator" is implemented — the local wakeup is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	Standby preamble.
Test execution	a) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. b) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Apply a negative wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4.

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to local wakeup (negative pulse)
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs after the beginning of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal shall be LOW at the host interface of node 24 after the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs + 100 µs after the beginning of the local wakeup event). — In case that SPI as host interface is implemented: The error signal shall be LOW at the host interface of node 24 after the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs + 200 µs after the beginning of the local wakeup event). — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs after the beginning of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state.

Table 53 defines the test instances for operation mode change from BD_Standby to BD_Standby due to local wakeup (negative pulse) test case define in Table 52.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 53 — Test instances for operation mode change from *BD_Standby* to *BD_Standby* due to local wakeup (negative pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.8 Operation mode change from *BD_Standby* to *BD_Standby* due to local wakeup (positive pulse)

Table 54 defines the test case for operation mode change from BD_Standby to BD_Standby due to local wakeup (positive pulse).

Table 54 — Test case for operation mode change from *BD_Standby* to *BD_Standby* due to local wakeup (positive pulse)

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to local wakeup (positive pulse)
Test purpose	This test checks the ability of the IUT to change from *BD_Standby* mode to *BD_Standby* due to a local wakeup event according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the local wakeup (positive pulse) is not implemented — neither the Functional class “Bus Driver voltage regulator control” nor the Functional class “Bus Driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standby preamble. — Set *uWAKE* to logical LOW before the IUT is set to *BD_Standby*.
Test execution	a) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. b) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Apply a positive wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE*

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to local wakeup (positive pulse)
	according to *dBDWakePulseFilter* in ISO 17458-4.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected between 1µs after the beginning of the local wakeup event and 100 µs + 500 µs after the beginning of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal shall be LOW at the host interface of node 24 after the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs + 100 µs after the beginning of the local wakeup event). — In case that SPI as host interface is implemented: The error signal shall be LOW at the host interface of node 24 after the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs + 200 µs after the beginning of the local wakeup event). — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the beginning of the local wakeup event and 100 µs + 500 µs after the beginning of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state.

Table 55 defines the test instances for operation mode change from BD_Standby to BD_Standby due to local wakeup (positive pulse) test case defined in Table 54.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 55 — Test instances for operation mode change from *BD_Standby* to *BD_Standby* due to local wakeup (positive pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.9 Insufficient local wakeup (negative pulse)

Table 56 defines the test case for insufficient local wakeup (negative pulse).

Table 56 — Test case for insufficient local wakeup (negative pulse)

Name	Insufficient local wakeup (negative pulse)
Test purpose	This test checks the ability of the IUT to reject spikes on the WAKE pin and to stay in *BD_Standby* mode if the negative wake pulse width is insufficient according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — neither the Functional class “Bus Driver voltage regulator control” nor the Functional class “Bus Driver internal voltage regulator” is implemented — the local wakeup is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	Standby preamble.
Test execution	a) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. b) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Apply a negative wakeup pulse of 1 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4.
Postamble	Standard postamble.

Name	Insufficient local wakeup (negative pulse)
Pass criteria	Due to *dBDWakeupReaction*$_{local}$ the observed signals shall be observed and acquired for at least 100 µs + 200 µs after the wakeup pulse has been applied. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — The error signal shall be HIGH at the host interface of node 24 after the wakeup event is sent. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 57 defines the test instances for insufficient local wakeup (negative pulse) test case defined in Table 56.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 57 — Test instances for insufficient local wakeup (negative pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.10 Insufficient local wakeup (positive pulse)

Table 58 defines the test case for insufficient local wakeup (positive pulse).

Table 58 — Test case for insufficient local wakeup (positive pulse)

Name	Insufficient local wakeup (positive pulse)
Test purpose	This test checks the ability of the IUT to reject spikes on the WAKE pin and to stay in *BD_Standby* mode if the positive wake pulse width is insufficient according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — neither the Functional class “Bus Driver voltage regulator control” nor the Functional class “Bus Driver internal voltage regulator” is implemented — the local wakeup (positive pulse) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	Standby preamble.
Test execution	a) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. b) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Apply a positive wakeup pulse of 1 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4.
Postamble	Standard postamble.

Name	Insufficient local wakeup (positive pulse)
Pass criteria	Due to *dBDWakeupReaction*$_{local}$ the observed signals shall be observed and acquired for at least 100 µs + 200 µs after the wakeup pulse has been applied. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — The error signal shall be HIGH at the host interface of node 24 after the wakeup event is sent. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 59 defines the test instances for insufficient local wakeup (positive pulse) test case defined in Table 58.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 59 — Test instances for insufficient local wakeup (positive pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.11 Operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{CC}

Table 60 defines the test case for operation mode change from BD_Normal to BD_Standby due to undervoltage of V_{CC}.

Table 60 — Test case for operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{CC}

Name	Operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{CC}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_Normal* mode to *BD_Standby* in case of an undervoltage on V_{CC} according to ISO 17458-4 while V_{BAT} is implemented and no other stress condition is present. In case of a missing V_{BAT} supply input, see test case 9.3.14.1 and skip this test case. This test case is skipped if — the Functional class “Bus Driver voltage regulator control” is not implemented — the Functional class “Bus Driver logic level adaptation” is not implemented — a V_{CC} supply input is not available.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — External V_{CC} power supply of the IUT in node 24: +5,0V. — V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	Operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{CC}
	TP_N24_INTN) of node 24. i) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. j) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. k) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. m) Wait 5,0 µs. n) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 61 defines the test instances for operation mode change from BD_Normal to BD_Standby due to undervoltage of V_{CC} test case defined in Table 60.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 61 — Test instances for operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{CC}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.12 Operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{IO}

Table 62 defines the test case for operation mode change from BD_Normal to BD_Standby due to undervoltage of V_{IO}.

Table 62 — Test case for operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{IO}

Name	Operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_Normal* mode to *BD_Standby* in case of an undervoltage on V_{IO} according to ISO 17458-4 while no other stress condition is present. If the *BD_Sleep* mode is implemented, see test case 9.3.7.4 and following and skip this test case. This test case is skipped if — the Functional class “Bus Driver voltage regulator control” or the subgroup BDControl within the Functional class “Bus Driver internal voltage regulator” is implemented — the Functional class “Bus Driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. g) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. h) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and

Name	Operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{IO}
	TP_N24_TxEN by one TSS pattern, followed by one 10Bit High pattern. i) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. j) Wait 5,0 µs. k) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 63 defines the test instances for operation mode change from BD_Normal to BD_Standby due to undervoltage of V_{IO} test case defined in Table 62.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 63 — Test instances for operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{IO}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_IVR without BDControl
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.13 Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{CC}

Table 64 defines the test case for operation mode change from BD_ReceiveOnly to BD_Standby due to undervoltage of V_{CC}.

Table 64 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{CC}

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{CC}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_ReceiveOnly* mode to *BD_Standby* in case of an undervoltage on V_{CC} according to ISO 17458-4 while V_{BAT} is implemented and no other stress condition is present. In case of a missing V_{BAT} supply input, see test case 9.3.12.1 and skip this test case. This test case is skipped if — the Functional class “Bus Driver voltage regulator control” is not implemented — the Functional class “Bus Driver logic level adaptation” is not implemented — the *BD_ReceiveOnly* mode is not implemented — a V_{CC} supply input is not available.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — External V_{CC} power supply of the IUT in node 24: +5,0V. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{CC}
	node 24. h) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. i) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. j) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. k) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. m) Wait 5,0 µs. n) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — in case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 65 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Standby due to undervoltage of V_{CC} test case defined in Table 64.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 65 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{CC}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.14 Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{IO}

Table 66 defines the test case for operation mode change from BD_ReceiveOnly to BD_Standby due to undervoltage of V_{IO}.

Table 66 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{IO}

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from BD_ReceiveOnly mode to BD_Standby in case of an undervoltage on V_{IO} according to ISO 17458-4 while no other stress condition is present. If the *BD_Sleep* mode is implemented, see test case 9.3.7.5 and following and skip this test case. This test case is skipped if — the Functional class “Bus Driver voltage regulator control” or the subgroup BDControl within the Functional class “Bus Driver internal voltage regulator” is implemented — the Functional class “Bus Driver logic level adaptation” is not implemented — the BD_ReceiveOnly mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{IO}
	TP_N24_INTN) of node 24. g) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. h) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. i) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. j) Wait 5,0 µs. k) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 67 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Standby due to undervoltage of V_{IO} test case defined in Table 66.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 67 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{IO}

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_IVR without BDControl
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.15 Operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{CC}

Table 68 defines the test case for operation mode change from BD_Standby to BD_Standby due to undervoltage of V_{CC}.

Table 68 — Test case for operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{CC}

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{CC}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_Standby* mode to *BD_Standby* in case of an undervoltage on V_{CC} according to ISO 17458-4 while V_{BAT} is implemented and no other stress condition is present. In case of a missing V_{BAT} supply input, see test case 9.3.12.1 and skip this test case. This test case is skipped if — the Functional class “Bus Driver voltage regulator control” is not implemented — the Functional class “Bus Driver logic level adaptation” is not implemented — a V_{CC} supply input is not available.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — External V_{CC} power supply of the IUT in node 24: +5,0V. — V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{CC}
	TP_N24_INTN) of node 24. i) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. j) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. k) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. m) Wait 5,0 µs. n) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected. — In case of an available ERRN signal *uERRN* of node 24 shall be in logical HIGH state during the test execution. — In case of an available INTN signal *uINTN* of node 24 shall be in logical LOW state latest 1 000 ms + 200 µs after the undervoltage is applied. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 69 defines the test instances for operation mode change from BD_Standby to BD_Standby due to undervoltage of V_{CC} test case defined in Table 68.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 69 — Test instances for operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{CC}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.16 Operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{IO}

Table 70 defines the test case for operation mode change from BD_Standby to BD_Standby due to undervoltage of V_{IO}.

Table 70 — Test case for operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{IO}

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_Standby* mode to *BD_Standby* in case of an undervoltage on V_{IO} according to ISO 17458-4 while no other stress condition is present. If the *BD_Sleep* mode is implemented, see test case 9.3.7.4 and following and skip this test case. This test case is skipped if — the Functional class “Bus Driver voltage regulator control” is implemented — the subgroup BDControl within the Functional class “Bus Driver internal voltage regulator” is implemented — the Functional class “Bus Driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{IO}
	TP_N24_INTN) of node 24. g) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. h) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. i) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. j) Wait 5,0 µs. k) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 71 defines the test instances for operation mode change from BD_Standby to BD_Standby due to undervoltage of V_{IO} test case defined in Table 70.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 71 — Test instances for operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{IO}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_IVR without BDControl
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.17 IUT enter *BD_Standby* (power on event)

Table 72 defines the test case for IUT enter BD_Standby (power on event).

Table 72 — Test case for IUT enter *BD_Standby* (power on event)

Name	IUT enter *BD_Standby* (power on event)
Test purpose	This test checks the behaviour and the ability of the IUT to enter *BD_Standby* in case of a power on event according to ISO 17458-4 while no stress condition is present.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that only V_{CC} is implemented:
	  — V_{CC} power supply of all nodes: +5,0V.
	  — External V_{CC} power supply of the IUT in node 24: +5,0V.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — External V_{BAT} power supply of the IUT in node 24: default.
	  — V_{CC} power supply of all nodes: +5,0V.
	  — External V_{CC} power supply of the IUT in node 24: +5,0V.
	— In case that only V_{BAT} is implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — External V_{BAT} power supply of the IUT in node 24: default.
	— In case of an available V_{IO} supply input:
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: Node 24 and node 23 as transmitter.

Preamble (setup state)	— Standard preamble. — Disable the outputs of the external power supplies of IUT in node 24. — If host interface option A is implemented: Switch STBN signal of node 24 and all available mode control signals (EN) to unconnected. This is to make the IUTs state independent from a host command. — If host interface option B is implemented: Do not send any host command to the IUT during the test execution.

Name	IUT enter *BD_Standby* (power on event)
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. g) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. h) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. i) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. j) Enable the power supplies of the IUT in node 24. k) After the maximal wakeup detection time of 100 µs, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. m) Wait 5,0 µs. n) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Power on wakeup detection timeout measurement requires a trigger event when voltages at the IUTs supply inputs have raised to sufficient values. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The error signal of the IUT of node 24 shall be in HIGH state latest 100 µs after the power on event, i.e. no wakeup indication shall be signaled via the host interface of node 24. — In case that SPI as host interface is implemented: The error signal of the IUT of node 24 shall be in HIGH state latest 200 µs after the power on event, i.e. no wakeup indication shall be signaled via the host interface of node 24. — *uRxD* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected as wakeup event. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window,

Name	IUT enter *BD_Standby* (power on event)
	beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV (*uBDTx*$_{idle}$). — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state after the maximal detection time of 100 µs.

Table 73 defines the test instances for IUT enter BD_Standby (power on event) test case defined in Table 72.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 73 — Test instances for IUT enter *BD_Standby* (power on event)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	External V_{BAT} at n24 = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.18 IUT remains in *BD_Standby* (RWU violation)

Table 74 defines the test case for IUT remains in BD_Standby (RWU violation).

Table 74 — Test case for IUT remains in *BD_Standby* (RWU violation)

Name	IUT remains in *BD_Standby* (RWU violation)
Test purpose	This test checks the ability of the IUT to ignore non suitable remote wakeup (RWU) patterns with shorted idle phase and to remain in *BD_Standby* mode according to ISO 17458-4 while no stress condition is present. This test case is skipped in case the Functional class “Bus Driver remote wakeup” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0V. — In case that V_{IO} is implemented: V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one non wakeup

Name	IUT remains in *BD_Standby* (RWU violation)
	short idle phase pattern as specified in 9.1.3.9.
Postamble	Standard postamble.
Pass criteria	The observation shall be at least 100 µs + 200 µs, because the IUT may wakeup within this time and signal this wakeup at the host interface. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution, i.e. node 24 shall remain in *BD_Standby*. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — The error signal shall be HIGH at the host interface of node 24 after the wakeup event is sent.

Table 75 defines the test instances for IUT remains in BD_Standby (RWU violation) test case defined in Table 74.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 75 — Test instances for IUT remains in *BD_Standby* (RWU violation)

Instance		**1**	**2**	**3**
Purpose	**Purpose**	IUT shall ignore non suitable remote wakeup patterns with shorted idle phase	IUT shall ignore non suitable remote wakeup patterns with shorted low phase	IUT shall ignore non suitable prolonged remote wakeup patterns
	Stress	—	—	—
	Precondition	—	—	—
Configuration	**Power supply**	—	—	—
	Ground shift	—	—	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	Stimulate the IUT in n23 at *TP_N23_TxD* and *TP_N23_TxEN* by one non wakeup short low phase pattern as specified in 9.1.3.10.	Stimulate the IUT in n23 at *TP_N23_TxD* and *TP_N23_TxEN* by one non wakeup prolonged pattern as specified in 9.1.3.11.
Pass criteria		—	—	—

9.3.5.19 RWU detection while undervoltage conditions

Table 76 defines the test case for RWU detection while undervoltage conditions.

Table 76 — Test case for RWU detection while undervoltage conditions

Name	RWU detection while undervoltage conditions
Test purpose	This test checks the ability of the IUT to detect a remote wakeup (RWU) when V_{CC} and V_{IO} are concurrently in undervoltage conditions according to ISO 17458-4. This test case is skipped if — the Functional class “Bus Driver voltage regulator control” is not implemented — the Functional class “Bus Driver logic level adaptation” is not implemented — the V_{CC} supply input is not available — the Functional class “Bus Driver remote wakeup” is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{BAT} power supply of all nodes: default.
	— V_{CC} power supply of all nodes: +5,0V.
	— External V_{CC} power supply of the IUT in node 24: +5,0V.
	— V_{IO} reference voltage:
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: V_{CC} and V_{IO} in undervoltage condition.
	— Communication: node 23 as transmitter.

Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 23 via the host interface to enter *BD_Normal*. — Switch V_{CC} and V_{IO} of node 24 to external power supplies and set $uV_{CC}=V_{CCUndervoltage}$ and $uV_{IO}=V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes except node 23. d) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or

Name	RWU detection while undervoltage conditions
	TP_Nx_INTN) of all nodes. e) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uINH1* of all observed nodes shall be in logical LOW state (*Sleep*) at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uINH1* of all observed nodes shall change to logical HIGH state (*Not_Sleep*), i.e. shall contain one rising edge indicating the change to *BD_Standby* mode. — No error shall be signalled via the host interface of node 23. — In case that hard wired signals as host interface are implemented: — The IUT of node 24 shall signal an error to the host during the test execution. — The error signal shall be LOW at the host interface of all observed nodes except nodes 23 and 24 after the wakeup is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 100 µs after the beginning of the wakeup pattern). — In case that SPI as host interface is implemented: — The IUT of node 24 shall signal an error to the host during the test execution — The error signal shall be LOW at the host interface of all observed nodes except nodes 23 and 24 after the wakeup is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 200 µs after the beginning of the wakeup pattern).

Table 77 defines the test instances for RWU detection while undervoltage conditions test case defined in Table 76.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 77 — Test instances for RWU detection while undervoltage conditions

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	External V_{BAT} at all nodes = +7,0 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.20 LWU detection (negative pulse) while undervoltage conditions

Table 78 defines the test case for LWU detection (negative pulse) while undervoltage conditions.

Table 78 — Test case for LWU detection (negative pulse) while undervoltage conditions

Name	LWU detection (negative pulse) while undervoltage conditions
Test purpose	This test checks the ability of the IUT to detect a negative local wakeup (LWU) pulse when V_{CC} and V_{IO} concurrently in undervoltage conditions according to ISO 17458-4. This test case is skipped if — the Functional class “Bus Driver voltage regulator control” is not implemented — the Functional class “Bus Driver logic level adaptation” is not implemented — the V_{CC} supply input is not available — the local wakeup is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{BAT} power supply of all nodes: default.
	— V_{CC} power supply of all nodes: +5,0V.
	— External V_{CC} power supply of the IUT in node 24: +5,0V.
	— V_{IO} reference voltage:
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: V_{CC} and V_{IO} in undervoltage condition.
	— Communication: none.

Preamble (setup state)	— Sleep preamble. — Switch V_{CC} and V_{IO} of node 24 to external power supplies and set $uV_{CC}=V_{CCUndervoltage}$ and $uV_{IO}=V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. b) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Apply a negative wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4.
Postamble	Standard postamble.

Name	LWU detection (negative pulse) while undervoltage conditions
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uINH1* shall be in logical LOW state (*Sleep*) while the IUT of node 24 is in *BD_Sleep* mode, at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uINH1* shall change to logical HIGH state (*BD_Standby*: *Not_Sleep*), i.e. shall contain one rising edge indicating the change to *BD_Standby* mode. — The IUT of node 24 shall signal an error to the host during the test execution.

Table 79 defines the test instances for LWU detection (negative pulse) while undervoltage conditions test case defined in Table 78.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 79 — Test instances for LWU detection (negative pulse) while undervoltage conditions

Instance		**1**	**2**	**3**
Purpose	**Stress**	—	Ground shift	Low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	External V_{BAT} at N24 = +7,0 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.21 LWU detection (positive pulse) while undervoltage conditions

Table 80 defines the test case for LWU detection (positive pulse) while undervoltage conditions.

Table 80 — Test case for LWU detection (positive pulse) while undervoltage conditions

Name	LWU detection (positive pulse) while undervoltage conditions
Test purpose	This test checks the ability of the IUT to detect a positive local wakeup (LWU) pulse when V_{CC} and V_{IO} concurrently in undervoltage conditions according to ISO 17458-4. This test case is skipped if — the Functional class “Bus Driver voltage regulator control” is not implemented — the Functional class “Bus Driver logic level adaptation” is not implemented — a the V_{CC} input is not available — the local wakeup (positive pulse) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{BAT} power supply of all nodes: default.
	— V_{CC} power supply of all nodes: +5,0V.
	— External V_{CC} power supply of the IUT in node 24: +5,0V.
	— V_{IO} reference voltage:
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: V_{CC} and V_{IO} in undervoltage condition.
	— Communication: none.

Preamble (setup state)	— Sleep preamble. — Switch V_{CC} and V_{IO} of node 24 to external power supplies and set uV_{CC}=$V_{CCUndervoltage}$ and uV_{IO}=$V_{IOUndervoltage}$. — Wait 1 000 ms. — Set *uWAKE* to logical LOW before the IUT is set to *BD_Sleep*.
Test execution	a) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. b) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire the error signal of the host interface *TP_N24_ERRN* or *TP_N24_INTN* of node 24. d) Apply a positive wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4.

Name	LWU detection (positive pulse) while undervoltage conditions
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uINH1* shall be in logical LOW state (*Sleep*) while the IUT of node 24 is in *BD_Sleep* mode, at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uINH1* shall change to logical HIGH state (*BD_Standby*: *Not_Sleep*), i.e. shall contain one rising edge indicating the change to *BD_Standby* mode. — The IUT of node 24 shall signal an error to the host during the test execution.

Table 81 defines the test instances for LWU detection (positive pulse) while undervoltage conditions test case defined in Table 80.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 81 — Test instances for LWU detection (positive pulse) while undervoltage conditions

Instance		**1**	**2**	**3**
Purpose	**Stress**	—	Ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	External V_{BAT} at N24 = +7,0 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.22 Operation mode change from *BD_Sleep* to *BD_Standby* due to alternative remote wakeup

Table 82 defines the test case for operation mode change from *BD_Sleep* to *BD_Standby* due to alternative remote wakeup.

Table 82 — Test case for operation mode change from *BD_Sleep* to *BD_Standby* due to alternative remote wakeup

Name	Operation mode change from BD_Sleep to BD_Standby due to alternative remote wakeup
Test purpose	This test checks the ability of the IUT to change from *BD_Sleep* mode to *BD_Standby* due to an alternative remote wakeup according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — neither the Functional class “Bus Driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus Driver internal voltage regulator” is implemented — the Functional class “Bus Driver remote wakeup” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes except node 24. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 24. e) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of all nodes. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 24. g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one alternative

Name	Operation mode change from BD_Sleep to BD_Standby due to alternative remote wakeup
	wakeup pattern as specified in 9.1.3.12.
Postamble	Standard postamble.
Pass criteria	— *uINH1* of all observed nodes shall be in logical LOW state (*Sleep*) at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uINH1* of all observed nodes shall be in logical HIGH state (*Not_Sleep*), i.e. the IUTs are in *BD_Standby* mode. — *uRxD* of all observed nodes shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uRxD* of all observed nodes shall be in logical LOW state. — In case of an available RxEN signal *uRxEN* of all observed nodes shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uRxEN* of all observed nodes shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal shall be LOW at the host interface of all observed nodes except node 24 after the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 100 µs after the beginning of the wakeup pattern). — In case that SPI as host interface is implemented: The error signal shall be LOW at the host interface of all observed nodes except node 24 after the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 200 µs after the beginning of the wakeup pattern). — The error signal shall be HIGH at the host interface of node 24 during the test execution.

Table 83 defines the Test instances for operation mode change from BD_Sleep to BD_Standby due to alternative remote wakeup test case defined in Table 82.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 83 — Test instances for operation mode change from BD_Sleep to BD_Standby due to alternative remote wakeup

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.23 Operation mode change from *BD_Standby* to *BD_Standby* due to alternative remote wakeup

Table 84 defines the test case for operation mode change from BD_Standby to BD_Standby due to alternative remote wakeup.

Table 84 — Test case for operation mode change from *BD_Standby* to *BD_Standby* due to alternative remote wakeup

Name	Operation mode change from BD_Standby to BD_Standby due to alternative remote wakeup
Test purpose	This test checks the ability of the IUT to change from *BD_Standby* mode to *BD_Standby* due to an alternative remote wakeup according to ISO 17458-4 while no other stress condition is present. This test case is skipped if the Functional class “Bus Driver remote wakeup” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 24 via the host interface to enter BD_Normal.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes except node 24. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 24. e) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of all nodes. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 24. g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one alternative

Name	Operation mode change from BD_Standby to BD_Standby due to alternative remote wakeup
	wakeup pattern as specified in 9.1.3.12.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* of all observed nodes shall be in logical HIGH state (*Not_Sleep*). — *uRxD* of all observed nodes shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uRxD* of all observed nodes shall be in logical LOW state. — In case of an available RxEN signal *uRxEN* all observed nodes shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uRxEN* of all observed nodes shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal shall be LOW at the host interface of all observed nodes except node 24 after the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 100 µs after the beginning of the wakeup pattern). — In case that SPI as host interface is implemented: The error signal shall be LOW at the host interface of all observed nodes except node 24 after the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 200 µs after the beginning of the wakeup pattern). — The error signal shall be HIGH at the host interface of node 24 during the test execution.

Table 85 defines the test instances for operation mode change from BD_Standby to BD_Standby due to alternative remote wakeup test case defined in Table 84.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 85 — Test instances for operation mode change from *BD_Standby* to *BD_Standby* due to alternative remote wakeup

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.24 Operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)

Table 86 defines the Test case for operation mode change from BD_Normal to BD_Standby due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented).

Table 86 — Test case for operation mode change from BD_Normal to BD_Standby due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)

Name	**Operation mode change from BD_Normal to BD_Standby due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)**
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_Normal* mode to *BD_Standby* in case of an undervoltage on V_{CC} and V_{IO} according ISO 17458-4 while V_{BAT} is not implemented. This test case is skipped if — the V_{CC} power supply input is not implemented — the Functional class “Bus driver voltage regulator control” is implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{CC} power supply of all nodes: +5,0V.
	— External V_{CC} power supply of the IUT in node 24: +5,0V.
	— V_{IO} reference voltage:
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: Node 24 and node 23 as transmitter.

Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 24 and node 23 b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 24 and node 23 c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24.

Name	Operation mode change from BD_Normal to BD_Standby due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)
	f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. h) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. i) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Wait 5,0 µs. k) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. l) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uRxD* of node 24 shall change to logical LOW state latest 1 000 ms after the undervoltage is applied. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state latest 1 000 ms after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 87 defines the Test instances for operation mode change from BD_Normal to BD_Standby due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented) test case defined in Table 86.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 87 — Test instances for operation mode change from *BD_Normal* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.5.25 Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)

Table 88 defines the test case for operation mode change from BD_ReceiveOnly to BD_Standby due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented).

Table 88 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_ReceiveOnly* mode to *BD_Standby* in case of an undervoltage on V_{CC} and V_{IO} according to ISO 17458-4 while V_{BAT} is not implemented. This test case is skipped if — the V_{CC} power supply input is not implemented — the operation mode *BD_ReceiveOnly* is not implemented — the Functional class “Bus driver voltage regulator control” is implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{CC} power supply of all nodes: +5,0V.
	— External V_{CC} power supply of the IUT in node 24: +5,0V.
	— V_{IO} reference voltage:
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: Node 24 and node 23 as transmitter.

Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 24 to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 24 and node 23. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 24 and node 23. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24.

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)
	e) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. h) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. i) After the detection of the undervoltage condition at V_{CC} and V_{IO} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait 5,0 µs. l) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	— Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uRxD* of node 24 shall change to logical LOW state latest 1 000 ms after the undervoltage is applied. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state latest 1 000 ms after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 89 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Standby due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented) test cased defined in Table 88.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 89 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.5.26 Operation mode change from *BD_Sleep* to *BD_Standby* due to host command

Table 90 defines the test case for operation mode change from BD_Sleep to BD_Standby due to host command.

Table 90 — Test case for operation mode change from *BD_Sleep* to *BD_Standby* due to host command

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to host command
Test purpose	This test checks the ability of the IUT to change from *BD_Sleep* mode to *BD_Standby* due to host command according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus Driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus Driver internal voltage regulator” is implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 23 via the host interface to enter *BD_Normal*. — Wait 100 µs.
Test execution	The observation shall start 100 µs (*$dBDModeChange_{SPI}$*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2.

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to host command
	f) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. i) Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. j) Wait 100 µs (the IUT shall change to *BD_Standby*). k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Trigger the scope to start the observation synchronously with the stimulation at node 24. m) Wait until end of the scope observation window, i.e. 5,0 µs. n) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	— *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of TxEN of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected. — *uINH1* of all nodes except node 24 and node 23 shall be in logical LOW state (*Not_Sleep*) during the test execution. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the observation window.

Table 91 defines the test instances for operation mode change from BD_Sleep to BD_Standby due to host command test case defined in Table 90.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 91 — Test instances for operation mode change from *BD_Sleep* to *BD_Standby* due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.27 Operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)

Table 92 defines the test case for operation mode change from BD_Standby to BD_Standby due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented).

Table 92 — Test case for operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_Standby* mode to *BD_Standby* in case of an undervoltage on V_{CC} and V_{IO} according to ISO 17458-4 while V_{BAT} is not implemented. This test case is skipped if the V_{CC} power supply input is not implemented — the Functional class “Bus driver voltage regulator control” is implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{CC} power supply of all nodes: +5,0V.
	— External V_{CC} power supply of the IUT in node 24: +5,0V.
	— V_{IO} reference voltage:
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: Node 24 and node 23 as transmitter.

Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 to enter *BD_Standby*.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 24 and node 23 b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 24 and node 23 c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)
	node 24. g) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. h) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. i) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait 5,0 µs. l) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000ms + 200 µs after the undervoltage is applied. — Latest 1 000ms after the undervoltage is applied *uRxD* of node 24 shall change to logical LOW state. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state latest 1 000 ms after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 93 defines the test instances for operation mode change from BD_Standby to BD_Standby due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented) test case defined in Table 92.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 93 — Test instances for operation mode change from *BD_Standby* to *BD_Standby* due to undervoltage of V_{CC} and V_{IO} (V_{BAT} not implemented)

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.5.28 Operation mode change from *BD_Sleep* to *BD_Standby* due to wakeup frame

Table 94 defines the test case for operation mode change from BD_Sleep to BD_Standby due to wakeup frame.

Table 94 — Test case for operation mode change from *BD_Sleep* to *BD_Standby* due to wakeup frame

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to wakeup frame
Test purpose	This test checks the ability of the IUT to change from *BD_Sleep* mode to *BD_Standby* due to a wakeup frame according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver remote wakeup” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes except node 24. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 24. e) Observe and acquire the error signal of the host interface (TP_Nx_ERRN or TP_Nx_INTN) of all nodes. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 24. g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one wakeup frame

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to wakeup frame
	containing the payload as specified in 9.1.3.13.
Postamble	Standard postamble.
Pass criteria	— *uINH1* of all observed nodes shall be in logical LOW state (*Sleep*) before the negative edge on *TP_N24_TxEN*, i.e. all observed nodes shall be in *BD_Sleep* mode initially. Then, latest 100 µs after the positive edge on *TP_N24_TxEN*, *uINH1* of all observed nodes shall be in logical HIGH state (*Not_Sleep*), i.e. the IUTs are in *BD_Standby* mode. — *uRxD* of all observed nodes shall be in logical HIGH state before the negative edge on *TP_N24_TxEN*. Then, latest 100 µs after the positive edge on *TP_N24_TxEN*, *uRxD* of all observed nodes shall be in logical LOW state. — In case of an available RxEN signal *uRxEN* of all observed nodes shall be in logical HIGH state before the negative edge on *TP_N24_TxEN*. Then, latest 100 µs after the positive edge on *TP_N24_TxEN*, *uRxEN* of all observed nodes shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal of all observed nodes except node 24 shall be in logical HIGH state before the negative edge on *TP_N24_TxEN*. Then, latest 100 µs + 100 µs after the positive edge on *TP_N24_TxEN*, the error signal of all observed nodes shall be in logical LOW state. — In case that SPI as host interface is implemented: The error signal of all observed nodes except node 24 shall be in logical HIGH state before the negative edge on *TP_N24_TxEN*. Then, latest 100 µs + 200 µs after the positive edge on *TP_N24_TxEN*, the error signal of all observed nodes shall be in logical LOW state. — The error signal shall be HIGH at the host interface of node 24 during the test execution.

Table 95 defines the test instances for operation mode change from BD_Sleep to BD_Standby due to wakeup frame test case defined in Table 94.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 95 — Test instances for operation mode change from *BD_Sleep* to *BD_Standby* due to wakeup frame

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.29 Operation mode change from *BD_Standby* to *BD_Standby* due to wakeup frame

Table 96 defines the test case for operation mode change from BD_Standby to BD_Standby due to wakeup frame.

Table 96 — Test case for operation mode change from *BD_Standby* to *BD_Standby* due to wakeup frame

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to wakeup frame
Test purpose	This test checks the ability of the IUT to change from *BD_Standby* mode to *BD_Standby* due to a remote wakeup according to ISO 17458-4 while no other stress condition is present. This test case is skipped if the Functional class “Bus driver remote wakeup” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 24. d) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of all nodes. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes except node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 24. g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one wakeup frame

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to wakeup frame
	containing the payload as specified in 9.1.3.13.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all observed nodes shall be in logical HIGH state before the negative edge on *TP_N24_TxEN*. Then, latest 100 µs after the positive edge on *TP_N24_TxEN*, *uRxD* of all observed nodes shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal of all observed nodes except node 24 shall be in logical HIGH state before the negative edge on *TP_N24_TxEN*. Then, latest 100 µs + 100 µs after the positive edge on *TP_N24_TxEN*, the error signal of all observed nodes shall be in logical LOW state. — In case that SPI as host interface is implemented: The error signal of all observed nodes except node 24 shall be in logical HIGH state before the negative edge on *TP_N24_TxEN*. Then, latest 100 µs + 200 µs after the positive edge on *TP_N24_TxEN*, the error signal of all observed nodes shall be in logical LOW state. — The error signal shall be HIGH at the host interface of node 24 during the test execution. — In case of an available INH1 signal *uINH1* of all observed nodes shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of all observed nodes shall be in logical HIGH state before the negative edge on *TP_N24_TxEN*. Then, latest 100 µs after the positive edge on *TP_N24_TxEN*, *uRxEN* of all observed nodes shall be in logical LOW state.

Table 97 defines the test instances for operation mode change from BD_Standby to BD_Standby due to wakeup frame test case defined in Table 96.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 97 — Test instances for operation mode change from *BD_Standby* to *BD_Standby* due to wakeup frame

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.30 Operation mode change from *BD_Sleep* to *BD_Standby* due to shorted remote wakeup

Table 98 defines the test case for operation mode change from BD_Sleep to BD_Standby due to shorted remote wakeup.

Table 98 — Test case for operation mode change from *BD_Sleep* to *BD_Standby* due to shorted remote wakeup

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to shorted remote wakeup
Test purpose	This test checks the ability of the IUT to change from *BD_Sleep* mode to *BD_Standby* due to a shorted remote wakeup according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver remote wakeup” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_N23_INH1* of node 23. d) Observe and acquire *uRxD* at *TP_N23_RxD* of node 23. e) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of node 23 and node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N23_RxEN* of node 23.

Name	Operation mode change from *BD_Sleep* to *BD_Standby* due to shorted remote wakeup
	g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one shorted wakeup pattern as specified in 9.1.3.14.
Postamble	Standard postamble.
Pass criteria	— *uINH1* of node 23 shall be in logical LOW state (*Sleep*) at least until 13,3 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup is detected (between 13,3 µs after the beginning of the wakeup pattern and 116,3 µs after the beginning of the wakeup pattern), *uINH1* of node 23 shall be in logical HIGH state (*Not_Sleep*), i.e. the IUT is in *BD_Standby* mode. — *uRxD* of node 23 shall be in logical HIGH state at least until 13,3 µs after the first falling edge of *uTxEN* of node 24. After the wakeup is detected (between 13,3 µs after the beginning of the wakeup pattern and 116,3 µs after the beginning of the wakeup pattern), *uRxD* of node 23 shall be in logical LOW state. — In case of an available RxEN signal *uRxEN* all node 23 shall be in logical HIGH state at least until 13,3 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup is detected (between 13,3 µs after the beginning of the wakeup pattern and 116,3 µs after the beginning of the wakeup pattern), *uRxEN* of all node 23 shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal shall be LOW at the host interface of node 23 after the wakeup is detected (between 13,3 µs after the beginning of the wakeup pattern and 116,3 µs + 100 µs after the beginning of the wakeup pattern). — In case that SPI as host interface is implemented: The error signal shall be LOW at the host interface of node 23 after the wakeup is detected (between 13,3 µs after the beginning of the wakeup pattern and 116,3 µs + 200 µs after the beginning of the wakeup pattern). — The error signal shall be HIGH at the host interface of node 24 during the test execution.

Table 99 defines the test instances for operation mode change from BD_Sleep to BD_Standby due to shorted remote wakeup test case defined in Table 98.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 99 — Test instances for operation mode change from *BD_Sleep* to *BD_Standby* due to shorted remote wakeup

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.5.31 Operation mode change from *BD_Standby* to *BD_Standby* due to shorted remote wakeup

Table 100 defines the test case for operation mode change from BD_Standby to BD_Standby due to shorted remote wakeup.

Table 100 — Test case for operation mode change from *BD_Standby* to *BD_Standby* due to shorted remote wakeup

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to shorted remote wakeup
Test purpose	This test checks the ability of the IUT to change from *BD_Standby* mode to *BD_Standby* due to a shorted remote wakeup according to ISO 17458-4 while no other stress condition is present. This test case is skipped if the Functional class “Bus driver remote wakeup” is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that only V_{CC} is implemented:
	— V_{CC} power supply of all nodes: +5,0V.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes: +5,0V.
	— In case that only V_{BAT} is implemented:
	V_{BAT} power supply of all nodes: default.
	— V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 24 as transmitter.

Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uRxD* at *TP_N23_RxD* of node 23. d) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of node 23 and node 24. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N23_INH1* of node 23. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N23_RxEN* of node 23. g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one shorted wakeup pattern as specified in 9.1.3.14.

Name	Operation mode change from *BD_Standby* to *BD_Standby* due to shorted remote wakeup
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 23 shall be in logical HIGH state at least until 13,3 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup is detected (between 13,3 µs after the beginning of the wakeup pattern and 116,3 µs after the beginning of the wakeup pattern), *uRxD* of node 23 shall be in logical LOW state. — In case that hard wired signals as host interface are implemented: The error signal shall be LOW at the host interface of node 23 after the wakeup is detected (between 13,3 µs after the beginning of the wakeup pattern and 116,3 µs + 100 µs after the beginning of the wakeup pattern). — In case that SPI as host interface is implemented: The error signal shall be LOW at the host interface of node 23 after the wakeup is detected (between 13,3 µs after the beginning of the wakeup pattern and 116,3 µs + 200 µs after the beginning of the wakeup pattern). — The error signal shall be HIGH at the host interface of node 24 during the test execution. — In case of an available INH1 signal *uINH1* of node 23 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of node 23 shall be in logical HIGH state at least until 13,3 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup is detected (between 13,3 µs after the beginning of the wakeup pattern and 116,3 µs after the beginning of the wakeup pattern), *uRxEN* of node 23 shall be in logical LOW state.

Table 101 defines the test instances for operation mode change from BD_Standby to BD_Standby due to shorted remote wakeup test case defined in Table 100.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 101 — Test instances for operation mode change from *BD_Standby* to *BD_Standby* due to shorted remote wakeup

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.6 Mode.Bus Driver.Normal

9.3.6.1 Operation mode change from *BD_Standby* to *BD_Normal* due to host command

Table 102 defines the test case for operation mode change from BD_Standby to BD_Normal due to host command.

Table 102 — Test case for operation mode change from *BD_Standby* to *BD_Normal* due to host command

Name	Operation mode change from *BD_Standby* to *BD_Normal* due to host command
Test purpose	This test checks the ability of the IUT to change from *BD_Standby* mode to *BD_Normal* due to host command according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test).
Preamble (setup state)	Standby preamble.
Test execution	The observation shall start 100µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Stimulate the IUTs in all nodes via the host interface to enter *BD_Normal*. g) Wait 100µs for the IUT to enter *BD_Normal*. h) Stimulate the IUT in the first transmitting node according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern.

Name	Operation mode change from *BD_Standby* to *BD_Normal* due to host command
	i) Stimulate the IUTs of the transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall contain all 50/50 patterns transmitted at *uTxD* and *uTxEN* of all nodes, i.e. all transmitted data shall be received by all nodes (loopback functionality). — In case of an available INH1 signal *uINH1* of all nodes shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical HIGH state before the first node according to the sequence described on matrix A is stimulated (falling edge of *uTxD* and *uTxEN*) and shall be in logical LOW state while *uRxD* of the corresponding node signals the received patterns.

Table 103 defines the test instances for operation mode change from BD_Standby to BD_Normal due to host command test case defined in Table 102.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 103 — Test instances for operation mode change from *BD_Standby* to *BD_Normal* due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.6.2 Operation mode change from *BD_Sleep* to *BD_Normal* due to host command

Table 104 defines the test case for operation mode change from BD_Sleep to BD_Normal due to host command.

Table 104 — Test case for operation mode change from *BD_Sleep* to *BD_Normal* due to host command

Name	Operation mode change from *BD_Sleep* to *BD_Normal* due to host command
Test purpose	This test checks the ability of the IUT to change its mode from *BD_Sleep* to *BD_Normal* due to host command according to ISO 17458-4 while no stress condition is present. This test case is skipped if neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 and node 1 as transmitter.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Sleep*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. d) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. e) Observe and acquire *uSTBN* or *uSCSN* at *TP_N24_STBN* or *TP_N24_SCSN* of node 24. f) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes.

Name	Operation mode change from *BD_Sleep* to *BD_Normal* due to host command
	i) Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. j) Wait 100 µs for the IUT to enter *BD_Normal*. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern. l) Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state before this node is stimulated to transmit, i.e. until the first falling edge of *uTxD* and *uTxEN* of node 24. — *uRxD* of all nodes shall contain all 50/50 patterns transmitted at *TP_N24_TxD* and *TP_N24_TxEN* of node 24 and node 1, i.e. all transmitted data shall be received by all nodes (loopback functionality). — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state before this node is stimulated to transmit, i.e. until the first falling edge of *uTxD* and *uTxEN* of node 24. Then, *uRxEN* of node 24 shall be in logical LOW state while *uRxD* of node 24 signals the received patterns.

Table 105 defines the test instances for operation mode change from BD_Sleep to BD_Normal due to host command test cased defined in Table 104.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 105 — Test instances for operation mode change from *BD_Sleep* to *BD_Normal* due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.6.3 Operation mode change from *BD_ReceiveOnly* to *BD_Normal* due to host command

Table 106 defines the test case for operation mode change from BD_ReceiveOnly to BD_Normal due to host command.

Table 106 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Normal* due to host command

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Normal* due to host command
Test purpose	This test checks the ability of the IUT to change from *BD_ReceiveOnly* mode to *BD_Normal* due to host command according to ISO 17458-4 while no stress condition is present. This test case is skipped if the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test).
Preamble (setup state)	ReceiveOnly preamble.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Stimulate the IUTs in all nodes via the host interface to enter *BD_Normal*. g) Wait 100 µs for the IUT to enter *BD_Normal*. h) Stimulate the IUT in the first transmitting node according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern.

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Normal* due to host command
	i) Stimulate the IUTs in the transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall contain all 50/50 patterns transmitted at *uTxD* and *uTxEN* of all nodes, i.e. all transmitted data shall be received by all nodes (loopback functionality). — In case of an available INH1 signal *uINH1* of all nodes shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical HIGH state before the first node according to the sequence described on matrix A is stimulated (falling edge of *uTxD* and *uTxEN*) and shall be in logical LOW state while *uRxD* of the corresponding node signals the received patterns.

Table 107 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Normal due to host command test case defined in Table 106.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 107 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Normal* due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7 Mode.Bus Driver.Low Power.Sleep

9.3.7.1 Operation mode change from *BD_Normal* to *BD_Sleep* due to host command

Table 108 defines the test case for operation mode change from BD_Normal to BD_Sleep due to host command.

Table 108 — Test case for operation mode change from *BD_Normal* to *BD_Sleep* due to host command

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to host command
Test purpose	This test checks the ability of the IUT to change from *BD_Normal* mode to *BD_Sleep* due to host command according to ISO 17458-4 while no stress condition is present. This test case is skipped if neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	Standard preamble.
Test execution	a) The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. b) Observe and acquire *uSTBN* or *uSCSN* at *TP_Nx_STBN* or *TP_Nx_SCSN* of all nodes. c) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Stimulate the IUTs in all nodes via the host interface to enter *BD_Sleep*. g) Wait 100 µs for the IUTs to enter *BD_Sleep*.
Postamble	Standard postamble.
Pass criteria	— *uINH1* shall be in logical LOW state (*Sleep*) during the observation window.

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to host command
	— *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 109 defines the test instances for operation mode change from BD_Normal to BD_Sleep due to host command test case defined in Table 108.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 109 — Test instances for operation mode change from *BD_Normal* to *BD_Sleep* due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.2 Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT}

Table 110 defines the test case for operation mode change from BD_Normal to BD_Sleep due to undervoltage of V_{BAT}.

Table 110 — Test case for operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT}

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_Normal* to *BD_Sleep* in case of an undervoltage on V_{BAT} according to ISO 17458-4 while V_{CC} is implemented and no other stress condition is present. In case of a missing V_{CC} supply input, see test case 9.3.11.1 and skip this test case. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{BAT} and V_{CC} supplies:
	  — V_{BAT} power supply of all nodes: default.
	  — External V_{BAT} power supply of the IUT in node 24: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	— V_{IO} reference voltage (in case of an available V_{IO} input):
	V_{IO} reference voltage of all nodes: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 24 as transmitter.

Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT}
	the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. i) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. j) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case that hard wired signals as host interface are implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 111 defines the test instances for operation mode change from BD_Normal to BD_Sleep due to undervoltage of V_{BAT} test case defined in Table 110.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 111 — Test instances for operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT}

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.3 Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT}

Table 112 defines the test case for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{BAT}.

Table 112 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT}

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_ReceiveOnly* to *BD_Sleep* in case of an undervoltage on V_{BAT} according to ISO 17458-4 while V_{CC} is implemented and no other stress condition is present. In case of a missing V_{CC} supply input, see test case 9.3.11.1 and skip this test case. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the BD_ReceiveOnly mode is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} and V_{CC} supplies: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	ReceiveOnly preamble.
Test execution	INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT}
	TP_N24_INTN) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. i) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. j) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 113 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{BAT} test case defined in Table 112.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 113 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT}

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.4 Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{IO}

Table 114 defines the test case for operation mode change from BD_Normal to BD_Sleep due to undervoltage of V_{IO}.

Table 114 — Test case for operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{IO}

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_Normal* to *BD_Sleep* in case of an undervoltage on V_{IO} according to ISO 17458-4 while no other stress condition is present. If the *BD_Sleep* mode is not implemented, see test case 9.3.5.12 (the IUT shall then change to *BD_Standby*) and following and skip this test case. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented. — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24 c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$.

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{IO}
	g) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) not later than 1 000 ms after undervoltage is present. — In case that hard wired signals as host interface are implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 115 defines the test instances for operation mode change from BD_Normal to BD_Sleep due to undervoltage of V_{IO} test case defined in Table 114.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 115 — Test instances for operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{IO}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.5 Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{IO}

Table 116 defines the test case for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{IO}.

Table 116 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{IO}

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_ReceiveOnly* to *BD_Sleep* in case of an undervoltage on V_{IO} according to ISO 17458-4 while no other stress condition is present. If the *BD_Sleep* mode is not implemented, see test case 9.3.7.13 and following and skip this test case. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the BD_ReceiveOnly mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	ReceiveOnly preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{IO}
	TP_N24_INTN) of node 24. f) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. g) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) not later than 1 000 ms after undervoltage is present. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 117 — Test instances for

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.6 Operation mode change from *BD_Standby* to *BD_Sleep* due to host command

Table 118 defines the test case for operation mode change from BD_Standby to BD_Sleep due to host command.

Table 118 — Test case for operation mode change from *BD_Standby* to *BD_Sleep* due to host command

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to host command
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_ReceiveOnly* to *BD_Sleep* in case of an undervoltage on V_{IO} according to ISO 17458-4 while no other stress condition is present. If the *BD_Sleep* mode is not implemented, see 9.3.7.13 and following and skip this test case. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the BD_ReceiveOnly mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	ReceiveOnly preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to host command
	TP_N24_INTN) of node 24. f) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. g) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) not later than 1 000 ms after undervoltage is present. — In case that hard wired signals as host interface are implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 119 defines the test instances for operation mode change from BD_Standby to BD_Sleep due to host command test case defined in Table 118.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 119 — Test instances for operation mode change from *BD_Standby* to *BD_Sleep* due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.7 Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT}

Table 120 defines the test case for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{BAT}.

Table 120 — Test case for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT}

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD*_Standby to BD_Sleep in case of an undervoltage on V_{BAT} according to ISO 17458-4 while V_{CC} is implemented and no other stress condition is present. In case of a missing V_{CC} supply input, see test case 9.3.11.1 and skip this test case. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standby preamble.
Test execution	INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$.

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT}
	h) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. i) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. j) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case that hard wired signals as host interface are implemented: no error shall be signalled via the host interface of node 24, because the IUT is in a low power operation mode. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 121 defines the test instances for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{BAT} test case defined in Table 120.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 121 — Test instances for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT}

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.8 Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{IO}

Table 122 defines the test case for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{IO}.

Table 122 — Test case for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{IO}

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_Standby* to *BD_Sleep* in case of an undervoltage on V_{IO} according to ISO 17458-4 while no other stress condition is present. If the *BD_Sleep* mode is not implemented, see test case 9.3.7.15 and following and skip this test case. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standby preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24.

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{IO}
	f) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. g) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) not later than 1 000 ms after undervoltage is present. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 123 defines the test instances for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{IO} test case define in Table 122.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 123 — Test instances for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{IO}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.9 Insufficient wakeup pulse (negative pulse)

Table 124 defines the test case for insufficient wakeup pulse (negative pulse).

Table 124 — Test case for insufficient wakeup pulse (negative pulse)

Name	Insufficient wakeup pulse (negative pulse)
Test purpose	This test checks the ability of the IUT to reject spikes on the WAKE pin and to stay in *BD_Sleep* mode if the negative wake-pulse width is insufficient according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the local wakeup is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	Sleep preamble.
Test execution	a) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. b) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Apply a negative wakeup pulse of 1 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4.
Postamble	Standard postamble.

Name	Insufficient wakeup pulse (negative pulse)
Pass criteria	Due to *dBDWakeupReaction*$_{local}$ the observed signals shall be observed and acquired for at least 100 µs + 200 µs after the wakeup pulse has been applied. — *uINH1* shall be in logical LOW state (*Sleep*) during the test execution. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — No error shall be signalled via the host interface of node 24, i.e. no wakeup was detected. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 125 defines the test instances for insufficient wakeup pulse (negative pulse) test case defined in Table 124.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 125 — Test instances for insufficient wakeup pulse (negative pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.10 Insufficient wakeup pulse (positive pulse)

Table 126 defines the test case for insufficient wakeup pulse (positive pulse).

Table 126 — Test case for insufficient wakeup pulse (positive pulse)

Name	Insufficient wakeup pulse (positive pulse)
Test purpose	This test checks the ability of the IUT to reject spikes on the WAKE pin and to stay in *BD_Sleep* mode if the positive wake-pulse width is insufficient according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the local wakeup (positive pulse) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	Sleep preamble.
Test execution	a) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. b) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Apply a positive wakeup pulse of 1 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4.
Postamble	Standard postamble.

Name	Insufficient wakeup pulse (positive pulse)
Pass criteria	Due to *dBDWakeupReaction*$_{local}$ the observed signals shall be observed and acquired for at least 100 µs + 200 µs after the wakeup pulse has been applied. — *uINH1* shall be in logical LOW state (*Sleep*) during the test execution. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — The error signal shall be HIGH at the host interface of node 24 after the wakeup event has been applied. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 127 defines the test instances for insufficient wakeup pulse (positive pulse) test case defined in Table 126.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 127 — Test instances for insufficient wakeup pulse (positive pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.11 IUT remains in *BD_Sleep* (RWU violation)

Table 128 defines the test case for IUT remains in BD_Sleep (RWU violation).

Table 128 — Test case for IUT remains in *BD_Sleep* (RWU violation)

Name	IUT remains in *BD_Sleep* (RWU violation)
Test purpose	This test checks the ability of the IUT to ignore non suitable remote wakeup patterns with shortened idle phase and to remain in *BD_Sleep* mode according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver remote wakeup” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Sleep*.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one non wakeup

Name	IUT remains in *BD_Sleep* (RWU violation)
	short idle phase pattern as specified in 9.1.3.8.
Postamble	Standard postamble.
Pass criteria	The observation shall be at least 100 µs + 200 µs, because the IUT may wake up within this time and signal this wakeup at the host interface. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution, i.e. node 24 shall remain in *BD_Sleep*. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — The error signal shall be HIGH at the host interface of node 24 after the wakeup event has been applied.

Table 129 defines the test instances for IUT remains in BD_Sleep (RWU violation) test case defined in Table 128.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 129 — Test instances for IUT remains in *BD_Sleep* (RWU violation)

Instance		**1**	**2**	**3**
Purpose	**Purpose**	IUT shall ignore non suitable remote wakeup patterns with shortened idle phase	IUT shall ignore non suitable remote wakeup patterns with shortened low phase	IUT shall ignore non suitable prolonged remote wakeup patterns
	Stress	—	—	—
	Precondition	—	—	—
Configuration	**Power supply**	—	—	—
	Ground shift	—	—	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one non wakeup short low phase pattern as specified in 9.1.3.9.	Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one non wakeup prolonged pattern as specified in 9.1.3.10.
Pass criteria		—	—	—

9.3.7.12 Operation mode change from *BD_Normal* to *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC} & V_{IO}

Table 130 defines the test case for operation mode change from BD_Normal to BD_Standby to BD_Sleep due to undervoltage of V_{CC} & V_{IO}.

Table 130 — Test case for operation mode change from *BD_Normal* to *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC} & V_{IO}

Name	Operation mode change from *BD_Normal* to *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC} & V_{IO}
Test purpose	This test checks the ability of the IUT to change from *BD_Normal* to *BD_Standby* and then to *BD_Sleep* mode while first V_{CC} is in undervoltage condition and then V_{IO} is in undervoltage condition according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the V_{CC} supply input is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. b) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. c) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.4. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN* f) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$.Wait at least

Name	Operation mode change from *BD_Normal* to *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC} & V_{IO}
	1 000 ms. h) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$.Synchronously with the configuration of the external Vcc power supply of the IUT in node 24 to $V_{CCUndervoltage}$, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one 10Bit Low pattern followed by one 10Bit High pattern followed by one 10Bit Low pattern. Repeat this sequence with a gap of 9,25 ms until the end of the scope observation window. The bit duration in this test case shall be *gdBit*=25 µs, because the memory depth of the logic analyzer is much too small to acquire seconds with a 100 ns bit time. j) Trigger the scope to start the observation one second after the undervoltage at V_{CC}.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) before detecting the V_{IO} undervoltage, i.e. node 24 shall change from *BD_Normal* to *BD_Standby*. After detecting the V_{IO} undervoltage *uINH1* of node 24 shall be in logical LOW state (*Sleep*) until the end of the test execution, i.e. node 24 shall enter in *BD_Sleep*. — In case that hard wired signals as host interface are implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{CC}. — In case that SPI as host interface is implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{CC}. — *uBus* at *TP4_N23* of node 23 shall stay within idle range during the observation window, beginning one second after undervoltage in V_{CC}. The absolute bus voltage shall not exceed 30 mV (uBD_{Txidle}).

Table 131 defines the test instances for operation mode change from BD_Normal to BD_Standby to BD_Sleep due to undervoltage of V_{CC} & V_{IO} test case defined in Table 130.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 131 — Test instances for operation mode change from BD_Normal to BD_Standby to BD_Sleep due to undervoltage of V_{CC} & V_{IO}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.13 IUT remains in *BD_Sleep* while EN is set to low

Table 132 defines the test case for IUT remains in BD_Sleep while EN is set to low.

Table 132 — Test case for IUT remains in *BD_Sleep* while EN is set to low

Name	Test case for IUT remains in *BD_Sleep* while EN is set to low
Test purpose	This test checks the ability of the IUT to remain *BD_Sleep* mode while EN is set to low by the host according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standard preamble. — Stimulate the host interface of node 24 to switch the IUT to *BD_Sleep*, i.e. the EN signal of node 24 shall be HIGH. — Wait 100 µs.
Test execution	The observation shall start 100 µs after the first host command is applied. a) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. b) Observe and acquire *uEN* at *TP_N24_EN* of node 24. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Stimulate the host interface of node 24 to switch the IUT to *BD_Standby*, i.e. the STBN and EN signals of node 24 shall both be LOW.

Name	Test case for IUT remains in *BD_Sleep* while EN is set to low
	g) Wait 100 µs.
Postamble	Standard postamble.
Pass criteria	— *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the whole test execution, i.e. the IUT shall not leave the *BD_Sleep* mode. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 133 defines the test instances for IUT remains in BD_Sleep while EN is set to low test case defined in Table 132.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 133 — Test instances for IUT remains in BD_Sleep while EN is set to low

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.14 IUT remains in *BD_Sleep* while UV of V_{CC}

Table 134 defines the test case for IUT remains in BD_Sleep while UV of V_{CC}.

Table 134 — Test case for IUT remains in *BD_Sleep* while UV of V_{CC}

Name	IUT remains in *BD_Sleep* while UV of V_{CC}
Test purpose	This test checks the ability of the IUT to remain in *BD_Sleep* mode while an undervoltage of V_{CC} is present according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that V_{IO} is implemented: V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 23 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and

Name	IUT remains in *BD_Sleep* while UV of V_{CC}
	TP_N24_TxEN by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait 5,0 µs. l) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that V_{IO} is not implemented: — *uRxD* of node 24 shall be in logical LOW state latest 1 000 ms after the undervoltage is applied. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state latest 1 000 ms after the undervoltage is applied. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — In case that V_{IO} is implemented: — *uRxD* of node 24 shall be in logical HIGH state during the test execution, i.e. the ongoing pattern shall not be detected as wakeup event. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution, i.e. bus activity shall not be detected. — In case that hard wired signals as host interface are implemented: No error shall be signalled by the IUT of node 24 after the undervoltage is applied because in a low power mode no undervoltage detection is required. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 135 defines the test instances for IUT remains in BD_Sleep while UV of V_{CC} test case defined in Table 134.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 135 — Test instances for IUT remains in *BD_Sleep* while UV of V_{CC}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.15 Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{CC} and V_{IO}

Table 136 defines the test case for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{CC} and V_{IO}.

Table 136 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{CC} and V_{IO}

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{CC} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_ReceiveOnly* to *BD_Sleep* in case of an undervoltage on V_{CC} and V_{IO} according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	ReceiveOnly preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{CC} and V_{IO}
	node 24. g) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. j) After the detection of the undervoltage condition at V_{CC} and V_{IO} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. l) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) not later than 1 000 ms after undervoltage at V_{IO} is present. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 137 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{CC} and V_{IO} test case defined in Table 136.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 137 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{CC} and V_{IO}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.16 IUT remains in *BD_Sleep* while undervoltage of V_{BAT} and V_{CC}

Table 138 defines the test case for IUT remains in BD_Sleep while undervoltage of V_{BAT} and V_{CC}.

Table 138 — Test case for IUT remains in *BD_Sleep* while undervoltage of V_{BAT} and V_{CC}

Name	Test case for IUT remains in *BD_Sleep* while undervoltage of V_{BAT} and V_{CC}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to remain in *BD_Sleep* mode in case of an undervoltage on V_{BAT} and V_{CC} according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{BAT} power supply of all nodes: default.
	— External V_{BAT} power supply of the IUT in node 24: default.
	— V_{CC} power supply of all nodes: +5,0 V.
	— External V_{CC} power supply of the IUT in node 24: +5,0 V.
	— V_{IO} reference voltage (in case of an available V_{IO} input):
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 24 as transmitter.

Preamble (setup state)	Sleep preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24.

Name	Test case for IUT remains in *BD_Sleep* while undervoltage of V_{BAT} and V_{CC}
	g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) After the detection of the undervoltage condition at V_{CC} and V_{BAT} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$ and V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that V_{IO} is not implemented: — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — In case that V_{IO} is implemented: — *uRxD* of node 24 shall be in logical HIGH state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the observation window. — In case that hard wired signals as host interface are implemented: No error shall be signalled via the host interface of the IUT of node 24 because in a low power operation mode no undervoltage signaling is required. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{CC}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 139 defines the test instances for IUT remains in BD_Sleep while undervoltage of V_{BAT} and V_{CC} test case defined in Table 138.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 139 — Test instances for IUT remains in *BD_Sleep* while undervoltage of V_{BAT} and V_{CC}

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.17 Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}

Table 140 defines the test case for operation mode change from BD_Normal to BD_Sleep due to undervoltage of V_{BAT} and V_{CC}.

Table 140 — Test case for operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_Normal* to *BD_Sleep* in case of an undervoltage on V_{BAT} and V_{CC} according to ISO 17458-4. This test case is skipped — if the Functional class "Bus driver voltage regulator control" is not implemented — the Functional class "Bus driver internal voltage regulator" is implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{BAT} power supply of all nodes: default.
	— External V_{BAT} power supply of the IUT in node 24: default.
	— V_{CC} power supply of all nodes: +5,0 V.
	— External V_{CC} power supply of the IUT in node 24: +5,0 V.
	— V_{IO} reference voltage (in case of an available V_{IO} input):
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 24 as transmitter.

Preamble (setup state)	Standard preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}
	TP_N24_INTN) of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) After the detection of the undervoltage condition at V_{CC} and V_{BAT} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$ and V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that V_{IO} is not implemented: — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state observation window. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — In case that V_{IO} is implemented: — *uRxD* of node 24 shall be in logical HIGH state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the observation window. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{CC}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 141 defines the test instances for operation mode change from BD_Normal to BD_Sleep due to undervoltage of V_{BAT} and V_{CC} test case defined in Table 140.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 141 — Test instances for operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.18 Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}

Table 142 defines the test case for operation mode change from BD_Normal to BD_Sleep due to undervoltage of V_{BAT} and V_{IO}.

Table 142 — Test case for operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_Normal* to *BD_Sleep* in case of an undervoltage on V_{BAT} and V_{IO} according to ISO 17458-4. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{IO} reference voltage: — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}
	described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. i) After the detection of the undervoltage condition at V_{IO} and V_{BAT} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 143 defines the test instances for operation mode change from BD_Normal to BD_Sleep due to undervoltage of V_{BAT} and V_{IO} test case defined in Table 142.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 143 — Test instances for operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.19 Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}

Table 144 defines the test case for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{BAT} and V_{IO}.

Table 144 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_ReceiveOnly* to *BD_Sleep* in case of an undervoltage on V_{BAT} and V_{IO} according to ISO 17458-4. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the operation mode BD_ReceiveOnly is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — External V_{BAT} power supply of the IUT in node 24: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	  — External V_{CC} power supply of the IUT in node 24: +5,0 V.
	— In case that only V_{BAT} is implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — External V_{BAT} power supply of the IUT in node 24: default.
	— V_{IO} reference voltage (in case of an available V_{IO} input):
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 24 as transmitter.

Preamble (setup state)	ReceiveOnly preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V.

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}
	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. i) After the detection of the undervoltage condition at V_{IO} and V_{BAT} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 145 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{BAT} and V_{IO} test case defined in Table 144.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 145 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.20 Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}

Table 146 defines the test case for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{BAT} and V_{CC}.

Table 146 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_ReceiveOnly* to *BD_Sleep* in case of an undervoltage on V_{BAT} and V_{CC} according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the *BD_ReceiveOnly* mode is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{BAT} power supply of all nodes: default.
	— External V_{BAT} power supply of the IUT in node 24: default.
	— V_{CC} power supply of all nodes: +5,0 V.
	— External V_{CC} power supply of the IUT in node 24: +5,0 V.
	— V_{IO} reference voltage (in case of an available V_{IO} input):
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 24 as transmitter.

Preamble (setup state)	ReceiveOnly preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24.

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}
	f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) After the detection of the undervoltage condition at V_{CC} and V_{BAT} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$ and V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that V_{IO} is not implemented: — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — In case that V_{IO} is implemented: — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{CC}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{CC}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 147 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{BAT} and V_{CC} test case defined in Table 146.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 147 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.21 Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}

Table 148 defines the test case for operation mode change from BD_Standby to BD_Sleep due to undervoltage. of V_{BAT} and V_{CC}

Table 148 — Test case for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_Standby* to *BD_Sleep* in case of an undervoltage on V_{BAT} and V_{CC} according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{BAT} power supply of all nodes: default.
	— External V_{BAT} power supply of the IUT in node 24: default.
	— V_{CC} power supply of all nodes: +5,0 V.
	— External V_{CC} power supply of the IUT in node 24: +5,0 V.
	— V_{IO} reference voltage (in case of an available V_{IO} input):
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 24 as transmitter.

Preamble (setup state)	Standby preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}
	TP_N24_INTN) of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) After the detection of the undervoltage condition at V_{CC} and V_{BAT} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$ and V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that V_{IO} is not implemented: — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{CC}. — In case that V_{IO} is implemented: — *uRxD* of node 24 shall be in logical HIGH state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the observation window. — In case that hard wired signals as host interface are implemented: No error shall be signalled via the host interface of the IUT after the undervoltage is applied at V_{CC}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{CC}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 149 defines the test instances for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{BAT} and V_{CC} test case defined in Table 148.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 149 — Test instances for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{CC}

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.22 Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}

Table 150 defines the test case for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{BAT} and V_{IO}.

Table 150 — Test case for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_Standby* to *BD_Sleep* in case of an undervoltage on V_{BAT} and V_{IO} according to ISO 17458-4. This test case is skipped if neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{IO} reference voltage: — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standby preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2.

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}
	d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{IO} power supply of the IUT in node 24 to $V_{IOUndervoltage}$. i) After the detection of the undervoltage condition at V_{BAT} and V_{IO} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$ and V_{CC} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 151 defines the test instances for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{BAT} and V_{IO} test case defined in Table 150.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 151 — Test instances for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT} and V_{IO}

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.23 Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC} and V_{IO}

Table 152 defines the test case for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{CC} and V_{IO}.

Table 152 — Test case for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC} and V_{IO}

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_Standby* to *BD_Sleep* in case of an undervoltage on V_{CC} and V_{IO} according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standby preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24.

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC} and V_{IO}
	h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) Set the external V_{IO} power supply of the IUT in node 24 to $V_{IOUndervoltage}$. j) After the detection of the undervoltage condition at V_{CC} and V_{IO} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. l) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$ and V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$ Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) not later than 1 000 ms after undervoltage is present at V_{IO}. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 153 defines the test instances for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{CC} and V_{IO} test case defined in Table 152.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 153 — Test instances for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC} and V_{IO}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.24 Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}

Table 154 defines the test case for operation mode change from BD_Normal to BD_Sleep due to undervoltage of V_{BAT}, V_{CC} and V_{IO}.

Table 154 — Test case for operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_Normal* to *BD_Sleep* in case of an undervoltage on V_{BAT}, V_{CC} and V_{IO} according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of

Name	Operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}
	node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. j) After the detection of the undervoltage condition at V_{BAT}, V_{CC} and V_{IO} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. l) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$, V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 155 defines the test instances for operation mode change from BD_Normal to BD_Sleep due to undervoltage of V_{BAT}, V_{CC} and V_{IO} test case defined in Table 154.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 155 — Test instances for operation mode change from *BD_Normal* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.25 Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}

Table 156 defines the test case for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{BAT}, V_{CC} and V_{IO}.

Table 156 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_ReceiveOnly* to *BD_Sleep* in case of an undervoltage on V_{BAT}, V_{CC} and V_{IO} according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the *BD_ReceiveOnly* mode is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	ReceiveOnly preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2.

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}
	e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. j) After the detection of the undervoltage condition V_{BAT}, V_{CC} and V_{IO} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. l) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$, V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 157 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Sleep due to undervoltage of V_{BAT}, V_{CC} and V_{IO} test case defined in Table 156.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 157 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.26 Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}

Table 158 defines the test case for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{BAT}, V_{CC} and V_{IO}.

Table 158 — Test case for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change its mode from *BD_ReceiveOnly* to *BD_Sleep* in case of an undervoltage on V_{BAT}, V_{CC} and V_{IO} according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standby preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}
	node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. j) After the detection of the undervoltage condition at V_{BAT}, V_{CC} and V_{IO} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. l) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$, V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 159 defines the test instances for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{BAT}, V_{CC} and V_{IO} test case defined in Table 158.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 159 — Test instances for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{BAT}, V_{CC} and V_{IO}

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.27 IUT remains in *BD_Sleep* while undervoltage of V_{BAT}, V_{CC} and V_{IO}

Table 160 defines the test case for IUT remains in BD_Sleep while undervoltage of V_{BAT}, V_{CC} and V_{IO}.

Table 160 — Test case for IUT remains in *BD_Sleep* while undervoltage of V_{BAT}, V_{CC} and V_{IO}

Name	IUT remains in *BD_Sleep* while undervoltage of V_{BAT}, V_{CC} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to remain in *BD_Sleep* mode in case of an undervoltage on V_{BAT}, V_{CC} and V_{IO} according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Sleep preamble.
Test execution	INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of

Name	IUT remains in *BD_Sleep* while undervoltage of V_{BAT}, V_{CC} and V_{IO}
	node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. i) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. j) After the detection of the undervoltage condition at V_{BAT}, V_{CC} and V_{IO} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. l) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$, V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 161 — Test instances for

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.28 IUT remains in *BD_Sleep* while undervoltage of V_{BAT} and V_{IO}

Table 162 defines the test case for IUT remains in BD_Sleep while undervoltage of V_{BAT} and V_{IO}.

Table 162 — Test case for IUT remains in *BD_Sleep* while undervoltage of V_{BAT} and V_{IO}

Name	IUT remains in *BD_Sleep* while undervoltage of V_{BAT} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to remain in *BD_Sleep* mode in case of an undervoltage on V_{BAT} and V_{IO} according to ISO 17458-4. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{IO} reference voltage: — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Sleep preamble.
Test execution	NOTE INH1 is not observed nor acquired because *uINH1* depends on the level of uV_{BAT} and will change to logical LOW state as soon as uV_{BAT} falls below 5,5 V. a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24.

Name	IUT remains in *BD_Sleep* while undervoltage of V_{BAT} and V_{IO}
	e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. h) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. i) After the detection of the undervoltage condition at V_{BAT} and V_{IO} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. k) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$ and V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 163 defines the test instances for IUT remains in BD_Sleep while undervoltage of V_{BAT} and V_{IO} test case defined in Table 162.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 163 — Test instances for IUT remains in *BD_Sleep* while undervoltage of V_{BAT} and V_{IO}

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at N24
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

9.3.7.29 IUT remains in *BD_Sleep* while undervoltage of V_{CC} and V_{IO}

Table 164 defines the test case for IUT remains in BD_Sleep while undervoltage of V_{CC} and V_{IO}.

Table 164 — Test case for IUT remains in *BD_Sleep* while undervoltage of V_{CC} and V_{IO}

Name	IUT remains in *BD_Sleep* while undervoltage of V_{CC} and V_{IO}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to remain in *BD_Sleep* mode in case of an undervoltage on V_{CC} and V_{IO} according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Sleep preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Set the external V_{IO} power supply of the IUT in node 24 to $V_{IOUndervoltage}$.

Name	IUT remains in *BD_Sleep* while undervoltage of V_{CC} and V_{IO}
	i) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. j) After the detection of the undervoltage condition at V_{CC} and V_{IO} by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. l) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$ and V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the observation window. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the observation window. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied at V_{IO}. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied at V_{IO}. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 165 defines the test instances for IUT remains in BD_Sleep while undervoltage of V_{CC} and V_{IO} test case defined in Table 164.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 165 — Test instances for IUT remains in *BD_Sleep* while undervoltage of V_{CC} and V_{IO}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.30 Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to host command

Table 166 defines the test case for operation mode change from BD_ReceiveOnly to BD_Sleep due to host command.

Table 166 — Test case for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to host command

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to host command
Test purpose	This test checks the ability of the IUT to change its mode from *BD_ReceiveOnly* to *BD_Sleep* due to host command according to ISO 17458-4 while no other stress condition is present. If the *BD_Sleep* mode is not implemented, see test case 9.3.7.13 and following and skip this test case. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. d) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes except node 24. e) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of all nodes except node 24. f) Stimulate the IUTs of all nodes except node 24 via the host interface to enter *BD_Sleep*. g) After 100 µs (the IUTs shall change to *BD_Sleep*), stimulate the IUT in node 24 at

Name	Operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to host command
	TP_N24_TxD and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window.
Postamble	Standard postamble.
Pass criteria	— *uINH1* of all observed nodes shall be in logical LOW state (*Sleep*) during the observation window. — No error shall be signalled at the host interface of all observed nodes. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 167 defines the test instances for operation mode change from BD_ReceiveOnly to BD_Sleep due to host command test case defined in Table 166.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 167 — Test instances for operation mode change from *BD_ReceiveOnly* to *BD_Sleep* due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.31 Operation mode change from *BD_Normal* via *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}

Table 168 defines the test case for Operation mode change from BD_Normal via BD_Standby to BD_Sleep due to undervoltage of V_{CC}.

Table 168 — Test case for operation mode change from *BD_Normal* via *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}

Name	Operation mode change from *BD_Normal* via *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_Normal* mode via *BD_Standby* to *BD_Sleep* in case of an undervoltage on V_{CC} according to ISO 17458-4 while V_{BAT}, but not V_{IO} is implemented and no other stress condition is present. In case of a missing V_{BAT} supply input, see test case 9.3.14.1 and skip this test case. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is implemented — a V_{CC} supply input is not available.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — Ground shift: 0 V. — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24.

Name	Operation mode change from *BD_Normal* via *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}
	i) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. j) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. k) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. m) Wait 5,0 µs. n) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the test execution. — *uINH1* of node 24 shall be in logical LOW state (*Not_Sleep*) during the test execution. — In case that hard wired signals as host interface are implemented: — The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 169 defines the test instances for operation mode change from BD_Normal via BD_Standby to BD_Sleep due to undervoltage of V_{CC} test case defined in Table 168.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 169 — Test instances for operation mode change from *BD_Normal* via *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.32 Operation mode change from *BD_ReceiveOnly* via *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}

Table 170 defines the test case for operation mode change from BD_ReceiveOnly via BD_Standby to BD_Sleep due to undervoltage of V_{CC}.

Table 170 — Test case for operation mode change from *BD_ReceiveOnly* via *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}

Name	Operation mode change from *BD_ReceiveOnly* via *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_ReceiveOnly* mode via *BD_Standby* to *BD_Sleep* in case of an undervoltage on V_{CC} according to ISO 17458-4 while V_{BAT}, but no V_{IO} is implemented and no other stress condition is present. In case of a missing V_{BAT} supply input, see test 9.3.12.1 and skip this test case. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is implemented — the *BD_ReceiveOnly* mode is not implemented — a V_{CC} supply input is not available.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — Ground shift: 0 V — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24.

Name	Operation mode change from *BD_ReceiveOnly* via *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}
	g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. i) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. j) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. k) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. m) Wait 5,0 µs. n) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the test execution. — in case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the test execution. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 171 defines the test instances for operation mode change from BD_ReceiveOnly via BD_Standby to *Sleep* due to undervoltage of V_{CC} test case defined in Table 170.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 171 — Test instances for operation mode change from *BD_ReceiveOnly* via *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.7.33 Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}

Table 172 defines the test case for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{CC}.

Table 172 — Test case for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}
Test purpose	This test checks the fail silent behaviour and the ability of the IUT to change from *BD_Standby* mode to *BD_Standby* in case of an undervoltage on V_{CC} according to ISO 17458-4 while V_{BAT}, but no V_{IO} is implemented and no other stress condition is present. In case of a missing V_{BAT} supply input, see test 9.3.12.1 and skip this test case. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is implemented — a V_{CC} supply input is not available.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — Ground shift: 0 V — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24.

Name	Operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}
	i) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. j) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. k) After the detection of the undervoltage condition by the IUT, i.e. after the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. m) Wait 5,0 µs. n) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the test execution. — In case of an available ERRN signal *uERRN* of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case of an available INTN signal *uINTN* of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

Table 173 defines the test instances for operation mode change from BD_Standby to BD_Sleep due to undervoltage of V_{CC} test case defined in Table 172.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 173 — Test instances for operation mode change from *BD_Standby* to *BD_Sleep* due to undervoltage of V_{CC}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8 Mode.Bus Driver.ReceiveOnly

9.3.8.1 Operation mode change from *BD_Normal* to *BD_ReceiveOnly* due to host command

Table 174 defines the test case for operation mode change from BD_Normal to BD_ReceiveOnly due to host command.

Table 174 — Test case for operation mode change from *BD_Normal* to *BD_ReceiveOnly* due to host command

Name	**Operation mode change from *BD_Normal* to *BD_ReceiveOnly* due to host command**
Test purpose	This test checks the ability of the IUT to change its mode from *BD_Normal* to *BD_ReceiveOnly* due to host command according to ISO 17458-4 while no stress condition is present. This test case is skipped if the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test).
Preamble (setup state)	Standard preamble.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. f) Stimulate the IUTs in all nodes except node 24 via the host interface to enter *BD_ReceiveOnly*. The IUT in node 24 remains in *BD_Normal*.

Name	Operation mode change from *BD_Normal* to *BD_ReceiveOnly* due to host command
	g) Wait 100 µs for the IUT to enter *BD_ReceiveOnly*. h) Stimulate the IUTs of transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall not contain any 50/50 pattern transmitted at *uTxD* and *uTxEN* of all other nodes, i.e. the IUTs in all nodes except node 24 shall not transmit any data while in *BD_ReceiveOnly* mode. — *uRxD* of node 24 shall contain the 50/50 pattern transmitted at *uTxD* and *uTxEN* of node 24 due to loopback functionality. — *uRxD* of all nodes shall contain the 50/50 pattern transmitted at *uTxD* and *uTxEN* of node 24, i.e. the IUTs in all nodes except node 24 shall receive data while in *BD_ReceiveOnly* mode. — *uRxD* of all nodes shall be in logical HIGH state before the negative edge on *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical HIGH state before the IUT in node 24 is stimulated to transmit (falling edge of *uTxD* and *uTxEN* of node 24) and shall be in logical LOW state while the signal *uRxD* of the corresponding node signals the received pattern. — In case of an available INH1 signal *uINH1* of all observed nodes shall be in logical HIGH state (*Not_Sleep*) during the observation window.

Table 175 defines the test instances for operation mode change from BD_Normal to BD_ReceiveOnly due to host command test case defined in Table 174.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 175 — Test instances for operation mode change from *BD_Normal* to *BD_ReceiveOnly* due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.2 Operation mode change from *BD_Standby* to *BD_ReceiveOnly* due to host command

Table 176 defines the test case for operation mode change from BD_Standby to BD_ReceiveOnly due to host command.

Table 176 — Test case for operation mode change from *BD_Standby* to *BD_ReceiveOnly* due to host command

Name	**Operation mode change from *BD_Standby* to *BD_ReceiveOnly* due to host command**
Test purpose	This test checks the ability of the IUT to change its mode from *BD_Standby* to *BD_ReceiveOnly* due to host command according to ISO 17458-4 while no stress condition is present. This test case is skipped if the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test).
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of all nodes. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. g) Stimulate the IUTs in all nodes except node 24 via the host interface to enter

Name	Operation mode change from *BD_Standby* to *BD_ReceiveOnly* due to host command
	BD_ReceiveOnly. The IUT in node 24 remains in *BD_Normal*. h) Wait 100 µs for the IUT to enter *BD_ReceiveOnly*. i) Stimulate the IUTs of transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall not contain any 50/50 patterns transmitted at *uTxD* and *uTxEN* of all other nodes, i.e. the IUTs in all nodes except node 24 shall not transmit any data while in *BD_ReceiveOnly* mode. — *uRxD* of node 24 shall contain the 50/50 pattern transmitted at *uTxD* and *uTxEN* of node 24 due to loopback functionality. — *uRxD* of all nodes shall contain the 50/50 pattern transmitted at *uTxD* and *uTxEN* of node 24, i.e. the IUTs in all nodes except node 24 shall receive data while in *BD_ReceiveOnly* mode. — *uRxD* of all nodes shall be in logical HIGH state before the negative edge on *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical HIGH state before the IUT in node 24 is stimulated to transmit (falling edge of *uTxD* and *uTxEN* of node 24) and shall be in logical LOW state while *uRxD* of the corresponding node signals the received pattern. — No error shall be signalled via the host interfaces of all nodes. — In case of an available INH1 signal *uINH1* of all nodes shall be in logical HIGH state (*Not_Sleep*) during the test execution.

Table 177 defines the test instances for operation mode change from BD_Standby to BD_ReceiveOnly due to host command test case defined in Table 176.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 177 — Test instances for operation mode change from *BD_Standby* to *BD_ReceiveOnly* due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.3 Wakeup source indication (RWU, initial operation mode is *BD_Sleep*)

Table 178 defines the test case for wakeup source indication (RWU, initial operation mode is BD_Sleep).

Table 178 — Test case for wakeup source indication (RWU, initial operation mode is *BD_Sleep*)

Name	Wakeup source indication (RWU, initial operation mode is *BD_Sleep*)
Test purpose	This test checks the ability of the IUT to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a remote wakeup (RWU) event according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver remote wakeup” is not implemented — the *BD_ReceiveOnly* mode is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Sleep*. The IUTs of all other nodes remain in *BD_Normal*. — Set the EN signal of node 24 to LOW.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24.

Name	Wakeup source indication (RWU, initial operation mode is *BD_Sleep*)
	e) Observe and acquire *uEN* at *TP_N24_EN* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. i) Stimulate the IUT of node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1. j) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern) *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern) *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — INH1 signal *uINH1* of node 24 shall be in logical LOW state (*Sleep*) at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. the IUT is in *BD_Standby* mode. — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 100 µs after the beginning of the wakeup pattern), *uERRN* of node 24 shall be in logical LOW state. Due to wakeup source indication, the ERRN signal shall be in logical LOW state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 179 defines the test instances for wakeup source indication (RWU, initial operation mode is BD_Sleep) test case defined in Table 178.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 179 — Test instances for wakeup source indication (RWU, initial operation mode is *BD_Sleep*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.4 Wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*)

Table 180 defines the test case for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*).

Table 180 — Test case for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*)

Name	Wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*)
Test purpose	This test checks the ability of the IUT to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event (negative pulse) according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Sleep*. The IUTs of all other nodes remain in *BD_Normal*. — Set the EN signal of node 24 to LOW.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. b) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24.

Name	Wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*)
	c) Observe and acquire *uEN* at *TP_N24_EN* of node 24. d) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. f) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Apply a negative wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. i) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — INH1 signal *uINH1* of node 24 shall be in logical LOW state (*Sleep*) while the IUT of node 24 is in *BD_Sleep* mode at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uINH1* shall be in logical HIGH state (*Not_Sleep*). — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. Due to wakeup source indication, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 181 defines the test instances for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*) test case defined in Table 180.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 181 — Test instances for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.5 Wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*)

Table 182 defines the test case for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*).

Table 182 — Test case for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*)

Name	Wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*)
Test purpose	This test checks the ability of the IUT to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event (positive pulse) according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup (positive pulse) is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Sleep*. The IUTs of all other nodes remain in *BD_Normal*. — Set the EN signal of node 24 to LOW.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. b) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. c) Observe and acquire *uEN* at *TP_N24_EN* of node 24.

Name	Wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*)
	d) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. f) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Apply a positive wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. i) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — INH1 signal *uINH1* of node 24 shall be in logical LOW state (*Sleep*) while the IUT of node 24 is in *BD_Sleep* mode at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 600 µs after the occurrence of the local wakeup event), *uINH1* shall be in logical HIGH state (*Not_Sleep*). — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. Due to wakeup source indication, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 183 defines the test instances for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*) test case defined in Table 182.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 183 — Test instances for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.6 Wakeup source indication (RWU, initial operation mode is *BD_Standby*)

Table 184 defines the test case for wakeup source indication (RWU, initial operation mode is BD_Standby).

Table 184 — Test case for wakeup source indication (RWU, initial operation mode is *BD_Standby*)

Name	Wakeup source indication (RWU, initial operation mode is *BD_Standby*)
Test purpose	This test checks the ability of the IUT to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a remote wakeup (RWU) event according to ISO 17458-4 and no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver remote wakeup” is not implemented — the *BD_ReceiveOnly* mode is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. The IUTs of all other nodes remain in *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. e) Observe and acquire *uEN* at *TP_N24_EN* of node 24.

Name	Wakeup source indication (RWU, initial operation mode is ***BD_Standby***)
	f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. i) Stimulate the IUT of node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1. j) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern) *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly.* — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern) *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected between 31 µs after the beginning of the wakeup pattern and 134 µs + 100 µs after the beginning of the wakeup pattern), *uERRN* of node 24 shall be in logical LOW state. Due to wakeup source indication, the ERRN signal shall be in logical LOW state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 185 defines the test instances for wakeup source indication (RWU, initial operation mode is BD_Standby) test case defined in Table 184.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 185 — Test instances for wakeup source indication (RWU, initial operation mode is *BD_Standby*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.7 Wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Standby*)

Table 186 defines the test case for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Standby*).

Table 186 — Test case for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Standby*)

Name	Wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Standby*)
Test purpose	This test checks the ability of the IUT to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event (negative pulse) according to ISO 17458-4 and no stress condition is present. This test case is skipped if — neither the Functional class "Bus driver voltage regulator control" nor the subgroup BDControl within the Functional class "Bus driver internal voltage regulator" is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup is not implemented — the host interface A (hard-wired signals) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	— In case that only V_{BAT} is implemented:
	V_{BAT} power supply of all nodes: default.
	— V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: none.

Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. The IUTs of all other nodes remain in *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. b) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. c) Observe and acquire *uEN* at *TP_N24_EN* of node 24. d) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24.

Name	Wakeup source indication (LWU, negative pulse, initial operation mode is ***BD_Standby***)
	f) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Apply a negative wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. i) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. Due to wakeup source indication, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 187 defines the test instances for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Standby*) test case defined in Table 186.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 187 — Test instances for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Standby*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.8 Wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Standby*)

Table 188 defines the test case for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Standby*).

Table 188 — Test case for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Standby*)

Name	Wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Standby*)
Test purpose	This test checks the ability of the IUT to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event (positive pulse) according to ISO 17458-4 and no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup (positive pulse) is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. The IUTs of all other nodes remain in *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. b) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. c) Observe and acquire *uEN* at *TP_N24_EN* of node 24. d) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24.

Name	Wakeup source indication (LWU, positive pulse, initial operation mode is ***BD_Standby***)
	e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. f) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Apply a positive wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. i) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. Due to wakeup source indication, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 189 defines the test instances for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Standby*) test case defined in Table 188.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 189 — Test instances for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Standby*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.9 Wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*, active failure)

Table 190 defines the test case for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*, active failure).

Table 190 — Test case for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*, active failure)

Name	**Wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*, active failure)**
Test purpose	This test checks the ability of the IUT to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event (negative pulse) according to ISO 17458-4 while an active failure in *BD_ReceiveOnly* mode is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Sleep*. The IUTs of all other nodes remain in *BD_Normal*. — Set the EN signal of node 24 to LOW.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24.

Name	Wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*, active failure)
	c) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. d) Observe and acquire *uEN* at *TP_N24_EN* of node 24. e) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. i) Apply a negative wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. j) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*. k) Short-circuit TxEN and GND of the IUT in node 24 according to Figure 19 and Table 26, failure FL4. l) Wait 2 600 µs.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the beg occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — *uINH1* shall be in logical LOW state (Sleep) while the IUT of node 24 is in *BD_Sleep* mode at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uINH1* shall be in logical HIGH state (*Not_Sleep*). — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. Due to wakeup source indication, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 191 defines the test instances for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*, active failure) test case defined in Table 190.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 191 — Test instances for wakeup source indication (LWU, negative pulse, initial operation mode is *BD_Sleep*, active failure)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.10 Wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*, active failure)

Table 192 defines the test case for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*, active failure).

Table 192 — Test case for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*, active failure)

Name	**Wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*, active failure)**
Test purpose	This test checks the ability of the IUT to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event (positive pulse) according to ISO 17458-4 while an active failure in *BD_ReceiveOnly* mode is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup (positive pulse) is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} supply input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Sleep*. The IUTs of all other nodes remain in *BD_Normal*. — Set the EN signal of node 24 to LOW.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24.

Name	Wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*, active failure)
	b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. d) Observe and acquire *uEN* at *TP_N24_EN* of node 24. e) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. i) Apply a positive wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. j) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*. k) Short-circuit TxEN and GND of the IUT in node 24 according to Figure 19 and Table 26, failure FL4. l) Wait 2 600 µs.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_ReceiveOnly*. — *uINH1* shall be in logical LOW state (Sleep) while the IUT of node 24 is in *BD_Sleep* mode at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uINH1* shall be in logical HIGH state (*Not_Sleep*). — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. Due to wakeup source indication, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 193 defines the test instances for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*, active failure) test case defined in Table 192.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 193 — Test instances for wakeup source indication (LWU, positive pulse, initial operation mode is *BD_Sleep*, active failure)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.11 No wakeup source indication after passing *BD_Normal* (RWU, initial operation mode is *BD_Standby*)

Table 194 defines the test case for no wakeup source indication after passing BD_Normal (RWU, initial operation mode is *BD_Standby*).

Table 194 — Test case for no wakeup source indication after passing *BD_Normal* (RWU, initial operation mode is *BD_Standby*)

Name	**No wakeup source indication after passing *BD_Normal* (RWU, initial operation mode is *BD_Standby*)**
Test purpose	This test checks the ability of the IUT not to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a remote wakeup (RWU) event according to ISO 17458-4 and entering *BD_Normal* mode while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver remote wakeup” is not implemented — the *BD_ReceiveOnly* mode is not implemented — the host interface A (hard-wired signals) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	— In case that only V_{BAT} is implemented:
	V_{BAT} power supply of all nodes: default.
	— V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 as transmitter.

Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. The IUTs of all other nodes remain in *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24.

Name	**No wakeup source indication after passing *BD_Normal* (RWU, initial operation mode is *BD_Standby*)**
	e) Observe and acquire *uEN* at *TP_N24_EN* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. i) Stimulate the IUT of node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1. j) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. k) Wait 100 µs for the IUT in node 24 to enter *BD_Normal*. l) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern) *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern) *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 100 µs after the beginning of the wakeup pattern), *uERRN* of node 24 shall be in logical LOW state. Due to not signaling the wakeup source, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_Normal* mode.

Table 195 defines the test instances for no wakeup source indication after passing BD_Normal (RWU, initial operation mode is *BD_Standby*) test case defined in Table 194.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 195 — Test instances for no wakeup source indication after passing *BD_Normal* (RWU, initial operation mode is *BD_Standby*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.12 No wakeup source indication after passing *BD_Normal* (LWU, negative pulse, initial operation mode is *BD_Standby*)

Table 196 defines the test case for no wakeup source indication after passing BD_Normal (LWU, negative pulse, initial operation mode is *BD_Standby*).

Table 196 — Test case for no wakeup source indication after passing *BD_Normal* (LWU, negative pulse, initial operation mode is *BD_Standby*)

Name	**No wakeup source indication after passing *BD_Normal* (LWU, negative pulse, initial operation mode is *BD_Standby*)**
Test purpose	This test checks the ability of the IUT not to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event (negative pulse) according to ISO 17458-4 and entering *BD_Normal* mode while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup (negative pulse) is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. The IUTs of all other nodes remain in *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. b) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. c) Observe and acquire *uEN* at *TP_N24_EN* of node 24.

Name	**No wakeup source indication after passing *BD_Normal* (LWU, negative pulse, initial operation mode is *BD_Standby*)**
	d) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. f) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Apply a negative wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. i) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. j) Wait 100 µs for the IUT in node 24 to enter *BD_Normal*. k) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. Due to not signaling the wakeup source, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_Normal* mode.

Table 197 defines the test instances for no wakeup source indication after passing BD_Normal (LWU, negative pulse, initial operation mode is *BD_Standby*) test case defined in Table 196.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 197 — Test instances for no wakeup source indication after passing *BD_Normal* (LWU, negative pulse, initial operation mode is *BD_Standby*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.13 No wakeup source indication after passing *BD_Normal* (LWU, positive pulse, initial operation mode is *BD_Standby*)

Table 198 defines the test case for no wakeup source indication after passing BD_Normal (LWU, positive pulse, initial operation mode is *BD_Standby*).

Table 198 — Test case for no wakeup source indication after passing *BD_Normal* (LWU, positive pulse, initial operation mode is *BD_Standby*)

Name	**No wakeup source indication after passing *BD_Normal* (LWU, positive pulse, initial operation mode is *BD_Standby*)**
Test purpose	This test checks the ability of the IUT not to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event (positive pulse) according to ISO 17458-4 and entering *BD_Normal* mode while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup (positive pulse) is not implemented — the host interface A (hard-wired signals) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	— In case that only V_{BAT} is implemented:
	V_{BAT} power supply of all nodes: default.
	— V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: none.

Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. The IUTs of all other nodes remain in *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. b) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. c) Observe and acquire *uEN* at *TP_N24_EN* of node 24. d) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24.

Name	**No wakeup source indication after passing *BD_Normal* (LWU, positive pulse, initial operation mode is *BD_Standby*)**
	e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. f) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Apply a positive wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. i) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. j) Wait 100 µs for the IUT in node 24 to enter *BD_Normal*. k) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. Due to not signaling the wakeup source, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_Normal* mode.

Table 199 defines the test instances for no wakeup source indication after passing BD_Normal (LWU, positive pulse, initial operation mode is *BD_Standby*) test case defined in Table 198.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 199 — Test instances for no wakeup source indication after passing *BD_Normal* (LWU, positive pulse, initial operation mode is *BD_Standby*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.14 No wakeup source indication after passing *BD_Normal* (RWU, initial operation mode is *BD_Sleep*)

Table 200 defines the test case for no wakeup source indication after passing BD_Normal (RWU, initial operation mode is *BD_Sleep*).

Table 200 — Test case for no wakeup source indication after passing *BD_Normal* (RWU, initial operation mode is *BD_Sleep*)

Name	**No wakeup source indication after passing *BD_Normal* (RWU, initial operation mode is *BD_Sleep*)**
Test purpose	This test checks the ability of the IUT not to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a remote wakeup (RWU) event according to ISO 17458-4 and entering *BD_Normal* mode while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver remote wakeup” is not implemented — the *BD_ReceiveOnly* mode is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Sleep*. The IUTs of all other nodes remain in *BD_Normal*. — Set the EN signal of node 24 to LOW.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23.

Name	**No wakeup source indication after passing *BD_Normal* (RWU, initial operation mode is *BD_Sleep*)**
	b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. e) Observe and acquire *uEN* at *TP_N24_EN* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. i) Stimulate the IUT of node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1. j) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. k) Wait 100 µs for the IUT in node 24 to enter *BD_Normal*. l) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern) *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern) *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. the IUT is in *BD_Standby* mode. — *uERRN* of node 24 shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs + 100 µs after the beginning of the wakeup pattern), *uERRN* of node 24 shall be in logical LOW state. Due to not signaling the wakeup source, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_Normal* mode.

Table 201 defines the test instances for no wakeup source indication after passing BD_Normal (RWU, initial operation mode is *BD_Sleep*) test case defined in Table 200.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 201 — Test instances for no wakeup source indication after passing *BD_Normal* (RWU, initial operation mode is *BD_Sleep*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.15 No wakeup source indication after passing *BD_Normal* (LWU, negative pulse, initial operation mode is *BD_Sleep*)

Table 202 defines the test case for no wakeup source indication after passing BD_Normal (LWU, negative pulse, initial operation mode is *BD_Sleep*).

Table 202 — Test case for no wakeup source indication after passing *BD_Normal* (LWU, negative pulse, initial operation mode is *BD_Sleep*)

Name	**No wakeup source indication after passing *BD_Normal* (LWU, negative pulse, initial operation mode is *BD_Sleep*)**
Test purpose	This test checks the ability of the IUT not to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event according to ISO 17458-4 and entering *BD_Normal* mode while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup (negative pulse) is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Sleep*. The IUTs of all other nodes remain in *BD_Normal*. — Set the EN signal of node 24 to LOW.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. b) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24.

Name	**No wakeup source indication after passing *BD_Normal* (LWU, negative pulse, initial operation mode is *BD_Sleep*)**
	c) Observe and acquire *uEN* at *TP_N24_EN* of node 24. d) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. f) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Apply a negative wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. i) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. j) Wait 100 µs for the IUT in node 24 to enter *BD_Normal*. k) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — INH1 signal *uINH1* of node 24 shall be in logical LOW state (*Sleep*) while the IUT of node 24 is in *BD_Sleep* mode at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the be occurrence of the local wakeup event), *uINH1* shall be in logical HIGH state (*Not_Sleep*). — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. Due to not signaling the wakeup source, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_Normal* mode.

Table 203 defines the test instances for no wakeup source indication after passing BD_Normal (LWU, negative pulse, initial operation mode is *BD_Sleep*) test case defined in Table 202.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 203 — Test instances for no wakeup source indication after passing *BD_Normal* (LWU, negative pulse, initial operation mode is *BD_Sleep*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.16 No wakeup source indication after passing *BD_Normal* (LWU, positive pulse, initial operation mode is *BD_Sleep*)

Table 204 defines the test case for no wakeup source indication after passing BD_Normal (LWU, positive pulse, initial operation mode is *BD_Sleep*).

Table 204 — Test case for no wakeup source indication after passing *BD_Normal* (LWU, positive pulse, initial operation mode is *BD_Sleep*)

Name	**No wakeup source indication after passing *BD_Normal* (LWU, positive pulse, initial operation mode is *BD_Sleep*)**
Test purpose	This test checks the ability of the IUT not to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event according to ISO 17458-4 and entering *BD_Normal* mode while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup (positive) is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Sleep*. The IUTs of all other nodes remain in *BD_Normal*. — Set the EN signal of node 24 to LOW.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24.

Name	**No wakeup source indication after passing *BD_Normal* (LWU, positive pulse, initial operation mode is *BD_Sleep*)**
	b) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. c) Observe and acquire *uEN* at *TP_N24_EN* of node 24. d) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. f) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Apply a positive wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. i) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. j) Wait 100 µs for the IUT in node 24 to enter *BD_Normal*. k) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state until the IUT is stimulated to enter *BD_Normal*. — INH1 signal *uINH1* of node 24 shall be in logical LOW state (*Sleep*) while the IUT of node 24 is in *BD_Sleep* mode at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uINH1* shall be in logical HIGH state (*Not_Sleep*) — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. Due to not signaling the wakeup source, the ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 205 defines the test instances for for no wakeup source indication after passing BD_Normal (LWU, positive pulse, initial operation mode is *BD_Sleep*) test case defined in Table 204.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 205 — Test instances for for no wakeup source indication after passing *BD_Normal* (LWU, positive pulse, initial operation mode is *BD_Sleep*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.17 Wakeup source indication with active failure (LWU, negative pulse, initial operation mode is *BD_Standby*)

Table 206 defines the test case for wakeup source indication with active failure (LWU, negative pulse, initial operation mode is *BD_Standby*).

Table 206 — Test case for wakeup source indication with active failure (LWU, negative pulse, initial operation mode is *BD_Standby*)

Name	**Wakeup source indication with active failure (LWU, negative pulse, initial operation mode is *BD_Standby*)**
Test purpose	This test checks the ability of the IUT to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup (LWU) event (negative pulse) according to ISO 17458-4 while an active failure in *BD_ReceiveOnly* mode is present. This test case is skipped if neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented the *BD_ReceiveOnly* mode is not implemented the local wakeup is not implemented the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. The IUTs of all other nodes remain in *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. b) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. c) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. d) Observe and acquire *uEN* at *TP_N24_EN* of node 24. e) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24.

Name	**Wakeup source indication with active failure (LWU, negative pulse, initial operation mode is *BD_Standby*)**
	f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. i) Apply a negative wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in [EPL09]. j) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*. k) Short-circuit TxEN and GND of the IUT in node 24 according to Figure 19 and Table 26, failure FL4. l) Wait 2 600 µs.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. The ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 207 defines the test instances for wakeup source indication with active failure (LWU, negative pulse, initial operation mode is *BD_Standby*) test case defined in Table 206.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 207 — Test instances for wakeup source indication with active failure (LWU, negative pulse, initial operation mode is *BD_Standby*)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.18 Wakeup source indication with active failure (LWU, positive pulse, initial operation mode is *BD_Standby*)

Table 208 defines the test case for wakeup source indication with active failure (LWU, positive pulse, initial operation mode is *BD_Standby*).

Table 208 — Test case for wakeup source indication with active failure (LWU, positive pulse, initial operation mode is *BD_Standby*)

Name	**Wakeup source indication with active failure (LWU, positive pulse, initial operation mode is *BD_Standby*)**
Test purpose	This test checks the ability of the IUT to signal the wakeup source while the IUT is in *BD_ReceiveOnly* mode after a local wakeup event (positive pulse) according to ISO 17458-4 while an active failure in *BD_ReceiveOnly* mode is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the local wakeup (positive pulse) is not implemented — the host interface A (hard-wired signals) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	— In case that only V_{BAT} is implemented:
	V_{BAT} power supply of all nodes: default.
	— V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: none.

Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. The IUTs of all other nodes remain in *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. b) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. c) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24.

Name	**Wakeup source indication with active failure (LWU, positive pulse, initial operation mode is *BD_Standby*)**
	d) Observe and acquire *uEN* at *TP_N24_EN* of node 24. e) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. i) Apply a positive wakeup pulse of 500 µs to the IUT in node 24 at *TP_N24_WAKE* according to *dBDWakePulseFilter* in ISO 17458-4. j) After at least 100 µs + 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. The IUTs of all other nodes remain in *BD_Normal*. k) Short-circuit TxEN and GND of the IUT in node 24 according to Figure 19 and Table 26, failure FL4. l) Wait 2 600 µs.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxD* of node 24 shall be in logical LOW state. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uRxEN* of node 24 shall be in logical LOW state. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — The ERRN signal *uERRN* of node 24 shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs + 100 µs after the occurrence of the local wakeup event), *uERRN* of node 24 shall be in logical LOW state. The ERRN signal shall be in logical HIGH state 100 µs + 100 µs after entering the *BD_ReceiveOnly* mode.

Table 209 defines the test instances for wakeup source indication with active failure (LWU, positive pulse, initial operation mode is *BD_Standby*) test case defined in Table 208.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 209 — Test instances for wakeup source indication with active failure (LWU, positive pulse, initial operation mode is *BD_Standby*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.19 Operation mode change from *BD_Sleep* to *BD_ReceiveOnly* due to host command

Table 210 defines the test case for operation mode change from BD_Sleep to BD_ReceiveOnly due to host command.

Table 210 — Test case for operation mode change from *BD_Sleep* to *BD_ReceiveOnly* due to host command

Name	Operation mode change from *BD_Sleep* to *BD_ReceiveOnly* due to host command
Test purpose	This test checks the ability of the IUT to change its mode from *BD_Sleep* to *BD_ReceiveOnly* due to host command according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test).
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	The observation shall start 100 µs (*dBDModeChange*) after the host command is applied. a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of all nodes. e) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. g) Stimulate the IUTs in all nodes except node 24 via the host interface to enter

Name	Operation mode change from *BD_Sleep* to *BD_ReceiveOnly* due to host command
	BD_ReceiveOnly. The IUT in node 24 remains in *BD_Normal*. h) Wait 100 µs for the IUTs to enter *BD_ReceiveOnly*. i) Stimulate the IUTs of transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall not contain any 50/50 pattern transmitted at *uTxD* and *uTxEN* of all other nodes, i.e. the IUTs in all nodes except node 24 shall not transmit any data while in *BD_ReceiveOnly* mode. — *uRxD* of all nodes shall contain the 50/50 pattern transmitted at *uTxD* and *uTxEN* of node 24, i.e. the IUTs in all nodes except node 24 shall receive data while in *BD_ReceiveOnly* mode. — *uRxD* of node 24 shall contain the 50/50 pattern transmitted at *uTxD* and *uTxEN* of node 24 due to loopback functionality. — *uRxD* of all nodes shall be in logical HIGH state before the negative edge on *uTxEN* of node 24. — *uINH1* of all nodes shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical HIGH state before the IUT in node 24 is stimulated to transmit (falling edge of *uTxD* and *uTxEN* of node 24) and shall be in logical LOW state while the signal *uRxD* of the corresponding node signals the received pattern. — No error shall be signalled via the host interfaces of all nodes.

Table 211 defines the test instances for operation mode change from BD_Sleep to BD_ReceiveOnly due to host command test case defined in Table 210.

Table 211 — Test instances for operation mode change from *BD_Sleep* to *BD_ReceiveOnly* due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.8.20 Failure indication after wakeup (RWU, initial operation mode is *BD_Standby*)

Table 212 defines the test case for failure indication after wakeup (RWU, initial operation mode is *BD_Standby*).

Table 212 — Test case for failure indication after wakeup (RWU, initial operation mode is *BD_Standby*)

Name	Failure indication after wakeup (RWU, negative pulse, initial operation mode is *BD_Standby*)
Test purpose	This test checks the ability of the IUT to signal an error while the IUT is in *BD_ReceiveOnly* mode when EN has been set to HIGH after a previous remote wakeup (RWU) event according ISO 17458-4 while an active failure in *BD_ReceiveOnly* mode is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — the Functional class “Bus driver remote wakeup” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. The IUTs of all other nodes remain in *BD_Normal*. — Switch TxD signal of node 24 to unconnected according to Figure 19 and Table 26, failure FL6.
Test execution	a) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. b) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. c) Observe and acquire *uSTBN* at *TP_N24_STBN* of node 24. d) Observe and acquire *uEN* at *TP_N24_EN* of node 24. e) Observe and acquire *uWAKE* at *TP_N24_WAKE* of node 24.

Name	Failure indication after wakeup (RWU, negative pulse, initial operation mode is *BD_Standby*)
	f) Observe and acquire the error signal of the host interface (*TP_N24_WERN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. i) Stimulate the IUT of node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1. j) After at least 100 µs stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. The IUTs of all other nodes remain in *BD_Normal*. k) After 100 µs + 100 µs short-circuit TxEN and GND of the IUT in node 24 according to Figure 19 and Table 26, failure FL4. l) After at least 2 600 µs stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly.* The IUTs of all other nodes remain in *BD_Normal*. m) Wait 100 µs + 100 µs. n) Trigger the logic analyzer to start the observation synchronously with the stimulation of node 24 to enter *BD_ReceiveOnly* mode.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall be in logical HIGH state after the stimulation of node 24 to enter *BD_ReceiveOnly* mode. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state after the stimulation of node 24 to enter *BD_ReceiveOnly* mode. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) after the stimulation of node 24 to enter *BD_ReceiveOnly* mode. — The ERRN signal *uERRN* of node 24 shall be in logical LOW state latest 100 µs + 100 µs after the stimulation of node 24 to enter BD_ReceiveOnly mode.

Table 213 defines the test instances for failure indication after wakeup (RWU, initial operation mode is *BD_Standby*) test case defined in Table 212.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 213 — Test instances for failure indication after wakeup (RWU, initial operation mode is *BD_Standby*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.9 Failure.Loss

9.3.9.1 Failure: STBN unconnected

Table 214 defines the test case for failure: STBN unconnected.

Table 214 — Test case for failure: STBN unconnected

Name	Failure: STBN unconnected
Test purpose	This test checks the behaviour of the IUT in case of an unconnected STBN signal according ISO 17458-4. This test case is skipped if the STBN signal (host interface option A) is not implemented. This test case considers only the *BD_Normal* mode.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: STBN unconnected. — Communication: node 24 and 1 as transmitter.
Preamble (setup state)	— Standard preamble. — Switch STBN signal of node 24 to unconnected according to Figure 19 and Table 26, failure FL9 and all available mode control signals (EN) to logical LOW state.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. d) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of

Name	Failure: STBN unconnected
	node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24., i) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by two wakeup patterns. j) Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by two wakeup patterns.
Postamble	Standard postamble.
Pass criteria	Due to $dWakeUpReaction_{remote}$ the observed signals shall be observed and acquired at least for 100 µs + 100 µs. — *uRxD* of all nodes shall be in logical HIGH state while the IUT in node 24 is stimulated to transmit (while *uTxEN* of node 24 is in logical LOW), i.e. the IUT in node 24 shall not transmit any pattern in *BD_Standby* mode. — *uRxD* of node 24 shall contain one falling edge (remote wakeup detection implemented) or no falling edge (remote wakeup not implemented), i.e. node 24 may receive the wakeup patterns applied to *uTxD* and *uTxEN* of node 1. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state before the first falling edge of *uTxD* or *uTxEN* of node 1. After the first falling edge of *uTxD* or *uTxEN* of node 1, *uRxEN* of node 24 shall contain one falling edge (remote wakeup detection implemented) or no falling edge (remote wakeup not implemented), i.e. node 24 may receive the wakeup patterns applied to *TP_N1_TxD* and *TP_N1_TxEN* of node 1. — The error signal at the host interface of node 24 shall be in logical HIGH state before the first falling edge of *uTxD* and *uTxEN* of node. After the first falling edge of *uTxD* or *uTxEN* of node 1, the error signal of node 24 shall contain one falling edge (remote wakeup detection implemented) or no falling edge (remote wakeup not implemented), i.e. the wakeup event may have been detected.

9.3.9.2 Failure: EN unconnected

Table 215 defines the test case for failure: EN unconnected.

Table 215 — Test case for failure: EN unconnected

Name	Failure: EN unconnected
Test purpose	This test checks the behaviour of the IUT in case of an unconnected EN signal according to ISO 17458-4. This test case considers only the *BD_Normal* mode. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the host interface A (hard-wired signals) is not implemented
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: EN unconnected. — Communication: node 24 and 1 as transmitter.
Preamble (setup state)	— Standard preamble. — Switch EN signal of node 24 to unconnected according to Figure 19 and Table 26, failure FL18 and all other available mode control signals (EN) and STBN to logical LOW state.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. d) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. f) Observe and acquire the error signal of the host interface (*TP_N24_ERRN*) of node 24. g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of

Name	Failure: EN unconnected
	node 24. i) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by two wakeup patterns. j) Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by two wakeup patterns.
Postamble	Standard postamble.
Pass criteria	Due to $dWakeUpReaction_{remote}$ the observed signals shall be observed and acquired at least for 100 µs + 100 µs. — *uRxD* of all nodes shall be in logical HIGH state while the IUT in node 24 is stimulated to transmit (while *uTxEN* of node 24 is in logical LOW), i.e. the IUT in node 24 shall not transmit any pattern in *BD_Standby* mode. — *uRxD* of node 24 shall contain one falling edge (remote wakeup detection implemented) or no falling edge (remote wakeup not implemented), i.e. node 24 may receive the wakeup patterns applied to *uTxD* and *uTxEN* of node 1. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state before the first falling edge of *uTxD* or *uTxEN* of node 1. After the first falling edge of *uTxD* or *uTxEN* of node 1, *uRxEN* of node 24 shall contain one falling edge (remote wakeup detection implemented) or no falling edge (remote wakeup not implemented), i.e. node 24 may receive the wakeup patterns applied to *TP_N1_TxD* and *TP_N1_TxEN* of node 1. — The error signal at the host interface of node 24 shall be in logical HIGH state before the first falling edge of *uTxD* and *uTxEN* of node. After the first falling edge of *uTxD* or *uTxEN* of node 1, the error signal of node 24 shall contain one falling edge (remote wakeup detection implemented) or no falling edge (remote wakeup not implemented), i.e. the wakeup event may have been detected.

9.3.9.3 Failure: TxEN unconnected

Table 216 defines the test case for failure: TxEN unconnected.

Table 216 — Test case for failure: TxEN unconnected

Name	Failure: TxEN unconnected
Test purpose	This test checks the behaviour of the IUT in case of an unconnected TxEN signal according to ISO 17458-4. This test case considers only the *BD_Normal* mode.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: TxEN unconnected. — Communication: node 24 and 1 as transmitter.
Preamble (setup state)	— Standard preamble. — Switch TxEN signal of node 24 to unconnected according to Figure 19 and Table 26, failure FL5.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. c) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 50/50 pattern. h) Wait 5 µs.

Name	Failure: TxEN unconnected
	i) Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall be in logical HIGH state while the IUT in node 24 is stimulated to transmit, i.e. the IUT in node 24 shall be fail silent while TxEN is unconnected. — *uRxD* of node 24 shall contain the 50/50 pattern transmitted by node 1. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state before the first falling edge of *uTxD* or *uTxEN* of node 1. Then, *uRxEN* of node 24 shall be in logical LOW state while *uRxD* of node 24 signals the received patterns.

9.3.9.4 Failure: TxD unconnected

Table 217 defines the test case for failure: TxD unconnected.

Table 217 — Test case for failure: TxD unconnected

Name	Failure: TxD unconnected
Test purpose	This test checks the behaviour of the IUT in case of an unconnected TxD signal according to ISO 17458-4. This test case considers only the *BD_Normal* mode.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: TxD unconnected. — Communication: node 24 and 1 as transmitter.
Preamble (setup state)	— Standard preamble. — Switch TxD signal of node 24 to unconnected according to Figure 19 and Table 26, failure FL6.
Test execution	a) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. b) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. c) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. e) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. f) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one wakeup

Name	Failure: TxD unconnected
	pattern, followed by one TSS pattern, followed by one 50/50 pattern. i) Wait 5 µs. j) Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes except node 24 shall contain a logical LOW state sequence of at least 11 bit times after the IUT in node 24 starts TSS pattern transmission (corresponding falling edge of *uTxEN* of node 24), i.e. the IUT in node 24 reads TxD as logical LOW state while TxD is unconnected. — *uRxD* of node 24 shall contain the 50/50 pattern transmitted by node 1. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while *uRxD* of node 24 signals the received patterns. — No error shall be signalled via the host interface of node 24.

9.3.9.5 Failure: BGE unconnected

Table 218 defines the test case for failure: BGE unconnected.

Table 218 — Test case for failure: BGE unconnected

Name	Failure: BGE unconnected
Test purpose	This test checks the behaviour of the IUT in case of an unconnected BGE signal according to ISO 17458-4. This test case is skipped if the Functional class “Bus driver – bus guardian interface” is not implemented. This test case considers only the *BD_Normal* mode.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: BGE unconnected. — Communication: node 24 and 1 as transmitter.
Preamble (setup state)	— Standard preamble. — Switch BGE signal of node 24 to unconnected according to Figure 19 and Table 26, failure FL10.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. d) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. f) In case of an available RxEN signal, observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24.

Name	Failure: BGE unconnected
	h) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 50/50 pattern. i) Wait 5 µs. j) Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall be in logical HIGH state while the IUT in node 24 is stimulated to transmit, i.e. the IUT in node 24 shall be fail silent while BGE is unconnected. — *uRxD* of node 24 shall contain the 50/50 pattern transmitted by node 1. — In case of an available RxEN signal, *uRxEN* of node 24 shall be in logical HIGH state before the first falling edge of *uTxD* or *uTxEN* of node 1. Then, *uRxEN* of node 24 shall be in logical LOW state while *uRxD* of node 24 signals the received patterns. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution.

9.3.9.6 Failure: V_{BAT} interrupted, V_{CC} implemented

Table 219 defines the test case for failure: V_{BAT} interrupted, V_{CC} implemented.

Table 219 — Test case for failure: V_{BAT} interrupted, V_{CC} implemented

Name	**Failure: V_{BAT} interrupted, V_{CC} implemented**
Test purpose	This test checks the behaviour of the IUT in case of an interruption of V_{BAT} according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{BAT} power supply of all nodes: default.
	— V_{CC} power supply of all nodes: +5,0 V.
	— External V_{CC} power supply of the IUT in node 24: +5,0 V.
	— V_{IO} reference voltage (in case of an available V_{IO} input):
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: V_{BAT} interrupted.
	— Communication: none.

Preamble (setup state)	— Standard preamble. — Interrupt supply wire V_{BAT} of the IUT in node 24 according to Figure 19 and Table 26, failure FL1.
Test execution	a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. b) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. c) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. d) Wait at least 200 µs. The duration of the observation and acquisition shall be at least 100 samples for each signal.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled via the host interface of node 24.

Name	Failure: V_{BAT} interrupted, V_{CC} implemented
	— In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.9.7 Failure: V_{CC} interrupted, V_{BAT} implemented

Table 220 defines the test case for failure: V_{CC} interrupted, V_{BAT} implemented.

Table 220 — Test case for failure: V_{CC} interrupted, V_{BAT} implemented

Name	Failure: V_{CC} interrupted, V_{BAT} implemented
Test purpose	This test checks the behaviour of the IUT in case of an interruption of V_{CC} according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— V_{BAT} power supply of all nodes: default.
	— External V_{BAT} power supply of node 24: default.
	— V_{CC} power supply of all nodes: +5,0 V.
	— V_{IO} reference voltage (in case of an available V_{IO} input):
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: V_{CC} interrupted.
	— Communication: none.

Preamble (setup state)	— Standard preamble. — Interrupt supply wire V_{CC} of the IUT in node 24 according to Figure 19 and Table 26, failure FL2.
Test execution	a) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. b) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. c) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. The duration of the observation and acquisition shall be at least 100 samples for each signal.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case that V_{IO} is not implemented: — *uRxD* of node 24 shall be in logical LOW state during the test execution.

Name	Failure: V_{CC} interrupted, V_{BAT} implemented
	— In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the test execution. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution. — In case that V_{IO} is implemented: — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — An error shall be signalled via the host interface of node 24.

9.3.9.8 Failure: BP and BM interrupted

Table 221 defines the test case for failure: BP and BM interrupted.

Table 221 — Test case for failure: BP and BM interrupted

Name	Failure: BP and BM interrupted
Test purpose	This test checks the behaviour of the IUT in case of an interruption of the bus lines BP and BM according to ISO 17458-4. This test case considers only the *BD_Normal* mode.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: BP and BM interrupted. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Interrupt the bus wires BP and BM of the IUT in node 23 according to Figure 23and Table 26, failure FL25. The interruption of the bus wires BP and BM of the IUT in node 23 shall be performed between the termination and the test plane TP2.
Test execution	The observation of *uBus* shall ensure that the bus lines signal *Idle* state due to the failure according to ISO 17458-4. The observation window for the scope shall be 5 µs. The trigger of the oscilloscope shall be synchronously with the first falling edge of *N24_TxEN*. a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 24 and node 23. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 24 and node 23. c) Observe and acquire *uRxD* at *TP_N23_RxD* of node 23. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N23_RxEN* of node 23. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2.

Name	Failure: BP and BM interrupted
	f) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N23_INH1* of node 23. g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Wait 5 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— Due to loopback functionality, *uRxD* of node 23 shall contain the transmitted pattern while node 23 is stimulated to transmit and *uRxEN* of node 23 (in case of an available RxEN signal) shall be in logical LOW state. — *uRxD* of node 23 shall be in logical HIGH state while node 24 is stimulated to transmit, i.e. it shall not contain the 50/50 pattern transmitted by node 24. — In case of an available RxEN signal *uRxEN* of node 23 shall be in logical HIGH state while node 24 is stimulated to transmit, i.e. node 23 shall not receive the 50/50 pattern transmitted by node 24. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — In case of an available INH1 signal *uINH1* of node 23 shall be in logical HIGH state (*Not_Sleep*) during the test execution.

9.3.10 Failure.Short-circuits

9.3.10.1 TxEN shorted to GND

Table 222 defines the test case for TxEN shorted to GND.

Table 222 — Test case for TxEN shorted to GND

Name	**TxEN shorted to GND**
Test purpose	This test checks the behaviour of the IUT when TxEN is shorted to GND according to ISO 17458-4.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: short-circuit of TxEN and GND. — Communication: node 24 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uRxD* at *TP_N23_RxD* of node 23. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N23_RxEN* of node 23. g) Short-circuit TxEN and GND of the IUT in node 24 according to Figure 19 and Table 26, failure FL4. h) Stimulate the IUT in node 24 at *TP_N24_TxD* synchronously with the falling edge of *uTxEN* of node 24 by a logical LOW state sequence of at least 2 600 µs.

Name	TxEN shorted to GND
Postamble	Standard postamble.
Pass criteria	For *dBDTxActiveMax* timeout measurement, a trigger event on the falling edge of *uTxEN* is required. — *uRxD* of node 23 shall be in logical HIGH state before the falling edge of *uTxD* of node 24. After the falling edge of *uTxEN* of node 24, *uRxD* of node 23 shall receive the logical LOW sequence applied at *TP_N24_TxD* of node 24 until the IUT of node 24 disables the transmission after a transmission length of at least 650 µs and not more than 2 600 µs. Thus, *uRxD* of node 23 shall return to logical HIGH state not later than 2 600 µs after the falling edge of *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 23 shall be in logical HIGH state before the falling edge of *uTxD* of node 24. After the falling edge of *uTxEN* of node 24, *uRxEN* of node 23 shall be the logical LOW state according to the sequence applied at *TP_N24_TxD* of node 24 until the IUT of node 24 disables the transmission after a transmission length of at least 650 µs and not more than 2 600 µs. Thus, *uRxEN* of node 23 shall return to logical HIGH state not later than 2 600 µs after the falling edge of *uTxEN* of node 24. — In case that hard wired signals as host interface are implemented: An error shall be signaled via the host interface of node 24 not earlier than 650 µs and not later than 2 600 µs + 100 µs after the falling edge of *uTxEN* of node 24. — In case that SPI as host interface is implemented: An error shall be signaled via the host interface of node 24 not earlier than 650 µs and not later than 2 600 µs + 200 µs after the falling edge of *uTxEN* of node 24. — In case of an available INH1 signal uINH1 of node 24 shall be in logical HIGH state during the test execution.

9.3.11 Power Supply.Undervoltage V_{BAT}

9.3.11.1 Undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_Normal* mode

Table 223 defines the test case for undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in BD_Normal mode.

Table 223 — Test case for undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_Normal* mode

Name	Undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_Normal* mode
Test purpose	This test checks the behaviour of the IUT under the fault condition of an undervoltage of V_{BAT} occurring in *BD_Normal* mode if V_{CC} is not implemented and no other stress condition is present according to ISO 17458-4. In case of an available V_{CC} supply input, see test case 9.3.7.2 and following and skip this test case. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is implemented — the Functional class “Bus driver internal voltage regulator” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. f) After the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. g) Trigger the scope to start the observation synchronously with the stimuli at

Name	Undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_Normal* mode
	TP_N24_TxEN of node 24. h) Wait until the end of the scope observation window, i.e. 5 µs.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

9.3.11.2 Undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_Standby* mode

Table 224 defines the test case for undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in BD_Standby mode.

Table 224 — Test case for undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_Standby* mode

Name	Undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_Standby* mode
Test purpose	This test checks the behaviour of the IUT under the fault condition of an undervoltage of V_{BAT} occurring in *BD_Standby* mode if V_{CC} is not implemented and no other stress condition is present according to ISO 17458-4. In case of an available V_{CC} supply input, see test case 9.3.7.7 and following and skip this test case. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is implemented — the Functional class “Bus driver internal voltage regulator” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standby preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) In case of an available V_{IO} input observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. f) After the undervoltage reaction time, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. g) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. h) Wait until the end of the scope observation window, i.e. 5 µs.

Name	**Undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_Standby* mode**
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented and a V_{IO} input is available: No error shall be signalled via the host interface of node 24 during the test execution signaling that no wakeup was received according ISO 17458-4. — In case that SPI as host interface is implemented and a V_{IO} input is available: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

9.3.11.3 Undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_ReceiveOnly* mode

Table 225 defines the test case for undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in BD_ReceiveOnly mode.

Table 225 — Test case for undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_ReceiveOnly* mode

Name	Undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_ReceiveOnly* mode
Test purpose	This test checks the behaviour of the IUT under the fault condition of an undervoltage of V_{BAT} occurring in *BD_ReceiveOnly* mode if V_{CC} is not implemented and no other stress condition is present according to ISO 17458-4. In case of an available V_{CC} supply input, see test case 9.3.7.3 and following and skip this test case. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is implemented — the Functional class “Bus driver internal voltage regulator” is not implemented — the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	ReceiveOnly preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. f) After the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. g) Trigger the scope to start the observation synchronously with the stimuli at

Name	**Undervoltage of V_{BAT}, V_{CC} = not implemented, occuring in *BD_ReceiveOnly* mode**
	TP_N24_TxEN of node 24. h) Wait until the end of the scope observation window, i.e. 5 µs.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

9.3.11.4 Undervoltage of V_{BAT}, occuring in *BD_Sleep* mode

Table 226 defines the test case for undervoltage of V_{BAT}, occuring in BD_Sleep mode.

Table 226 — Test case for undervoltage of V_{BAT}, occuring in *BD_Sleep* mode

Name	Undervoltage of V_{BAT}, occuring in *BD_Sleep* mode
Test purpose	This test checks the behaviour of the IUT under the fault condition of an undervoltage of V_{BAT} occurring in *BD_Sleep* mode if no other stress condition is present according to ISO 17458-4. This test case is skipped if neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Sleep preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) In case a V_{IO} or a V_{CC} input is implemented, observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. f) After the undervoltage is applied, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. g) Trigger the scope to start the observation synchronously with the stimuli at

Name	Undervoltage of V_{BAT}, occuring in *BD_Sleep* mode
	TP_N24_TxEN of node 24. h) Wait until the end of the scope observation window, i.e. 5 µs.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case a V_{IO} or a V_{CC} input is implemented and hard wired signals as host interface are implemented: No error shall be signalled via the host interface of node 24 during the test execution, i.e. no wakeup was received. — In case a V_{IO} or a V_{CC} input is implemented and SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

9.3.11.5 IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_Normal* mode

Table 227 defines the test case for IUT remains in BD_Sleep mode while undervoltage of V_{BAT} and host commands *BD_Normal* mode.

Table 227 — Test case for IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_Normal* mode

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_Normal* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Sleep* mode while undervoltage of V_{BAT} and the host commands a mode change to *BD_Normal* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — neither a V_{IO} reference voltage nor a V_{CC} power supply is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24.

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_Normal* mode**
	c) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. d) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. h) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. i) Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. j) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Wait 5,0 µs. l) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. m) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. n) Trigger the logic analyzer to start the observation synchronously with the stimulation at the host interface of node 24.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: An error shall be signaled via the host interface of node 24 latest 100 µs after the host command is applied. — In case that SPI as host interface is implemented: An error shall be signaled via the host interface of node 24 latest 200 µs after the host command is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 24 and node 23 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.11.6 IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_ReceiveOnly* mode

Table 228 defines the test case for IUT remains in BD_Sleep mode while undervoltage of V_{BAT} and host commands *BD_ReceiveOnly* mode.

Table 228 — Test case for IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_ReceiveOnly* mode

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_ReceiveOnly* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Sleep* mode while undervoltage of V_{BAT} and the host commands a mode change to *BD_ReceiveOnly* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented — neither a V_{IO} reference voltage nor a V_{CC} power supply is implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — External V_{BAT} power supply of the IUT in node 24: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	— In case that only V_{BAT} is implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — External V_{BAT} power supply of the IUT in node 24: default.
	— V_{IO} reference voltage (in case of an available V_{IO} input):
	V_{IO} reference voltage of all nodes: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— Sleep preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24.

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_ReceiveOnly* mode**
	b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. d) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. h) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. i) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. j) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Wait 5,0 µs. l) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. m) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. n) Trigger the logic analyzer to start the observation synchronously with the stimulation at the host interface of node 24.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 100 µs after the host command is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 200 µs after the host command is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 24 and node 23 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.11.7 IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_Standby* mode

Table 229 defines the test case for IUT remains in BD_Sleep mode while undervoltage of V_{BAT} and host commands *BD_Standby* mode.

Table 229 — Test case for IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_Standby* mode

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_Standby* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Sleep* mode while undervoltage of V_{BAT} and the host commands a mode change to *BD_Standby* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — neither a V_{IO} reference voltage nor a V_{CC} power supply is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23.

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{BAT} and host commands *BD_Standby* mode**
	d) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. h) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. i) Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. j) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Wait 5,0 µs. l) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. m) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. n) Trigger the logic analyzer to start the observation synchronously with the stimulation at the host interface of node 24.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: No error shall be signalled via the host interface of node 24 100 µs after the host command is applied, i.e. no wakeup was received. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 200 µs after the host command is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 24 and node 23 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.11.8 IUT remains in *BD_Standby* while undervoltage V_{BAT} and host commands *BD_Normal* (*BD_Sleep* not implemented)

Table 230 defines the test case for IUT remains in BD_Standby while undervoltage V_{BAT} and host commands *BD_Normal* (*BD_Sleep* not implemented).

Table 230 — Test case for IUT remains in *BD_Standby* while undervoltage V_{BAT} and host commands *BD_Normal* (*BD_Sleep* not implemented)

Name	**IUT remains in *BD_Standby* while undervoltage V_{BAT} and host commands *BD_Normal* (*BD_Sleep* not implemented)**
Test purpose	This test checks the ability of the IUT to remain in *BD_Standby* mode due to an undervoltage of V_{BAT} and to ignore the host command to change to *BD_Normal* mode because undervoltage conditions overrule the host command while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver internal voltage regulator” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— Standby preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window

Name	**IUT remains in *BD_Standby* while undervoltage V_{BAT} and host commands *BD_Normal* (*BD_Sleep* not implemented)**
	described in 9.1.4.2. h) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. i) Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. j) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Wait 5,0 µs. l) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. m) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. n) Trigger the logic analyzer to start the observation synchronously with the stimulation at the host interface of node 24.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: An error shall be signalled via the host interface of node 24 latest 100 µs after the host command is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 200 µs after the host command is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 24 and node 23 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.11.9 IUT remains in *BD_Standby* while undervoltage V_{BAT} and host commands *BD_ReceiveOnly*

Table 231 defines the test case for IUT remains in BD_Standby while undervoltage V_{BAT} and host commands *BD_ReceiveOnly*.

Table 231 — Test case for IUT remains in *BD_Standby* while undervoltage V_{BAT} and host commands *BD_ReceiveOnly*

Name	**IUT remains in *BD_Standby* while undervoltage V_{BAT} and host commands *BD_ReceiveOnly***
Test purpose	This test checks the ability of the IUT to remain in *BD_Standby* mode due to an undervoltage of V_{BAT} and to ignore the host command to change to *BD_ReceiveOnly* mode because undervoltage conditions overrule the host command while no stress condition is present. This test case is skipped if — either the Functional class “Bus driver voltage regulator control” or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver internal voltage regulator” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the *BD_ReceiveOnly* is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V — Failure: none. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— Standby preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. d) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window

Name	IUT remains in *BD_Standby* while undervoltage V_{BAT} and host commands *BD_ReceiveOnly*
	described in 9.1.4.2. h) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24. i) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. j) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Wait 5,0 µs. l) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. m) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. n) Trigger the logic analyzer to start the observation synchronously with the stimulation at the host interface of node 24.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: An error shall be signalled via the host interface of node 24 latest 100 µs after the host command is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 200 µs after the host command is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 24 and node 23 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.11.10 Reset SPI interrupt line after undervoltage of V_{BAT}

Table 232 defines the test case for reset SPI interrupt line after undervoltage of V_{BAT}.

Table 232 — Test case for reset SPI interrupt line after undervoltage of V_{BAT}

Name	Reset SPI interrupt line after undervoltage of V_{BAT}
Test purpose	This test checks the behaviour of the IUT when the SPI interrupt line is been reset due to host command according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver internal voltage regulator” is implemented and the Functional class “Bus driver logic level adaptation” is not implemented; i.e. if V_{CC} is not implemented then V_{IO} shall be implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of the IUT in node 24: default. — V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standby preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uINTN* at *TP_N24_INTN* of node 24. b) Observe and acquire *uSCSN* at *TP_N24_SCSN* of node 24 c) Set the external V_{BAT} power supply of the IUT in node 24 to the default implementation

Name	Reset SPI interrupt line after undervoltage of V_{BAT}
	value. d) After at least 10 ms reset the SPI interrupt line of the IUT in node 24 via *uSCSN* at *TP_N24_SCSN* of node 24. e) Trigger the logic analyzer to start the observation synchronously with the stimuli at the host interface of node 24, i.e. with the first falling edge of *uSCSN* signal at *TP_N24_SCSN* of node 24.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. *uINTN* at *TP_N24_INTN* of node 24 shall be in logical LOW state initially. Latest 100 us after *uSCSN* at *TP_N24_SCSN* of node 24 returns to high *uINTN* at *TP_N24_INTN* of node 24 shall change to logical HIGH state.

9.3.12 Power Supply.Undervoltage V_{CC}

9.3.12.1 Undervoltage of V_{CC}, V_{BAT} not implemented, occuring in *BD_Normal* mode

Table 233 defines the test case for undervoltage of V_{CC}, V_{BAT} not implemented, occuring in BD_Normal mode.

Table 233 — Test case for undervoltage of V_{CC}, V_{BAT} not implemented, occuring in *BD_Normal* mode

Name	Undervoltage of V_{CC}, V_{BAT} not implemented, occuring in *BD_Normal* mode
Test purpose	This test checks the behaviour of the IUT under the fault condition of an undervoltage of V_{CC} occurring in *BD_Normal* mode if V_{BAT} is not implemented and no other stress condition is present according to ISO 17458-4. In case of an available V_{BAT} supply input, see test case 9.3.5.10 and following and skip this test case. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver voltage regulator control” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} supply input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. f) After the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. g) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. h) Wait until the end of the scope observation window, i.e. 5 µs.

Name	**Undervoltage of V_{CC}, V_{BAT} not implemented, occuring in *BD_Normal* mode**
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{BAT} voltage at the IUTs supply input has dropped to $V_{BATUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface and V_{IO} is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

9.3.12.2 Undervoltage of V_{CC}, V_{BAT} = not implemented, occuring in *BD_Standby* mode

Table 234 defines the test case for undervoltage of V_{CC}, V_{BAT} = not implemented, occuring in BD_Standby mode.

Table 234 — Test case for undervoltage of V_{CC}, V_{BAT} = not implemented, occuring in *BD_Standby* mode

Name	Undervoltage of V_{CC}, V_{BAT} = not implemented, occuring in *BD_Standby* mode
Test purpose	This test checks the behaviour of the IUT under the fault condition of an undervoltage of V_{CC} occurring in *BD_Standby* mode if V_{BAT} is not implemented and no other stress condition is present according to ISO 17458-4. In case of an available V_{BAT} supply input, see test case 9.3.5.13 and following and skip this test case. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver voltage regulator control” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} supply input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Standby preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) In case that V_{IO} is implemented observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. f) Wait 1 000 ms. g) After the undervoltage reaction time, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window, i.e. 5 µs.

Name	**Undervoltage of V_{CC}, V_{BAT} = not implemented, occuring in *BD_Standby* mode**
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that V_{IO} is implemented: — In case that hard wired signals as host interface are implemented: No error shall be signalled via the host interface of node 24 during the test execution signaling that no wakeup was received according ISO 17458-4. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

9.3.12.3 Undervoltage of V_{CC}, V_{BAT} = not implemented, occuring in *BD_ReceiveOnly* mode

Table 235 defines the test case for undervoltage of V_{CC}, V_{BAT} = not implemented, occuring in BD_ReceiveOnly mode.

Table 235 — Test case for undervoltage of V_{CC}, V_{BAT} = not implemented, occuring in *BD_ReceiveOnly* mode

Name	Undervoltage of V_{CC}, V_{BAT} = not implemented, occuring in *BD_ReceiveOnly* mode
Test purpose	This test checks the behaviour of the IUT under the fault condition of an undervoltage of V_{CC} occurring in *BD_ReceiveOnly* mode if V_{BAT} is not implemented and no other stress condition is present according to ISO 17458-4. In case of an available V_{BAT} supply input, see test case 9.3.5.11 and following and skip this test case. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver voltage regulator control” is implemented — the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	ReceiveOnly preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. f) After the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. g) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24.

Name	**Undervoltage of V_{CC}, V_{BAT} = not implemented, occuring in *BD_ReceiveOnly* mode**
	h) Wait until the end of the scope observation window, i.e. 5 µs.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{CC} voltage at the IUTs supply input has dropped to $V_{CCUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface and V_{IO} is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

9.3.12.4 IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_Normal* mode

Table 236 defines the test case for IUT remains in BD_Sleep mode while undervoltage of V_{CC} and host commands *BD_Normal* mode.

Table 236 — Test case for IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_Normal* mode

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_Normal* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Sleep* mode while undervoltage of V_{CC} and the host commands a mode change to *BD_Normal* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. e) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. f) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_Normal* mode**
	TP_N24_INTN) of node 24. i) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. j) Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. k) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Wait 5,0 µs. m) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. n) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. o) Trigger the logic analyzer to start the observation synchronously with the stimulation at the host interface of node 24.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the test execution. — An error shall be signaled via the host interface of node 24 during the test execution. — *uBus* at TP4_N23 of node 23 shall stay within Idle range during the observation window, beginning with the falling edge of uTxEN of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution.

9.3.12.5 IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode

Table 237 defines the test case for IUT remains in BD_Sleep mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode.

Table 237 — Test case for IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Sleep* mode while undervoltage of V_{CC} and the host commands a mode change to *BD_ReceiveOnly* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is implemented — the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. e) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. f) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode**
	node 24. h) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. i) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. j) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. k) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Wait 5,0 µs. m) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. n) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. o) Trigger the logic analyzer to start the observation synchronously with the stimulation at the host interface of node 24.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the test execution. — An error shall be signaled via the host interface of node 24 during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within Idle range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution.

9.3.12.6 IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_Standby* mode

Table 238 defines the test case for IUT remains in BD_Sleep mode while undervoltage of V_{CC} and host commands *BD_Standby* mode.

Table 238 — Test case for IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_Standby* mode

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_Standby* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Sleep* mode while undervoltage of V_{CC} and the host commands a mode change to *BD_Standby* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. e) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24.

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{CC} and host commands *BD_Standby* mode**
	h) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. i) Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. j) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. k) Wait 5,0 µs. l) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. m) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. n) Trigger the logic analyzer to start the observation synchronously with the stimulation at the host interface of node 24.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall be in logical LOW state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state during the test execution. — An error shall be signaled via the host interface of node 24 during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within Idle range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — uINH1 of node 24 shall be in logical LOW state (Sleep) during the test execution.

9.3.12.7 IUT remains in *BD_Standby* mode while undervoltage of V_{CC} and host commands *BD_Normal* mode

Table 239 defines the test case for IUT remains in BD_Standby mode while undervoltage of V_{CC} and host commands *BD_Normal* mode.

Table 239 — Test case for IUT remains in *BD_Standby* mode while undervoltage of V_{CC} and host commands *BD_Normal* mode

Name	**IUT remains in *BD_Standby* mode while undervoltage of V_{CC} and host commands *BD_Normal* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Standby* mode while undervoltage of V_{CC} and the host commands a mode change to *BD_Normal* if no other stress condition is present according to table ISO 17458-4. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — In case that only V_{CC} is implemented: — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24.

Name	**IUT remains in *BD_Standby* mode while undervoltage of V_{CC} and host commands *BD_Normal* mode**
	d) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. h) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. i) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. j) Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. k) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. l) Wait 5,0 µs. m) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. n) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. o) Trigger the logic analyzer to start the observation synchronously with the stimulation at the host interface of node 24.

Name	**IUT remains in *BD_Standby* mode while undervoltage of V_{CC} and host commands *BD_Normal* mode**
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal uINH1 of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — *uRxD* of node 24 and node 23 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 100 µs after the host command is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 200 µs after the host command is applied. — *uBus* at TP4_N23 of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30mV ($uBDTx_{idle}$).

9.3.12.8 IUT remains in *BD_Standby* mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode

Table 240 defines the test case for IUT remains in BD_Standby mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode.

Table 240 — Test case for IUT remains in *BD_Standby* mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode

Name	**IUT remains in *BD_Standby* mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Standby* mode while undervoltage of V_{CC} and the host commands a mode change to *BD_ReceiveOnly* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — In case that only V_{CC} is implemented: — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of the IUT in node 24: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of

Name	IUT remains in *BD_Standby* mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode
	node 24. d) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. e) In case of an available V_{IO} input: f) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. h) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. i) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. j) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. k) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. l) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High pattern. m) Wait 5,0 µs. n) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by two 50/50 patterns. o) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. p) Trigger the logic analyzer to start the observation synchronously with the stimulation at the host interface of node 24.

Name	**IUT remains in *BD_Standby* mode while undervoltage of V_{CC} and host commands *BD_ReceiveOnly* mode**
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case of an available V_{IO} input: — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — *uRxD* of node 24 and node 23 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 100 µs after the host command is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 200 µs after the host command is applied. — In case that a V_{IO} input is not available: In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*) during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$).

9.3.13 Power Supply.Undervoltage V_{IO}

9.3.13.1 Undervoltage of V_{IO} occuring in *BD_Sleep* mode

Table 241 defines the test case for undervoltage of V_{IO} occuring in BD_Sleep mode.

Table 241 — Test case for undervoltage of V_{IO} occuring in *BD_Sleep* mode

Name	Undervoltage of V_{IO} occuring in *BD_Sleep* mode
Test purpose	This test checks the behaviour of the IUT under the fault condition of an undervoltage of V_{IO} occurring in *BD_Sleep* mode if no other stress condition is present according to ISO 17458-4. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	Sleep preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. g) After the falling edge of the error signal of node 24, stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 10Bit High

Name	Undervoltage of V_{IO} occuring in *BD_Sleep* mode
	pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24.
Postamble	Standard postamble.
Pass criteria	Undervoltage detection timeout measurement requires a trigger event when V_{IO} voltage at the IUTs supply input has dropped to $V_{IOUndervoltage}$. Adaptation of the thresholds for digital signals may be required. — In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 100 µs after the undervoltage is applied. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 1 000 ms + 200 µs after the undervoltage is applied. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution.

9.3.13.2 IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_Normal* mode

Table 242 defines the test case for IUT remains in BD_Sleep mode while undervoltage of V_{IO} and host commands *BD_Normal* mode.

Table 242 — Test case for IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_Normal* mode

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_Normal* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Sleep* mode while undervoltage of V_{IO} and the host commands a mode change to *BD_Normal* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage: — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_Normal* mode**
	TP_N24_INTN) of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. g) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window, i.e. 5 µs.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — An error shall be signalled via the host interface of node 24 during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution.

9.3.13.3 IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_ReceiveOnly* mode

Table 243 defines the test case for IUT remains in BD_Sleep mode while undervoltage of V_{IO} and host commands *BD_ReceiveOnly* mode.

Table 243 — Test case for IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_ReceiveOnly* mode

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_ReceiveOnly* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Sleep* mode while undervoltage of V_{IO} and the host commands a mode change to *BD_ReceiveOnly* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage: — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$ — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24.

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_ReceiveOnly* mode**
	d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. g) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window, i.e. 5 µs.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — An error shall be signalled via the host interface of node 24 during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution.

9.3.13.4 IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_Standby* mode

Table 244 defines the test case for IUT remains in BD_Sleep mode while undervoltage of V_{IO} and host commands *BD_Standby* mode.

Table 244 — Test case for IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_Standby* mode

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_Standby* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Sleep* mode while undervoltage of V_{IO} and the host commands a mode change to *BD_Standby* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage: — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$ — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	**IUT remains in *BD_Sleep* mode while undervoltage of V_{IO} and host commands *BD_Standby* mode**
	TP_N24_INTN) of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Stimulate the IUT in node 24 via the host interface to enter *BD_Standby*. g) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window, i.e. 5 µs.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — An error shall be signalled via the host interface of node 24 during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution.

9.3.13.5 IUT remains in *BD_Standby* mode while undervoltage of V_{IO} and host commands *BD_Normal* mode

Table 245 defines the test case for IUT remains in BD_Standby mode while undervoltage of V_{IO} and host commands *BD_Normal* mode.

Table 245 — Test case for IUT remains in *BD_Standby* mode while undervoltage of V_{IO} and host commands *BD_Normal* mode

Name	**IUT remains in *BD_Standby* mode while undervoltage of V_{IO} and host commands *BD_Normal* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Standby* mode while undervoltage of V_{IO} and the host commands a mode change to *BD_Normal* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — either the Functional class “Bus driver voltage regulator control” or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} is both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or

Name	**IUT remains in *BD_Standby* mode while undervoltage of V_{IO} and host commands *BD_Normal* mode**
	TP_N24_INTN) of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. g) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window, i.e. 5 µs.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — An error shall be signalled via the host interface of node 24 during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) during the test execution.

9.3.13.6 IUT remains in *BD_Standby* mode while undervoltage of V_{IO} and host commands *BD_ReceiveOnly* mode

Table 246 defines the test case for IUT remains in BD_Standby mode while undervoltage of V_{IO} and host commands *BD_ReceiveOnly* mode.

Table 246 — Test case for IUT remains in *BD_Standby* mode while undervoltage of V_{IO} and host commands *BD_ReceiveOnly* mode

Name	**IUT remains in *BD_Standby* mode while undervoltage of V_{IO} and host commands *BD_ReceiveOnly* mode**
Test purpose	This test checks the behaviour of the IUT to remain in *BD_Standby* mode while undervoltage of V_{IO} and the host commands a mode change to *BD_ReceiveOnly* if no other stress condition is present according to ISO 17458-4. This test case is skipped if — either the Functional class “Bus driver voltage regulator control” or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} is both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V — Failure: none. — Communication: node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24.

Name	**IUT remains in *BD_Standby* mode while undervoltage of V_{IO} and host commands *BD_ReceiveOnly* mode**
	d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) Stimulate the IUT in node 24 via the host interface to enter *BD_ReceiveOnly*. g) After 100 µs stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N24_TxEN* of node 24. i) Wait until the end of the scope observation window, i.e. 5 µs.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — An error shall be signalled via the host interface of node 24 during the test execution. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, beginning with the falling edge of *uTxEN* of node 24. The absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uINH1* of node 24 shall be in logical LOW state (Sleep) during the test execution.

9.3.14 Dynamic Low Battery Voltage

9.3.14.1 Dynamic low battery occuring in *BD_Normal* mode

Table 247 defines the test case for dynamic low battery occuring in BD_Normal mode.

Table 247 — Test case for dynamic low battery occuring in *BD_Normal* mode

Name	Dynamic low battery occuring in *BD_Normal* mode
Test purpose	This test checks the behaviour of the IUT after a dynamic low battery voltage pulse according to 7.4 occuring in *BD_Normal* mode. This test case is skipped if the Functional class “Bus driver voltage regulator control” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: 11,6 V. — V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test). — Test signal: U_S/t_{r1} as specified in 7.4.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Stimulate the IUTs of transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low battery voltage pulse. The bit duration in this test case shall be *gdBit*=25 µs, because the memory depth of the logic analyzer is much too small to acquire 10 seconds with a 100 ns bit time. The gap between the messages in matrix A shall be 9,25 ms. g) After the first communication round trigger the dynamic low battery pulse.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall contain all 50/50 patterns transmitted by all nodes (according to *uTxD* and

Name	Dynamic low battery occuring in *BD_Normal* mode
	uTxEN of all nodes), i.e. all data shall be transmitted and received by the IUTs in all nodes. — *uINH1* of all nodes shall be in logical HIGH state during the test execution.

9.3.14.2 Dynamic low battery occuring in *BD_Standby* mode

Table 248 defines the test case for dynamic low battery occuring in BD_Standby mode.

Table 248 — Test case for dynamic low battery occuring in *BD_Standby* mode

Name	Dynamic low battery occuring in *BD_Standby* mode
Test purpose	This test checks the behaviour of the IUT after a dynamic low battery voltage pulse according to 7.4 occuring in *BD_Standby* mode. This test case is skipped if the Functional class “Bus driver voltage regulator control” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: 11,6 V. — V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A. — Test signal: U_S/t_{r1} as specified in 7.4.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Stimulate the IUTs of transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low battery voltage pulse. The bit duration in this test case shall be *gdBit* = 25 µs, because the memory depth of the logic analyzer is much too small to acquire 10 seconds with a 100 ns bit time. The gap between the messages in matrix A shall be 9,25 ms. g) After the first communication round trigger the dynamic low battery pulse.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall not contain any pattern of any other node, i.e. nothing is transmitted by the IUTs of all nodes except node 24.

Name	Dynamic low battery occuring in *BD_Standby* mode
	— *uRxD* of all nodes except node 24 shall not contain any pattern of node 24, i.e. the IUTs in all nodes except node 24 shall not receive any data. — *uRxD* of node 24 shall contain the pattern sent by himself, i.e. node 24 is able to receive its own transmission via the loopback interface. — *uINH1* of all nodes shall be in logical HIGH during the test execution.

9.3.14.3 Dynamic low battery occuring in *BD_Sleep* mode

Table 249 defines the test case for dynamic low battery occuring in BD_Sleep mode.

Table 249 — Test case for dynamic low battery occuring in *BD_Sleep* mode

Name	Dynamic low battery occuring in *BD_Sleep* mode
Test purpose	This test checks the behaviour of the IUT after a dynamic low battery voltage pulse according to 7.4 occuring in *BD_Sleep* mode. This test case is skipped if the Functional class "Bus driver voltage regulator control" is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: 11,6 V. — V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A. — Test signal: U_S/t_{r1} as specified in 7.4.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. The observation shall start 100 µs (*dBDModeChange*) after the host command is applied.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes except node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Stimulate the IUTs of transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low battery voltage pulse. The bit duration in this test case shall be *gdBit* = 25 µs, because the memory depth of the logic analyzer is much too small to acquire 10 seconds with a 100 ns bit time. The gap between the messages in matrix A shall be 9,25 ms. g) After the first communication round trigger the dynamic low battery pulse.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of node 24 shall not contain any pattern of any other node, i.e. nothing is transmitted by the

Name	Dynamic low battery occuring in *BD_Sleep* mode
	IUTs of all nodes except node 24. — *uRxD* of all nodes except node 24 shall not contain any pattern of node 24, i.e. the IUTs in all nodes except node 24 shall not receive any data. — *uRxD* of node 24 shall contain the pattern sent by himself, i.e. node 24 is able to receive its own transmission via the loopback interface. — *uINH1* of all nodes except node 24 shall be in logical LOW state during the test execution.

9.3.14.4 Dynamic low battery occuring in *BD_ReceiveOnly* mode

Table 250 defines the test case for dynamic low battery occuring in BD_ReceiveOnly mode.

Table 250 — Test case for dynamic low battery occuring in *BD_ReceiveOnly* mode

Name	Dynamic low battery occuring in *BD_ReceiveOnly* mode
Test purpose	This test checks the behaviour of the IUT after a dynamic low battery voltage pulse according to 7.4 occuring in *BD_ReceiveOnly* mode. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the *BD_ReceiveOnly* mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: 11,6 V. — V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A. — Test signal: U_S/t_{r1} as specified in 7.4.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 24 via the host interface to enter *BD_Normal*. The observation shall start 100 µs (*dBDModeChange*) after the host command is applied.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Stimulate the IUTs of transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low battery voltage pulse. The bit duration in this test case shall be *gdBit* = 25 µs, because the memory depth of the logic analyzer is much too small to acquire 10 seconds with a 100 ns bit time. The gap between the messages in matrix A shall be 9,25 ms. g) After the first communication round trigger the dynamic low battery pulse.

Name	**Dynamic low battery occuring in *BD_ReceiveOnly* mode**
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall contain the 50/50 patterns transmitted by node 24 (according to *uTxD* and *uTxEN* of node 24), i.e. all data transmitted shall be received by the IUTs in *BD_ReceiveOnly* mode. — *uRxD* of node 24 shall not contain any pattern of any other node, i.e. nothing is transmitted by the IUTs of all nodes except node 24. — *uINH1* of all nodes shall be in logical HIGH state during the test execution.

9.3.15 Communication.Truncation

9.3.15.1 Path truncation

Table 251 defines the test case for path truncation.

Table 251 — Test case for path truncation

Name	Path truncation
Test purpose	This test checks the overall channel truncation if no stress condition is present according to the sum of all allowed truncation effects specified in ISO 17458-4. This test shall verify, that only the transmission start sequence is affected by truncation effects and that a protocol controller would decode the following data properly.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test).
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Stimulate the IUT in the first transmitting node according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. e) Stimulate the IUTs in transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	NOTE The maximum allowed truncation depends on the presence or not of the active star in the path between transmitter and receiver. The width of all received TSS patterns (logical LOW phase from the falling edge of the received TSS pattern to the rising edge of the first bit of the following 10/90 pattern) in *uRxD* of all nodes shall be as follow: — If the active star is present in the path between transmitter and receiver, the received TSS pattern

Name	Path truncation
	should be at least 250 ns, i.e. the channel truncation shall be within the allowed range. — If the active star is not present in the path between transmitter and receiver, the received TSS pattern should be at least 700 ns, i.e. the channel truncation shall be within the allowed range.

Table 252 defines the test instances for path truncation test case defined in Table 251.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 252 — Test instances for path truncation

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.16 Failure.Short-circuit Bus Wires

9.3.16.1 Short-circuit bus wires to GND

Table 253 defines the test case for short-circuit bus wires to GND.

Table 253 — Test case for short-circuit bus wires to GND

Name	Short-circuit bus wires to GND
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit of the bus wire to GND. Additionally it is checked that the IUT is not permanently damaged by the short-circuit.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case of an available V_{IO} input: V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to GND. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Short-circuit BP (failure FL11) of node 24 to GND at *TP2_N24*.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. e) Observe and acquire $iBP_{GNDShortMax}$ at $TP\_N24\_R_{iBP}$ of node 24 (shall be at *TP1_N24*). f) Stimulate the IUT of node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by a short-circuit current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples where taken by the data acquisition unit. g) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at node 24. Acquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*.

Name	Short-circuit bus wires to GND
	h) Switch off short-circuit BP (failure FL11) of node 24. Wait at least 12 seconds. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— $\lvert iBP_{GNDShortMax} \rvert \leq 60$ mA. — The IUT of node 24 shall signal an error to the host after detecting the failure. — After switching off the failure: — *uRxD* of the IUT in node 24 shall receive the patterns that are stimulated at *TP_N23_TxD* and *TP_N23_TxEN* of node 23 and signal them at *TP_N24_RxD* accordingly. — *uRxD* of the IUT in node 23 shall receive the patterns that are stimulated at *TP_N24_TxD* and *TP_N24_TxEN* of node 24 and signal them at *TP_N23_RxD* accordingly. — In case of an available RxEN signal *uRxEN* at *TP_N24_RxEN* of the IUT in node 24 shall be in logical LOW state while receiving the patterns that are stimulated at *TP_N23_TxD* and *TP_N23_TxEN* of node 23. — In case of an available RxEN signal *uRxEN* at *TP_N23_RxEN* of the IUT in node 23 shall be in logical LOW state while receiving the patterns that are stimulated at *TP_N24_TxD* and *TP_N24_TxEN* of node 24.

Table 254 defines the test instances for short-circuit bus wires to GND test case defined in Table 253.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 254 — Test instances for short-circuit bus wires to GND

Instance		**1**	**2**
Purpose	**Stress**	S/C BP to GND at node 24	S/C BM to GND at node 24
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to GND	S/C BM to GND
Preamble		Standard Short-circuit BP (failure FL11) of node 24 to GND at *TP2_N24*.	Standard Short-circuit BM (failure FL12) of node 24 to GND at *TP2_N24.*
Test execution		… Observe and acquire $iBP_{GNDShortMax}$ at $TP\_N24\_R_{iBP}$ of node 24 (shall be at *TP1_N24*). … Switch off short-circuit BP (failure FL11) of node 24. Wait at least 12 seconds. …	… Observe and acquire $iBM_{GNDShortMax}$ at $TP\_N24\_R_{iBM}$ of node 24 (shall be at *TP1_N24*). … Switch off short-circuit BM (failure FL12) of node 24. Wait at least 12 seconds. …
Pass criteria		$\lvert iBP_{GNDShortMax} \rvert \leq 60$ mA. …	$\lvert iBM_{GNDShortMax} \rvert \leq 60$ mA. …

9.3.16.2 Short-circuit bus wires to V_{BAT}

Table 255 defines the test case for short-circuit bus wires to V_{BAT}.

Table 255 — Test case for short-circuit bus wires to V_{BAT}

Name	Short-circuit bus wires to V_{BAT}
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit of the bus wire to +48 V[25]. Additionally it is checked that the IUT is not permanently damaged by the short-circuit.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case of an available V_{IO} input: V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to +48 V[25]. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Short-circuit BP (failure FL13) of node 24 to +48 V[25] at *TP2_N24*.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. e) Observe and acquire $iBP_{BAT48ShortMax}$[26] or $iBP_{BAT27ShortMax}$[27] at $TP\_N24\_R_{iBP}$ of node 24 (shall be at *TP1_N24*). f) Stimulate the IUT of node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by a short-circuit current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples where taken by the data acquisition unit. g) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at

Name	Short-circuit bus wires to V_{BAT}
	node 24. Acquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*. h) Switch off short-circuit BP (failure FL13) of node 24. Wait at least 12 seconds. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— In case the IUT does not support 42 V systems: $\lvert iBP_{BAT27ShortMax}\rvert \leq 60$ mA. — In case the IUT does support 42 V systems: $\lvert iBP_{BAT48ShortMax}\rvert \leq 72$ mA. — The IUT of node 24 shall signal an error to the host after detecting the failure. — After switching off the failure: — *uRxD* of the IUT in node 24 shall receive the patterns that are stimulated at *TP_N23_TxD* and *TP_N23_TxEN* of node 23 and signal them at *TP_N24_RxD* accordingly. — *uRxD* of the IUT in node 23 shall receive the patterns that are stimulated at *TP_N24_TxD* and *TP_N24_TxEN* of node 24 and signal them at *TP_N23_RxD* accordingly. — In case of an available RxEN signal *uRxEN* at *TP_N24_RxEN* of the IUT in node 24 shall be in logical LOW state while receiving the patterns that are stimulated at *TP_N23_TxD* and *TP_N23_TxEN* of node 23. — In case of an available RxEN signal *uRxEN* at *TP_N23_RxEN* of the IUT in node 23 shall be in logical LOW state while receiving the patterns that are stimulated at *TP_N24_TxD* and *TP_N24_TxEN* of node 24.

Table 256 defines the test instances for short-circuit bus wires to V_{BAT} test case defind in Table 255.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 256 — Test instances for short-circuit bus wires to V_{BAT}

Instance		**1**	**2**
Purpose	**Stress**	S/C BP to V_{BAT} at node 24	S/C BM to V_{BAT} at node 24
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to +48 V [a]	S/C BM to +48 V [a]
Preamble		Standard. Short-circuit BP (failure FL13) of node 24 to +48 V [a] at *TP2_N24*.	Standard. Short-circuit BM (failure FL14) of node 24 to +48 V [a] at *TP2_N24*
Test execution		… Observe and acquire $iBP_{BAT48ShortMax}$ [b] or $iBP_{BAT27ShortMax}$ [c] at $TP\_N24\_R_{iBP}$ of node 24 (shall be at *TP1_N24*). … Switch off short-circuit BP (failure FL13) of node 24. Wait at least 12 seconds. …	… Observe and acquire $iBM_{BAT48ShortMax}$ [b] or $iBM_{BAT27ShortMax}$ [c] at $TP\_N24\_R_{iBM}$ of node 24 (shall be at *TP1_N24*). … Switch off short-circuit BM (failure FL14) of node 24. Wait at least 12 seconds …
Pass criteria		In case the IUT does not support 42 V systems: $\lvert iBP_{BAT27ShortMax}\rvert \leq 60$ mA. In case the IUT does support 42 V systems: $\lvert iBP_{BAT48ShortMax}\rvert \leq 72$ mA. …	In case the IUT does not support 42 V systems: $\lvert iBM_{BAT27ShortMax}\rvert \leq 60$ mA. In case the IUT does support 42 V systems: $\lvert iBM_{BAT48ShortMax}\rvert \leq 72$ mA. …

[a] In case the IUT does not support 42 V systems the V_{BAT} shall be +27 V

[b] In case the IUT does support 42 V systems

[c] In case the IUT does not support 42 V systems

9.3.16.3 Short-circuit bus wires to -5 V

Table 257 defines the test case for short-circuit bus wires to -5 V.

Table 257 — Test case for short-circuit bus wires to -5 V

Name	Short-circuit bus wires to -5 V
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit of the bus wire to -5 V. Additionally it is checked that the IUT is not permanently damaged by the short-circuit.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case of an available V_{IO} input: V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to -5 V. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Short-circuit BP (failure FL19) of node 24 to -5 V at *TP2_N24*.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. e) Observe and acquire $iBP_{-5VshortMax}$ at $TP\_N24\_R_{iBP}$ of node 24 (shall be at *TP1_N24*). f) Stimulate the IUT of node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by a short-circuit current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples where taken by the data acquisition unit. g) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at node 24. Acquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*. h) Switch off short-circuit BP (failure FL19) of node 24. Wait at least 12 seconds.

Name	Short-circuit bus wires to -5 V
	i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— $\|iBP_{-5VshortMax}\| \leq 60$ mA. — The IUT of node 24 shall signal an error to the host after detecting the failure. — After switching off the failure: — *uRxD* of the IUT in node 24 shall receive the patterns that are stimulated at *TP_N23_TxD* and *TP_N23_TxEN* of node 23 and signal them at *TP_N24_RxD* accordingly. — *uRxD* of the IUT in node 23 shall receive the patterns that are stimulated at *TP_N24_TxD* and *TP_N24_TxEN* of node 24 and signal them at *TP_N23_RxD* accordingly. — In case of an available RxEN signal *uRxEN* at *TP_N24_RxEN* of the IUT in node 24 shall be in logical LOW state while receiving the patterns that are stimulated at *TP_N23_TxD* and *TP_N23_TxEN* of node 23. — In case of an available RxEN signal *uRxEN* at *TP_N23_RxEN* of the IUT in node 23 shall be in logical LOW state while receiving the patterns that are stimulated at *TP_N24_TxD* and *TP_N24_TxEN* of node 24.

Table 258 defines the test instances for short-circuit bus wires to -5 V test case defined in Table 257.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 258 — Test instances for short-circuit bus wires to -5 V

Instance		**1**	**2**
Purpose	**Stress**	S/C BP to -5 V at node 24	S/C BM to -5 V at node 24
	Test description	—	—
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to -5 V	S/C BM to -5 V
Preamble		Standard. Short-circuit BP (failure FL19) of node 24 to -5 V at *TP2_N24*.	Standard. Short-circuit BM (failure FL20) of node 24 to -5 V at *TP2_N24*
Test execution		… Observe and acquire $iBP_{-5VshortMax}$ at $TP\_N24\_R_{iBP}$ of node 24 (shall be at *TP1_N24*). … Switch off short-circuit BP (failure FL19) of node 24. Wait at least 12 seconds. …	… Observe and acquire $iBM_{-5VshortMax}$ at $TP\_N24\_R_{iBM}$ of node 24 (shall be at *TP1_N24*). … Switch off short-circuit BM (failure FL20) of node 24. Wait at least 12 seconds …
Pass criteria		$\lvert iBP_{-5VshortMax} \rvert \leq 60$ mA. …	$\lvert iBM_{-5VshortMax} \rvert \leq 60$ mA. …

9.3.16.4 S/C BP to BM at node

Table 259 defines the test case for S/C BP to BM at node.

Table 259 — Test case for S/C BP to BM at node

Name	S/C BP to BM at node
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit between both bus wires. Additionally it is checked that the IUT is not permanently damaged by the short-circuit.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case of an available V_{IO} input: V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to BM. — Communication: Node 24 and node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Short-circuit BP to BM (failure FL21) of node 24 at *TP2_N24*.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. e) Observe and acquire $iBM_{BPShortMax}$ at $TP\_N24\_R_{iBM}$ of node 24 (shall be at *TP1_N24*). f) Stimulate the IUT of node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by a short-circuit current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples where taken by the data acquisition unit. g) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at node 24. Acquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*.

Name	S/C BP to BM at node
	h) Switch off short-circuit BP to BM (failure FL21) of node 24. Wait at least 12 seconds. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— $\|iBM_{BPShortMax}\| \leq 60$ mA. — The IUT of node 24 shall signal an error to the host after detecting the failure. — After switching off the failure: — *uRxD* of the IUT in node 24 shall receive the patterns and signal at *TP_N24_RxD* and *TP_N24_RxEN* that are stimulated at *TP_N23_TxD* and *TP_N23_TxEN* of node 23. — *uRxD* of the IUT in node 23 shall receive the patterns and signal at *TP_N23_RxD* and *TP_N23_RxEN* that are stimulated at *TP_N24_TxD* and *TP_N24_TxEN* of node 24. — In case of an available RxEN signal *uRxEN* of the IUT in node 24 shall receive the patterns and signal them at *TP_N24_RxD* and *TP_N24_RxEN* that are stimulated at *TP_N23_TxD* and *TP_N23_TxEN* of node 23. — In case of an available RxEN signal *uRxEN* of the IUT in node 23 shall receive the patterns and signal them at *TP_N23_RxD* and *TP_N23_RxEN* that are stimulated at *TP_N24_TxD* and *TP_N24_TxEN* of node 24.

9.3.16.5 S/C BP to BM at node with data frame

Table 260 defines the test case for S/C BP to BM at node with data frame.

Table 260 — Test case for S/C BP to BM at node with data frame

Name	S/C BP to BM at node with data frame
Test purpose	This test checks the ability of the IUT to signal an error to the host in case of a short-circuit between both bus wires while actively transmitting a data frame.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case of an available V_{IO} input: V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to BM. — Communication: Node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Short-circuit BP to BM (failure FL21) of node 24 at *TP2_N24*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Stimulate the IUT of node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern according to 9.1.3.2 followed by eight 50/50 patterns according to9.1.3.8. e) Switch off short-circuit BP to BM (failure FL21) of node 24 after *uTxEN* is switched back to logical HIGH.
Postamble	Standard postamble.
Pass criteria	— In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 100 µs after the transmission stops, i.e. TxEN switches from LOW to HIGH. — In case that SPI as host interface is implemented:

Name	S/C BP to BM at node with data frame
	The IUT of node 24 shall signal an error to the host latest 200 µs after the transmission stops, i.e. TxEN switches from LOW to HIGH.

9.3.16.6 Short-circuit bus wires to -5 V with data frame

Table 261 defines the test case for short-circuit bus wires to -5 V with data frame.

Table 261 — Test case for short-circuit bus wires to -5 V with data frame

Name	Short-circuit bus wires to -5 V with data frame
Test purpose	This test checks the ability of the IUT to signal an error to the host in case of a short-circuit of the bus wire to -5 V while actively transmitting a data frame.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case of an available V_{IO} input: V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to -5,0 V. — Communication: Node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Short-circuit BP (failure FL19) of node 24 to -5 V at *TP2_N24*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Stimulate the IUT of node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern according to 9.1.3.2 followed by eight 50/50 patterns according to9.1.3.8. e) Switch off short-circuit BP (failure FL19) of node 24 after *uTxEN* is switched back to logical HIGH.
Postamble	Standard postamble.
Pass criteria	— In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 100 µs after the transmission stops, i.e. TxEN switches from LOW to HIGH. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 200 µs after the transmission stops, i.e. TxEN switches from LOW to HIGH.

Table 262 defines the test instances for short-circuit bus wires to -5 V with data frame test case defined in Table 261.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 262 — Test instances for short-circuit bus wires to -5 V with data frame

Instance		**1**	**2**
Purpose	**Stress**	S/C BP to -5 V at node 24	S/C BM to -5 V at node 24
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to -5 V	S/C BM to -5 V
Preamble		Standard Short-circuit BP (failure FL19) of node 24 to -5 V at *TP2_N24*.	Standard Short-circuit BM (failure FL20) of node 24 to -5 V at *TP2_N24*.
Test execution		Switch off short-circuit BP (failure FL19) of node 24 to -5 V at *TP2_N24*.	Switch off Short-circuit BM (failure FL20) of node 24 to -5 V at *TP2_N24*.
Pass criteria		—	—

9.3.16.7 Short-circuit bus wires to 27 V with data frame

Table 263 defines the test case for short-circuit bus wires to 27 V with data frame.

Table 263 — Test case for short-circuit bus wires to 27 V with data frame

Name	Short-circuit bus wires to 27 V with data frame
Test purpose	This test checks the ability of the IUT to signal an error to the host in case of a short-circuit of the bus wire to 27 V while actively transmitting a data frame.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case of an available V_{IO} input: V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to 27 V. — Communication: Node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Short-circuit BP (failure FL13) of node 24 to 27V at *TP2_N24*.
Test execution	a) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24. b) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24. c) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. d) Stimulate the IUT of node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern according to 9.1.3.2 followed by eight 50/50 patterns according to 9.1.3.8. e) Switch off short-circuit BP (failure FL13) of node 24 after *uTxEN* is switched back to logical HIGH.
Postamble	Standard postamble.
Pass criteria	— In case that hard wired signals as host interface are implemented: The IUT of node 24 shall signal an error to the host latest 100 µs after the transmission stops, i.e. TxEN switches from LOW to HIGH. — In case that SPI as host interface is implemented: The IUT of node 24 shall signal an error to the host latest 200 µs after the transmission stops, i.e. TxEN switches from LOW to HIGH.

Table 264 defines the test instances for short-circuit bus wires to 27 V with data frame test case defined in Table 263.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 264 — Test instances for short-circuit bus wires to 27 V with data frame

Instance		1	2
Purpose	**Stress**	S/C BP to 27 V at node 24	S/C BM to 27 V at node 24
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to 27 V	S/C BM to 27 V
Preamble		Standard Short-circuit BP (failure FL13) of node 24 to 27 V at *TP2_N24*.	Standard Short-circuit BM (failure FL14) of node 24 to 27 V at *TP2_N24*.
Test execution		Switch off short-circuit BP (failure FL19) of node 24 to 27 V at *TP2_N24*.	Switch off Short-circuit BM (failure FL14) of node 24 to 27 V at *TP2_N24*.
Pass criteria		—	—

9.3.17 Environment.Ground Shift.Dynamic Ground Shift

9.3.17.1 Dynamic ground shift at transmitter

Table 265 defines the test case for dynamic ground shift at transmitter.

Table 265 — Test case for dynamic ground shift at transmitter

Name	Dynamic ground shift at transmitter
Test purpose	This test checks the ability of the IUT to transmit a test pattern while dynamic ground shift is present.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: Dynamic at node 23. — Failure: None. — Communication: Node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uGS_dyn* at *TP_N23_UGS* of node 23 according to the observation window described in 9.1.4.3. b) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23 according to the observation window described in 9.1.4.3. c) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23 according to the observation window described in 9.1.4.3. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24 according to the observation window described in 9.1.4.3. e) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1, followed by one TSS pattern, followed by nine 50/50 patterns, followed by one 10Bit High pattern. Trigger the dynamic ground shift curve synchronously with the first rising edge after the TSS pattern.
Postamble	Standard postamble.
Pass criteria	— The IUT of node 24 shall receive all patterns after the trigger event in *uTxD* of node 23, i.e. the dynamic ground shift shall not disturb the communication.

9.3.17.2 Dynamic ground shift at receiver

Table 266 defines the test case for dynamic ground shift at receiver.

Table 266 — Test case for dynamic ground shift at receiver

Name	**Dynamic ground shift at receiver**
Test purpose	This test checks the ability of the IUT to receive a test pattern while dynamic ground shift is present.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: Dynamic at node 23. — Failure: None. — Communication: Node 24 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uGS_dyn* at *TP_N23_UGS* of node 23 according to the observation window described in 9.1.4.3. b) Observe and acquire *uTxD* at *TP_N24_TxD* of node 24 according to the observation window described in 9.1.4.3. c) Observe and acquire *uTxEN* at *TP_N24_TxEN* of node 24 according to the observation window described in 9.1.4.3. d) Observe and acquire *uRxD* at *TP_N23_RxD* of node 23 according to the observation window described in 9.1.4.3. e) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one wakeup pattern as described in 9.1.3.1, followed by one TSS pattern, followed by nine 50/50 patterns, followed by one 10Bit High pattern. Trigger the dynamic ground shift curve synchronously with the first rising edge after the TSS pattern.
Postamble	Standard postamble.
Pass criteria	— The IUT of node 23 shall receive all patterns after the trigger event in *uTxD* of node 24, i.e. the dynamic ground shift shall not disturb the communication.

9.3.18 Dynamic Low Supply

9.3.18.1 Mode change back to *BD_Normal* (hard-wired signals) after dynamic low supply voltage

Table 267 defines the test case for mode change back to BD_Normal (hard-wired signals) after dynamic low supply voltage.

Table 267 — Test case for mode change back to *BD_Normal* (hard-wired signals) after dynamic low supply voltage

Name	**Mode change back to *BD_Normal* (hard-wired signals) after dynamic low supply voltage**
Test purpose	This test checks the behaviour of the IUT after a dynamic low supply voltage pulse according to 7.5 occuring in *BD_Normal* mode. This test case is skipped if host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes except node 24: 11,6 V. — External V_{BAT} power supply of node 24: 11,6 V. — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes except node 24: 11,6 V. — External V_{BAT} power supply of node 24: 11,6 V. — V_{IO} reference voltage (in case of an available V_{IO} input): — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test). — Test signal: Case 1.1 as specified in 7.5.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes.

Name	Mode change back to *BD_Normal* (hard-wired signals) after dynamic low supply voltage
	b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Trigger the dynamic low supply voltage pulse at the power supply of node 24. g) Wait until all implemented power supply voltages rise above their undervoltage detection thresholds. h) • After 10 ms + 100 µs, stimulate the IUTs of transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low supply voltage pulse. The bit duration in this test case shall be *gdBit*=25 µs, because the memory depth of the logic analyzer is much too small to acquire 4 seconds with a 100 ns bit time. The gap between the messages in matrix A shall be 9,25 ms. i) Trigger the logic analyzer to start synchronously with the first falling edge of *uTxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The observation window shall start with the first falling edge of *uTxEN* of node 1. Adaptation of the thresholds for digital signals may be required. — *uRxD* of all nodes shall contain all 50/50 patterns transmitted by all nodes (according to *uTxD* and *uTxEN* of all nodes), i.e. all data shall be transmitted and received by the IUTs in all nodes. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical HIGH state before the first node according to the sequence described on matrix A is stimulated (falling edge of *uTxD* and *uTxEN*) and shall be in logical LOW state while *uRxD* of the corresponding node signals the received patterns. — In case of an available INH1 signal *uINH1* at *TP_N24_INH1* of node 24 shall be in logical HIGH state during the test execution.

Table 268 defines the test instances for mode change back to BD_Normal (hard-wired signals) after dynamic low supply voltage test case defined in Table 267.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 268 — Test instances for mode change back to *BD_Normal* (hard-wired signals) after dynamic low supply voltage

Instance		1	2	3	4
Purpose	**Stress**	—	—	—	—
	Precondition	—	—	—	—
Configuration	**Power supply**	Test signal: Case 1.1 as specified in 7.5	Test signal: Case 1.2 as specified in 7.5	Test signal: Case 2.1 as specified in 7.5	Test signal: Case 2.2 as specified in 7.5
	Ground shift	—	—	—	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

9.3.18.2 Mode change from *BD_Normal* to BD_Sleep due to dynamic low supply voltage (SPI)

Table 269 defines the test case for mode change from BD_Normal to BD_Sleep due to dynamic low supply voltage (SPI).

Table 269 — Test case for mode change from *BD_Normal* to *BD_Sleep* due to dynamic low supply voltage (SPI)

Name	**Mode change from *BD_Normal* to *BD_Sleep* due to dynamic low supply voltage (SPI)**
Test purpose	This test checks the behaviour of the IUT after a dynamic low supply voltage pulse according to 7.5 occuring in *BD_Normal* mode. This test case is skipped if: — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the host interface B (SPI) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes except node 24: 11,6 V.
	  — External V_{BAT} power supply of node 24: 11,6 V.
	  — V_{CC} power supply of all nodes: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— In case that only V_{BAT} is implemented:
	  — V_{BAT} power supply of all nodes except node 24: 11,6 V.
	  — External V_{BAT} power supply of node 24: 11,6 V.
	— V_{IO} reference voltage (in case of an available V_{IO} input):
	  — V_{IO} reference voltage of all nodes: depends on implementation.
	  — External V_{IO} reference voltage of the IUT in node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: matrix A (round robin test).
	— Test signal: Case 1.1 as specified in 7.5

Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes.

Name	Mode change from *BD_Normal* to *BD_Sleep* due to dynamic low supply voltage (SPI)
	c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire the error signal of the host interface (*TP_Nx_INTN*) at all nodes. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. g) Trigger the dynamic low supply voltage pulse at the power supply of node 24. h) Wait until all implemented power supply voltages rise above their undervoltage detection thresholds. i) After 10 ms + 100 µs, stimulate the IUTs of transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low supply voltage pulse. The bit duration in this test case shall be gdBit=25 µs, because the memory depth of the logic analyzer is much too small to acquire 4 seconds with a 100 ns bit time. The gap between the messages in matrix A shall be 9,25 ms. j) Trigger the logic analyzer to start synchronously with the first falling edge of *uTxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of all nodes except node 24 shall contain all 50/50 patterns transmitted by all nodes except node 24 (according to uTxD and uTxEN of all nodes), i.e. all data shall be transmitted and received by the IUTs in all nodes that are not stressed by the dynamic low supply voltage curve. — In case of an available RxEN signal *uRxEN* of all nodes except node 24 shall be in logical LOW state while *uRxD* of the corresponding node signals the received patterns. — *uINH1* at *TP_N24_INH1* of node 24 shall be in logical LOW state during the test execution; i.e. node 24 shall be in *BD_Sleep* mode at the end of the dynamic low supply voltage curve. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — The error signal shall be HIGH at the host interface of all observed nodes except node 24. — An error shall be signaled via the host interface of node 24 during the test execution.

Table 270 defines the test instances for mode change from BD_Normal to BD_Sleep due to dynamic low supply voltage (SPI) test case defined in Table 269.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 270 — Test instances for mode change from *BD_Normal* to *BD_Sleep* due to dynamic low supply voltage (SPI)

Instance		**1**	**2**	**3**	**4**
Purpose	**Stress**	—	—	—	—
	Precondition	—	—	—	—
Configuration	**Power supply**	Test signal: Case 1.1 as specified in 7.5	Test signal: Case 1.2 as specified in 7.5	Test signal: Case 2.1 as specified in 7.5	Test signal: Case 2.2 as specified in 7.5
	Ground shift	—	—	—	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

9.3.18.3 Mode change from *BD_Normal* to BD_Standby due to dynamic low supply voltage (SPI)

Table 271 defines the test case for mode change from BD_Normal to BD_Standby due to dynamic low supply voltage (SPI).

Table 271 — Test case for mode change from *BD_Normal* to *BD_Standby* due to dynamic low supply voltage (SPI)

Name	Mode change from *BD_Normal* to *BD_Standby* due to dynamic low supply voltage (SPI)
Test purpose	This test checks the behaviour of the IUT after a dynamic low supply voltage pulse according to 7.5 occuring in *BD_Normal* mode. This test case is skipped if: — either the Functional class “Bus driver voltage regulator control” or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes except node 24: 11,6 V. — External V_{BAT} power supply of node 24: 11,6 V. — In case that only V_{CC} is implemented: — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage (in case of an available V_{IO} input): — V_{IO} reference voltage of all nodes: depends on implementation. — External V_{IO} reference voltage of the IUT in node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test). — Test signal: Case 1.1 as specified in 7.5.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire the error signal of the host interface (*TP_Nx_INTN*) of all nodes. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all

Name	Mode change from *BD_Normal* to *BD_Standby* due to dynamic low supply voltage (SPI)
	nodes. f) Trigger the dynamic low supply voltage pulse at the power supply of node 24. g) Wait until all implemented power supply voltages rise above their undervoltage detection thresholds. h) After 10 ms + 100 µs, stimulate the IUTs of transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low supply voltage pulse. The bit duration in this test case shall be gdBit=25 µs, because the memory depth of the logic analyzer is much too small to acquire 4 seconds with a 100 ns bit time. The gap between the messages in matrix A shall be 9,25 ms. i) Trigger the logic analyzer to start synchronously with the first falling edge of *uTxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of all nodes except node 24 shall contain all 50/50 patterns transmitted by all nodes except node 24 (according to *uTxD* and *uTxEN* of all nodes), i.e. all data shall be transmitted and received by the IUTs in all nodes that are not stressed by the dynamic low supply voltage curve. — In case of an available RxEN signal *uRxEN* of all nodes except node 24 shall be in logical LOW state while *uRxD* of the corresponding node signals the received patterns. — *uRxD* of node 24 shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — The error signal shall be HIGH at the host interface of all observed nodes except node 24. — An error shall be signaled via the host interface of node 24 during the test execution.

Table 272 defines the test instances for mode change from BD_Normal to BD_Standby due to dynamic low supply voltage (SPI) test case defined in Table 271.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 272 — Test instances for modechange from *BD_Normal* to *BD_Standby* due to dynamic low supply voltage (SPI)

Instance		1	2	3	4
Purpose	**Stress**	—	—	—	—
	Precondition	—	—	—	—
Configuration	**Power supply**	Test signal: Case 1.1 as specified in 7.5	Test signal: Case 1.2 as specified in 7.5	Test signal: Case 2.1 as specified in 7.5	Test signal: Case 2.2 as specified in 7.5
	Ground shift	—	—	—	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

9.3.19 Communication.Transmitter Activation

9.3.19.1 Transmission enable after uTxD changes to logical LOW state

Table 273 defines the test case for transmission enable after uTxD changes to logical LOW state.

Table 273 — Test case for transmission enable after *uTxD* changes to logical LOW state

Name	**Transmission enable after *uTxD* changes to logical LOW state**
Test purpose	This test checks the ability of the IUT not to start a transmission with a *Data_1* as specified in ISO 17458-4. The transmitter shall not be enabled by setting *uTxEN* to logical LOW state while *uTxD* is in logical HIGH state. The transmitter shall be enabled as soon as *uTxD* changes to logical LOW state, too.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) Observe and acquire *uBus* at *TP1_N23* of node 23. e) Observe and acquire the error signal of the host interface (*TP_N23_ERRN* or *TP_N23_INTN*) of node 23 f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. g) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by six 10Bit High pattern as specified in 9.1.3.7, followed by a TSS pattern and a 50/50 pattern. h) Trigger the scope to start synchronously with the stimulation of the IUT in node 23

Name	Transmission enable after *uTxD* changes to logical LOW state
	according to the observation window described in 9.1.4.2. i) Trigger the logic analyzer to start synchronously with the stimulation of the IUT in node 23.
Postamble	Standard postamble.
Pass criteria	— *uBus* at *TP1_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 24 shall contain the 50/50 pattern sent by node 23. — In case a RxEN signal is implemented *uRxEN* of node 24 shall be in logical HIGH state initially. While *uRxD* of node 24 signals the 50/50 pattern sent by node 23 *uRxEN* of node 24 shall be in logical LOW state. — No error shall be signalled at the host interface of node 23.

Table 274 defines the test instances for transmission enable after uTxD changes to logical LOW state test case defined in Table 273.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 274 — Test instances for transmission enable after *uTxD* changes to logical LOW state

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N23	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.19.2 No transmission enable while uTxD remains in logical HIGH state

Table 275 defines the test case for no transmission enable while uTxD remains in logical HIGH state.

Table 275 — Test case for no transmission enable while *uTxD* remains in logical HIGH state

Name	**No transmission enable while *uTxD* remains in logical HIGH state**
Test purpose	This test checks the ability of the IUT to ignore a transmission enable with a permanent *Data_1* phase at TxD while *uTxEN* is in logical LOW state as specified in ISO 17458-4. The transmitter shall not be enabled by setting *uTxEN* to logical LOW state while *uTxD* is in logical HIGH state. The bus shall not be disturbed when *uTxEN* is set to logical LOW state and returns to logical HIGH state while *uTxD* is permanently logical HIGH state.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_N24_RxEN* of node 24. e) Observe and acquire the error signal of the host interface (*TP_N23_ERRN* or *TP_N23_INTN*) of node 23. f) Observe and acquire *uBus* at *TP1_N23* of node 23. g) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by four 10Bit High pattern as specified in 9.1.3.7. h) Trigger the scope to start synchronously with the stimulation of the IUT in node 23 according to the observation window described in 9.1.4.2.

Name	**No transmission enable while *uTxD* remains in logical HIGH state**
	i) Trigger the logic analyzer to start synchronously with the stimulation of the IUT in node 23.
Postamble	Standard postamble.
Pass criteria	— *uBus* at *TP1_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 24 shall be in HIGH state during the test execution. — In case a RxEN signal is implemented *uRxEN* shall be permanently in HIGH state during the test execution. — No error shall be signalled at the host interface of node 23.

Table 276 defines the test instances for no transmission enable while uTxD remains in logical HIGH state test case defined in Table 275.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 276 — Test instances for no transmission enable while *uTxD* remains in logical HIGH state

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC or BD_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N23	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20 Power Supply.Undervoltage Recovery

9.3.20.1 V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Table 277 defines the test case for V_{IO} undervoltage recovery from BD_Sleep back to BD_Normal (hard-wired host interface).

Table 277 — Test case for V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Name	V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_Normal* in case of a recovery of the undervoltage of V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24.

Name	V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)
	d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{IO} reference voltage of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Normal*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 23 signals the received pattern.

Table 278 defines the test instances for V_{IO} undervoltage recovery from BD_Sleep back to BD_Normal (hard wired host interface) test case defined in Table 277.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 278 — Test instances for V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.2 V_{IO} undervoltage recovery from *BD_Standby* back to *BD_Normal* (hard-wired host interface, *BD_Sleep* not implemented)

Table 279 defines the test case for V_{IO} undervoltage recovery from BD_Standby back to BD_Normal (hard-wired host interface, *BD_Sleep* not implemented).

Table 279 — Test case for V_{IO} undervoltage recovery from *BD_Standby* back to *BD_Normal* (hard-wired host interface, *BD_Sleep* not implemented)

Name	**V_{IO} undervoltage recovery from *BD_Standby* back to *BD_Normal* (hard-wired host interface, *BD_Sleep* not implemented)**
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Standby* back to *BD_Normal* in case of a recovery of an undervoltage of V_{IO} according to ISO 17458-4 while no stress condition is present and *BD_Sleep* is not implemented. This test case is skipped if — either the Functional class “Bus driver voltage regulator control” or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24 c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. e) Set the external V_{IO} reference voltage of the IUT in node 24 to the default

Name	V_{IO} undervoltage recovery from *BD_Standby* back to *BD_Normal* (hard-wired host interface, *BD_Sleep* not implemented)
	implementation value. f) Wait 10 ms + 100 µs. g) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. h) Wait 5 µs. i) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms+ 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 24 signals the received pattern.

Table 280 defines the test instances for V_{IO} undervoltage recovery from BD_Standby back to BD_Normal (hard wired host interface, *BD_Sleep* not implemented) test case defined in Table 279.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 280 — Test instances for V_{IO} undervoltage recovery from *BD_Standby* back to *BD_Normal* (hard-wired host interface, *BD_Sleep* not implemented)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_IVR implemented without BDControl
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.3 V_{CC} undervoltage recovery from *BD_Standby* back to *BD_Normal* (hard-wired host interface)

Table 281 defines the test case for V_{CC} undervoltage recovery from BD_Standby back to BD_Normal (hard wired host interface).

Table 281 — Test case for V_{CC} undervoltage recovery from *BD_Standby* back to *BD_Normal* (hard-wired host interface)

Name	V_{CC} undervoltage recovery from *BD_Standby* back to *BD_Normal* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Standby* back to *BD_Normal* in case of a recovery of the undervoltage of V_{CC} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes except node 24: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— In case that only V_{CC} is implemented:
	  — V_{CC} power supply of all nodes: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— V_{IO} reference voltage of all nodes except node 24: depends on implementation.
	— External V_{IO} reference voltage of node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24 c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24.

Name	V_{CC} undervoltage recovery from *BD_Standby* back to *BD_Normal* (hard-wired host interface)
	d) In case of an available INH signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{CC} power supply of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — In case of an available INH signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Normal*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 24 signals the received pattern.

Table 282 defines the test instances for V_{CC} undervoltage recovery from BD_Standby back to BD_Normal (hard-wired host interface) test case defined in Table 281.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 282 — Test instances for V_{CC} undervoltage recovery from *BD_Standby* back to *BD_Normal* (hard-wired host interface)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.4 V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Table 283 defines the test case for V_{BAT} undervoltage recovery from BD_Sleep back to BD_Normal (hard-wired host interface).

Table 283 — Test case for V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Name	V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_Normal* in case of a recovery of the undervoltage of V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — external V_{BAT} power supply of node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes: default. — external V_{BAT} power supply of node 24: default. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24 c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24.

Name	V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)
	d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{BAT} power supply of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Normal*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 24 signals the received pattern.

Table 284 defines the test instances for V_{BAT} undervoltage recovery from BD_Sleep back to BD_Normal (hard wired host interface) test case defined in Table 283.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 284 — Test instances for V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.5 V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Table 285 defines the test case for V_{IO} undervoltage recovery from BD_Sleep back to BD_ReceiveOnly (hard wired host interface).

Table 285 — Test case for V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Name	V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_ReceiveOnly* in case of a recovery of the undervoltage of V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the operation mode *BD_ReceiveOnly* in not implemented — the host interface option A (hard-wired signals) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes except node 24: +5,0 V.
	— In case that only V_{BAT} is implemented:
	V_{BAT} power supply of all nodes: default.
	— V_{IO} reference voltage of all nodes except node 24: depends on implementation.
	— External V_{IO} reference voltage of node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24.

Name	V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)
	c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{IO} reference voltage of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_ReceiveOnly*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24 — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal uRxD of node 24 signals the received pattern.

Table 286 defines the test instances for V_{IO} undervoltage recovery from BD_Sleep back to BD_ReceiveOnly (hard-wired host interface) test case defined in Table 285.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 286 — Test instances for V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.6 V_{IO} undervoltage recovery from *BD_Standby* back to *BD_ReceiveOnly* (hard-wired host interface, *BD_Sleep* not implemented)

Table 287 defines the test case for V_{IO} undervoltage recovery from BD_Standby back to BD_ReceiveOnly (hard wired host interface, *BD_Sleep* not implemented).

Table 287 — Test case for V_{IO} undervoltage recovery from *BD_Standby* back to *BD_ReceiveOnly* (hard-wired host interface, *BD_Sleep* not implemented)

Name	**V_{IO} undervoltage recovery from *BD_Standby* back to *BD_ReceiveOnly* (hard-wired host interface, *BD_Sleep* not implemented)**
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Standby* back to *BD_ReceiveOnly* in case of a recovery of an undervoltage of V_{IO} according to ISO 17458-4 while no stress condition is present and *BD_Sleep* is not implemented. This test case is skipped if — either the Functional class “Bus driver voltage regulator control” or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the operation mode *BD_ReceiveOnly* is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24.

Name	**V_{IO} undervoltage recovery from *BD_Standby* back to *BD_ReceiveOnly* (hard-wired host interface, *BD_Sleep* not implemented)**
	c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. e) Set the external V_{IO} reference voltage of the IUT in node 24 to the default implementation value. f) Wait 10 ms + 100 µs. g) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. h) Wait 5 µs. i) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24 — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal uRxD of node 24 signals the received pattern.

Table 288 defines the test instances for V_{IO} undervoltage recovery from BD_Standby back to BD_ReceiveOnly hard-wired host interface, *BD_Sleep* not implemented) test case defined in Table 287.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 288 — Test instances for V_{IO} undervoltage recovery from *BD_Standby* back to *BD_ReceiveOnly* (hard-wired host interface, *BD_Sleep* not implemented)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_IVR implemented without BDControl
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.7 V_{CC} undervoltage recovery from *BD_Standby* back to *BD_ReceiveOnly* (hard-wired host interface)

Table 289 defines the test case for V_{CC} undervoltage recovery from BD_Standby back to BD_ReceiveOnly hard-wired host interface).

Table 289 — Test case for V_{CC} undervoltage recovery from *BD_Standby* back to *BD_ReceiveOnly* (hard-wired host interface)

Name	**V_{CC} undervoltage recovery from *BD_Standby* back to *BD_ReceiveOnly* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Standby* back to *BD_ReceiveOnly* in case of a recovery of the undervoltage of V_{CC} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the operation mode *BD_ReceiveOnly* is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that only V_{CC} is implemented: — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24

Name	**V_{CC} undervoltage recovery from *BD_Standby* back to *BD_ReceiveOnly* (hard-wired host interface)**
	b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24 c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{CC} power supply of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_ReceiveOnly*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24 — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal uRxD of node 24 signals the received pattern.

Table 290 defines the test instances for V_{CC} undervoltage recovery from BD_Standby back to BD_ReceiveOnly (hard-wired host interface) test case defined in Table 289.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 290 — Test instances for V_{CC} undervoltage recovery from *BD_Standby* back to *BD_ReceiveOnly* (hard-wired host interface)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.8 V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Table 291 defines the test case for V_{BAT} undervoltage recovery from BD_Sleep back to BD_ReceiveOnly (hard wired host interface).

Table 291 — Test case for V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Name	**V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_ReceiveOnly* in case of a recovery of the undervoltage of V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the operation mode *BD_ReceiveOnly* in not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes except node 24: default. — external V_{BAT} power supply of node 24: default. — In case of an available V_{IO} input: V_{IO} reference voltage of all nodes except node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal* — Set the V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.

Name	V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{BAT} power supply of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_ReceiveOnly*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal uRxD of node 24 signals the received pattern.

Table 292 defines the test instances for V_{BAT} undervoltage recovery from BD_Sleep back to BD_ReceiveOnly (hard-wired host interface) test case defined in Table 291.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 292 — Test instances for V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.9 V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Table 293 defines the test case for V_{IO} undervoltage recovery from BD_Sleep back to BD_Standby (hard-wired host interface).

Table 293 — Test case for V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Name	V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_Standby* in case of a recovery of the undervoltage of V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window

Name	V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)
	described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{IO} reference voltage of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Standby.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 294 defines the test instances for V_{IO} undervoltage recovery from BD_Sleep back to BD_Standby (hard wired host interface) test case defined in Table 293.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 294 — Test instances for V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.10 V_{IO} undervoltage recovery from *BD_Standby* back to *BD_Standby* (hard-wired host interface, *BD_Sleep* not implemented)

Table 295 defines the test case for V_{IO} undervoltage recovery from BD_Standby back to BD_Standby (hard wired host interface, *BD_Sleep* not implemented).

Table 295 — Test case for V_{IO} undervoltage recovery from *BD_Standby* back to *BD_Standby* (hard-wired host interface, *BD_Sleep* not implemented)

Name	**V_{IO} undervoltage recovery from *BD_Standby* back to *BD_Standby* (hard-wired host interface, *BD_Sleep* not implemented)**
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Standby* back to *BD_Standby* in case of a recovery of an undervoltage of V_{IO} according to ISO 17458-4while no stress condition is present and *BD_Sleep* is not implemented. This test case is skipped if — either the Functional class “Bus driver voltage regulator control” or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window

Name	**V_{IO} undervoltage recovery from *BD_Standby* back to *BD_Standby* (hard-wired host interface, *BD_Sleep* not implemented)**
	described in 9.1.4.2. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{IO} reference voltage of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24 — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 296 defines the test instances for V_{IO} undervoltage recovery from BD_Standby back to BD_Standby (hard-wired host interface, *BD_Sleep* not implemented) test case defined in Table 295.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 296 — Test instances for V_{IO} undervoltage recovery from *BD_Standby* back to *BD_Standby* (hard-wired host interface, *BD_Sleep* not implemented)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_IVR implemented without BDControl
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.11 V_{CC} undervoltage recovery from *BD_Standby* back to *BD_Standby* (hard-wired host interface)

Table 297 defines the test case for V_{CC} undervoltage recovery from BD_Standby back to BD_Standby (hard wired host interface).

Table 297 — Test case for V_{CC} undervoltage recovery from *BD_Standby* back to *BD_Standby* (hard-wired host interface)

Name	V_{CC} undervoltage recovery from *BD_Standby* back to *BD_Standby* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Standby* back to *BD_Standby* in case of a recovery of the undervoltage of V_{CC} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes except node 24: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— In case that only V_{CC} is implemented:
	  — V_{CC} power supply of all nodes: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— V_{IO} reference voltage of all nodes: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24.

Name	V_{CC} undervoltage recovery from *BD_Standby* back to *BD_Standby* (hard-wired host interface)
	c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) Set the external V_{CC} power supply of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Standby.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 298 defines the test instances for V_{CC} undervoltage recovery from BD_Standby back to BD_Standby (hard-wired host interface) test case defined in Table 297.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 298 — Test instances for V_{CC} undervoltage recovery from *BD_Standby* back to *BD_Standby* (hard-wired host interface)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.12 V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Table 299 defines the test case for V_{BAT} undervoltage recovery from BD_Sleep back to BD_Standby (hard wired host interface).

Table 299 — Test case for V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Name	**V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_Standby* in case of a recovery of the undervoltage of V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of all nodes except node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24 b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24

Name	V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)
	c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Standby.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 300 defines the test instances for V_{BAT} undervoltage recovery from BD_Sleep back to BD_Standby (hard wired host interface) test case defined in Table 299.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 300 — Test instances for V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.13 V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Table 301 defines the test case for V_{IO} undervoltage recovery from BD_Sleep back to BD_Sleep (hard-wired host interface).

Table 301 — Test case for V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Name	V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_Sleep* in case of a recovery of the undervoltage of V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24 b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24 c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window

Name	V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)
	described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{IO} reference voltage of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24 — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 302 defines the test instances for V_{IO} undervoltage recovery from BD_Sleep back to BD_Sleep (hard wired host interface) test case defined in Table 301.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 302 — Test instances for V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.14 V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Table 303 defines the test case for V_{CC} undervoltage recovery from BD_Sleep back to BD_Sleep (hard-wired host interface).

Table 303 — Test case for V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Name	V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_Sleep* in case of a recovery of the undervoltage of V_{CC} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that V_{IO} is implemented: V_{IO} reference voltage of all nodes except node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	m) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. n) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. o) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. p) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2.

Name	V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)
	a) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. b) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. c) Set the external V_{CC} power supply of the IUT in node 24 to the default implementation value. d) Wait 10 ms + 100 µs. e) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. f) Wait 5 µs. g) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. h) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 304 defines the test instances for V_{CC} undervoltage recovery from BD_Sleep back to BD_Sleep (hard wired host interface) test case defined in Table 303.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 304 — Test instances for V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.15 V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Table 305 defines the test case for V_{BAT} undervoltage recovery from BD_Sleep back to BD_Sleep (hard-wired host interface).

Table 305 — Test case for V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Name	V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_Sleep* in case of a recovery of the undervoltage of V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — In case that V_{IO} is implemented: — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24 b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24

Name	V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)
	c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{BAT} power supply of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 306 defines the test instances for V_{BAT} undervoltage recovery from BD_Sleep back to BD_Sleep (hard wired host interface) test case defined in Table 305.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 306 — Test instances for V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.16 V_{CC} and V_{IO} undervoltage recovery from a low power mode back to *BD_Normal* (hard-wired host interface)

Table 307 defines the test case for V_{CC} and V_{IO} undervoltage recovery from a low power mode back to BD_Normal (hard-wired host interface).

Table 307 — Test case for V_{CC} and V_{IO} undervoltage recovery from a low power mode back to *BD_Normal* (hard-wired host interface)

Name	**V_{CC} and V_{IO} undervoltage recovery from a low power mode back to *BD_Normal* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Normal* in case of a recovery of the undervoltage of V_{CC} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes except node 24: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— In case that only V_{CC} is implemented:
	  — V_{CC} power supply of all nodes: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— V_{IO} reference voltage of all nodes except node 24: depends on implementation.
	— External V_{IO} reference voltage of node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms

Name	**V_{CC} and V_{IO} undervoltage recovery from a low power mode back to *BD_Normal* (hard-wired host interface)**
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24 b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24 c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) Set the external V_{CC} and V_{IO} reference voltage of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Normal*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 24 signals the received pattern.

9.3.20.17 V_{CC} and V_{IO} undervoltage recovery from *a low power mode* back to *BD_ReceiveOnly* (hard-wired host interface)

Table 308 defines the test case for V_{CC} and V_{IO} undervoltage recovery from *a low power mode* back to *BD_ReceiveOnly* (hard-wired host interface).

Table 308 — Test case for V_{CC} and V_{IO} undervoltage recovery from *a low power mode* back to *BD_ReceiveOnly* (hard-wired host interface)

Name	**V_{CC} and V_{IO} undervoltage recovery from *a low power mode* back to *BD_ReceiveOnly* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode to *BD_ReceiveOnly* in case of a recovery of the undervoltage of V_{CC} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented — the operation mode *BD_ReceiveOnly* in not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes except node 24: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— In case that only V_{CC} is implemented:
	  — V_{CC} power supply of all nodes: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— V_{IO} reference voltage of all nodes except node 24: depends on implementation.
	— External V_{IO} reference voltage of node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$.

Name	**V_{CC} and V_{IO} undervoltage recovery from *a low power mode* back to *BD_ReceiveOnly* (hard-wired host interface)**
	— Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. e) In case of an available INH1 signal at node 24 observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) Set the external V_{CC} and V_{IO} reference voltage of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal at node 24 *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_ReceiveOnly*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24 — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 24 signals the received pattern.

9.3.20.18 V_{CC} and V_{IO} undervoltage recovery from a low power mode back to *BD_Standby* (hard-wired host interface)

Table 309 defines the test case for V_{CC} and V_{IO} undervoltage recovery from a low power mode back to BD_Standby (hard-wired host interface).

Table 309 — Test case for V_{CC} and V_{IO} undervoltage recovery from a low power mode back to *BD_Standby* (hard-wired host interface)

Name	**V_{CC} and V_{IO} undervoltage recovery from a low power mode back to *BD_Standby* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Standby* in case of a recovery of the undervoltage of V_{CC} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that only V_{CC} is implemented: — V_{CC} power supply of all nodes: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$.

Name	**V_{CC} and V_{IO} undervoltage recovery from a low power mode back to *BD_Standby* (hard-wired host interface)**
	— Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) In case of an available INH1 signal at node 24 observe and acquire *uINH1* at *TP_N24_INH1* of node 24. g) Set the external V_{CC} and V_{IO} reference voltage of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Standby.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.20.19 V_{CC} and V_{IO} undervoltage recovery from a low power mode back to *BD_Sleep* (hard-wired host interface)

Table 310 defines the test case for V_{CC} and V_{IO} undervoltage recovery from a low power mode back to BD_Sleep (hard wired host interface).

Table 310 — Test case for V_{CC} and V_{IO} undervoltage recovery from a low power mode back to *BD_Sleep* (hard-wired host interface)

Name	**V_{CC} and V_{IO} undervoltage recovery from *a low power mode* back to *BD_Sleep* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Sleep* in case of a recovery of the undervoltage of V_{CC} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — a V_{CC} supply input is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24.

Name	**V_{CC} and V_{IO} undervoltage recovery from *a low power mode* back to *BD_Sleep* (hard-wired host interface)**
	c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{CC} and V_{IO} reference voltage of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.20.20 V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Table 311 defines the test case for V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to BD_Normal (hard-wired host interface).

Table 311 — Test case for V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Name	**V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Normal* in case of a recovery of the undervoltage of V_{IO} and V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes except node 24: default.
	  — External V_{BAT} power supply of node 24: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	— In case that only V_{BAT} is implemented:
	  — V_{BAT} power supply of all nodes except node 24: default.
	  — External V_{BAT} power supply of node 24: default.
	— V_{IO} reference voltage of all nodes except node 24: depends on implementation.
	— External V_{IO} reference voltage of node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— Standard preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$.

Name	**V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)**
	— Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{BAT} and V_{IO} reference voltage of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Normal*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 24 signals the received pattern.

9.3.20.21 V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Table 312 defines the test case for V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface).

Table 312 — Test case for V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Name	**V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_ReceiveOnly* in case of a recovery of the undervoltage of V_{IO} and V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented — the *BD_ReceiveOnly* mode is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes except node 24: default.
	  — External V_{BAT} power supply of node 24: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	— In case that only V_{BAT} is implemented:
	  — V_{BAT} power supply of all nodes except node 24: default.
	  — External V_{BAT} power supply of node 24: default.
	— V_{IO} reference voltage of all nodes except node 24: depends on implementation.
	— External V_{IO} reference voltage of node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.*

Name	**V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)**
	— Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{BAT} and V_{IO} reference voltage of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_ReceiveOnly*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 24 signals the received pattern.

9.3.20.22 V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Table 313 defines the test case for V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to BD_Standby (hard-wired host interface).

Table 313 — Test case for V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Name	**V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Standby* in case of a recovery of the undervoltage of V_{IO} and V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes except node 24: default.
	  — External V_{BAT} power supply of node 24: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	— In case that only V_{BAT} is implemented:
	  — V_{BAT} power supply of all nodes except node 24: default.
	  — External V_{BAT} power supply of node 24: default.
	— V_{IO} reference voltage of all nodes except node 24: depends on implementation.
	— External V_{IO} reference voltage of node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$.

Name	**V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)**
	— Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{BAT} and V_{IO} reference voltage of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Standby.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.20.23 V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Table 314 defines the test case for V_{IO} and V_{BAT} undervoltage recovery from BD_Sleep back to BD_Sleep(hard-wired host interface).

Table 314 — Test case for V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Name	**V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Sleep* in case of a recovery of the undervoltage of V_{IO} and V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$.

Name	**V_{IO} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)**
	— Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{BAT} and V_{IO} reference voltage of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.20.24 V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Table 315 defines the test case for V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to BD_Normal (hard-wired host interface).

Table 315 — Test case for V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Name	**V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Normal* in case of a recovery of the undervoltage of V_{CC} and V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that V_{IO} reference voltage is implemented: V_{IO} reference voltage of all nodes except node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24.

Name	**V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)**
	e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) Set the external V_{CC} and V_{BAT} power supply of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Normal*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 24 signals the received pattern.

9.3.20.25 V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Table 316 defines the test case for V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface).

Table 316 — Test case for V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Name	**V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_ReceiveOnly* in case of a recovery of the undervoltage of V_{CC} and V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the host interface A (hard-wired signals) is not implemented — the BD_ReceiveOnly mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: +5,0 V. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that V_{IO} reference voltage is implemented: V_{IO} reference voltage of all nodes except node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24.

Name	**V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)**
	c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{BAT} and V_{CC} power supply of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_RecieveOnly.* — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 24 signals the received pattern.

9.3.20.26 V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Table 317 defines the test case for V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface).

Table 317 — Test case for V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Name	**V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Standby* in case of a recovery of the undervoltage of V_{CC} and V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: +5,0 V. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that V_{IO} reference voltage is implemented: V_{IO} reference voltage of all nodes except node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24.

Name	**V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)**
	d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{BAT} and V_{CC} power supply of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Standby.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.20.27 V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Table 318 defines the test case for V_{CC} and V_{BAT} undervoltage recovery from BD_Sleep back to BD_Sleep (hard-wired host interface).

Table 318 — Test case for V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Name	**V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Sleep* in case of a recovery of the undervoltage of V_{CC} and V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: +5,0 V. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that V_{IO} reference voltage is implemented: V_{IO} reference voltage of all nodes except node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window

Name	V_{CC} and V_{BAT} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)
	described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{BAT} and V_{CC} power supply of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.20.28 V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Table 319 defines the test case for V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface).

Table 319 — Test case for V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Name	**V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Normal* in case of a recovery of the undervoltage of V_{CC}, V_{BAT} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24.

Name	**V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)**
	c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{CC}, V_{BAT} and V_{IO} reference voltage of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Normal*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal *uRxD* of node 24 signals the received pattern.

9.3.20.29 V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Table 320 defines the test case for V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface).

Table 320 — Test case for V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Name	**V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_ReceiveOnly* in case of a recovery of the undervoltage of V_{CC}, V_{BAT} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented — the BD_ReceiveOnly mode is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: +5,0 V. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.

Name	**V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)**
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{CC}, V_{BAT} and V_{IO} voltages of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_ReceiveOnly*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal uRxD of node 24 signals the received pattern.

9.3.20.30 V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Table 321 defines the test case for V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface).

Table 321 — Test case for V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Name	**V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Standby* in case of a recovery of the undervoltage of V_{CC}, V_{BAT} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: +5,0 V. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standby preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24.

Name	**V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)**
	b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{CC}, V_{BAT} and V_{IO} voltages of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23 according to the observation window described in 9.1.4.2.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Standby*. — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.20.31 V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Table 322 defines the test case for V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from BD_Sleep back to BD_Sleep (hard-wired host interface).

Table 322 — Test case for V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)

Name	**V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)**
Test purpose	This test checks the ability of the IUT to change the operation mode back to *BD_Sleep* in case of a recovery of the undervoltage of V_{CC}, V_{BAT} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: +5,0 V. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24.

Name	**V_{CC}, V_{BAT} and V_{IO} undervoltage recovery from *BD_Sleep* back to *BD_Sleep* (hard-wired host interface)**
	b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{CC}, V_{BAT} and V_{IO} voltages of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Not_Sleep*), i.e. node 24 shall be in *BD_Sleep*. — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

9.3.20.32 V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Table 323 defines the test case for V_{CC} undervoltage recovery from BD_Sleep back to BD_Normal (hard-wired host interface).

Table 323 — Test case for V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Name	V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_Normal* in case of a recovery of the undervoltage of V_{CC} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24 c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. f) Set the external V_{CC} power supply of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs.

Name	V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)
	h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Normal*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal uRxD of node 24 signals the received pattern.

Table 324 defines the test instances for V_{CC} undervoltage recovery from BD_Sleep back to BD_Normal (hard-wired host interface) test case defined in Table 323.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 324 — Test instances for V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Normal* (hard-wired host interface)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.33 V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Table 325 defines the test case for V_{CC} undervoltage recovery from BD_Sleep back to BD_ReceiveOnly (hard wired host interface).

Table 325 — Test case for V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Name	V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_ReceiveOnly* in case of a recovery of the undervoltage of V_{CC} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is implemented — the operation mode BD_ReceiveOnly is not implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— ReceiveOnly preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24 b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24 c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24.

Name	V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)
	f) Set the external V_{CC} power supply of the IUT in node 24 to the default implementation value. g) Wait 10 ms + 100 µs. h) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. i) Wait 5 µs. j) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_ReceiveOnly*. — *uRxD* of node 24 shall contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24 — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical LOW state while the signal uRxD of node 24 signals the received pattern.

Table 326 defines the test instances for V_{CC} undervoltage recovery from BD_Sleep back to BD_ReceiveOnly (hard-wired host interface) test case defined in Table 325.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 326 — Test instances for V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_ReceiveOnly* (hard-wired host interface)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.34 V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Table 327 defines the test case for V_{CC} undervoltage recovery from BD_Sleep back to BD_Standby (hard-wired host interface).

Table 327 — Test case for V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Name	V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* back to *BD_Standby* in case of a recovery of the undervoltage of V_{CC} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is implemented — the host interface A (hard-wired signals) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Sleep preamble. — Stimulate the IUT in node 23 at the host interface to enter *BD_Normal.* — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24 b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24 c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uRxD* at *TP_N24_RxD* of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24.

Name	V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)
	g) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. h) Set the external V_{CC} power supply of the IUT in node 24 to the default implementation value. i) Wait 10 ms + 100 µs. j) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Wait 5 µs. l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. m) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Standby.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution.

Table 328 defines the test instances for V_{CC} undervoltage recovery from BD_Sleep back to BD_Standby (hard wired host interface) test case defined in Table 327.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 328 — Test instances for V_{CC} undervoltage recovery from *BD_Sleep* back to *BD_Standby* (hard-wired host interface)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.20.35 V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Table 329 defines the test case for V_{IO} undervoltage recovery, remain in BD_Sleep (host interface as SPI).

Table 329 — Test case for V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Name	V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
Test purpose	This test checks the ability of the IUT to go from *BD_Normal* to *BD_Sleep* in case of an undervoltage of V_{IO} and to remain in the operation mode *BD_Sleep* in case of a recovery of the undervoltage of V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms + 200 µs + 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24.

Name	V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
	f) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. h) Set the external V_{IO} reference voltage of the IUT in node 24 to the default implementation value. i) Wait 10 ms + 100 µs. j) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Wait 5 µs. l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. m) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.20.36 V_{IO} undervoltage recovery, remain in *BD_Standby* (host interface as SPI, *BD_Sleep* not implemented)

Table 330 defines the test case for V_{IO} undervoltage recovery, remain in BD_Standby (host interface as SPI, *BD_Sleep* not implemented).

Table 330 — Test case for V_{IO} undervoltage recovery, remain in *BD_Standby* (host interface as SPI, *BD_Sleep* not implemented)

Name	**V_{IO} undervoltage recovery, remain in *BD_Standby* (host interface as SPI, *BD_Sleep* not implemented)**
Test purpose	This test checks the ability of the IUT to remain in the operation mode *BD_Standby* in case of a recovery of an undervoltage of V_{IO} according to ISO 17458-4 while no stress condition is present and BD_Sleep is not implemented. This test case is skipped if — either the Functional class “Bus driver voltage regulator control” is implemented or the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — In case that V_{CC} is implemented: V_{CC} power supply of all nodes except node 24: +5,0 V — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms + 200 µs + 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24.

Name	**V_{IO} undervoltage recovery, remain in *BD_Standby* (host interface as SPI, *BD_Sleep* not implemented)**
	f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{IO} reference voltage of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24 — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.20.37 V_{CC} undervoltage recovery, remain in *BD_Standby* (host interface as SPI)

Table 331 defines the test case for V_{CC} undervoltage recovery, remain in BD_Standby (host interface as SPI).

Table 331 — Test case for V_{CC} undervoltage recovery, remain in *BD_Standby* (host interface as SPI)

Name	V_{CC} undervoltage recovery, remain in *BD_Standby* (host interface as SPI)
Test purpose	This test checks the ability of the IUT to remain in the operation mode *BD_Standby* in case of a recovery of an undervoltage of V_{CC} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — In case that only V_{CC} is implemented: — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms + 200 µs + 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of

Name	V_{CC} undervoltage recovery, remain in *BD_Standby* (host interface as SPI)
	node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. h) Set the external V_{CC} power supply of the IUT in node 24 to the default implementation value. i) Wait 10 ms + 100 µs. j) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Wait 5 µs. l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. m) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Standby.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.20.38 V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Table 332 defines the test case for V_{BAT} undervoltage recovery, remain in BD_Sleep (host interface as SPI).

Table 332 — Test case for V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Name	V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
Test purpose	This test checks the ability of the IUT to remain in the operation mode *BD_Sleep* in case of a recovery of an undervoltage of V_{BAT} according to ISO 17458-4 while no stress condition is present. In case that the Functional class “Bus driver logic level adaptation” is not implemented see test case 9.3.20.44 and skip this case. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default. — V_{IO} reference voltage of all nodes: depends on implementation — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Wait 1 000 ms + 200 µs + 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window

Name	V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
	described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. h) Set the external V_{BAT} reference voltage of the IUT in node 24 to the default implementation value. i) Wait 10 ms + 100 µs. j) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Wait 5 µs. l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. m) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.20.39 V_{CC} and V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Table 333 defines the test case for V_{CC} and V_{IO} undervoltage recovery, remain in BD_Sleep (host interface as SPI).

Table 333 — Test case for V_{CC} and V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Name	V_{CC} and V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
Test purpose	This test checks the ability of the IUT to remain in the operation mode *BD_Sleep* in case of a recovery of an undervoltage of V_{CC} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms + 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24.

Name	V_{CC} and V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
	f) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. h) Set the external V_{IO} and V_{CC} power supply of the IUT in node 24 to the default implementation value. i) Wait 10 ms + 100 µs. j) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Wait 5 µs. l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. m) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.20.40 V_{CC} and V_{IO} undervoltage recovery, remain in *BD_Standby* (host interface as SPI, *BD_Sleep* not implemented)

Table 334 defines the test case for V_{CC} and V_{IO} undervoltage recovery, remain in BD_Standby (host interface as SPI, *BD_Sleep* not implemented).

Table 334 — Test case for V_{CC} and V_{IO} undervoltage recovery, remain in *BD_Standby* (host interface as SPI, *BD_Sleep* not implemented)

Name	**V_{CC} and V_{IO} undervoltage recovery, remain in *BD_Standby* (host interface as SPI, *BD_Sleep* not implemented)**
Test purpose	This test checks the ability of the IUT to remain in the operation mode *BD_Standby* in case of a recovery of an undervoltage of V_{CC} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — either the Functional class “Bus driver voltage regulator control” or the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms + 200 µs + 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24.

Name	**V_{CC} and V_{IO} undervoltage recovery, remain in *BD_Standby* (host interface as SPI, *BD_Sleep* not implemented)**
	f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. g) Set the external V_{CC} and V_{IO} reference voltage of the IUT in node 24 to the default implementation value. h) Wait 10 ms + 100 µs. i) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. j) Wait 5 µs. k) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. l) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.20.41 V_{IO} and V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Table 335 defines the test case for V_{IO} and V_{BAT} undervoltage recovery, remain in BD_Sleep (host interface as SPI).

Table 335 — Test case for V_{IO} and V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Name	V_{IO} and V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
Test purpose	This test checks the ability of the IUT to remain in the operation mode *BD_Sleep* in case of a recovery of an undervoltage of V_{IO} and V_{BAT} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface B (SPI) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes except node 24: default.
	  — External V_{BAT} power supply of node 24: default.
	  — V_{CC} power supply of all nodes except node 24: +5,0 V.
	— In case that only V_{BAT} is implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — External V_{BAT} power supply of node 24: +5,0 V.
	— V_{IO} reference voltage of all nodes except node 24: depends on implementation.
	— External V_{IO} reference voltage of node 24: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— Standard preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms + 200 µs + 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24.

Name	V_{IO} and V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
	c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. h) Set the external V_{IO} and V_{BAT} power supply of the IUT in node 24 to the default implementation value. i) Wait 10 ms + 100 µs. j) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Wait 5 µs. l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. m) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.20.42 V_{BAT} and V_{CC} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Table 336 defines the test case for V_{BAT} and V_{CC} undervoltage recovery, remain in BD_Sleep (host interface as SPI).

Table 336 — Test case for V_{BAT} and V_{CC} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Name	V_{BAT} and V_{CC} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
Test purpose	This test checks the ability of the IUT to remain in the operation mode *BD_Sleep* in case of a recovery of an undervoltage of V_{BAT} and V_{CC} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: default — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V — V_{IO} reference voltage (in case of an available V_{IO} input): V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 and node 24 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms + 200 µs + 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. e) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2.

Name	V_{BAT} and V_{CC} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
	f) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. h) Set the external V_{CC} and V_{BAT} power supply of the IUT in node 24 to the default implementation value. i) Wait 10 ms + 100 µs. j) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Wait 5 µs. l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. m) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.20.43 V_{CC}, V_{BAT} and V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Table 337 defines the test case for V_{CC}, V_{BAT} and V_{IO} undervoltage recovery, remain in BD_Sleep (host interface as SPI).

Table 337 — Test case for V_{CC}, V_{BAT} and V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Name	**V_{CC}, V_{BAT} and V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)**
Test purpose	This test checks the ability of the IUT to change the operation mode to *BD_Sleep* in case of a recovery of the undervoltage of V_{CC}, V_{BAT} and V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the host interface B (SPI) is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes except node 24: default. — External V_{BAT} power supply of node 24: +5,0 V. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms + 200 µs + 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window

Name	V_{CC}, V_{BAT} and V_{IO} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
	described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. h) Set the external V_{CC}, V_{BAT} and V_{IO} voltages of the IUT in node 24 to the default implementation value. i) Wait 10 ms + 100 µs. j) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Wait 5 µs. l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. m) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.20.44 Signal V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI, V_{IO} not implemented)

Table 338 defines the test case for signal V_{BAT} undervoltage recovery, remain in BD_Sleep (host interface as SPI, V_{IO} not implemented).

Table 338 — Test case for signal V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI, V_{IO} not implemented)

Name	**Signal V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI, V_{IO} not implemented)**
Test purpose	This test checks the ability of the IUT to remain in the operation mode *BD_Sleep* in case of a recovery of an undervoltage of V_{BAT} according to ISO 17458-4 and signal this recovery at the SPI to the host while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver logic level adaptation” is implemented — the host interface B (SPI) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes except node 24: default.
	  — External V_{BAT} power supply of node 24: default.
	  — V_{CC} power supply of all nodes: +5,0 V.
	— In case that only V_{BAT} is implemented:
	  — V_{BAT} power supply of all nodes except node 24: default.
	  — External V_{BAT} power supply of node 24: default.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— Standard preamble. — Set the external V_{BAT} power supply of the IUT in node 24 to $V_{BATUndervoltage}$. — After 1 000 ms + 200 µs + 100 µs reset the SPI interrupt line of node 24 via *uSCSN* at *TP_24_SCSN* of node 24.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24.

Name	**Signal V_{BAT} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI, V_{IO} not implemented)**
	d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. h) Set the external V_{BAT} reference voltage of the IUT in node 24 to the default implementation value. i) Wait 10 ms + 100 µs. j) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Wait 5 µs. l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. m) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep.* — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.20.45 V_{CC} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Table 339 defines the test case for V_{CC} undervoltage recovery, remain in BD_Sleep (host interface as SPI).

Table 339 — Test case for V_{CC} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)

Name	V_{CC} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
Test purpose	This test checks the ability of the IUT to remain in the operation mode *BD_Sleep* in case of a recovery of an undervoltage of V_{CC} according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is implemented — the host interface B (SPI) is not implemented.

Configuration	— Topology: as specified in previous configuration see 9.1.
	— In case that V_{BAT} and V_{CC} are both implemented:
	  — V_{BAT} power supply of all nodes: default.
	  — V_{CC} power supply of all nodes except node 24: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— In case that only V_{CC} is implemented:
	  — V_{CC} power supply of all nodes except node 24: +5,0 V.
	  — External V_{CC} power supply of node 24: +5,0 V.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: node 23 and node 24 as transmitter.

Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms + 200 µs + 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 23 and node 24. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 23 and node 24. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 23 and node 24. d) Observe and acquire *uBus* at *TP4_N23* of node 23 according to the observation window described in 9.1.4.2. e) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. f) Observe and acquire the error signal of the host interface (*TP_N24_INTN*) of node 24.

Name	V_{CC} undervoltage recovery, remain in *BD_Sleep* (host interface as SPI)
	g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 23 and node 24. h) Set the external V_{CC} power supply of the IUT in node 24 to the default implementation value. i) Wait 10 ms + 100 µs. j) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. k) Wait 5 µs. l) Stimulate the IUT in node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by one TSS pattern, followed by one 50/50 pattern as specified in 9.1.3.3. m) Trigger the scope to start the observation 5 µs after the falling edge of *uTxEN* at *TP_N23_TxEN* of node 23.
Postamble	Standard postamble.
Pass criteria	The observation shall start 10 ms + 100 µs after the undervoltage recovery, i.e. synchronously with the stimulation of the IUT in node 23. Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*), i.e. node 24 shall be in *BD_Sleep*. — *uRxD* of node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 23. — *uBus* at *TP4_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of node 23 and node 24 shall not contain the pattern transmitted at *uTxD* and *uTxEN* of node 24. — In case of an available RxEN signal *uRxEN* of node 24 shall be in logical HIGH state during the test execution. — An error shall be signalled at the host interface of node 24.

9.3.21 Power Supply.Wakeup Detection.Undervoltage Detection Timeout

9.3.21.1 V_{IO} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)

Table 340 defines the test case for V_{IO} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*).

Table 340 — Test case for V_{IO} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)

Name	**V_{IO} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)**
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* (in case of an undervoltage of V_{IO}) to *BD_Standby* (temporarily) due to a remote wakeup event and then back to *BD_Sleep* due to V_{IO} undervoltage detection timeout according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Bus driver voltage regulator control” nor the subgroup BDControl within the Functional class “Bus driver internal voltage regulator” is implemented — the Functional class “Bus driver remote wakeup” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23.

Name	**V_{IO} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)**
	c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern. f) Wait 1 000 ms + 100 ms (safety margin for measurement).
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uINH* of node 24 shall be in logical LOW state (*Sleep*) at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 100 µs + 34 µs after the beginning of the wakeup pattern), *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. the IUTs are in *BD_Standby* mode. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) not later than 1 000 ms after the wakeup was detected. — The IUT of node 24 shall signal an error to the host during the test execution.

Table 341 defines the test instances for V_{IO} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*) test case defined in Table 340.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 341 — Test instances for V_{IO} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.21.2 V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Standby* to *BD_Standby* to *BD_Standby*)

Table 342 defines the test case for V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Standby* to *BD_Standby* to *BD_Standby*).

Table 342 — Test case for V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Standby* to *BD_Standby* to *BD_Standby*)

Name	**V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Standby* to *BD_Standby* to *BD_Standby*)**
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Standby* (in case of an undervoltage of V_{CC}) to *BD_Standby* (temporarily) due to a remote wakeup event and then back to *BD_Standby* due to V_{CC} undervoltage detection timeout according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver remote wakeup” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: — V_{CC} power supply of all nodes except node 24: +5,0. — External V_{CC} power supply of node 24: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_N24_INH1* of

Name	**V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Standby* to *BD_Standby* to *BD_Standby*)**
	node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern. f) Wait 1 000 ms + 100 ms (safety margin for measurement).
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. node 24 shall be in *BD_Standby*. — The IUT of node 24 shall signal an error to the host during the test execution.

Table 343 defines the test instances for V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Standby* to *BD_Standby* to *BD_Standby*) test case defined in Table 342.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 343 — Test instances for V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Standby* to *BD_Standby* to *BD_Standby*)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	BD_VRC implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.21.3 V_{IO} and V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)

Table 344 defines the test case for V_{IO} and V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*).

Table 344 — Test case for V_{IO} and V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)

Name	**V_{IO} and V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)**
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* (in case of an undervoltage of V_{IO} and V_{CC}) to *BD_Standby* (temporarily) due to a remote wakeup event and then back to *BD_Sleep* due to V_{IO} and V_{CC} undervoltage detection timeout according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver voltage regulator control” is not implemented — the Functional class “Bus driver logic level adaptation” is not implemented — the Functional class “Bus driver internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — V_{IO} reference voltage of all nodes except node 24: depends on implementation. — External V_{IO} reference voltage of node 24: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{IO} reference voltage of the IUT in node 24 to $V_{IOUndervoltage}$. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24.

Name	**V_{IO} and V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)**
	e) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern. f) Wait 1 000 ms + 100 ms (safety margin for measurement)
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uINH* of node 24 shall be in logical LOW state (*Sleep*) at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 24. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 100 µs + 34 µs after the beginning of the wakeup pattern), uINH1 of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. the IUTs are in *BD_Standby* mode. — *uINH1* of node 24 shall be in logical LOW state (*Sleep)* not later than 1 000 ms after the wakeup was detected. — The IUT of node 24 shall signal an error to the host during the test execution.

Table 345 defines the test instances for V_{IO} and V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*) test case defined in Table 344.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 345 — Test instances for V_{IO} and V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.21.4 V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)

Table 346 defines the test case for V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*).

Table 346 — Test case for V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)

Name	V_{CC} **undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)**
Test purpose	This test checks the ability of the IUT to change the operation mode from *BD_Sleep* (in case of an undervoltage of V_{CC}) to *BD_Standby* (temporarily) due to a remote wakeup event and then back to *BD_Sleep* due to V_{CC} undervoltage detection timeout of according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the Functional class “Bus driver remote wakeup” is not implemented — the Functional class “Bus driver logic level adaptation” is implemented — the Functional class “Bus driver voltage regulator control” is not implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes except node 24: +5,0 V. — External V_{CC} power supply of node 24: +5,0 V. — Ground shift: 0 V. — Failure: none. — Communication: Node 23 as transmitter.
Preamble (setup state)	— Standard preamble. — Set the external V_{CC} power supply of the IUT in node 24 to $V_{CCUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uINH1* at *TP_N24_INH1* of node 24. d) Observe and acquire the error signal of the host interface (*TP_N24_ERRN* or *TP_N24_INTN*) of node 24. e) Stimulate the IUT in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern. f) Wait 1 000 ms + 100 ms (safety margin for measurement).
Postamble	Standard postamble.

Name	V_{CC} **undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)**
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uINH1* of node 24 shall be in logical LOW state (*Sleep*) at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 23. After the wakeup event is detected (between 31 µs after the beginning of the wakeup pattern and 134 µs after the beginning of the wakeup pattern), *uINH1* of node 24 shall be in logical HIGH state (*Not_Sleep*), i.e. the IUT is in *BD_Standby* mode. — Latest 1 000 ms + 134 µs after the beginning of the wakeup pattern, *uINH1* of node 24 shall be in logical LOW state (*Sleep*) again, i.e. the undervoltage at V_{DIG} is recognized and the IUT shall be in *BD_Sleep* mode at the end of the test execution. — The IUT of node 24 shall signal an error to the host during the test execution.

Table 347 defines the test instances for V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*) test case defined in Table 346.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 347 — Test instances for V_{CC} undervoltage detection timeout after remote wakeup detection (*BD_Sleep* to *BD_Standby* to *BD_Sleep*)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V
	Ground shift	—	+5,0 V at N24	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

9.3.22 Environment.Common Mode Offset

9.3.22.1 Negative common mode offset at passive bus

Table 348 defines the test case for negative common mode offset at passive bus.

Table 348 — Test case for negative common mode offset at passive bus

Name	Negative common mode offset at passive bus
Test purpose	This test checks the behavior of the IUTs when a negative common mode offset occurs in *BD_Normal* normal mode while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test).
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Apply a negative common mode offset of -12,5 V at the passive bus (V_2) to BP and BM according to 7.12. g) Wait 15 µs. h) Stimulate the IUTs of the transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.

Name	Negative common mode offset at passive bus
Pass criteria	The asymmetry that is described in 9.1.16 is considered within the pass-/fail assessment of this test case. — *uRxD* of all nodes shall contain all 50/50 patterns transmitted at *uTxD* and *uTxEN* of all nodes, i.e. all transmitted data shall be received by all nodes (loopback functionality). — In case of an available INH1 signal *uINH1* of all nodes shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical HIGH state before the first node according to the sequence described on matrix A is stimulated (falling edge of *uTxD* and *uTxEN*) and shall be in logical LOW state while uRxD of the corresponding node signals the received patterns.

9.3.22.2 Positive common mode offset at passive bus

Table 349 defines the test case for positive common mode offset at passive bus.

Table 349 — Test case for positive common mode offset at passive bus

Name	Positive common mode offset at passive bus
Test purpose	This test checks the behavior of the IUTs when a positive common mode offset occurs in *BD_Normal* normal mode while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of all nodes: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of all nodes: default. — V_{CC} power supply of all nodes: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of all nodes: default. — V_{IO} reference voltage of all nodes (in case of an available V_{IO} input): depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test).
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_Nx_INH1* of all nodes. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Apply a positive common mode offset of +12,5 V at the passive bus (V_2) to BP and BM according to 7.12. g) Wait 15 µs. h) Stimulate the IUTs of the transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	The asymmetry that is described in 9.1.16 is considered within the pass-/fail assessment of this test

Name	Positive common mode offset at passive bus
	case. — *uRxD* of all nodes shall contain all 50/50 patterns transmitted at *uTxD* and *uTxEN* of all nodes, i.e. all transmitted data shall be received by all nodes (loopback functionality). — In case of an available INH1 signal *uINH1* of all nodes shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical HIGH state before the first node according to the sequence described on matrix A is stimulated (falling edge of *uTxD* and *uTxEN*) and shall be in logical LOW state while uRxD of the corresponding node signals the received patterns.

10 Test cases for Active Stars

10.1 General

This test case section is applicable to all active stars, independent from an implemented communication controller, bus guardian interface or host interface. In such case, TxD and TxEN of the communication controller interface and BGE of the bus guardian interface shall be set to logical HIGH state permanently, if implemented.

In case the active star device has an Intra Star Interface available, this interface shall be tested by coupling two of such devices together and executing the respective test cases while using only two branches of each device.

10.2 Configuration

10.2.1 Topology

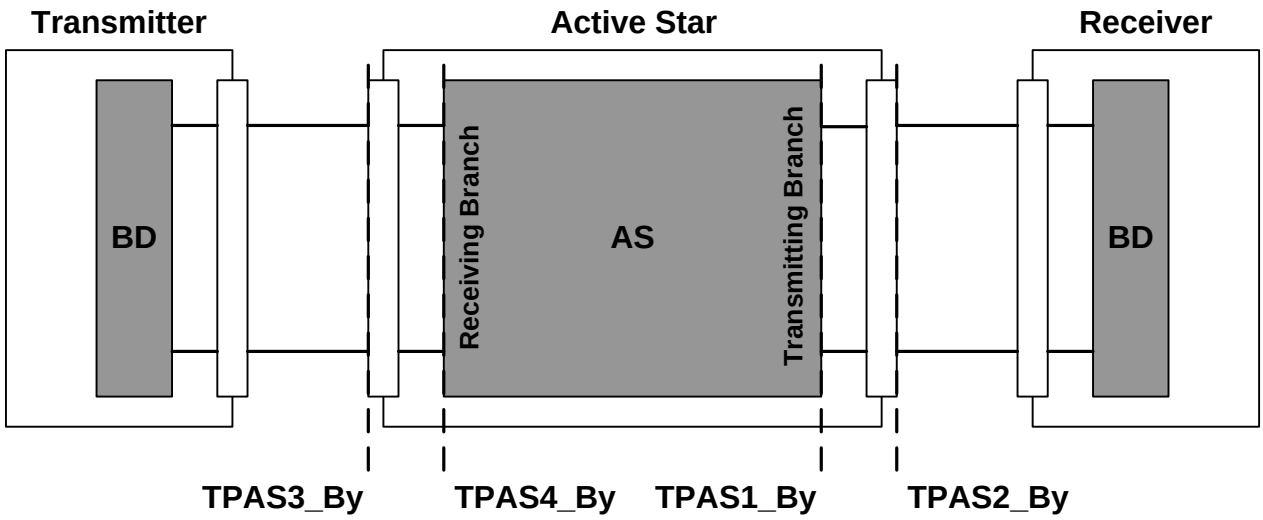
As specified in 6.4. All IUTs of the Active Star are of the same type and from the same manufacturer.

10.2.2 Test planes

10.2.2.1 Analog signals

The Active Star has four specified test planes. Two test planes for the transmitting branch and two for the receiving branch.

Figure 54 depicts the test planes a the Active Star for analog signals.



Components

AS Active Star

BD Bus Driver

Connections and supplies

TPASx_By Test plane x at the Active Star branch y (see Table 350)

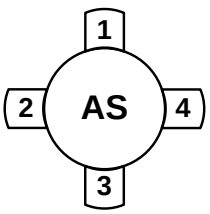
Figure 54 — Test planes at the Active Star for analog signals

Table 350 defines the test planes at the Active Star for analog signals.

Table 350 — Test planes at the Active Star for analog signals

TP Name	Signal	Description
TPAS1_By	*uBus*	Transmitting branch, test plane as close as possible to the IUT
TPAS1_By_BP	*uBP*	Transmitting branch, test plane as close as possible to the IUT
TPAS1_By_BM	*uBM*	Transmitting branch, test plane as close as possible to the IUT
TPAS2_By	*uBus*	Transmitting branch, test plane as close as possible to the network
TPAS3_By	*uBus*	Receiving branch, test plane as close as possible to the network
TPAS4_By	*uBus*	Receiving branch, test plane as close as possible to the IUT

Figure 55 depicts the branches of the Active Star.



Key

AS Active Star

Figure 55 — Branches of the Active Star

The AS has 4 branches that are named for the test planes as *TPASx_By* where

— x stands for the test plane

— y stands for the branch of the AS

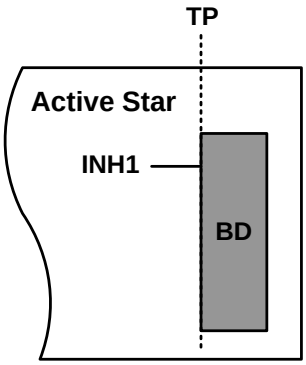
EXAMPLE

TPAS1_B2 represents the test plane 1 at the branch 2 of the Active Star.

10.2.2.2 Digital signals

The test planes at the Active Star for digital signals (observation by logic analyzer) are specified as:

Figure 54 depicts the test planes at the Active Star.



Components

BD Bus Driver

Connections and supplies

INH1 Inhibit 1 pin

TP Test plane

Figure 56 — Test planes at the Active Star

Table 351 defines the test planes at the Active Star (digital signals).

Table 351 — Test planes at the Active Star (digital signals)

TP Name	Signals	Description
TP_AS_INH1	INH1	INH1 signal of the IUT

10.2.2.3 Test planes for current measurement

A shunt shall be implemented in order to measure the current of the bus wires:

— *TP_AS_B2_*R_{iBP}[24)]

24) Only branch 1 is affected

— *TP_AS_B2_R$_{iBM}$*

10.2.2.4 Test planes for the oscilloscope

The oscilloscope observes the following test planes:

— *TP_N23_RxD*

— *TP_N23_TxEN*

— *TP_N23_TxD*

— *TP_N2_RxD*

— *TP_N2_TxEN*

— *TP_N2_TxD*

— *TP4_N2*

— *TP4_N12*

— *TPAS1_By_BM*

— *TPAS1_By_BP*

— *TP_AS_UGS* (dynamic ground shift voltage)

10.2.2.5 Test planes for the logic analyzer

The logic analyzer observes the following test planes:

— *TP_Nx_RxD*[25)]

— *TP_Nx_RxEN*

— *TP_Nx_TxD*

— *TP_Nx_TxEN*

— *TP_Nx_STBN*

— *TP_Nx_ERRN*

— *TP_Nx_INH1*

— *TP_Nx_WAKE*

— *TP_Nx_BGE*

— *TP_Nx_EN*

— *TP_Nx_INTN*

25) The number of the node depends on the test case

— *TP_Nx_SCSN*

10.2.2.6 Test planes for the pattern generator

The pattern generator stimulates the following test planes:

— *TP_Nx_TxD*[26)]

— *TP_Nx_TxEN*

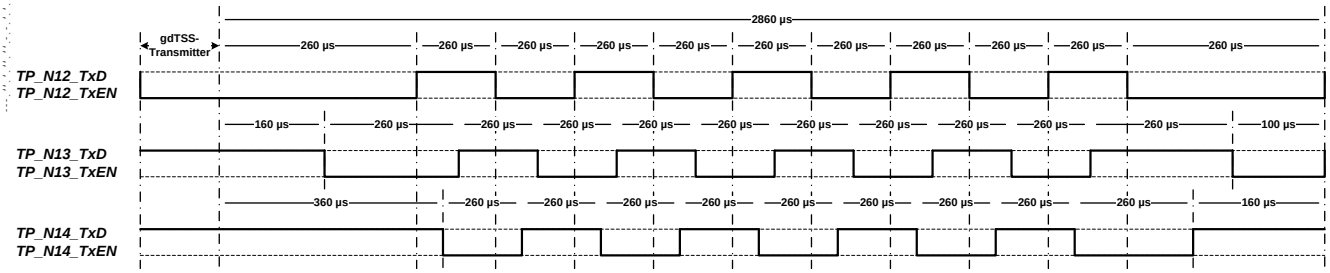
— *TP_Nx_BGE*

— *TP_AS_WAKE*

10.2.3 Test patterns

10.2.3.1 Babbling idiot

Figure 57 depicts the test pattern for a babbling idiot simulation.



Key

TP_N12_TxD	Transmit Data input signal of the IUT at node 12
TP_N12_TxEN	Transmit Data Enable Not input signal of the IUT at node 12
TP_N13_TxD	Transmit Data input signal of the IUT at node 13
TP_N13_TxEN	Transmit Data Enable Not input signal of the IUT at node 13
TP_N14_TxD	Transmit Data input signal of the IUT at node 14
TP_N14_TxEN	Transmit Data Enable Not input signal of the IUT at node 14

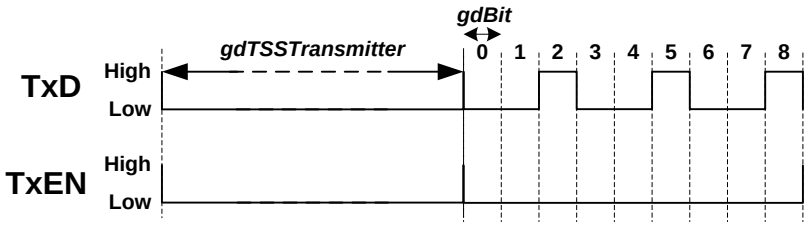
Figure 57 — Test pattern for a babbling idiot simulation

10.2.3.2 Star setup delay

These test signals are specified to check the parameter *dStarSetUpDelay*.

Figure 58 depicts the test signal for node 1 (star setup delay).

26) The number of the node depends on the test case



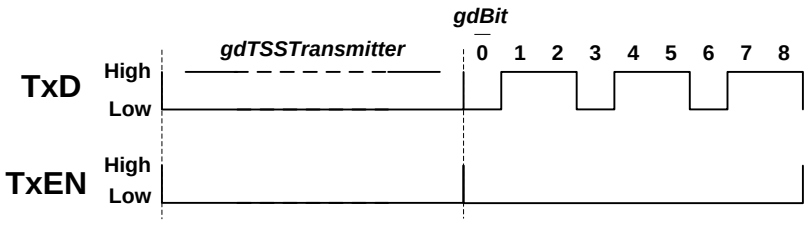
Key

TxD Transmit data

TxEN Transmit enable not

Figure 58 — Test signal for node 1 (star setup delay)

Figure 59 depicts the test signal for node 2 (star setup delay).



Key

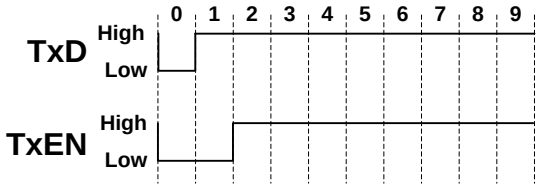
TxD Transmit data

TxEN Transmit enable not

Figure 59 — Test signal for node 2 (star setup delay)

10.2.3.3 Frame end sequence (FES)

Figure 60 depicts the test pattern for simulation of a frame end sequence.



Key

TxD Transmit data

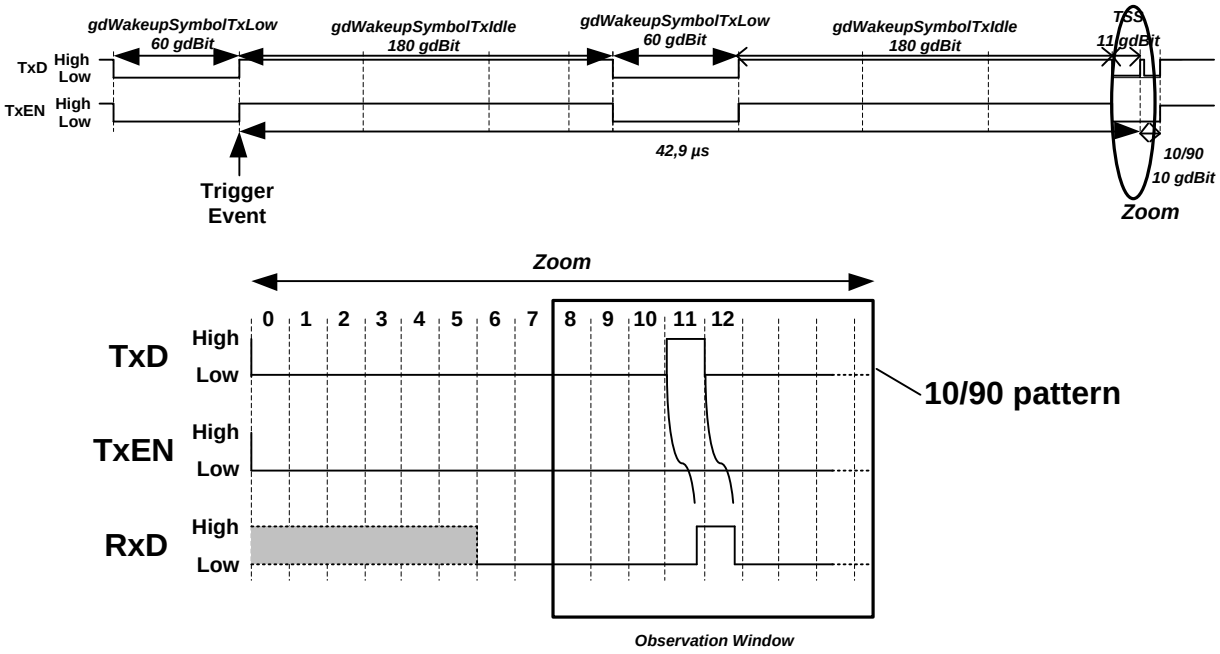
TxEN Transmit enable not

Figure 60 — Test pattern FES

10.2.4 Observation windows

10.2.4.1 Parameters *dStarDelay10* and *dStarDelay01*

Figure 61 depicts the observation point for the analysis of the star delay.



Key

RxD	Receive data
TxD	Transmit data
TxEN	Transmit enable not

Figure 61 — Observation point for the analysis of the star delay

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point 1: 42,9 µs after the trigger event.

— Start acquisition point 2: 65 µs after the trigger event.

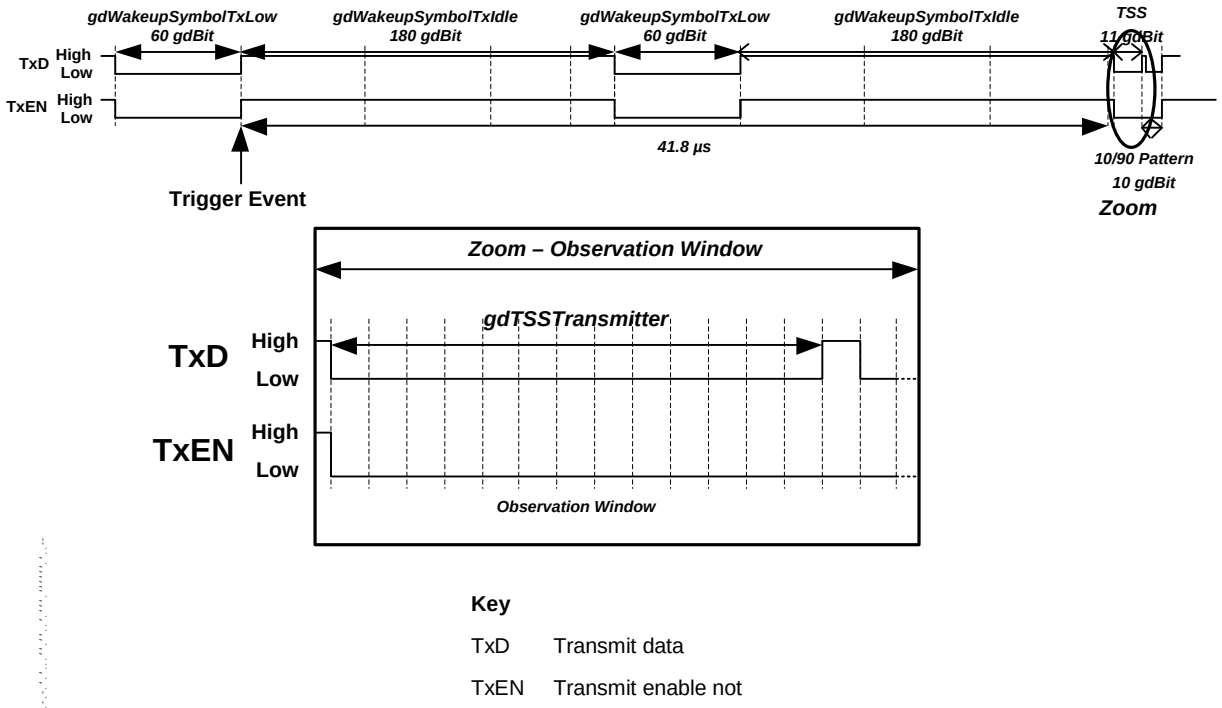
— Observation Window: 0,75 µs.

When this observation window is used in matrix E (see 10.2.10), a repetition may be used delayed according to the start acquisition point 2.

ISO 17458-4 shows the measurement descriptions of the parameters [*dStarDelay10*, *dStarDelay01*].

10.2.4.2 Parameter *dStarTSSLengthChange*

Figure 62 depicts the observation point for the analysis of the Active Star truncation.



Key

TxD	Transmit data
TxEN	Transmit enable not

Figure 62 — Observation point for the analysis of the Active Star truncation

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point 1: 41,8 µs after the trigger event.

— Start acquisition point 2: 63,9 µs after the trigger event.

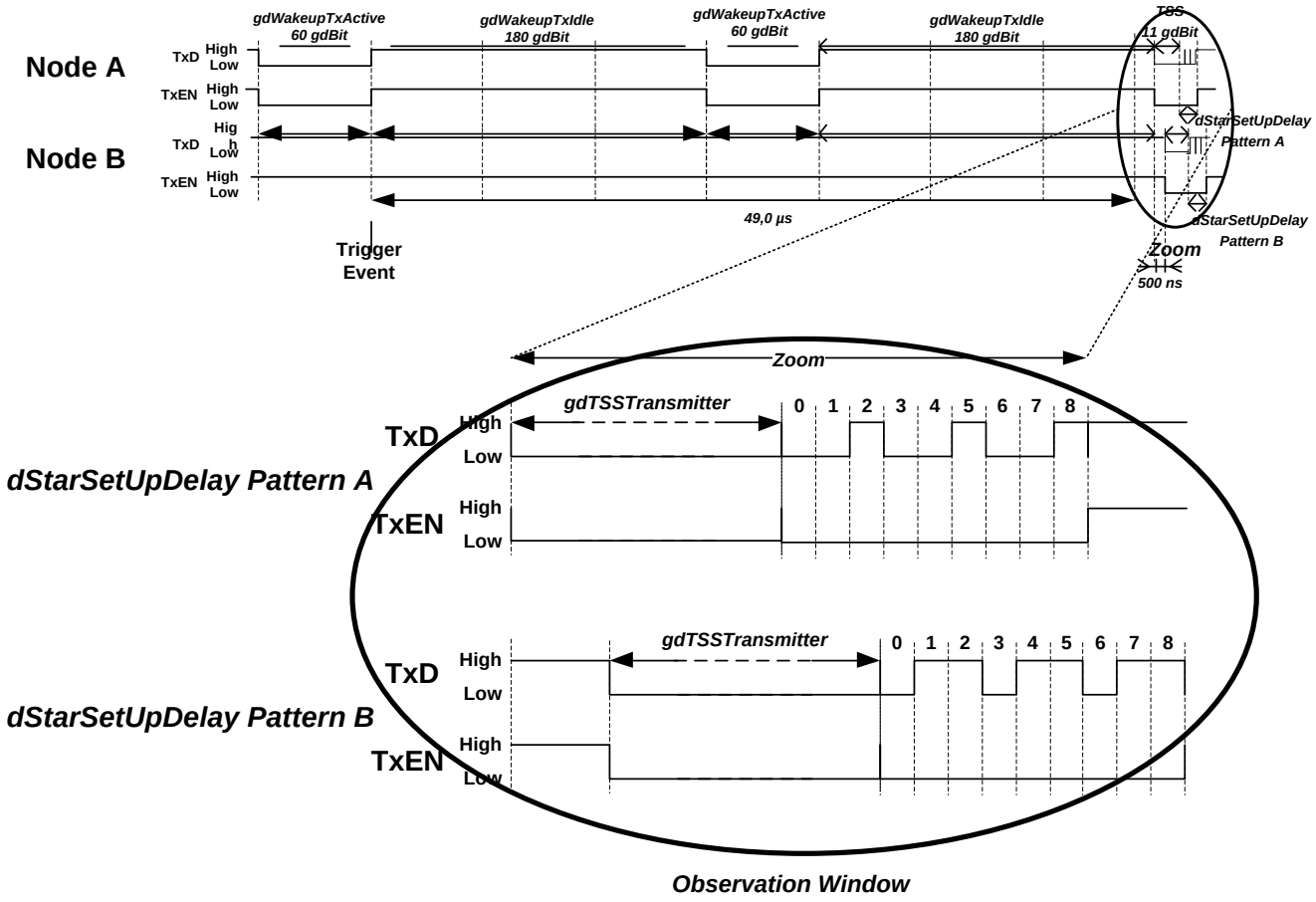
— Observation Window: 1,75 µs.

When this observation window is used in matrix E (see 10.2.10), a repetition may be used delayed according to the start acquisition point 2.

ISO 17458-4 shows the measurement description of the parameter *dStarTSSLengthChange*.

10.2.4.3 Parameter *dStarSetUpDelay*

Figure 63 depicts the observation point for the analysis of the Active Star setup delay.



Key

TxD	Transmit data
TxEN	Transmit enable not

Figure 63 — Observation point for the analysis of the Active Star setup delay

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point: 41 µs after the trigger event.

— Observation Window: 4,2 µs.

ISO 17458-4 shows the measurement description of the parameter *dStarSetUpDelay*.

10.2.4.4 Parameter *dStarWakeupReaction* after RWU

This observation window is to verify the bus state change from *Idle_LP* to *Idle* after detection of a remote wakeup event.

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point: 0 µs after the trigger event.

— Observation Window: 73 µs + 1 µs security.

10.2.4.5 Parameter *dStarWakeupReaction* before RWU

This observation window is to verify the bus state *Idle_LP* before detection of a remote wakeup event.

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point: 0 µs after the trigger event.

— Observation Window: 25 µs.

10.2.4.6 Parameter *dStarGoToSleep*

This observation window is to verify the bus state stay in *Idle_LP* while the branch is in *Branch_LowPower* state or change from *Idle* to *Idle_LP*, i.e. change the branch to *Branch_LowPower* state when the Active Star is in *AS_Normal* for longer than *dStarGoToSleep* and the branches are not in *Branch_Transmit* or *Branch_Receive* state.

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point: 0 µs after the trigger event.

— Observation Window: 6 400 ms + 100 ms.

10.2.4.7 Bus states

This observation window is to verify the bus states of the branches of the Active Star, i.e. *Idle, Data_1* and *Data_0*.

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point: 0 µs after the trigger event.

— Observation Window: 5 µs.

10.2.4.8 Parameter *dBranchRxActiveMax*

This observation window is to verify the branch noise detection time *dBranchRxActiveMax*.

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point: 0 µs after the trigger event.

— Observation Window: 2 600 µs.

10.2.4.9 Dynamic low battery – *AS_Sleep*

This observation window is to verify the bus state of the branches of the Active Star during the dynamic low battery pulse. All branches shall be in *Idle_LP* state.

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point: 0 s after the trigger event.

— Observation Window: 10,2 s (max duration of low battery voltage pulse).

10.2.4.10 Parameter *dStarWakeupReaction$_{local}$* after LWU

This observation window is to verify the bus state change from *Idle_LP* to *Idle* after detection of a local wakeup event.

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point: 0 µs after the trigger event.

— Observation Window: 601 µs (100 µs + 500 µs + 1 µs)

10.2.4.11 Verification of bus in *idle* state (long)

The bus is verified to be in or *Idle_LP* state at the Active Star.

— Trigger event: first negative edge of external trigger signal.

— Start acquisition point: 0 µs after the trigger event.

— Observation Window: 1,2 ms.

The absolute differential voltage |*uBus*| shall not exceed 30 mV (*uStarTx$_{idle}$*) and/or *uBP* and *uBM* of the observed branches shall be within a voltage level between -200 mV and +200 mV

10.2.5 Operation modes of the AS

The AS has the following operation modes:

— *AS_Normal*: receive/transmit possible, transition to *AS_Sleep* and *AS_Standby* possible.

— *AS_Sleep*: receive/transmit NOT possible, transition to *AS_Standby* possible by wakeup.

— *AS_Standby*: receive/transmit NOT possible, transition to *AS_Normal* possible due to no undervoltage on supply and APM flag is set.

The AS performs autonomous power moding while the autonomous power moding flag (APM flag) is set. By default the APM flag is been set during power on of the Active Star (also set by undervoltage V_{IO} and $V_{StarSupply}$ and reception of a wakeup). The Active Star never resets this flag on its own but can be reset if an Active Star – host interface is implemented (see clause 12).

The Active Star reaches the operation modes by the conditions listed in Table 352.

Table 352 — Conditions of the Active Star operation modes

Operation mode	Condition
AS_Normal	No undervoltage on $uV_{StarSupply}$ and APM flag is set
AS_Sleep	Expiration of *dStarGoToSleep* timeout while APM flag is set
AS_Standby	Undervoltage condition $uV_{StarSupply}$ Local or remote wakeup Power on, $uV_{StarSupply}$ above power on threshold
AS_Off	Power off, $uV_{StarSupply}$ below power on threshold (transition can start from any other operation mode)

10.2.6 Power supplies

10.2.6.1 The used power supplies of the Active Star

— The $V_{StarSupply}$ is the power supply of the Active Star. The datasheet of the IUT shall state what supply is. It may depend on V_{BAT}, V_{CC} or on both.

  — The V_{CC} supply input of the AS is a feature of the optional functional class “Active Star – internal voltage regulator” and the Functional class “Active star – voltage regulator control”. The V_{CC} input of the IUT is supplied with different voltage levels:
  V_{CC}= $V_{CCUndervoltage}$, +5,0 V

  — The VBAT input of the AS is a feature of the optional Functional class “Active star – internal voltage regulator” and the Functional class “Active star – voltage regulator control”. The VBAT input of the IUT is supplied with different voltage levels:
  V_{BAT}= (default), +7,0 V, +5,5 V, $V_{BATUndervoltage}$.

— In case of undervoltage at $V_{StarSupply}$, $V_{StarSupply}$ shall be set to the product specific supply undervoltage detection threshold that depends on implementation, and might have product specific effects to the levels of V_{BAT} and/or V_{CC} (in case the $V_{StarSupply}$ is derived from them). Due to that, all available supplies shall be set to undervoltage. The datasheet of an AS shall state the exact derivation of $V_{StarSupply}$.

— The V_{IO} supply input of the AS is a feature of the optional functional class “Active Star – logic level adaptation”. It may be connected to the IUT with different voltages, depending on implementation: V_{IO}= (depending on implementation), $V_{IOUndervoltage}$.

10.2.6.2 The power supply configuration of all nodes

— In case that V_{BAT} and V_{CC} are both implemented:

  — V_{CC} power supply of all nodes: +5,0 V

  — V_{BAT} power supply of all nodes: (default)

— In case that only V_{CC} is implemented:

  — V_{CC} power supply of all nodes: +5,0 V

— In case that only V_{BAT} is implemented:

— V_{BAT} power supply of all nodes: (default)

— In case that V_{IO} is implemented:

— V_{IO} reference voltage of all nodes: (depending on implementation)

10.2.7 Stress

— The ground shift is located as shown in Figure 14.

— The low battery affects the Active Star only.

NOTE The common nodes including their Bus Drivers are not stressed at all in Active Star test cases. All nodes are always supplied with all implemented supply voltages and not stressed by low battery or ground shift.

10.2.8 Failures

Failures of the AS are also described in 7.6.

10.2.9 Optional features

10.2.9.1 General

The features stated in the following subclauses are optional as specified in ISO 17458-4 and shall be tested in the test cases if available in the IUT:

10.2.9.2 Functional class “Active Star – voltage regulator control”

This functional class requires the following optional features to be implemented in coexistence:

— Signal INH1

— Power supply input V_{BAT}

— Power supply input V_{CC}

— Active Star – wake interface (optional within this functional class)

10.2.9.3 Functional class “Active Star – internal voltage regulator”

This functional class requires the following optional features to be implemented in coexistence:

— Power supply input V_{BAT}

— Signal INH1 (optional within this functional class)

— Active Star – wake interface (optional within this functional class)

This functional class requires that no V_{CC} supply input is present.

10.2.9.4 Functional class “Active Star – logic level adaptation”

This class requires the implementation of a logic level-shift interface and that the thresholds of all digital inputs are controlled by this voltage as well as all digital outputs are related to this level.

10.2.9.5 Functional class “Active Star increased voltage amplitude transmitter”

This class requires the shift of the minimum of $uStarTx_{Active}$ to a voltage of 900 mV

10.2.10 Definition of communication

10.2.10.1 Matrix C

Some test instances need only 2 transmitters as depicted in Figure 64.

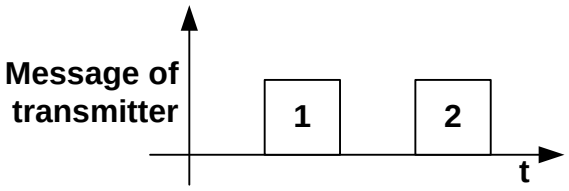


Figure 64 — Communication matrix C

Delay between the messages: 500 ns. The second transmitter (node 2) starts transmission only 500 ns after the first transmitter (node 1). So, the transmission of node 2 shall reach the Active Star slightly later than 500 ns after the transmission of node 1, because the propagation delay between node 2 to the Active Star (3,5 m) is greater than between node 1 and the Active Star (1 m).

10.2.10.2 Matrix E

Some test cases need a matrix for the passive networks as depicted in Figure 65.

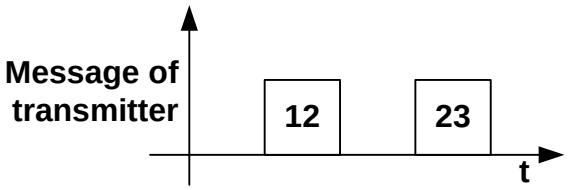


Figure 65 — Communication matrix E

Pause between the messages: 20 µs

10.2.10.3 Single node

In some test cases only one transmitter is required; this is either node 1, 2 or 11.

10.2.10.4 Node 1 and 2 as transmitter

In some test cases node 1 and 2 as transmitter are required.

10.2.10.5 Node 23 as transmitter

In this communication node 23 is the transmitter.

10.2.11 Standard preamble

The standard preamble shall be executed as follows:

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure state.

e) TxEN and TxD of all nodes shall be in logical HIGH state, i.e. the Bus Drivers shall signal *Idle* on the bus.

f) In case a BGE signal is available, this signal shall be in logical HIGH state at all nodes and the Active Star.

g) In case of a WAKE pin this signal shall be in logical HIGH state.

h) Stimulate Bus Drivers of all nodes via host commands to enter *BD_Normal*.

i) Make sure that the Active Star is in *AS_Normal* mode when this preamble is left and the test execution is entered, e.g. by switching on the power supply of the Active Star just before the end of the preamble.

10.2.12 Sleep preamble

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure state.

e) TxEN and TxD of all nodes shall be in logical HIGH state, i.e. the Bus Drivers shall signal *Idle* on the bus.

f) In case a BGE signal is available, this signal shall be in logical HIGH state at all nodes and the Active Star.

g) In case of a WAKE pin this signal shall be in logical HIGH state.

h) Stimulate Bus Drivers of all nodes via host commands to enter *BD_Normal*.

i) Wait 6 400 ms to make sure that the AS enters *AS_Sleep*.

10.2.13 Standard postamble

a) Set ground shift to 0 V.

b) Reset failures.

c) Switch off all power supplies.

10.3 Static test cases

The motivation of static test cases is to check the availability and the boundaries in the data sheet of the IUT (topology independent check).

Every parameter shall be part of the data sheet and fulfill the specified boundaries. If at least one parameter does not pass this test, the result of the whole conformance test is failed.

Table 353 defines the static test cases for Active Stars.

Table 353 – Static test cases for Active Stars

Index	Parameter	SOVS Brace	Description	Min	Max	Unit
1.	*dBusTx01*	Communication. Signal Shape	Rise time differential bus voltage (20 % → 80 %) [a]	6	18,75	ns
2.	*dBusTx10*	Communication. Signal Shape	Fall time differential bus voltage (80 % → 20 %) [a]	6	18,75	ns
3.	$uStarTx_{active}$	Communication. Signal Shape	Absolute value of *uBus*, while sending [b, c]	600	2 000	mV
4.	$uStarTx_{idle}$	Communication. Signal Shape	Absolute value of *uBus* voltage while *Idle* [b]	0	30	mV
5.	*dBranchRx ActiveMax*	Communication.Timing. Active Star	Noise detection time	650	2 600	µs
6.	R_{CM1}, R_{CM2}	Environment	Common mode input resistance	10	40	kΩ
7.	*uCM*	Environment. Ground shift	Common mode voltage range that does not disturb the receive function [d, e]	-10	+15	V
8.	$uStarUVV_{BAT}$	Power Supply. Active Star. Undervoltage V_{BAT}	V_{BAT} undervoltage detection threshold	4	5,5	V
9.	$uStarUVV_{CC}$	Power Supply. Active Star. Undervoltage V_{CC}	V_{CC} undervoltage detection threshold	4	—	V
10.	$dStarUVV_{CC}$	Power Supply. Active Star. Undervoltage V_{CC}	V_{CC} undervoltage detection time	—	1 000	ms
11.	iBP_{Leak}	Mode.Active Star. Off	Absolute leakage current, when in *AS_Off* [f]	—	25	µA
12.	iBM_{Leak}	Mode.Active Star. Off	Absolute leakage current, when in *AS_Off* [f]	—	25	µA
13.	$iBM_{GNDShortMax}$	Failure. Short-circuit.BM	Maximum output current when shorted to GND	—	60	mA
14.	$iBP_{GNDShortMax}$	Failure. Short-circuit.BP	Maximum output current when shorted to GND	—	60	mA
15.	$iBM_{BAT48ShortMax}$	Failure. Short-circuit.BM	Maximum output current when shorted to V_{BAT} =+48 V [g]	—	72	mA
16.	$iBP_{BAT48ShortMax}$	Failure. Short-circuit.BP	Maximum output current when shorted	—	72	mA

Index	Parameter	SOVS Brace	Description	Min	Max	Unit
			to V_{BAT} =+48 V [g]			
17.	*$iBM_{BAT27ShortMax}$*	Failure. Short-circuit.BM	Maximum output current when shorted to V_{BAT} =+27 V	—	60	mA
18.	*$iBP_{BAT27ShortMax}$*	Failure. Short-circuit.BP	Maximum output current when shorted to V_{BAT} =+27 V	—	60	mA
19.	Functional Class ”Active Star – Bus Guardian interface”	Functional Class	Checks the complete implementation of all specified options	—	—	—
20.	*dStarDelay10*	Communication.Delay	Propagation delay through an Active Star	—	150	ns
21.	*dStarDelay01*	Communication.Delay	Propagation delay through an Active Star	—	150	ns
22.	*dStarAsym*	Communication.Delay	Asymmetric propagation delay for monolithic devices [h]	0	8	ns
23.	*dStarAsym2*	Communication.Delay	Asymmetric propagation delay for non-monolithic devices [h]	0	10	ns
24.	*dStarSetUp Delay*	Communication.Delay	Set up delay	—	500	ns
25.	*dStarGoTo Sleep*	Mode.Active Star. Low Power	Go-to-Sleep timeout	640	6 400	ms
26.	*dStarWakeup ReactionTime*	Mode.Active Star. Low Power	Active Star wakeup reaction time	—	70	µs
27.	Device qualification according to [13]	—	Checks the existence of this qualification in the datasheet	—	—	—
28.	*T_{AMB_Class0}*	Environment	Ambient temperature for class 0 [e, i]	-40	+150	°C
29.	*T_{AMB_Class1}*	Environment	Ambient temperature for class 1 [e, i]	-40	+125	°C
30.	*T_{AMB_Class2}*	Environment	Ambient temperature for class 2 [e, i]	-40	+105	°C
31.	*T_{AMB_Class3}*	Environment	Ambient temperature for class 3 [e, i]	-40	+85	°C
32.	*$iBM_{-5VshortMax}$*	Failure. Short-circuit.BM	Maximum output current when shorted to V_{BAT} = -5 V	—	60	mA
33.	*$iBP_{-5VshortMax}$*	Failure. Short-circuit.BP	Maximum output current when shorted to V_{BAT} = -5 V	—	60	mA
34.	Functional Class	Functional Class	Checks the complete implementation of all	—	—	—

Index	Parameter	SOVS Brace	Description	Min	Max	Unit
	”Active Star – Voltage regulator control”		specified options			
35.	Functional Class ”Active Star – Internal voltage regulator”	Functional Class	Checks the complete implementation of all specified options	—	—	—
36.	$iBM_{BPShortMax}$	Failure. Short-circuit.BM	Maximum output current when BM shorted BP	—	60	mA
37.	$iBP_{BMShortMax}$	Failure. Short-circuit.BP	Maximum output current when BP shorted BM	—	60	mA
38.	$iBM_{BAT60ShortMax}$	Failure. Short-circuit.BM	Maximum output current when shorted to V_{BAT} =+60 V [g, j]	—	90	mA
39.	$iBP_{BAT60ShortMax}$	Failure. Short-circuit.BP	Maximum output current when shorted to V_{BAT} =+60 V [g, j]	—	90	mA
40.	*uBias* – Non Low Power	Mode.Active Star. Normal	Voltage at BP & BM during bus state *Idle* [k, l]	1 800	3 200	mV
41.	*uBias* – Low Power	Mode.Active Star. Low Power	Voltage at BP & BM during bus state *Idle_LP* [k, l, m]	-200	+200	mV
42.	$dStarUVV_{BAT}$	Power Supply. Active Star. Undervoltage V_{BAT}	Reaction time for V_{BAT} undervoltage detection	—	1 000	ms
43.	$uStarUVV_{IO}$	Power Supply. Active Star. Undervoltage V_{IO}	Transition to low power when V_{IO} voltage falls below product specific threshold	2	—	V
44.	$dStarUVV_{IO}$	Power Supply. Active Star. Undervoltage V_{IO}	Reaction time for V_{IO} undervoltage detection	—	1 000	ms
45.	$uINH1_{Not\_Sleep}$	Communication. Threshold	*Voltage on inhibit pin, when signaling Not_Sleep at 200 µA load, uVBAT > 5,5 V*	*uVBAT* – 1 V	—	V
46.	$iINH1_{Leak}$	Mode.Active Star. Low Power	*Absolute leakage current while signaling Sleep, uVBAT > 5,5 V* [n]	—	10	µA
47.	*dStarTSS LengthChange*	Communication Truncation	*Frame TSS length change* caused *by Active Star (= $dTSS_B$ – $dTSS_A$)*	-450	0	ns
48.	*dStarFES1 LengthChange*	Communication Truncation	*Prolongation of last bit of a frame (=$dFES1_B$ – $dFES1_A$)*	0	450	ns

Index	Parameter	SOVS Brace	Description	Min	Max	Unit
49.	$dStarUVV_{Supply}$	Power Supply. Active Star. Undervoltage $V_{StarSupply}$	*Supply undervoltage reaction time*	—	1	ms
50.	$dStarRV_{Supply}$	Power Supply. Active Star. Undervoltage $V_{StarSupply}$	Supply undervoltage recovery time	—	10	ms
51.	$uStarUVV_{Supply}$	Power Supply. Active Star. Undervoltage $V_{StarSupply}$	Supply undervoltage detection threshold	4	—	V
52.	$dStarRV_{BAT}$	Power Supply. Active Star. Undervoltage V_{BAT}	V_{BAT} Undervoltage recovery time for Active Star	—	10	ms
53.	$dStarRV_{CC}$	Power Supply. Active Star. Undervoltage V_{CC}	V_{CC} Undervoltage recovery time for Active Star	—	10	ms
54.	$dStarRV_{IO}$	Power Supply. Active Star. Undervoltage V_{IO}	V_{IO} Undervoltage recovery time for Active Star	—	10	ms
55.	$dWU_{Interrupt}$	Mode.Active Star. Low Power.Wakeup	Acceptance timeout for interruptions	0,13 [o]	1	µs
56.	$dWU_{0Detect}$	Mode.Active Star. Low Power.Wakeup	Time for detection of a *Data_0* phase in WU pattern	1	4	µs
57.	$dWU_{IdleDetect}$	Mode.Active Star. Low Power.Wakeup	Time for detection of an *Idle* phase in WU pattern	1	4	µs
58.	$dWU_{Timeout}$	Mode.Active Star. Low Power.Wakeup	Acceptance timeout for WU pattern recognition	48	140	µs
59.	*dStarWake PulseFilter*	Mode.Active Star. Low Power.Wakeup	Duration of a valid wake pulse at local WAKE pin	1	500	µs
60.	$iBP_{LeakGND}$	Failure. Loss.GND.IUT	Absolute leakage current in case of loss of GND [p]	—	1 600	µA
61.	$iBM_{LeakGND}$	Failure. Loss.GND.IUT	Absolute leakage current in case of loss of GND [p]	—	1 600	µA
62.	$dStarWakeup Reaction_{local}$	Mode.Active Star. Low Power.Wakeup	Active Star reaction time on a local wakeup event	—	100	µs
63.	*dStarSymbol LengthChange*	Communication Truncation	Symbol length change (only static portion) = $dSymbol_B - dSymbol_A$	-300	450	ns
64.	Functional Class ”Active Star – logic level adaption”	Functional Class	Checks the complete implementation of all specified options	—	—	—

Index	Parameter	SOVS Brace	Description	Min	Max	Unit
65.	Functional Class ”Increased voltage amplitude transmitter”	Functional Class	Checks the complete implementation of all specified options	—	—	—
66.	*uESD$_{EXT}$*	Environment	ESD protection on pins that lead to ECU terminals [q]	6	—	kV
67.	*uESD$_{INT}$*	Environment	ESD on all other pins	2	—	kV
68.	*uESD$_{IEC}$*	Environment	ESD protection on BP and BM	6	—	kV
69.	*uV$_{BAT-WAKE}$*	Power Supply	Minimum battery voltage required for wakeup detector (local and remote) operation in case that V_{CC} is implemented	—	7	V
70.	*dBusTxai*	Communication. Signal Shape	Transition time active → idle [r]	—	30	ns
71.	*dBusTxia*	Communication. Signal Shape	Transition time idle → active [r]	—	30	ns
72.	Operation modes in case of VStarSupply = nominal, $V_{BAT} \geq 5{,}5$ V and V_{CC} = nominal (if implemented)	—	*The Active Star shall be able to operate in all operation modes (in case that V_{CC} is implemented, wakeup detection is not mandatory)*	—	—	—
73.	Operation modes in case of VStarSupply = nominal, $V_{BAT} \geq 7$ V and V_{CC} = nominal	—	*The Active Star shall be able to operate in all operation modes (wakeup detection mandatory)*	—	—	—
74.	*uV$_{BAT-WAKE}$*	Power Supply	Minimum battery voltage required for wakeup detector (local and remote) operation in case that V_{CC} is not implemented	—	5,5	V
75.	*dBusTxDif*	Communication. Signal Shape	*Difference between differential rise and all time | dBusTx10 - dBusTx01 |*	—	3	ns
76.	*R$_{StarTransmitter}$*	Simulation	*Active Star - Bus* interface *simulation*	product specific	product specific	—

Index	Parameter	SOVS Brace	Description	Min	Max	Unit
			resistor			
77.	*dStarSymbol EndLength Change*	Communication.Truncation	*Prolongation of symbol at symbol end*	0	450	ns

[a] Load on BP/BM: 40 Ω || 100 pF.

[b] Load on BP/BM: 40..55 Ω || 100 pF.

[c] In case the functional class “Bus Driver increased voltage amplitude transmitter” or the functional class “Active Star increased voltage amplitude transmitter” is implemented, the minimum of *uBDTxActive* or *uStarTxAcive* shall be shifted to 900 mV.

[d] *uCM* = (*uBP* + *uBM*) / 2. To be tested on a receiving Bus Driver with a sending Bus Driver that has a ground offset voltage in the range of [-12,5 V – +12,5 V] and sends a 50/50 pattern.

[e] The device shall meet at least the range as given in ISO 0 0000-4, but can be better than the minimum and maximum values.

[f] Test conditions: *uBP* = *uBM* = 5 V, all other pins connected to GND. GND pin connected directly to 0 V.

[g] These limitations are only valid for devices that are meant to be used in “42 V board net” systems.

[h] *dStarAsym* = |*dStarDelay10* – *dStarDelay01*|, for *uBus* > 400 mV and 4 400 ns > *dBit* at TP14 > 80 ns.

[i] At least one of the classes shall be implemented.

[j] 400 ms originated from load dump conditions.

[k] Prerequisite is that the Bus Driver is connected to GND and *uVCC* = 5 V (if applicable) and *uVBAT* ≥ 7 V (if applicable).

[l] Load on BP/BM: 40 Ω – 55 Ω || 100 pF. Nominal voltage of *uBias* is 2 500 mV in normal mode and 0 mV in low power modes.

[m] The internal resistance of the *uBias* voltage source in low power modes can be significantly higher than in non-low power modes.

[n] Leakage current can be tested by applying a 100 kΩ to INH1 and checking for |*uINH1*| < 1 V.

[o] The minimum value is only guaranteed, when the phase that is interrupted was continuously present for at least 870 ns.

[p] Test conditions: *uBP* = *uBM* = 0 V, all other pins connected via 0 Ω to 16 V.

[q] Typically: BM, BP, WAKE and V_{BAT}.

[r] Load on BP/BM: 40 Ω || 100 pF.

10.4 Test cases

10.4.1 Communication.Delay.dStarDelay10

10.4.1.1 Communication delay *dStarDelay10*

Table 354 defines the test case for communication delay dStarDelay10.

Table 354 — Test case for communication delay *dStarDelay10*

Name	**Communication delay *dStarDelay10***
Test purpose	This test checks the FlexRay parameter *dStarDelay10* (propagation delay of a negative edge through the active star) in the test system while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. e) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one

Name	Communication delay *dStarDelay10*
	10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay10* ≤ 150ns. — in case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 355 defines the test instances for communication delay dStarDelay10 test case defined in Table 354.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 355 — Test instances for communication delay *dStarDelay10*

Instance		1	2	3	4
Purpose	**Stress**	none	ground shift at AS	ground shift at node	low battery
	Precondition	—	—	—	AS_VRC or AS_IVR impl.
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	+5,0 V at N23	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

10.4.2 Communication.Delay.dStarDelay01

10.4.2.1 Communication delay *dStarDelay01*

Table 356 defines the test case for communication delay dStarDelay01.

Table 356 — Test case for communication delay *dStarDelay01*

Name	**Communication delay *dStarDelay01***
Test purpose	This test checks the FlexRay parameter *dStarDelay01* (propagation delay of a positive edge through the active star) in the test system while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. e) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.

Name	Communication delay *dStarDelay01*
Pass criteria	— *dStarDelay01* ≤ 150ns. — in case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 357 defines the test instances for communication delay dStarDelay01 test case defined in Table 356.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 357 — Test instances for communication delay *dStarDelay01*

Instance		1	2	3	4
Purpose	**Stress**	none	ground shift at AS	ground shift at node	low battery
	Precondition	—	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	-+5,0 V at N23	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

10.4.3 Communication.Delay.dStarSetUpDelay

10.4.3.1 Communication delay *dStarSetUpDelay*

Table 358 defines the test case for communication delay *dStarSetUpDelay*.

Table 358 — Test case for communication delay *dStarSetUpDelay*

Name	**Communication delay *dStarSetUpDelay***
Test purpose	This test checks the FlexRay parameter *dStarSetUpDelay* while no stress condition is present. This test case verifies that a second incoming data stream reaching the active star slightly after *dStarSetUpDelay* is ignored by the active star.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix C.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of the transmitting nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of the transmitting nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all receiving nodes in the branches B2 and B4 of the active star. d) Observe and acquire *uBus* at *TPAS4_B1* of the receiving branch according to the observation window described in 10.2.4.3. e) Observe and acquire *uBus* at *TPAS1_B3* of the transmitting branch according to the observation window described in 10.2.4.3. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all receiving nodes in the branches B2 and B4 of the active star. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. h) Stimulate the bus driver of the first transmitting node according to the sequence

Name	Communication delay *dStarSetUpDelay*
	described on matrix C at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. i) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix C at *TP_Nx_TxD* and *TP_Nx_TxEN* by the Star Setup Delay 1[a] pattern. j) Stimulate the bus driver of the second transmitting node according to the sequence described on matrix C at *TP_Nx_TxD* and *TP_Nx_TxEN* by the Star Setup Delay 2 pattern. Start stimulation delayed by 500 ns to the first transmitting node.
Postamble	Standard postamble.
Pass criteria	The pattern sent by the second transmitting node shall not be retransmitted by the active star because the incoming data stream shall be ignored after *dStarSetUpDelay*. — Branch 2 and 4 shall retransmit the pattern transmitted by node 1, only. That means, that the RxD signal of nodes 11, 12, 13, 14, 21, 22, 23 and 24 shall contain the pattern applied to node 1. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.
a Test signals “Star Setup Delay 1 and 2" are specified in 10.2.3.2.	

Table 359 defines the test instances for communication delay *dStarSetUpDelay* test case defined in Table 358.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 359 — Test instances for communication delay *dStarSetUpDelay*

Instance		1	2	3	4
Purpose	**Stress**	none	ground shift at AS	ground shift at node	low battery
	Precondition	—	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	+5,0 V at N23	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

10.4.4 Communication.Truncation.dFrameTSSLengthChange$_{M,N}$

10.4.4.1 Communication truncation *dFrameTSSLengthChange$_{M,N}$*

Table 360 defines the test case for communication truncation dFrameTSSLengthChange$_{M,N}$.

Table 360 — Test case for communication truncation *dFrameTSSLengthChange$_{M,N}$*

Name	**Communication truncation *dFrameTSSLengthChange$_{M,N}$***
Test purpose	This test checks the overall channel truncation while no stress condition is present according to the sum of all allowed truncation effects specified in ISO 17458-4. This test shall verify, that only the transmission start sequence is affected by truncation effects and that a protocol controller would decode the following data properly.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test).
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.

Name	Communication truncation *dFrameTSSLengthChange$_{M,N}$*
Postamble	Standard postamble.
Pass criteria	— The width of all received TSS patterns (logical LOW phase from the falling edge of the received TSS pattern to the rising edge of the first bit of the following 10/90 pattern) in *uRxD* of all nodes shall be at least 1 100 ns - |-850 ns| and is not lengthened more than 50 ns, i.e. the channel truncation shall be within the allowed range. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 361 defines the test instances for communication truncation dFrameTSSLengthChangeM,N test case defined in Table 360.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 361 — Test instances for communication truncation *dFrameTSSLengthChangeM,N*

Instance		1	2	3	4
Purpose	**Stress**	none	ground shift at AS	ground shift at node	low battery
	Precondition	—	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	+5,0 V at N23	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

10.4.5 Communication.Truncation.dStarTSSLengthChange

10.4.5.1 Communication truncation *dStarTSSLengthChange*

Table 362 defines the test case for communication truncation dStarTSSLengthChange.

Table 362 — Test case for communication truncation *dStarTSSLengthChange*

Name	**Communication truncation *dStarTSSLengthChange***
Test purpose	This test checks the FlexRay parameter *dStarTSSLengthChange* while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the truncation is measured twice for each transmitted data — 1 st pass (receiving branch 4, node 12 as transmitter) according to 10.2.4.2 (41,8 µs, N12) — 2 nd pass (receiving branch 2, node 23 as transmitter) according to 10.2.4.2 (41,8 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.2. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.2. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. e) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern.

Name	Communication truncation *dStarTSSLengthChange*
Postamble	Standard postamble.
Pass criteria	— 0 ns ≤ |*dStarTSSLengthChange*| ≤ |-450 ns|. — in case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 363 defines the test instances for communication truncation dStarTSSLengthChange test cased defined in Table 362.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 363 — Test instances for communication truncation *dStarTSSLengthChange*

Instance		1	2	3	4
Purpose	**Stress**	none	ground shift at AS	ground shift at node	low battery
	Precondition	—	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	+5,0 V at N23	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

10.4.6 Mode.Active Star.Normal

10.4.6.1 Operation mode change to *AS_Normal* in case of power on of $V_{StarSupply}$

Table 364 defines the test case for operation mode change to AS_Normal in case of power on of VStarSupply.

Table 364 — Test case for operation mode change to *AS_Normal* in case of power on of VStarSupply

Name	Operation mode change to *AS_Normal* in case of power on of VStarSupply
Test purpose	This test checks the ability of the IUT to change from *AS_Off* mode to *AS_Standby* to *AS_Normal* due to power on and autonomous power moding flag (APM flag) according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{CC} is implemented: external V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: external V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Disable outputs of power supplies of IUT in active star from where the supply is derivated.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 2. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 2. e) In case of an available INH signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Enable outputs of power supplies of IUT in active star from where the supply is derivated. g) Wait 100 µs + 10 ms for the active star to enter *AS_Normal.* h) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of all observed nodes shall contain the 50/50 pattern transmitted by node 2, i.e. the active

Name	Operation mode change to *AS_Normal* in case of power on of VStarSupply
	star shall enter *AS_Normal* mode within 10 ms after power on and retransmit the test patterns of node 2. — In case of an available INH signal *uINH1* shall be in logical HIGH state (*Not_Sleep)* after switching on the power supplies up to the end of the test execution.

Table 365 defines the test instances for operation mode change to AS_Normal in case of power on of VStarSupply test case defined in Table 364.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 365 — Test instances for operation mode change to *AS_Normal* in case of power on of VStarSupply

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

10.4.6.2 Operation mode change to *AS_Normal* in case of power on of $V_{StarSupply}$ (while undervoltage V_{IO})

Table 366 defines the test case for operation mode change to AS_Normal in case of power on of VStarSupply (while undervoltage V_{IO}).

Table 366 — Test case for operation mode change to *AS_Normal* in case of power on of VStarSupply (while undervoltage V_{IO})

Name	**Operation mode change to *AS_Normal* in case of power on of VStarSupply (while undervoltage V_{IO})**
Test purpose	This test checks the ability of the IUT to change from *AS_Off* mode to *AS_Standby* to *AS_Normal* due to power on and autonomous power moding flag (APM flag) according to ISO 17458-4 while undervoltage condition at V_{IO} is present. This test case is skipped if the Functional class "Active star – logic level adaptation" is not implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{CC} is implemented: external V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: external V_{BAT} power supply of active star: default. — External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Disable outputs of power supplies of IUT in active star from where the supply is derivated. — Set the external V_{IO} reference voltage of active star to $V_{IOUndervoltage}$. — Wait 1 000 ms for the active star to react on the undervoltage condition.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 2. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 2. e) In case of an available INH signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Enable outputs of power supplies of IUT in active star from where the supply is derivated. g) Wait 100 µs + 10 ms for the active star to enter *AS_Normal.* h) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS

Name	Operation mode change to *AS_Normal* in case of power on of VStarSupply (while undervoltage V_{IO})
	pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of all observed nodes shall contain the 50/50 pattern transmitted by node 2, i.e. the active star shall enter *AS_Normal* mode within 10 ms after power on and retransmit the test patterns of node 2. — In case of an available INH signal *uINH1* shall be in logical HIGH state (*Not_Sleep)* after switching on the power supplies up to the end of the test execution.

Table 367 defines the test instances for operation mode change to AS_Normal in case of power on of VStarSupply (while undervoltage V_{IO}) test case defined in Table 366.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 367 — Test instances for operation mode change to *AS_Normal* in case of power on of VStarSupply (while undervoltage V_{IO})

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

10.4.6.3 Active star remains in *AS_Normal* in case of undervoltage V_{IO}

Table 368 defines the test case for active star remains in AS_Normal in case of undervoltage V_{IO}.

Table 368 — Test case for active star remains in *AS_Normal* in case of undervoltage V_{IO}

Name	**Active star remains in *AS_Normal* in case of undervoltage V_{IO}**
Test purpose	This test checks the ability of the active star to remain in *AS_Normal* in case of undervoltage at V_{IO} while no stress condition is present. This test case is skipped if the Functional class "Active star – logic level adaptation" is not implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — external V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 2. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 2. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Set the external V_{IO} reference voltage of active star to $V_{IOUndervoltage}$. g) Wait 1 000 ms for the active star to react on the undervoltage condition. h) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence for longer than 1 100 ms. The bit duration in this test case shall be gdBit=25 µs, because the memory depth of the logic analyzer is much too small to acquire more than one second with a 100 ns bit time.

Name	Active star remains in *AS_Normal* in case of undervoltage V_{IO}
	The gap between the messages shall be 9,25 ms. i) Trigger the logic analyzer to start the observation synchronously with the stimulation of node 2.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of all observed nodes shall contain the 50/50 pattern transmitted by node 2, i.e. the active star shall remains in *AS_Normal* mode during the test execution. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state (*Not_Sleep*) after V_{IO} is switched to undervoltage up to the end of the test execution.

Table 369 defines the test instances for active star remains in AS_Normal in case of undervoltage V_{IO} test case defined in Table 368.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 369 — Test instances for active star remains in *AS_Normal* in case of undervoltage V_{IO}

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.6.4 Active star remains in *AS_Normal* while undervoltage at V_{BAT} (V_{CC} available)

Table 370 defines the test case for active star remains in AS_Normal while undervoltage at V_{BAT} (V_{CC} available).

Table 370 — Test case for active star remains in *AS_Normal* while undervoltage at V_{BAT} (V_{CC} available)

Name	Active star remains in *AS_Normal* while undervoltage at V_{BAT} (V_{CC} available)
Test purpose	This test checks the of the active star to remain in *AS_Normal* in case of undervoltage at V_{BAT} supply power if V_{CC} is still available according to ISO 17458-4 while no other stress condition is present and $V_{StarSupply}$ is constantly supplied within its normal operation range. This test case is skipped if — the Functional class “Active star – voltage regulator control” is not implemented — the Functional class “Active star – internal voltage regulator” is implemented and a V_{CC} supply input is not available.
Configuration	— Topology: as specified in previous configuration see 10.2. — External V_{BAT} power supply of the active star: default. — External V_{CC} power supply of the active star: +5,0 V. — In case that V_{IO} is implemented: External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 1, 2, 12 and 23. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 1, 2, 12 and 23. e) Set external V_{BAT} power supply of the active star to $V_{BATUndervoltage}$. f) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence for at least 1 000 ms to verify that communication is not disturbed even after the maximal undervoltage detection timeout ($dStarUVV_{BAT}$). The bit duration in this test case shall be *gdBit*=25 µs, because the memory depth of the logic analyzer is much too small to acquire 1 seconds with a 100 ns bit time. The gap between the messages shall be 9,25 ms.
Postamble	Standard postamble.
Pass criteria	This test case requires acquisition of at least 1 000 ms by the logic analyzer. A bit level resolution is not required. Adaptation of the thresholds for digital signals may be required.

Name	Active star remains in *AS_Normal* while undervoltage at V_{BAT} (V_{CC} available)
	uRxD of all observed nodes shall contain all logical 50/50 pattern sequences transmitted by node 2, i.e. the active star shall stay in *AS_Normal* mode and shall retransmit all patterns received on branch 3.

Table 371 defines the test instances for active star remains in AS_Normal while undervoltage at V_{BAT} (V_{CC} available) test case defined in Table 370.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 371 — Test instances for active star remains in *AS_Normal* while undervoltage at V_{BAT} (V_{CC} available)

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

10.4.7 Mode.Active Star.Normal.GoToSleep

10.4.7.1 Operation mode change from *AS_Normal* to *AS_Sleep* after dStarGoToSleep

Table 372 defines the test case for operation mode change from AS_Normal to AS_Sleep after dStarGoToSleep.

Table 372 — Test case for operation mode change from *AS_Normal* to *AS_Sleep* after *dStarGoToSleep*

Name	**Operation mode change from *AS_Normal* to *AS_Sleep* after *dStarGoToSleep***
Test purpose	This test checks the ability of the active star to go to *AS_Sleep* mode if all branches are in *Branch_Idle* for longer than *dStarGoToSleep* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of the nodes 21..24 (branch 2) and 11..14 (branch 4).
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.6. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.6. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.6. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.6. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.

Name	Operation mode change from *AS_Normal* to *AS_Sleep* after *dStarGoToSleep*
	g) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2. h) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2. The bit duration in this test case shall be *gdBit*=25 µs, because the memory depth of the logic analyzer is much too small to acquire 10 seconds with a 100 ns bit time. i) Wait 6 400 ms for the AS to enter *AS_Sleep*.
Postamble	Standard postamble.
Pass criteria	The period to observe is very long in this test case. But a bit level resolution is not required. The Go-To-Sleep timeout *dStarGoToSleep* shall be measured with an error of less than 1 %. The bit rate shall be chosen in that way that the oscilloscope is able to detect the retransmission of the AS, e.g. 50 ms. — For at least the first 640 ms after the transmission of node 2, *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle* state, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between 1 800 mV and 3 200 mV (*Idle*). — Between 640 ms and 6 400 ms after the transmission of node 2, *uBP* and *uBM* of branch 2 and 4 shall change to *Idle_LP* state, i.e. *uBP* and *uBM* of branch 2 and 4 shall change to a voltage level between -200 mV and +200 mV (*Idle_LP*). — In case of an available INH1 signal *uINH1* shall be initially in logical HIGH state for at least 640 ms. Between 640 ms and 6 400 ms after the start of the observation, *uINH1* shall change to logical LOW state.

Table 373 defines the test instances for operation mode change from AS_Normal to AS_Sleep after *dStarGoToSleep* test case defined in Table 372.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 373 — Test instances for operation mode change from *AS_Normal* to *AS_Sleep* after *dStarGoToSleep*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.8 Mode.Active Star.Normal.GoToSleep_Fail

10.4.8.1 Operation mode change to *AS_Sleep* after dStarGoToSleep (FailSilent)

Table 374 defines the test case for operation mode change to AS_Sleep after dStarGoToSleep (FailSilent).

Table 374 — Test case for operation mode change to *AS_Sleep* after *dStarGoToSleep* (FailSilent)

Name	Operation mode change to *AS_Sleep* after *dStarGoToSleep* (FailSilent)
Test purpose	This test checks the ability of the active star to go to *AS_Sleep* mode if one branch is in *Branch_FailSilent* and all other branches are in *Branch_Idle* for longer than *dStarGoToSleep* according to ISO 17458-4 while no stress condition is present. This test case is skipped if the Functional class “Active star – communication controller interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: none.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of the nodes 21..24 (branch 2), node 1 (branch 1) and node 2 (branch 3).
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.6. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.6. c) Observe and acquire *uBus* at *TPAS4_B4* of the receiving branch 4 according to the observation window described in 10.2.4.6. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. e) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1. Repeat this pattern for at least 6 400 ms+ 2 600 µs. f) Trigger the scope to start the observation synchronously with the beginning of the

Name	Operation mode change to *AS_Sleep* after *dStarGoToSleep* (FailSilent)
	babbling idiot stimuli. g) Trigger the logic analyzer to start the observation synchronously with the beginning of the babbling idiot stimuli.
Postamble	Standard postamble.
Pass criteria	The period to observe is very long in this test case. But a bit level resolution is not required. The Go-To-Sleep timeout *dStarGoToSleep* shall be measured with an error of less than 1 %. *uBP* and *uBM* of branch 2 indicate *Data_0* state initially, i.e. the active star retransmits the babbling idiot pattern before branch 4 enters *Branch_FailSilent*. Then, branch 2 enters *Idle* state. — Between 640 ms and 6 400 ms after branch 2 has entered *Idle* state, i.e. *uBP* and *uBM* of branch 2 are between 1 800 mV and 3 200 mV (*Idle*), *uBP* and *uBM* of branch 2 shall change to *Idle_LP* state, i.e. *uBP* and *uBM* of branch 2 shall change to a voltage level between -200 mV and +200 mV (*Idle_LP*). — In case of an available INH1 signal *uINH1* shall be initially in logical HIGH state for at least 640 ms + 650 µs. Between 640 ms + 650 µs and 6 400 ms + 2 600 µs after the start of the observation, *uINH1* shall change to logical LOW state.

Table 375 defines the test instances for operation mode change to AS_Sleep after dStarGoToSleep (FailSilent) test case defined in Table 374.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 375 — Test instances for operation mode change to *AS_Sleep* after *dStarGoToSleep* (FailSilent)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9 Mode.Active Star.Low Power.Sleep.Wakeup

10.4.9.1 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern

Table 376 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern.

Table 376 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern**
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of *dStarWakeupReactionTime* due to remote wakeup as specified in 9.1.3.1 and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present. This test case is skipped if the Functional class “Active star – communication controller interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern
	the observation window described in 10.2.4.4. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern as described in 9.1.3.1. g) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*. h) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern. i) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 104 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 31 µs after the beginning of the wakeup pattern and 104µs after the beginning of the wakeup pattern.

Table 377 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern test case defined in Table 376.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 377 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.2 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* (retransmission of wakeup symbols)

Table 378 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal (retransmission of wakeup symbols).

Table 378 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* (retransmission of wakeup symbols)

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* (retransmission of wakeup symbols)**
Test purpose	This test checks the ability of the active star to retransmit a sufficient number of received wakeup symbols during the operation mode transition from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	Sleep preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. b) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 1. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. e) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by 12 wakeup patterns as described in 9.1.3.1, i.e. a sequence of 24 wakeup symbols.
Postamble	Standard postamble.
Pass criteria	The verification of *uRxD* at *TP_Nx_RxD* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uRxD* of all observed nodes shall contain at least 19 wakeup symbols, i.e. the active star shall

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* (retransmission of wakeup symbols)
	enter *AS_Normal* latest 104 µs after the beginning of the first wakeup pattern and shall retransmit the 19 wakeup symbols transmitted by node 1. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. Then, *uINH1* shall change to logical HIGH state within 104 µs after the beginning of the first wakeup pattern.

Table 379 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal (retransmission of wakeup symbols) test case defined in Table 378.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 379 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* (retransmission of wakeup symbols)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.3 Ignore non suitable wakeup patterns (remain in *AS_Sleep*)

Table 380 defines the test case for ignore non suitable wakeup patterns (remain in AS_Sleep).

Table 380 — Test case for ignore non suitable wakeup patterns (remain in *AS_Sleep*)

Name	**Ignore non suitable wakeup patterns (remain in *AS_Sleep*)**
Test purpose	This test checks the ability of the IUT to ignore non suitable remote wakeup patterns with shortened idle phase and to remain in *AS_Sleep* mode according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. b) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. c) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. e) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. f) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the

Name	Ignore non suitable wakeup patterns (remain in *AS_Sleep*)
	AS. h) Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one non wakeup short idle phase pattern as specified in 9.1.3.8. i) Trigger the scope to start the observation synchronously with the first stimuli at *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	— *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* during the test execution, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). — In case of an available INH1 signal *uINH1* of the AS shall be in logical LOW state (*Sleep*) during the test execution, i.e. the AS shall remain in *AS_Sleep*.

Table 381 defines the test instances for ignore non suitable wakeup patterns (remain in AS_Sleep) test case defined in Table 380.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 381 — Test instances for ignore non suitable wakeup patterns (remain in *AS_Sleep*)

Instance		1	2	3
Purpose	**Stress**	—	—	—
	Precondition	—	—	—
Configuration	**Power supply**	—	—	—
	Ground shift	—	—	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		… Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one non wakeup short idle phase pattern as specified in 9.1.3.8. …	… Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one non wakeup short low phase pattern as specified in 9.1.3.9. …	… Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one non wakeup prolonged pattern as specified in 9.1.3.10. …
Pass criteria		—	—	—

10.4.9.4 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup

Table 382 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to alternative remote wakeup.

Table 382 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup**
Test purpose	This test checks the ability of the active star to wakeup after a wakeup reaction time of *dStarWakeupReactionTime* due to alternative remote wakeup as specified in 9.1.3.11 and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present. This test case is skipped if the Functional class “Active star – communication controller interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: V_{BAT} power supply of active star: default. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup
	active star. f) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one alternative wakeup pattern as described in 9.1.3.11. g) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*. h) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern. i) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 104 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. uINH1 shall change to logical HIGH state between 31 µs after the beginning of the wakeup pattern and 104 µs after the beginning of the wakeup pattern.

Table 383 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to alternative remote wakeup test case defined in Table 382.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 383 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.5 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse)

Table 384 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse).

Table 384 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse)

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse)**
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of $dStarWakeupReaction_{local}$ due to a negative local wakeup pulse and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the active star – wake interface is not implemented — neither the Functional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented — the Functional class “Active star – communication controller interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.10. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.10. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.10. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse)
	the observation window described in 10.2.4.10. e) Observe and acquire *uWAKE* at *TP_AS_WAKE* of the active star. f) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. g) Apply a negative wakeup pulse of 500 µs to the active star at *TP_AS_WAKE* according to *dStarWakePulseFilter* in ISO 17458-4. h) Wait 100 µs. i) Trigger the scope to start the observation 1 µs after the falling edge of *uWAKE* at *TP_AS_WAKE* of the active star. j) Trigger the logic analyzer to start the observation synchronously with the falling edge of *uWAKE* at *TP_AS_WAKE* of the active star.
Postamble	Standard postamble.
Pass criteria	The period to observe is very long in this test case. But a bit level resolution is not required. — *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* of branch 2 and 4 shall change to *Idle* state, i.e. *uBP* and *uBM* of branch 2 and 4 shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 100 µs + 500 µs after the occurrence of the local wakeup event. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event.

Table 385 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse) test case defined in Table 384.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 385 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.6 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse)

Table 386 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (positive pulse).

Table 386 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse)

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse)**
Test purpose	This test checks the ability of the active star to wakeup after a wakeup reaction time of $dStarWakeupReaction_{local}$ due to a positive local wakeup pulse and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented. — the active star – wake interface is not implemented — a positive local wakeup pulse is not supported by the IUT — the Functional class “Active star – communication controller interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.10. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.10.

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse)
	c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.10. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.10. e) Observe and acquire *uWAKE* at *TP_AS_WAKE* of the active star. f) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. g) Apply a positive wakeup pulse of 500 µs to the active star at *TP_AS_WAKE* according to *dStarWakePulseFilter* in ISO 17458-4. h) Wait 100 µs. i) Trigger the scope to start the observation 1 µs after the rising edge of *uWAKE* at *TP_AS_WAKE* of the active star. j) Trigger the logic analyzer to start the observation synchronously with the rising edge of *uWAKE* at *TP_AS_WAKE* of the active star.
Postamble	Standard postamble.
Pass criteria	The period to observe is very long in this test case. But a bit level resolution is not required. — *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* of branch 2 and 4 shall change to *Idle* state, i.e. *uBP* and *uBM* of branch 2 and 4 shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 100 µs + 500 µs after the occurrence of the local wakeup event — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event.

Table 387 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (positive pulse) test case defined in Table 386.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 387 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.7 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame

Table 388 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to wakeup frame.

Table 388 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of *dStarWakeupReactionTime* due to a wakeup frame payload as specified in 9.1.3.12 and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present. This test case is skipped if the Functional class "Active star – communication controller interface" is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star.

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame
	f) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup frame containing the payload as specified in 9.1.3.12. g) After the end of the wakeup frame wait at least 70 µs for the active star to enter *AS_Normal* via AS_Standby. h) Trigger the scope to start the observation 70 µs after the end of the wakeup frame; i.e. after the positive edge on *TP_N1_TxEN*. i) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate Idle, i.e. *uBP* and *uBM* of the observed branches shall be between 1800 mV and 3200 mV. — In case of an available INH1 signal *uINH1* shall be in logical LOW state (Sleep) before the negative edge on *TP_N1_TxEN*; i.e. the active star shall be in *AS_Sleep* mode initially. Then, latest 70 µs after the positive edge on *TP_N1_TxEN*, *uINH1* shall be in logical HIGH state (*Not_Sleep*).

Table 389 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to wakeup frame test case defined in Table 388.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 389 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.8 Detection of LWU (negative pulse) while undervoltage of V_{CC} and V_{IO}, V_{BAT} = +7,0 V

Table 390 defines the test case for detection of LWU (negative pulse) while undervoltage of V_{CC} and V_{IO}, V_{BAT} = +7,0 V.

Table 390 — Test case for detection of LWU (negative pulse) while undervoltage of V_{CC} and V_{IO}, V_{BAT} = +7,0 V

Name	Detection of LWU (negative pulse) while undervoltage of V_{CC} and V_{IO}, V_{BAT} = +7,0 V
Test purpose	This test checks the ability of the active star to detect a local wakeup event in case of undervoltage of V_{IO} and the V_{CC} power supply if V_{BAT} power supply is available and set to low battery voltage according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the Functional class “Active star – voltage regulator control” is not implemented — the Functional class “Active star – internal voltage regulator” is implemented — the active star – wake interface is not implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — V_{BAT} power supply of active star: +7,0 V. — External V_{CC} power supply of active star: +5,0 V. — External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches. — Set the external V_{CC} supply of the active star to VCCUndervoltage. — Set the external V_{IO} reference voltage of the active star to VIOUndervoltage. — Wait 1 000 ms (*dStarUVV$_{CC}$*) to let the active star detect the undervoltage condition.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.10. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.10. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.10. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.10.

Name	Detection of LWU (negative pulse) while undervoltage of V_{CC} and V_{IO}, V_{BAT} = +7,0 V
	e) Observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Apply a negative wakeup pulse of 500 µs to the active star at *TP_AS_WAKE* according to *dStarWakePulseFilter* in ISO 17458-4. g) Trigger the scope to start the observation 1 µs after the falling edge of *uWAKE* at *TP_AS_WAKE* of the active star. h) Trigger the logic analyzer to start the observation synchronously with the falling edge of *uWAKE* at *TP_AS_WAKE* of the active star. i) Wait 100 µs.
Postamble	Standard postamble.
Pass criteria	The period to observe is very long in this test case. But a bit level resolution is not required. The wakeup reaction time $dStarWakeupReaction_{local}$ shall be measured with an error of less than 1 %. Adaptation of the thresholds for digital signals may be required. — *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* of branch 2 and 4 shall change to *Idle* state, i.e. *uBP* and *uBM* of branch 2 and 4 shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 100 µs + 500 µs after the occurrence of the local wakeup event — *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event.

Table 391 defines the test instances for detection of LWU (negative pulse) while undervoltage of V_{CC} and V_{IO}, V_{BAT} = +7.0 V test case defined in Table 390.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 391 — Test instances for detection of LWU (negative pulse) while undervoltage of V_{CC} and V_{IO}, V_{BAT} = +7.0 V

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

10.4.9.9 Insufficient wakeup pulse (negative pulse, remain in *AS_Sleep*)

Table 392 defines the test case for insufficient wakeup pulse (negative pulse, remain in AS_Sleep).

Table 392 — Test case for insufficient wakeup pulse (negative pulse, remain in *AS_Sleep*)

Name	Insufficient wakeup pulse (negative pulse, remain in *AS_Sleep*)
Test purpose	This test checks the ability of the IUT to ignore spikes on the WAKE pin and to stay in *AS_Sleep* mode according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the active star – wake interface is not implemented — neither the Functional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.10. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.10. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.10. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.10. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the AS. f) Apply a negative wakeup pulse of 1 µs to the active star at *TP_AS_WAKE* according to

Name	Insufficient wakeup pulse (negative pulse, remain in *AS_Sleep*)
	dStarWakePulseFilter in ISO 17458-4. g) Trigger the scope to start the observation synchronously with the stimuli at *TP_AS_WAKE* of node the active star. h) Wait 100 µs.
Postamble	Standard postamble.
Pass criteria	— *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* during the test execution, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). — In case of an available INH1 signal *uINH1* of the AS shall be in logical LOW state (*Sleep*) during the test execution, i.e. the AS shall remain in *AS_Sleep*.

Table 393 defines the test instances for insufficient wakeup pulse (negative pulse, remain in AS_Sleep) test case defined in Table 392.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 393 — Test instances for insufficient wakeup pulse (negative pulse, remain in *AS_Sleep*)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.10 Insufficient wakeup pulse (positive pulse, remain in *AS_Sleep*)

Table 394 defines the test case for insufficient wakeup pulse (positive pulse, remain in AS_Sleep).

Table 394 — Test case for insufficient wakeup pulse (positive pulse, remain in *AS_Sleep*)

Name	Insufficient wakeup pulse (positive pulse, remain in *AS_Sleep*)
Test purpose	This test checks the ability of the IUT to ignore spikes on the WAKE pin and to stay in *AS_Sleep* mode according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the active star – wake interface is not implemented — neither the Functional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented — a positive local wakeup pulse is not supported by the IUT
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.10. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.10. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.10. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.10. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the AS.

Name	Insufficient wakeup pulse (positive pulse, remain in *AS_Sleep*)
	f) Apply a positive wakeup pulse of 1 µs to the active star at *TP_AS_WAKE* according to *dStarWakePulseFilter* in ISO 17458-4. g) Trigger the scope to start the observation synchronously with the stimuli at *TP_AS_WAKE* of node the active star. h) Wait 100 µs.
Postamble	Standard postamble.
Pass criteria	— *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* during the test execution, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). — In case of an available INH1 signal *uINH1* of the AS shall be in logical LOW state (*Sleep*) during the test execution, i.e. the AS shall remain in *AS_Sleep*.

Table 395 defines the test instances for insufficient wakeup pulse (positive pulse, remain in AS_Sleep) test case defined in Table 394.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 395 — Test instances for insufficient wakeup pulse (positive pulse, remain in *AS_Sleep*)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.11 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to shorted wakeup pattern

Table 396 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to shorted wakeup pattern.

Table 396 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to shorted wakeup pattern

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to shorted wakeup pattern**
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of *dStarWakeupReactionTime* due to a shorted remote wakeup as specified in 9.1.3.13 and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present. This test case is skipped if the Functional class “Active star – communication controller interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to shorted wakeup pattern
	active star. f) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one shorted wakeup pattern as specified in 9.1.3.13. g) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*. h) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern. i) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 86,3 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 13,3 µs after the beginning of the wakeup pattern and 86,3 µs after the beginning of the wakeup pattern.

Table 397 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to shorted wakeup pattern test case defined in Table 396.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 397 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to shorted wakeup pattern

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.12 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (V_{CC} interrupted)

Table 398 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (V_{CC} interrupted).

Table 398 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (V_{CC} interrupted)

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (V_{CC} interrupted)**
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of *dStarWakeupReactionTime* due to remote wakeup as specified in 9.1.3.1 and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while V_{BAT} is available and V_{CC} is interrupted, i.e. unsupplied. This test case is skipped if the Functional class “Active star – voltage regulator control” is not implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — V_{BAT} power supply of active star: default. — External V_{CC} power supply of active star: +5,0 V. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: loss of V_{CC} according to FL2 in 7.6. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches. — Interrupt supply wire V_{CC} of the active star according to 7.6. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4. e) Observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (V_{CC} interrupted)
	pattern as described in 9.1.3.1. g) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*. h) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern. i) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. Adaptation of the thresholds for digital signals may be required. The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 104 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal uINH1 shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 31 µs after the beginning of the wakeup pattern and 104 µs after the beginning of the wakeup pattern.

Table 399 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (V_{CC} interrupted) test case defined in Table 398.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 399 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (V_{CC} interrupted)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.13 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (Undervoltage at V_{CC})

Table 400 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (Undervoltage at V_{CC}).

Table 400 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (Undervoltage at V_{CC})

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (Undervoltage at V_{CC})**
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of *dStarWakeupReactionTime* and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present. This test case is skipped if the Functional class “Active star – voltage regulator control” is not implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — V_{BAT} power supply of active star: default. — External V_{CC} power supply of active star: +5,0 V. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Set the external V_{CC} power supply of the active star to $V_{CCUndervoltage}$. — Wait 1 000 ms. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4. e) Observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (Undervoltage at V_{CC})
	pattern as described in 9.1.3.1. g) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*. h) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern. i) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. Adaptation of the thresholds for digital signals may be required. The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 104 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 31 µs after the beginning of the wakeup pattern and 104 µs after the beginning of the wakeup pattern.

Table 401 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (Undervoltage at V_{CC}) test case defined in Table 400.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 401 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (Undervoltage at V_{CC})

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.9.14 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (retransmission of wakeup symbols while V_{CC} interrupted)

Table 402 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (retransmission of wakeup symbols while V_{CC} interrupted).

Table 402 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (retransmission of wakeup symbols while V_{CC} interrupted)

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (retransmission of wakeup symbols while V_{CC} interrupted)**
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of *dStarWakeupReactionTime* due to remote wakeup as specified in 9.1.3.1, i.e. to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* and retransmit the remaining wakeup symbols according to ISO 17458-4 while V_{BAT} is available and V_{CC} is interrupted, i.e. unsupplied. This test case is skipped if the Functional class “Active star – voltage regulator control” is not implemented. The used conformance test setup might be modified in this test case in comparison to the standard setup, because an optional external capacitor shall guarantee the retransmission of at least one wakeup pattern. This capacitor shall be calculated according to the device data sheet or equivalent documents.
Configuration	— Topology: as specified in previous configuration see 10.2. — V_{BAT} power supply of active star: default. — External V_{CC} power supply of active star: +5,0 V. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: loss of V_{CC} according to FL2 in 7.6. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Stimulate all nodes except node 1 via the host interface to enter *BD_Standby*. — Interrupt supply wire V_{CC} of the active star according to 7.6. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. b) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. c) Observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 1. e) Observe and acquire the error signal of the host interface (*TP_Nx_ERRN* or *TP_Nx_INTN*) of all nodes except node 1.

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (retransmission of wakeup symbols while V_{CC} interrupted)**
	f) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by seven wakeup patterns as described in 9.1.3.1. g) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. Adaptation of the thresholds for digital signals may be required. — *uINH1* at *TP_AS_INH1* of the active star shall be in logical LOW state initially. Then, *uINH1* shall change to logical HIGH state between 31 µs and 104 µs after the beginning of the wakeup pattern, i.e. the AS has entered *AS_Normal.* — *uRxD* of all observed nodes shall be in logical HIGH state initially. After the wakeup event is detected, *uRxD* of all observed nodes shall change to logical LOW state. — The error signal of all observed nodes shall be in logical HIGH state initially. After the wakeup event is detected, *uINTN* or *uERRN* of all observed nodes shall change to logical LOW state.

Table 403 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (retransmission of wakeup symbols while V_{CC} interrupted) test case defined in Table 402.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 403 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (retransmission of wakeup symbols while V_{CC} interrupted)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.10 Mode.Active Star.Low Power.Standby

10.4.10.1 Operation mode change to *AS_Standby* due to undervoltage $V_{StarSupply}$

Table 404 defines the test case for operation mode change to AS_Standby due to undervoltage VStarSupply.

Table 404 — Test case for operation mode change to *AS_Standby* due to undervoltage VStarSupply

Name	Operation mode change to *AS_Standby* due to undervoltage VStarSupply
Test purpose	This test checks the ability of the IUT to change from *AS_Normal* mode to *AS_Standby* due to undervoltage condition occurring at $V_{StarSupply}$ according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{CC} is implemented: In case that the $V_{StarSupply}$ power supply of the active star depends on V_{CC}: external V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: In case that the $V_{StarSupply}$ power supply of the active star depends on V_{BAT}: external V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	While setting $V_{StarSupply}$ at the active star to undervoltage, potential voltages at all implemented supplies, i.e. V_{BAT}, V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. Adaptation of the thresholds for digital signals may be required. a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5. e) Set $V_{StarSupply}$ power supply of the active star to undervoltage: depends on implementation. f) 1 ms[b] after the undervoltage is set stimulate the IUT in node 2 at *TP_N2_TxD* and

Name	Operation mode change to *AS_Standby* due to undervoltage VStarSupply
	TP_N2_TxEN by one TSS pattern, followed by ten [a] 50/50 patterns. g) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	*uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* during the test execution, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*).
[a] The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms [b] Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least.	

Table 405 defines the test instances for operation mode change to AS_Standby due to undervoltage VStarSupply test case defined in Table 404.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 405 — Test instances for operation mode change to *AS_Standby* due to undervoltage VStarSupply

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

10.4.10.2 Operation mode change from *AS_Off* to *AS_Standby* to *AS_Sleep* due to undervoltage $V_{StarSupply}$ during power on

Table 406 defines the test case for operation mode change from AS_Off to AS_Standby to AS_Sleep due to undervoltage VStarSupply during power on.

Table 406 — Test case for operation mode change from *AS_Off* to *AS_Standby* to *AS_Sleep* due to undervoltage VStarSupply during power on

Name	**Operation mode change from *AS_Off* to *AS_Standby* to *AS_Sleep* due to undervoltage VStarSupply during power on**
Test purpose	This test checks the ability of the IUT to change from *AS_Off* mode to *AS_Standby* due to undervoltage condition occurring at $V_{StarSupply}$ and to *AS_Sleep* due to remaining undervoltage condition according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{CC} is implemented: — External V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: — V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	While setting $V_{StarSupply}$ at the active star to undervoltage, potential voltages at all implemented supplies, i.e. V_{BAT}, V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. — Standard preamble. — Set $V_{StarSupply}$ power supply of the active star to undervoltage: depends on implementation. — Disable outputs of external power supplies of IUT in active star. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.6. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.6. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.6. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.6.

Name	**Operation mode change from *AS_Off* to *AS_Standby* to *AS_Sleep* due to undervoltage VStarSupply during power on**
	e) Observe and acquire *uRxD* signal at *TP_Nx_RxD* of all nodes. f) Enable outputs of external power supplies of IUT in active star. g) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten [a] 50/50 patterns. Repeat this sequence with a pause between the messages of 20 µs for at least 2 ms to assure that the stimulation reaches after the maximal undervoltage detection timeout ($dUV_{ASSupply}$). h) Wait 6 400 ms (*dStarGoToSleep*) for the active star to go to *AS_Sleep.* i) Trigger the scope to start the observation synchronously with the stimulation of the bus driver of node 2.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — Between 100 µs [b] and 100 µs + 1 ms [b] + 640 ms after the undervoltage is applied, *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* state, i.e. *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) and the absolute value of *uBus* shall be between 0 mV and 30 mV ($uStarTx_{idle}$). — *uRxD* of all nodes except node 2 shall stay HIGH, i.e. the active star shall not enter *AS_Normal* and shall not retransmit the pattern sent by node 2.

[a] The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms

[b] Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least.

Table 407 defines the test instances for operation mode change from AS_Off to AS_Standby to AS_Sleep due to undervoltage VStarSupply during power on test case defined in Table 406.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 407 — Test instances for operation mode change from *AS_Off* to *AS_Standby* to *AS_Sleep* due to undervoltage VStarSupply during power on

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

10.4.11 Mode.Active Star.Off

10.4.11.1 Operation mode change from *AS_Normal* to *AS_Off* due to power off of $V_{StarSupply}$

Table 408 defines the test case for operation mode change from AS_Normal to AS_Off due to power off of VStarSupply.

Table 408 — Test case for operation mode change from *AS_Normal* to *AS_Off* due to power off of VStarSupply

Name	Operation mode change from *AS_Normal* to *AS_Off* due to power off of VStarSupply
Test purpose	This test checks the ability of the IUT to change from *AS_Normal* mode to *AS_Off* due to power off event according to ISO 17458-4 while no stress condition is present and to change its branches from *Branch_Idle* to *Branch_Off*.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{CC} is implemented: In case that the $V_{StarSupply}$ power supply of the active star depends on V_{CC}: external V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: In case that the $V_{StarSupply}$ power supply of the active star depends on V_{BAT}: external V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 1 and node 2 as transmitter.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	While disabling the power supplies at the active star, potential voltages at all implemented supplies, i.e. V_{BAT}, V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. f) Disable all power supplies of the active star. g) After the active star has entered *AS_Off*, i.e. 100 µs + 1 ms[a] after the power supplies

Name	Operation mode change from *AS_Normal* to *AS_Off* due to power off of VStarSupply
	are disabled, stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern as described in 9.1.3.1. h) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs because the active star might wake up during this time. i) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. j) Trigger the scope and the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of all nodes except node 2 shall stay HIGH, i.e. the active star shall not be able to retransmit the patterns sent by node 2. — *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* during the observation window, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*).
a Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least.	

Table 409 defines the test instances for operation mode change from AS_Normal to AS_Off due to power off of VStarSupply test case defined in Table 408.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 409 — Test instances for operation mode change from *AS_Normal* to *AS_Off* due to power off of VStarSupply

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

10.4.12 Mode.Active Star.Branch.Receive.Transmit

10.4.12.1 Branch state transition from *Branch_Idle* to *Branch_Receive* and *Branch_Transmit*

Table 410 defines the test case for branch state transition from Branch_Idle to Branch_Receive and *Branch_Transmit*.

Table 410 — Test case for branch state transition from *Branch_Idle* to *Branch_Receive* and *Branch_Transmit*

Name	**Branch state transition from *Branch_Idle* to *Branch_Receive* and *Branch_Transmit***
Test purpose	This test checks the ability of the active star to switch its branch mode from *Branch_Idle* to *Branch_Receive* and *Branch_Transmit* according to ISO 17458-4 with consideration of the delays between branches of the active star during a retransmission while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS1_B1* of the transmitting branch according to the observation window described in 10.2.4.7. b) Observe and acquire *uBus* at *TPAS4_B3* of the receiving branch according to the observation window described in 10.2.4.7. c) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. d) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star.

Name	Branch state transition from *Branch_Idle* to *Branch_Receive* and *Branch_Transmit*
	h) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall contain the 50/50 pattern transmitted by node 2, i.e. the active star repeats the patterns received at branch 3 at all other branches. — In case of an available RxEN signal *uRxEN* of the observed nodes shall be in logical LOW state while *uRxD* of the same node signals the patterns received from node 2 and in logical HIGH state otherwise. — *uBus* at *TPAS1_B3* of the receiving branch 3 shall be within *Idle* range at the beginning of the observation window, i.e. the absolute bus voltage shall be smaller than 30 mV ($uStarTx_{idle}$) – the branch is in *Branch_Idle* state. *uBus* at *TPAS1_B3* shall exceed *Idle* range when the bus driver of node 2 is being stimulated at *TP_N2_TxD* and *TP_N2_TxEN*, i.e. the receiving branch enters *Branch_Receive* and shall contain the pattern sent by node 2. — *uBus* at *TPAS1_B1* of the transmitting branch 1 shall be within *Idle* range at the beginning of the observation window, i.e. the absolute bus voltage shall be smaller than 30 mV ($uStarTx_{idle}$) – the branch is in *Branch_Idle* state. *uBus* at *TPAS1_B1* shall exceed *Idle* range within 600 ns (*dStarDelay10* + |*dStarTSSLengthChange*| = 150 ns + |-450 ns|) after *uBus* at *TPAS4_B3* has exceeded *Idle* range, i.e. all transmitting branches enter *Branch_Transmit*. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 411 defines the test instances for branch state transition from Branch_Idle to Branch_Receive and *Branch_Transmit* test case defined in Table 410.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 411 — Test instances for branch state transition from *Branch_Idle* to *Branch_Receive* and *Branch_Transmit*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.13 Mode.Active Star.Branch.Idle

10.4.13.1 Branch operation state transition from *Branch_Receive* and *Branch_Transmit* to *Branche_Idle*

Table 412 defines the test case for branch operation state transition from Branch_Receive and Branch_Transmit to *Branche_Idle*.

Table 412 — Test case for branch operation state transition from *Branch_Receive* and *Branch_Transmit* to *Branche_Idle*

Name	**Branch operation state transition from *Branch_Receive* and *Branch_Transmit* to *Branche_Idle***
Test purpose	This test checks the ability of the active star to switch its branch operation state from *Branch_Receive* and *Branch_Transmit* to *Branch_Idle* according to ISO 17458-4 with consideration of the delays between branches of the active star during a retransmission while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS1_B1* of the transmitting branch according to the observation window described in 10.2.4.7. b) Observe and acquire *uBus* at *TPAS4_B3* of the receiving branch according to the observation window described in 10.2.4.7. c) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. d) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the

Name	Branch operation state transition from *Branch_Receive* and *Branch_Transmit* to *Branche_Idle*
	active star. h) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern, followed by one FES pattern. i) Trigger the scope synchronously with the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall contain the pattern transmitted by node 2, i.e. the active star repeats the patterns received at branch 3 at all other branches. — *uBus* at *TPAS1_B3* of the receiving branch 3 shall be within *Idle* range at the beginning of the observation window, i.e. the absolute bus voltage shall be smaller than 30 mV ($uStarTx_{idle}$) – the branch is in *Branch_Idle* state. *uBus* at *TPAS1_B3* shall exceed *Idle* range when the bus driver of node 2 is being stimulated at *TP_N2_TxD* and *TP_N2_TxEN*, i.e. the receiving branch enters *Branch_Receive* and shall contain the pattern sent by node 2. — *uBus* at *TPAS1_B1* of transmitting branch 1 shall exceed *Idle* range while the patterns received at branch 3 are retransmitted, i.e. the absolute bus voltage shall exceed 30 mV ($uStarTx_{idle}$) – the branch is in *Branch_Transmit* state. *uBus* at *TPAS1_B1* shall re-enter *Idle* range within 600 ns (*dStarDelay10 max* + *dStarFES1LengthChange max* = 150 ns + 450 ns) after *uBus* at *TPAS4_B3* has dropped below 30 mV ($uStarTx_{idle}$) again, i.e. the receiving branch is in *Idle* state again and all transmitting branches re-enter *Branch_Idle* after the transmission. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 413 defines the test instances for branch operation state transition from Branch_Receive and *Branch_Transmit* to *Branche_Idle* test case defined in Table 412.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 413 — Test instances for branch operation state transition from *Branch_Receive* and *Branch_Transmit* to *Branche_Idle*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.13.2 Operation state change from *Branch_LowPower* to *Branche_Idle*

Table 414 defines the test case for operation state change from Branch_LowPower to Branche_Idle.

Table 414 — Test case for operation state change from *Branch_LowPower* to *Branche_Idle*

Name	Operation state change from *Branch_LowPower* to *Branche_Idle*
Test purpose	This test checks the ability of the active star to change its branch mode from *Branch_LowPower* to *Branch_Idle* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern as described in 9.1.3.1. g) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern.

Name	Operation state change from *Branch_LowPower* to *Branche_Idle*
	h) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*.
Postamble	Standard postamble.
Pass criteria	The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 104 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 31 µs after the beginning of the wakeup pattern and 104 µs after the beginning of the wakeup pattern.

Table 415 defines the test instances for operation state change from Branch_LowPower to Branche_Idle test case defined in Table 414.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 415 — Test instances for operation state change from *Branch_LowPower* to *Branche_Idle*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.13.3 Operation state change from *Branch_TxOnly* to *Branch_Idle*

Table 416 defines the test case for operation state change from Branch_TxOnly to Branch_Idle.

Table 416 — Test case for operation state change from *Branch_TxOnly* to *Branch_Idle*

Name	Operation state change from *Branch_TxOnly* to *Branch_Idle*
Test purpose	This test checks the ability of the active star to change its branch mode from *Branch_TxOnly* to *Branch_Idle* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* and *TP_Nx_TxEN* of nodes 2, 11, 12, 13 and 14. b) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. c) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. e) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1. f) After 2 600 µs from the start of the babbling idiot sequence stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. g) Wait at least |-450 ns| for the active star to detect *Idle* on the branches. h) Stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. Branch shall change to BR_TxOnly

Name	Operation state change from *Branch_TxOnly* to *Branch_Idle*
	i) Wait 5,0 µs. j) Stimulate the IUT in node 11 at *TP_N11_TxD* and *TP_N11_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes except nodes 11..14 (branch 4) shall contain the 50/50 patterns transmitted by node 2 after 2 600µs from the start of the babbling idiot sequence, i.e. the active star has switched branch 4 to *Branch_FailSilent* within the maximal noise detection timeout of *dBranchRxActiveMax* = 2 600µs and has excluded this branch from communication. — *uRxD* of all nodes shall contain the 50/50 pattern transmitted by node 2 at the second stimulation after the end of the babbling idiot sequence, i.e. the active star has switched branch 4 from *Branch_FailSilent* to *Branch_TxOnly* after *Idle* on all branches is detected. — *uRxD* of all nodes shall contain the 50/50 pattern transmitted by node 11, i.e. the active star has switched branch 4 from *Branch_Idle* to *Branch_Receive*. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 417 defines the test instances for operation state change from Branch_TxOnly to Branch_Idle test case defined in Table 416.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 417 — Test instances for operation state change from *Branch_TxOnly* to *Branch_Idle*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.14 Mode.Active Star.Branch.TxOnly

10.4.14.1 Operation state change from *Branch_FailSilent* to *Branch_TxOnly*

Table 418 defines the test case for operation state change from Branch_FailSilent to Branch_TxOnly.

Table 418 — Test case for operation state change from *Branch_FailSilent* to *Branch_TxOnly*

Name	**Operation state change from *Branch_FailSilent* to *Branch_TxOnly***
Test purpose	This test checks the ability of the active star to change its branch mode from *Branch_FailSilent* to *Branch_TxOnly* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* and *uTxEN* at *TP_Nx_TxEN* of nodes 2, 11, 12, 13 and 14. b) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. e) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1. f) After 2 600 µs from the start of the babbling idiot sequence stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. g) Wait at least |-450 ns| for the active star to detect *Idle* on all branches. h) Stimulate the IUT in node 11 at *TP_N11_TxD* and *TP_N11_TxEN* by one TSS pattern,

Name	Operation state change from *Branch_FailSilent* to *Branch_TxOnly*
	followed by one 50/50 pattern. i) Stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. j) Wait 5,0 µs. k) Stimulate the IUT in node 11 at *TP_N11_TxD* and *TP_N11_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes except nodes 11..14 (branch 4) shall contain the 50/50 patterns transmitted by node 2 after 2 600 µs from the start of the babbling idiot sequence, i.e. the active star has switched branch 4 to *Branch_FailSilent* within the maximal noise detection timeout of *dBranchRxActiveMax* = 2 600 µs and has excluded this branch from communication. — In case of an available RxEN signal *uRxEN* of all nodes except nodes 11..14 (branch 4) shall be in logical LOW state while *uRxD* of the same node signals the patterns received from node 2 at the first stimulation and in logical HIGH state otherwise. — *uRxD* of all nodes except nodes 11..14 (branch 4) shall not contain the 50/50 pattern transmitted by node 11 at the first stimulation, i.e. the active star has switched branch 4 from *Branch_FailSilent* to *Branch_TxOnly* and receiving on this branch is not possible. — In case of an available RxEN signal *uRxEN* of all nodes except nodes 11..14 (branch 4) shall be in logical HIGH state while the first stimulation of node 11. — *uRxD* of all nodes shall contain the 50/50 pattern transmitted by node 2 at the second stimulation after the end of the babbling idiot sequence, i.e. the active star has switched branch 4 from *Branch_FailSilent* to *Branch_TxOnly* after *Idle* on all branches is detected. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical LOW state while *uRxD* of the same node signals the patterns received from node 2 at the second stimulation after the end of the babbling idiot sequence and in logical HIGH state otherwise. — *uRxD* of all nodes shall contain the 50/50 pattern transmitted by node 11 at the second stimulation, i.e. the active star has switched branch 4 from *Branch_Idle* to *Branch_Receive*. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 419 defines the test instances for operation state change from Branch_FailSilent to Branch_TxOnly test case defined in Table 418.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 419 — Test instances for operation state change from *Branch_FailSilent* to *Branch_TxOnly*

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.15 Mode.Active Star.Branch.FailSilent

10.4.15.1 Operation state change from *Branch_Receive* to *Branch_FailSilent*

Table 420 defines the test case for operation state change from Branch_Receive to Branch_FailSilent.

Table 420 — Test case for operation state change from *Branch_Receive* to *Branch_FailSilent*

Name	**Operation state change from *Branch_Receive* to *Branch_FailSilent***
Test purpose	This test checks the parameter *dBranchRxActiveMax* and the ability of the active star to change its branch mode from *Branch_Receive* to *Branch_FailSilent* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: none.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS1_B2* of the transmitting branch 2 according to the observation window described in 10.2.4.8. b) Observe and acquire *uBus* at *TPAS4_B4* of the receiving branch 4 according to the observation window described in 10.2.4.8. c) Observe and acquire *uTxD* at *TP_N12_TxD* of node 12, *TP_N13_TxD* of node 13 and *TP_N14_TxD* of node 14. d) Observe and acquire *uTxEN* at *TP_N12_TxEN* of node 12, *TP_N13_TxEN* of node 13 and *TP_N14_TxEN* of node 14. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1.

Name	Operation state change from *Branch_Receive* to *Branch_FailSilent*
	g) The observation window shall start synchronously with the stimuli at *TP_N12_TxD* and *TP_N12_TxEN* of node 12.
Postamble	Standard postamble.
Pass criteria	— *uBus* of all observed transmitting branches shall change to *Data_0* state, i.e. *uBus* shall fall below 600 mV ($uStarTx_{active}$) and shall remain in *Data_0* state for at least 650 µs and not more than 2 600 µs and shall return to *Idle* state afterwards, i.e. the absolute bus voltage shall no more exceed 30 mV ($uStarTx_{idle}$). This means that the active star shall switch branch 4 from *Branch_Receive* to *Branch_FailSilent* within the allowed range of the noise detection timeout of $dBranchRxActiveMax_{min}$ = 650 µs to $dBranchRxActiveMax_{max}$ = 2 600 µs. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 421 defines the test instances for operation state change from Branch_Receive to Branch_FailSilent test case defined in Table 420.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 421 — Test instances for operation state change from *Branch_Receive* to *Branch_FailSilent*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.15.2 Operation state change between *Branch_TxOnly* and *Branch_FailSilent*

Table 422 defines the test case for operation state change between Branch_TxOnly and Branch_FailSilent.

Table 422 — Test case for operation state change between *Branch_TxOnly* and *Branch_FailSilent*

Name	**Operation state change between *Branch_TxOnly* and *Branch_FailSilent***
Test purpose	This test checks the parameter *dBranchRxActiveMax* and the ability of the active star to change its branch mode from *Branch_TxOnly* to *Branch_FailSilent* according to ISO 17458-4 while no stress condition is present. This test case is skipped if the Functional class “Active star – host interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: none.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS1_B2* of the transmitting branch 2 according to the observation window described in 9.1.4.2. b) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1. c) 100 ms[a] after the end of the babbling idiot pattern short-circuit BP to BM (failure FL21) of the AS at *TPAS1_B4.* -> Bus Error detected; Branch_FailSilent d) Stimulate the bus driver of node 2 by one TSS pattern, followed by eight 50/50 patterns. e) 300 ms[a] after the end of the babbling idiot pattern disable the short-circuit of BP to BM (failure FL21) of the AS at *TPAS1_B4.* f) Stimulate the bus driver of node 11 by one TSS pattern, followed by one 50/50 pattern. -> Branch shall be in Tx_Only g) Trigger the scope to start the observation synchronously with the stimuli at

Name	Operation state change between *Branch_TxOnly* and *Branch_FailSilent*
	TP_N11_TxEN of node 11.
Postamble	Standard postamble.
Pass criteria	While the bus driver of node 11 is being stimulated the active star shall switch branch 4 back to *Branch_TxOnly*, i.e. the absolute value of *uBus* at branch 2 shall be between 0 mV and 30mV ($uStarTx_{idle}$) when node 11 is being stimulated. That means that the active star shall have detected that the bus error has been disabled before the stimulation of the bus driver of node 11 and shall not receive the pattern sent by node 11.
a Space time for measurement and reaction of the IUT, i.e. idle detection time, error detection time, etc.	

Table 423 defines the test instances for operation state change between Branch_TxOnly and Branch_FailSilent test case defined in Table 422.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 423 — Test instances for operation state change between *Branch_TxOnly* and *Branch_FailSilent*

Instance		1	2	3
Purpose	Stress	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	Power supply	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.16 Mode.Active Star.Branch.LowPower

10.4.16.1 Operation state change to *Branch_LowPower* while undervoltage $V_{StarSupply}$ after power on

Table 424 defines the test case for operation state change to Branch_LowPower while undervoltage VStarSupply after power on.

Table 424 — Test case for operation state change to *Branch_LowPower* while undervoltage VStarSupply after power on

Name	Operation state change to *Branch_LowPower* while undervoltage VStarSupply after power on
Test purpose	This test checks the ability of the IUT to change its branch from *Branch_Off* state to *Branch_LowPower* due to power on event while undervoltage condition occurring at $V_{StarSupply}$ according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{CC} is implemented: External V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	While setting $V_{StarSupply}$ at the active star to undervoltage, potential voltages at all implemented supplies, i.e. V_{BAT}, V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. — Standard preamble. — Set $V_{StarSupply}$ power supply of the active star to undervoltage: depends on implementation. — Disable the outputs of the external power supplies of the IUT in the active star. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.11. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.11. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.11. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.11.

Name	Operation state change to *Branch_LowPower* while undervoltage VStarSupply after power on
	e) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. f) Enable the outputs of the external power supplies of the IUT in the active star. g) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten [a] 50/50 patterns. Repeat this sequence with a pause between the messages of 20 µs for at least 1,5 ms to assure that the stimulation reaches after the maximal undervoltage detection timeout ($dUV_{ASSupply}$). h) Trigger the scope to start the observation synchronously with the stimulation at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. The observation window shall start synchronously with the power on event. — *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* state during the observation window, i.e. *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*). — *uRxD* of all nodes except node 2 shall stay HIGH, i.e. the active star shall stay at *AS_Standby* and shall not retransmit the pattern sent by node 2.
[a] The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 425 defines the test instances for operation state change to Branch_LowPower while undervoltage VStarSupply after power on test case defined in Table 424.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 425 — Test instances for operation state change to *Branch_LowPower* while undervoltage VStarSupply after power on

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

10.4.16.2 Operation state change from *Branch_Idle* to *Branch_LowPower* due to undervoltage $V_{StarSupply}$

Table 426 defines the test case for operation state change from Branch_Idle to Branch_LowPower due to undervoltage VStarSupply.

Table 426 — Test case for operation state change from *Branch_Idle* to *Branch_LowPower* due to undervoltage VStarSupply

Name	**Operation state change from *Branch_Idle* to *Branch_LowPower* due to undervoltage VStarSupply**
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_Idle* to *Branch_LowPower* due to undervoltage condition occurring at $V_{StarSupply}$ according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that V_{CC} is implemented: External V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) While setting $V_{StarSupply}$ at the active star to undervoltage, potential voltages at all implemented supplies, i.e. V_{BAT}, V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. b) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. e) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5. f) Set $V_{StarSupply}$ power supply of the active star to undervoltage: depends on implementation. g) 1 ms[a] after the undervoltage is set stimulate the IUT in node 2 at *TP_N2_TxD* and

Name	Operation state change from *Branch_Idle* to *Branch_LowPower* due to undervoltage VStarSupply
	TP_N2_TxEN by one TSS pattern, followed by ten[a] 50/50 patterns. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* state during the observation window, i.e. *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*).
a Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least. b The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 427 defines the test instances for operation state change from Branch_Idle to Branch_LowPower due to undervoltage VStarSupply test case defined in Table 426.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 427 — Test instances for operation state change from *Branch_Idle* to *Branch_LowPower* due to undervoltage VStarSupply

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

10.4.17 Failure.Loss

10.4.17.1 Interruption of V_{BAT} (V_{CC} available)

Table 428 defines the test case for interruption of V_{BAT} (V_{CC} available).

Table 428 — Test case for interruption of V_{BAT} (V_{CC} available)

Name	Interruption of V_{BAT} (V_{CC} available)
Test purpose	This test checks the of the active star to remain in *AS_Normal* in case of loss of the V_{BAT} supply power if V_{CC} is still available according to ISO 17458-4 while no other stress condition is present and $V_{StarSupply}$ is constantly supplied within its normal operation range. This test case is skipped if — the Functional class “Active star – voltage regulator control” is not implemented — the Functional class “Active star – internal voltage regulator” is implemented and a V_{CC} supply input is not available.
Configuration	— Topology: as specified in previous configuration see 10.2. — V_{BAT} power supply of the active star: default. — External V_{CC} power supply of the active star: +5,0 V. — In case that V_{IO} is implemented: external V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: loss of V_{BAT} according to FL1 in 7.6. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 1, 2, 12 and 23. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 1, 2, 12 and 23. e) Interrupt supply wire V_{BAT} of the active star according to 7.6. f) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence for at least 1 000 ms to verify that communication is not disturbed even after the maximal undervoltage detection timeout ($dStarUVV_{BAT}$). The bit duration in this test case shall be *gdBit*=25 µs, because the memory depth of the logic analyzer is much too small to acquire more than 1 seconds with a 100 ns bit time. The gap between the messages in matrix A shall be 9,25 ms.

Name	Interruption of V_{BAT} (V_{CC} available)
Postamble	Standard postamble.
Pass criteria	— This test case requires acquisition of at least 1 000 ms by the logic analyzer. A bit level resolution is not required. Adaptation of the thresholds for digital signals may be required. — *uRxD* of all observed nodes shall contain all logical logical 50/50 pattern sequences transmitted by node 2, i.e. the active star shall stay in *AS_Normal* mode and shall retransmit all patterns received on branch 3.

10.4.17.2 Interruption of V_{BAT} (V_{CC} not implemented)

Table 429 defines the test case for interruption of V_{BAT} (V_{CC} not implemented).

Table 429 — Test case for interruption of V_{BAT} (V_{CC} not implemented)

Name	Interruption of V_{BAT} (V_{CC} not implemented)
Test purpose	This test checks the ability of the active star to change to *AS_Off* mode in case of loss of the V_{BAT} supply power if V_{CC} is not implemented according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the Functional class "Active star – internal voltage regulator" is not implemented — a V_{CC} supply input is although available.
Configuration	— Topology: as specified in previous configuration see 10.2. — V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: external V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: loss of V_{BAT} according to FL1 in 7.6. — Communication: matrix A (round robin test).
Preamble (setup state)	Standard preamble.
Test execution	a) While interrupt $V_{StarSupply}$ at the active star, potential voltages at all implemented supplies, i.e. V_{BAT} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. b) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Interrupt supply wire V_{BAT} of the active star according to 7.6. g) Wait 1 ms [a] h) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of nodes 11..14 shall contain the 50/50 patterns transmitted by nodes 11..14 only, i.e. the active star shall not disturb the communication on the passive bus (branch 4) and shall not

Name	Interruption of V_{BAT} (V_{CC} not implemented)
	retransmit patterns received on other branches. — *uRxD* of nodes 21..24 shall contain the 50/50 patterns transmitted by nodes 21..24 only, i.e. the active star shall not disturb the communication on the passive star (branch 2) and shall not retransmit patterns received on other branches. — *uRxD* of nodes 1 and 2 shall contain the 50/50 patterns transmitted by themselves only (loopback functionality), i.e. the active star shall not disturb the communication of nodes 1 and 2 (branch 1 and 3) and shall not retransmit patterns received on other branches.
a Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least.	

10.4.17.3 Interruption of V_{CC} (V_{BAT} not implemented)

Table 430 defines the test case for interruption of V_{CC} (V_{BAT} not implemented).

Table 430 — Test case for interruption of V_{CC} (V_{BAT} not implemented)

Name	Interruption of V_{CC} (V_{BAT} not implemented
Test purpose	This test checks the checks the ability of the active star to change to *AS_Off* mode in case of loss of the V_{CC} supply power if V_{BAT} is not implemented according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the Functional class "Active star – voltage regulator control" is implemented — the Functional class "Active star – internal voltage regulator" is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — V_{CC} power supply of the active star: +5,0 V. — In case that V_{IO} is implemented: external V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: loss of V_{CC} according to FL2 in 7.6. — Communication: matrix A (round robin test).
Preamble (setup state)	Standard preamble.
Test execution	While interrupt $V_{StarSupply}$ at the active star, potential voltages at all implemented supplies, i.e. V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Interrupt supply wire V_{CC} of the active star according to 7.6. e) Wait 1 ms [a] f) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of nodes 11..14 shall contain the 50/50 patterns transmitted by nodes 11..14 only, i.e. the active star shall not disturb the communication on the passive bus (branch 4) and shall not retransmit patterns received on other branches. — *uRxD* of nodes 21..24 shall contain the 50/50 patterns transmitted by nodes 21..24 only, i.e. the active star shall not disturb the communication on the passive star (branch 2) and shall not

Name	Interruption of V_{CC} (V_{BAT} not implemented
	retransmit patterns received on other branches. — *uRxD* of nodes 1 and 2 shall contain the 50/50 patterns transmitted by themselves only (loopback functionality), i.e. the active star shall not disturb the communication of nodes 1 and 2 (branch 1 and 3) and shall not retransmit patterns received on other branches.
a Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least.	

10.4.17.4 Interruption of V_{BAT} and V_{CC}

Table 431 defines the test case for interruption of V_{BAT} and V_{CC}.

Table 431 — Test case for interruption of V_{BAT} and V_{CC}

Name	Interruption of V_{BAT} and V_{CC}
Test purpose	This test checks the ability of the active star to change to *AS_Off* mode in case of loss of the V_{BAT} and V_{CC} supply power according to ISO 17458-4 while no other stress condition is present. This test case is skipped if — the Functional class “Active star – voltage regulator control” is not implemented — the Functional class “Active star – internal voltage regulator” is implemented and a V_{CC} supply input is not available.
Configuration	— Topology: as specified in previous configuration see 10.2. — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that V_{IO} is implemented: external V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: loss of V_{CC} and V_{BAT} according to FL3 in 7.6. — Communication: matrix A (round robin test).
Preamble (setup state)	Standard preamble.
Test execution	While interrupt $V_{StarSupply}$ at the active star, potential voltages at all implemented supplies, i.e. V_{BAT}, V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. e) Interrupt V_{CC} and V_{BAT} of the active star according to 7.6. f) Wait 1 ms [a] g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required.

Name	Interruption of V_{BAT} and V_{CC}
	— *uRxD* of nodes 11..14 shall contain the 50/50 patterns transmitted by nodes 11..14 only, i.e. the active star shall not disturb the communication on the passive bus (branch 4) and shall not retransmit patterns received on other branches. — *uRxD* of nodes 21..24 shall contain the 50/50 patterns transmitted by nodes 21..24 only, i.e. the active star shall not disturb the communication on the passive star (branch 2) and shall not retransmit patterns received on other branches. — *uRxD* of nodes 1 and 2 shall contain the 50/50 patterns transmitted by themselves only (loopback functionality), i.e. the active star shall not disturb the communication of nodes 1 and 2 (branch 1 and 3) and shall not retransmit patterns received on other branches.
a Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least.	

10.4.18 Failure.Short-circuit Bus Wires

10.4.18.1 Short-circuit bus wires to GND

Table 432 defines the test case for short-circuit bus wires to GND.

Table 432 — Test case for short-circuit bus wires to GND

Name	**Short-circuit bus wires to GND**
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit of the bus wire to GND. Additionally it is checked that the IUT is not permanently damaged by the short-circuit. This test case is skipped if the Functional class “Active star – host interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to GND according to Figure 19 and Table 26, failure FL11. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 1 and 2. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 1 and 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 1 and 2. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 1 and 2. e) Observe and acquire $iBP_{GNDShortMax}$ at $TP\_AS\_B2\_R_{iBP}$ of the AS (shall be at *TPAS1_B2_BP*). f) Stimulate the bus driver of the transmitting node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by a current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples were taken by the data acquisition unit.

Name	Short-circuit bus wires to GND
	g) At least 500 ns after the start of transmission short-circuit BP (failure FL11) of the AS to GND at *TPAS1_B2_BP*. h) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at node 2. Acquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*. i) Switch off the short-circuit BP (failure FL11) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds. j) Stimulate node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. k) Stimulate node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— $\|iBP_{GNDShortMax}\| \leq 60$ mA. — After switching off the failure node 1 shall receive the patterns and signal them accordingly: *TP_N1_RxD* of node1 as stimulated at *TP_N2_TxD* at node 2. In case RxEN is implemented *TP_N1_RxEN* of node 1 as stimulated at *TP_N2_TxEN* at node 2. — After switching off the failure node 2 shall receive the patterns and signal them accordingly: *TP_N2_RxD* of node2 as stimulated at *TP_N1_TxD* at node 1. In case RxEN is implemented *TP_N2_RxEN* of node 2 as stimulated at *TP_N1_TxEN* at node 1.

Table 433 defines the test instances for short-circuit bus wires to GND test case defined in Table 432.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 433 — Test instances for short-circuit bus wires to GND

Instance		**1**	**2**
Purpose	**Stress**	S/C BP to GND at AS	S/C BM to GND at AS
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	—	—
Preamble		—	—
Test execution		… Observe and acquire $iBP_{GNDShortMax}$ at *TP_AS_B2_*R_{iBP} of the AS (shall be at *TPAS1_B2_BP*). Short-circuit BP (failure FL11) of the AS to GND at *TPAS1_B2_BP*. … Switch off short-circuit BP (failure FL11) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds….	… Observe and acquire $iBM_{GNDShortMax}$ at *TP_AS_B2_*R_{iBM} of the AS (shall be at *TPAS1_B2_BM*). Short-circuit BM (failure FL12) of the AS to GND at *TPAS1_B2_BM* … Switch off short-circuit BM (failure FL12) of the AS at *TPAS1_B2_BM*. Wait at least 12 seconds…
Pass criteria		$\lvert iBP_{GNDShortMax} \rvert \leq 60$ mA.	$\lvert iBM_{GNDShortMax} \rvert \leq 60$ mA.

10.4.18.2 Short-circuit bus wires to V_{ANY}

Table 434 defines the test case for short-circuit bus wires to V_{ANY}.

Table 434 — Test case for short-circuit bus wires to V_{ANY}

Name	Short-circuit bus wires to V_{ANY}
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit of the bus wire to +48 V [a]. Additionally it is checked that the IUT is not permanently damaged by the short-circuit. This test case is skipped if the Functional class "Active star – host interface" is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to +48 V [a] according to Figure 19 and Table 26, failure FL13. — Communication: Node 1 and 2 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 1 and 2. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 1 and 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 1 and 2. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 1 and 2. e) Observe and acquire $iBP_{BAT48ShortMax}$ [b] or $iBP_{BAT27ShortMax}$ [c] at *TP_AS_B2_*R_{iBP} of the AS (shall be at *TPAS1_B2_BP*). f) Stimulate the bus driver of the transmitting node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by a current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples were taken by the data acquisition unit. g) At least 500 ns after the start of transmission short-circuit BP (failure FL13) of the AS to +48 V [a] at *TPAS1_B2_BP*. h) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at

Name	Short-circuit bus wires to V_{ANY}
	node 2. Acquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*. i) Sripts are separated into 2 parts, devided by switching off the short-circuit. j) Switch off the short-circuit BP (failure FL13) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds. k) Stimulate node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. l) Stimulate node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— In case the IUT does not support 42 V systems: $\|iBP_{BAT27ShortMax}\| \leq 60$ mA. — In case the IUT does support 42 V systems: $\|iBP_{BAT48ShortMax}\| \leq 72$ mA. — After switching off the failure node 1 shall receive the patterns and signal them accordingly: *TP_N1_RxD* of node1 as stimulated at *TP_N2_TxD* at node 2. In case RxEN is implemented *TP_N1_RxEN* of node 1 as stimulated at *TP_N2_TxEN* at node 2. — After switching off the failure node 2 shall receive the patterns and signal them accordingly: *TP_N2_RxD* of node2 as stimulated at *TP_N1_TxD* at node 1. In case RxEN is implemented *TP_N2_RxEN* of node 2 as stimulated at *TP_N1_TxEN* at node 1.

a In case the IUT does not support 42 V systems the V_{BAT} shall be +27 V.

b In case the IUT does support 42 V systems.

c In case the IUT does not support 42 V systems.

Table 435 defines the test instances for short-circuit bus wires to V_{ANY} test case defined in Table 434.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 435 — Test instances for short-circuit bus wires to V_{ANY}

Instance		**1**	**2**
Purpose	**Stress**	S/C BP to +48 V at AS	S/C BM to +48 V at AS
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to +48 V [a]	S/C BM to +48 V [a]
Preamble		—	—
Test execution		… Observe and acquire $iBP_{BAT48ShortMax}$[b] or $iBP_{BAT27ShortMax}$[c] at $TP\_AS\_B2\_R_{iBP}$ of the AS (shall be at *TPAS1_B2_BP*). Short-circuit BP (failure FL13) of the AS to +48 V[a] at *TPAS1_B2_BP* …. Switch off short-circuit BP (failure FL13) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds. …	… Observe and acquire $iBM_{BAT48ShortMax}$[b] or $iBM_{BAT27ShortMax}$[c] at $TP\_AS\_B2\_R_{iBM}$ of the AS (shall be at *TPAS1_B2_BM*). Short-circuit BM (failure FL14) of the AS to +48 V[a] at *TPAS1_B2_BM* … Switch off short-circuit BM (failure FL14) of the AS at *TPAS1_B2_BM*. Wait at least 12 seconds …
Pass criteria		In case the IUT does not support 42 V systems: $\lvert iBP_{BAT27ShortMax}\rvert \leq 60$ mA. In case the IUT does support 42 V systems: $\lvert iBP_{BAT48ShortMax}\rvert \leq 72$ mA.	In case the IUT does not support 42 V systems: $\lvert iBM_{BAT27ShortMax}\rvert \leq 60$ mA In case the IUT does support 42 V systems: $\lvert iBM_{BAT48ShortMax}\rvert \leq 72$ mA

[a] In case the IUT does not support 42 V systems the V_{BAT} shall be +27 V.

[b] In case the IUT does support 42 V systems.

[c] In case the IUT does not support 42 V systems.

10.4.18.3 Short-circuit bus wires to -5 V

Table 436 defines the test case for short-circuit bus wires to -5 V.

Table 436 — Test case for short-circuit bus wires to -5 V

Name	**Short-circuit bus wires to -5 V**
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit of the bus wire to -5 V. Additionally it is checked that the IUT is not permanently damaged by the short-circuit. This test case is skipped if the Functional class “Active star – host interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to -5 V according to Figure 19 and Table 26, failure FL19. — Communication: Node 1 and 2 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 1 and 2. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 1 and 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 1 and 2. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 1 and 2. e) Observe and acquire $iBP_{-5VshortMax}$ at $TP\_AS\_B2\_R_{iBP}$ of the AS (shall be at *TPAS1_B2_BP*). f) Stimulate the bus driver of the transmitting node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by a current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples were taken by the data acquisition unit. g) At least 500 ns after the start of transmission short-circuit BP (failure FL19) of the AS to -

Name	Short-circuit bus wires to -5 V
	5 V at *TPAS1_B2_BP*. h) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at node 2. Acquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*. i) Switch off the short-circuit BP (failure FL19) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds. j) Stimulate node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. k) Stimulate node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— $\|iBP_{-5VshortMax}\| \leq 60$ mA. — After switching off the failure node 1 shall receive the patterns and signal them accordingly: *TP_N1_RxD* of node1 as stimulated at *TP_N2_TxD* at node 2. In case RxEN is implemented *TP_N1_RxEN* of node 1 as stimulated at *TP_N2_TxEN* at node 2. — After switching off the failure node 2 shall receive the patterns and signal them accordingly: *TP_N2_RxD* of node2 as stimulated at *TP_N1_TxD* at node 1. In case RxEN is implemented *TP_N2_RxEN* of node 2 as stimulated at *TP_N1_TxEN* at node 1.

Table 437 defines the test instances for short-circuit bus wires to -5 V test case defined in Table 436.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 437 — Test instances for short-circuit bus wires to -5 V

Instance		**1**	**2**
Purpose	**Stress**	S/C BP to -5 V at AS	S/C BM to -5 V at AS
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to -5 V	S/C BM to -5 V
Preamble		—	—
Test execution		… Observe and acquire $iBP_{-5VshortMax}$ at $TP\_AS\_B2\_R_{iBP}$ of the AS (shall be at *TPAS1_B2_BP*). Short-circuit BP (failure FL19) of the AS to -5 V at *TPAS1_B2_BP*. … Switch off short-circuit BP (failure FL19) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds. …	… Observe and acquire $iBM_{-5VshortMax}$ at $TP\_AS\_B2\_R_{iBM}$ of the AS (shall be at *TPAS1_B2_BM*). Short-circuit BM (failure FL20) of the AS to -5 V at *TPAS1_B2_BM* … Switch off short-circuit BM (failure FL20) of the AS at *TPAS1_B2_BM*. Wait at least 12 seconds …
Pass criteria		$\lvert iBP_{-5VshortMax}\rvert \leq 60$ mA.	$\lvert iBM_{-5VshortMax}\rvert \leq 60$ mA

10.4.18.4 S/C BP to BM at AS

Table 438 defines the test case for S/C BP to BM at AS.

Table 438 — Test case for S/C BP to BM at AS

Name	S/C BP to BM at AS
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit between both bus wires. Additionally it is checked that the IUT is not permanently damaged by the short-circuit. This test case is skipped if the Functional class “Active star – host interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: — V_{CC} power supply of the active star: +5,0 V. In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to BM. — Communication: Node 1 and 2 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 1 and 2. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 1 and 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 1 and 2. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 1 and 2. e) Observe and acquire $iBM_{BPShortMax}$ at *TP_AS_B2_*R_{iBM} of the AS (shall be at *TPAS1_B1*). f) Stimulate the bus driver of the transmitting node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by a current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples were taken by the data acquisition unit. g) At least 500 ns after the start of transmission short-circuit BP to BM (failure FL21) of the AS at *TPAS1_B1*. h) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at

Name	S/C BP to BM at AS
	node 2. Acquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*. i) Switch off the short-circuit BP to BM (failure FL21) of the AS at *TPAS1_B1*. Wait at least 12 seconds. j) Stimulate node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. k) Stimulate node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— $\|iBM_{BPShortMax}\| \leq 60$ mA. — After switching off the failure node 1 shall receive the patterns and signal them at *TP_N1_RxD* and *TP_N1_RxEN* that are stimulated at *TP_N2_TxD* and *TP_N2_TxEN* of node 2. — After switching off the failure node 2 shall receive the patterns and signal them at *TP_N2_RxD* and *TP_N2_RxEN* that are stimulated at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.

10.4.19 Environment.Ground Shift.Dynamic Ground Shift

10.4.19.1 Active star receives pattern during ground shift at transmitter

Table 439 defines the test case for active star receives pattern during ground shift at transmitter.

Table 439 — Test case for active star receives pattern during ground shift at transmitter

Name	**Active star receives pattern during ground shift at transmitter**
Test purpose	This test checks the ability of the AS to receive a test pattern while dynamic ground shift is present at the transmitter.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: Dynamic at node 23. — Failure: None. — Communication: Node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uRxD* at *TP_N2_RxD* of node 2. d) Observe and acquire the dynamic ground shift pulse at *TP_N23_UGS* applied to node 23 according to the observation window described in 9.1.4.3. e) Stimulate the bus driver of the transmitting node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1, followed by one TSS pattern, followed by nine 50/50 patterns, followed by one 10Bit High pattern. Trigger the dynamic ground shift curve synchronously with the first rising edge after the TSS pattern.
Postamble	Standard postamble.
Pass criteria	Node 2 shall receive all patterns transmitted by node 23, i.e. the dynamic ground shift in the receiving branch of the active star shall not disturb the communication.

10.4.19.2 Receiveability of test pattern during ground shift at the AS

Table 440 defines the test case for receiveability of test pattern during ground shift at the AS.

Table 440 — Test case for receiveability of test pattern during ground shift at the AS

Name	**Receiveability of test pattern during ground shift at the AS**
Test purpose	This test checks the ability of the IUT to receive and retransmit a test pattern while dynamic ground shift is present at the AS.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: Dynamic at the AS. — Failure: None. — Communication: Node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 23. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 23. e) Observe and acquire the dynamic ground shift pulse at *TP_AS_UGS* applied to the active star according to the observation window described in 9.1.4.3. f) Stimulate the bus driver of the transmitting node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1, followed by one TSS pattern, followed by nine 50/50 patterns, followed by one 10Bit High pattern. Trigger the dynamic ground shift curve synchronously with the first rising edge after the TSS pattern.
Postamble	Standard postamble.
Pass criteria	All observed nodes shall receive all patterns transmitted by node 23, i.e. the dynamic ground shift at the active star shall not disturb the communication.

10.4.19.3 Retransmitting of test pattern during ground shift at the receiver

Table 441 defines the test case for retransmitting of test pattern during ground shift at the receiver.

Table 441 — Test case for retransmitting of test pattern during ground shift at the receiver

Name	Retransmitting of test pattern during ground shift at the receiver
Test purpose	This test checks the ability of the IUT to receive and transmit a test pattern while dynamic ground shift is present at the receiver.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: dynamic at node 23. — Failure: None. — Communication: node 2 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_N23_RxD* of node 23. d) Observe and acquire the dynamic ground shift pulse at *TP_N23_UGS* applied to node 23 according to the observation window described in9.1.4.3. e) Stimulate the bus driver of the transmitting node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one wakeup pattern as described in 9.1.3.1, followed by one TSS pattern, followed by nine 50/50 patterns, followed by one 10Bit High pattern. Trigger the dynamic ground shift curve synchronously with the first rising edge after the TSS pattern.
Postamble	Standard postamble.
Pass criteria	Node 23 shall receive all patterns transmitted by node 2, i.e. the dynamic ground shift in the transmitting branch of the active star shall not disturb the communication.

10.4.20 Environment.Common Mode Voltages

10.4.20.1 Positive common mode offset at passive star (*dStarDelay10*)

Table 442 defines the test case for positive common mode offset at passive star (dStarDelay10).

Table 442 — Test case for positive common mode offset at passive star (*dStarDelay10*)

Name	**Positive common mode offset at passive star (*dStarDelay10*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay10* (propagation delay of a negative edge through the active star) in the test system while a positive common mode offset at the passive star is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply a positive common mode offset of +12,5 V at the passive star (V_1) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence

Name	Positive common mode offset at passive star (*dStarDelay10*)
	described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay10* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.2 Positive common mode offset at passive star (*dStarDelay01*)

Table 443 defines the test case for positive common mode offset at passive star (dStarDelay01).

Table 443 — Test case for positive common mode offset at passive star (*dStarDelay01*)

Name	**Positive common mode offset at passive star (*dStarDelay01*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay01* (propagation delay of a positive edge through the active star) in the test system while a positive common mode offset at the passive star is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply a positive common mode offset of +12,5 V at the passive star (V_1) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern.

Name	Positive common mode offset at passive star (*dStarDelay01*)
	g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay01* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.3 Negative common mode offset at passive star (*dStarDelay10*)

Table 444 defines the test case for negative common mode offset at passive star (dStarDelay10).

Table 444 — Test case for negative common mode offset at passive star (*dStarDelay10*)

Name	**Negative common mode offset at passive star (*dStarDelay10*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay10* (propagation delay of a negative edge through the active star) in the test system while a negative common mode offset at the passive star is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply a negative common mode offset of -12,5 V at the passive star (V_1) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern.

Name	Negative common mode offset at passive star (*dStarDelay10*)
	g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay10* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.4 Negative common mode offset at passive star (*dStarDelay01*)

Table 445 defines the test case for negative common mode offset at passive star (dStarDelay01).

Table 445 — Test case for negative common mode offset at passive star (*dStarDelay01*)

Name	**Negative common mode offset at passive star (*dStarDelay01*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay01* (propagation delay of a positive edge through the active star) in the test system while a negative common mode offset at the passive star is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply a negative common mode offset of -12,5 V at the passive star (V_1) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern.

Name	Negative common mode offset at passive star (*dStarDelay01*)
	g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay01* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.5 Positive common mode offset at passive bus (*dStarDelay10*)

Table 446 defines the test case for positive common mode offset at passive bus (dStarDelay10).

Table 446 — Test case for positive common mode offset at passive bus (*dStarDelay10*)

Name	**Positive common mode offset at passive bus (*dStarDelay10*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay10* (propagation delay of a negative edge through the active star) in the test system while a positive common mode offset at the passive bus is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply a positive common mode offset of +12,5 V at the passive bus (V_2) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern.

Name	Positive common mode offset at passive bus (*dStarDelay10*)
	g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay10* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.6 Positive common mode offset at passive bus (*dStarDelay01*)

Table 447 defines the test case for positive common mode offset at passive bus (dStarDelay01).

Table 447 — Test case for positive common mode offset at passive bus (*dStarDelay01*)

Name	**Positive common mode offset at passive bus (*dStarDelay01*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay01* (propagation delay of a positive edge through the active star) in the test system while a positive common mode offset at the passive bus is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply a positive common mode offset of +12,5 V at the passive bus (V_2) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern.

Name	Positive common mode offset at passive bus (*dStarDelay01*)
	g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay01* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.7 Negative common mode offset at passive bus (*dStarDelay10*)

Table 448 defines the test case for negative common mode offset at passive bus (dStarDelay10).

Table 448 — Test case for negative common mode offset at passive bus (*dStarDelay10*)

Name	**Negative common mode offset at passive bus (*dStarDelay10*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay10* (propagation delay of a negative edge through the active star) in the test system while a negative common mode offset at the passive bus is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply a negative common mode offset of -12,5 V at the passive bus (V_2) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern.

Name	Negative common mode offset at passive bus (*dStarDelay10*)
	g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay10* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.8 Negative common mode offset at passive bus (*dStarDelay01*)

Table 449 defines the test case for negative common mode offset at passive bus (dStarDelay01).

Table 449 — Test case for negative common mode offset at passive bus (*dStarDelay01*)

Name	**Negative common mode offset at passive bus (*dStarDelay01*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay01* (propagation delay of a positive edge through the active star) in the test system while a negative common mode offset at the passive bus is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply a negative common mode offset of -12,5 V at the passive bus (V_2) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern.

Name	Negative common mode offset at passive bus (*dStarDelay01*)
	g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay01* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.9 Positive common mode offset at passive star and negative common mode offset at passive bus (*dStarDelay10*)

Table 450 defines the test case for positive common mode offset at passive star and negative common mode offset at passive bus (*dStarDelay10*).

Table 450 — Test case for positive common mode offset at passive star and negative common mode offset at passive bus (*dStarDelay10*)

Name	**Positive common mode offset at passive star and negative common mode offset at passive bus (*dStarDelay10*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay10* (propagation delay of a negative edge through the active star) in the test system while a positive common mode offset at the passive star is and a negative common mode offset at the passive bus are present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply synchronously: 1) a positive common mode offset of +12,5 V at the passive star (V_1) to BP and BM of

Name	Positive common mode offset at passive star and negative common mode offset at passive bus (*dStarDelay10*)
	according to 7.12. 2) a negative common mode offset of -12,5 V at the passive bus (V_2) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay10* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.10 Positive common mode offset at passive star and negative common mode offset at passive bus (*dStarDelay01*)

Table 451 defines the test case for positive common mode offset at passive star and negative common mode offset at passive bus (*dStarDelay01*).

Table 451 — Test case for positive common mode offset at passive star and negative common mode offset at passive bus (*dStarDelay01*)

Name	**Positive common mode offset at passive star and negative common mode offset at passive bus (*dStarDelay01*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay01* (propagation delay of a positive edge through the active star) in the test system while a positive common mode offset at the passive star and a negative common mode offset at the passive bus are present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply synchronously: 1) a positive common mode offset of +12,5 V at the passive star (V_1) to BP and BM of

Name	Positive common mode offset at passive star and negative common mode offset at passive bus (*dStarDelay01*)
	according to 7.12. 2) a negative common mode offset of -12,5 V at the passive bus (V_2) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay01* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.11 Negative common mode offset at passive star and positive common mode offset at passive bus (*dStarDelay10*)

Table 452 defines the test case for negative common mode offset at passive star and positive common mode offset at passive bus (*dStarDelay10*).

Table 452 — Test case for negative common mode offset at passive star and positive common mode offset at passive bus (*dStarDelay10*)

Name	**Negative common mode offset at passive star and positive common mode offset at passive bus (*dStarDelay10*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay10* (propagation delay of a negative edge through the active star) in the test system while a negative common mode offset at the passive star and a positive common mode offset at the passive bus are present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply synchronously: 1) a positive common mode offset of +12,5 V at the passive bus (V_2) to BP and BM of

Name	Negative common mode offset at passive star and positive common mode offset at passive bus (*dStarDelay10*)
	according to 7.12. 2) a negative common mode offset of -12,5 V at the passive star (V_1) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay10* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.20.12 Negative common mode offset at passive star and positive common mode offset at passive bus (*dStarDelay01*)

Table 453 defines the test case for negative common mode offset at passive star and positive common mode offset at passive bus (*dStarDelay01*).

Table 453 — Test case for negative common mode offset at passive star and positive common mode offset at passive bus (*dStarDelay01*)

Name	**Negative common mode offset at passive star and positive common mode offset at passive bus (*dStarDelay01*)**
Test purpose	This test checks the FlexRay parameter *dStarDelay01* (propagation delay of a positive edge through the active star) in the test system while a negative common mode offset at the passive star and a positive common mode offset at the passive bus are present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix E; the delay is measured twice for each transmitted data — 1 st pass according to 10.2.4.1 (42,9 µs, N12) — 2 nd pass according to 10.2.4.1 (42,9 µs + 22,1 µs, N23)
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBus* at *TPAS4_B4/2* of the receiving branches according to the observation window described in 10.2.4.1. b) Observe and acquire *uBus* at *TPAS1_B2/4* of the transmitting branches according to the observation window described in 10.2.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Apply synchronously: 1) a positive common mode offset of +12,5 V at the passive bus (V_2) to BP and BM of

Name	Negative common mode offset at passive star and positive common mode offset at passive bus (*dStarDelay01*)
	according to 7.12. 2) a negative common mode offset of -12,5 V at the passive star (V_1) to BP and BM of according to 7.12. e) Wait at least 15 µs. f) Stimulate the bus driver of the first transmitting node according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one wakeup pattern. g) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix E at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarDelay01* ≤ 150ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

10.4.21 Communication.Truncation.dStarSymbolLengthChange

10.4.21.1 Communication truncation *dStarSymbolLengthChange*

Table 454 defines the test case for communication truncation dStarSymbolLengthChange.

Table 454 — Test case for communication truncation *dStarSymbolLengthChange*

Name	**Communication truncation *dStarSymbolLengthChange***
Test purpose	This test checks the FlexRay parameter *dStarSymbolLengthChange* while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uBP* at *TPAS4_B2_BP* of the receiving branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS4_B2_BM* of the receiving branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus driver of the node 24 at *TP_N24_TxD* and *TP_N24_TxEN* by ten[a] 10Bit Low patterns.

Name	Communication truncation *dStarSymbolLengthChange*
	g) Trigger the scope to start the observation synchronously with the stimulation of node 24.
Postamble	Standard postamble.
Pass criteria	— -300ns ≤ *dStarSymbolLengthChange* ≤ 450ns — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.
a The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 455 defines the test instances for communication truncation dStarSymbolLengthChange test case defined in Table 454.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 455 — Test instances for communication truncation *dStarSymbolLengthChange*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

10.4.22 Dynamic Low Battery Voltage

10.4.22.1 Dynamic low battery occuring in *AS_Normal* mode

Table 456 defines the test case for dynamic low battery occuring in AS_Normal mode.

Table 456 — Test case for dynamic low battery occuring in *AS_Normal* mode

Name	Dynamic low battery occuring in *AS_Normal* mode
Test purpose	This test checks the behaviour of the IUT after a dynamic low battery voltage pulse according to 7.4 in *AS_Normal* mode. This test case intends to test the capability of the active star to stay in *AS_Normal* mode during the dynamic low battery pulse. This test case is applicable to all IUTs, even if no V_{BAT} supply input is implemented. In this case, the input voltage of the V_{CC} voltage regulator (the battery voltage) is stressed by the dynamic low battery voltage pulse.
Configuration	— Topology: as specified in previous configuration see 10.2. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: 11,6 V. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: 11,6 V. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test). — Test signal: V_S/t_{f1} as specified in 7.4.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus drivers of the transmitting nodes according to the sequence described

Name	Dynamic low battery occuring in *AS_Normal* mode
	on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low battery voltage pulse The bit duration in this test case shall be *gdBit*=25 µs, because the memory depth of the logic analyzer is much too small to acquire 10 seconds with a 100 ns bit time. The gap between the messages in matrix A shall be 9,25 ms. g) After the first communication round trigger the dynamic low battery pulse.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall contain all 50/50 patterns transmitted by all nodes (according to *uTxD* and *uTxEN* of all nodes), i.e. all data shall be retransmitted by the active star. — In case of an available RxEN signal re *uRxEN* of all nodes shall be in logical LOW state while *uRxD* of the corresponding node signals the received patterns and shall be in logical HIGH state otherwise. — In case of an available INH1 signal *uINH1* of the active star shall be in logical HIGH state during the test execution.

10.4.23 Dynamic Low Supply

10.4.23.1 Mode change back to *AS_Normal* after dynamic low supply voltage

Table 457 defines the test case for mode change back to AS_Normal after dynamic low supply voltage.

Table 457 — Test case for mode change back to *AS_Normal* after dynamic low supply voltage

Name	Mode change back to *AS_Normal* after dynamic low supply voltage
Test purpose	This test checks the behaviour of the IUT after a dynamic low supply voltage pulse according to 7.5 occuring in *AS_Normal* mode. This test case is skipped if — the Functional class “Active star – host interface” is implemented — the Functional class “Active star – communication controller interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of the active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of the active star: 11,6 V. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of the active star: 11,6 V. — In case that V_{IO} is implemented: V_{IO} reference voltage of the active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test). — Test signal Case 1.1 as specified in 7.5.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star.

Name	Mode change back to *AS_Normal* after dynamic low supply voltage
	f) Start the dynamic low supply voltage pulse at the power supply of the active star. g) Wait until the power supply voltage(s) rise(s) above the specific undervoltage thresholds. h) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern as described in 9.1.3.1. i) Stimulate the bus drivers according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low supply voltage pulse. j) Trigger the logic analyzer to start synchronously with the first falling edge of *uTxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The observation window shall start with the first falling edge of *uTxEN* of node 1. Adaptation of the thresholds for digital signals may be required. — *uRxD* of all nodes shall contain all 50/50 patterns transmitted by all nodes (according to *uTxD* and *uTxEN* of all nodes) at least after the first communication round, i.e. all data shall be retransmitted by the active star after the wakeup has been detected. — In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical HIGH state latest 104 µs after the beginning of the first wakeup pattern until the end of the test execution.

Table 458 defines the test instances for mode change back to AS_Normal after dynamic low supply voltage test case defined in Table 457.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 458 — Test instances for mode change back to *AS_Normal* after dynamic low supply voltage

Instance		1	2	3	4
Purpose	**Stress**	—	—	—	—
	Precondition	—	—	—	—
Configuration	**Power supply**	Test signal: Case 1.1 as specified in 7.5	Test signal: case 1.2 as specified in 7.5	Test signal: Case 2.1 as specified in 7.5	Test signal: Case 2.2 as specified in 7.5
	Ground shift	—	—	—	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

11 Test cases for Active Stars with communication controller interface

11.1 Configuration

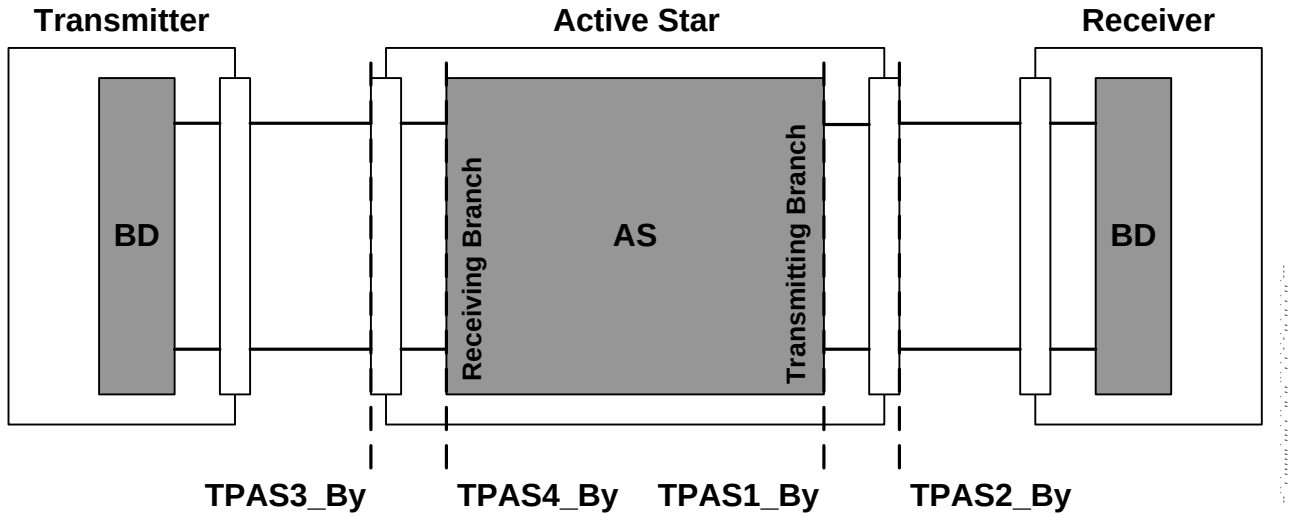
11.1.1 Topology

As specified in 6.4. All IUTs of the Active Star are of the same type and from the same manufacturer.

11.1.2 Test planes

11.1.2.1 Analog signals

The test planes at the FlexRay Active Star for analog signal measurement are specified as depicted in Figure 66.



Components

AS Active Star

BD Bus Driver

Connections and supplies

TPASx_By Test plane x at the Active Star branch y (see Table 459)

Figure 66 — Planes at the analog interface

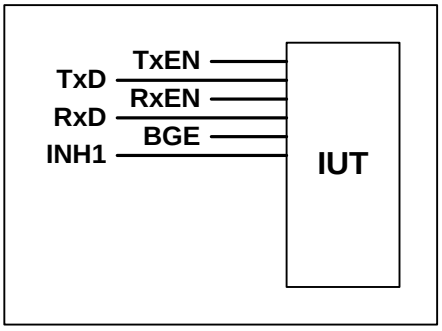
Table 459 defines the test planes at the analog interface.

Table 459 — Test planes at the analog interface

TP Name	Signals	Description
TPAS1_By [a]	*uBus*	Differential bus signal of the transmitting branch, as close as possible to the IUT
TPAS4_By [a]	*uBus*	Differential bus signal of the receiving branch, as close as possible to the IUT
TPAS1_By_BP	*uBP*	Transmitting branch, test plane as close as possible to the IUT
TPAS1_By_BM	*uBM*	Transmitting branch, test plane as close as possible to the IUT
NOTE The naming of the branches corresponds to 10.2.2.1.		
[a] y stands for the number of the branch of the Active Star.		

11.1.2.2 Digital signals

The test planes at the FlexRay Active Star for digital signals are specified as depicted in Figure 67.



Components

IUT Implementation Under Test

Connections and supplies

BGE BG Enable input signal

INH1 INH1 output signal

RxD Receive Data output signal of the IUT

RxEN Receive Data Enable Not output signal

TxEN Transmit Data Enable Not input signal

TxD Transmit Data input signal

Figure 67 — Test planes at digital interfaces of the Active Star for the logic analyzer

Table 460 defines the test planes at digital interfaces of the Active Star for the logic analyzer.

Table 460 — Test planes at digital interfaces of the Active Star for the logic analyzer

TP Name	Signals	Description
TP_AS_TxD	TxD	Transmit Data signal of the IUT
TP_AS_TxEN	TxEN	Transmit Enable Not signal of the IUT
TP_AS_RxD	RxD	Receive Data signal of the IUT
TP_AS_BGE	BGE	Bus Guardian Enable signal of the IUT (optional)
TP_AS_RxEN	RxEN	Receive Enable Not signal of the IUT (optional)
TP_AS_INH1	INH1	Inhibit signal of the IUT (optional)

11.1.2.3 Naming convention

This subclause corresponds to 9.1.2.3 where "*Nx*" shall be read as "*AS*".

11.1.2.4 Test planes for the oscilloscope

The oscilloscope observes the following test planes:

— *TP_AS_RxD*

— *TP_AS_TxD*

— *TP_N23_RxD*

— *TP_N23_TxD*

— *TP_N23_TxEN*

— *TP_N2_TxD*

— *TP_N2_TxEN*

— *TPAS1_By* [27)]

— *TPAS4_By* [28)]

— *TPAS1_By_BM*

— *TPAS1_By_BP*

— *TP_AS_UGS* (dynamic ground shift voltage)

27) y stands for the number of the branch of the Active Star.

28) y stands for the number of the branch of the Active Star.

11.1.2.5 Test planes for the pattern generator

The pattern generator stimulates the following test planes:

— *TP_AS_TxD*

— *TP_AS_TxEN*

— *TP_AS_WAKE*

11.1.3 Test patterns

This subclause corresponds to 9.1.3 and 10.2.3.

11.1.4 Observation windows

This subclause corresponds to 9.1.4 where "*BD*" shall be read as "*AS*".

11.1.5 Operation modes of the Active Star

This subclause corresponds to 10.2.5.

11.1.6 Power supplies

This subclause corresponds to 10.2.6.

11.1.7 Stress

This subclause corresponds to 10.2.7.

11.1.8 Failures

Failures of the Active Star are also described in 7.6.

11.1.9 Mandatory features

11.1.9.1 General

The features stated in the following subclauses are mandatory and shall be tested in the test cases for Active Stars.

11.1.9.2 Functional class "Active Star – communication controller interface"

This functional class requires the following optional features to be implemented in coexistence:

— Signal RxD

— Signal TxD

— Signal TxEN

11.1.10 Optional features

The features stated in the following subclauses are optional as specified in ISO 17458-4 and shall only be tested in the test cases for Active Stars if available in the IUT.

11.1.10.1 Functional class “Active Star – bus guardian interface”

This functional class requires the following optional features to be implemented in coexistence:

— Signal RxEN (optional within this functional class)

— Signal BGE

11.1.10.2 Functional class “Active Star – voltage regulator control”

This functional class requires the following optional features to be implemented in coexistence:

— Signal INH1

— Power supply input V_{BAT}

— Power supply input V_{CC}

— Active Star – wake interface (optional within this functional class)

11.1.10.3 Functional class “Active Star – internal voltage regulator”

This functional class requires the following optional features to be implemented in coexistence:

— Power supply input V_{BAT}

— Signal INH1 (optional within this functional class)

— Active Star – wake interface (optional within this functional class)

This functional class requires that no V_{CC} supply input is present.

11.1.10.4 Functional class “Active Star – logic level adaptation”

This functional class requires the implementation of a logic level-shift interface and requires that the thresholds of all digital inputs are controlled by this voltage as well as all digital outputs are related to this level.

11.1.10.5 Functional class “Active Star increased voltage amplitude transmitter”

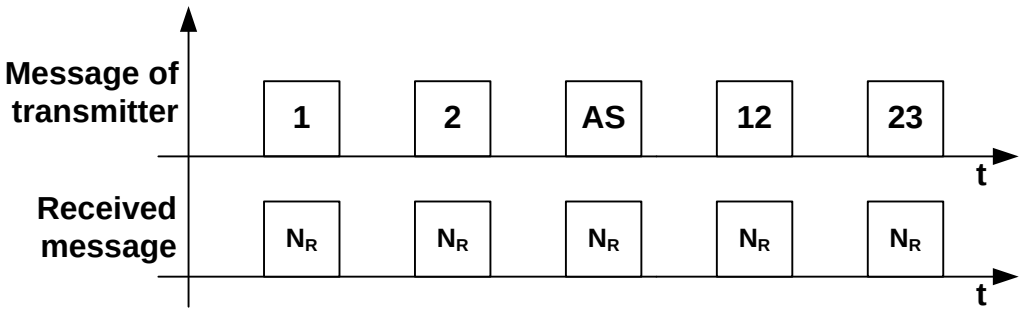
This Functional Class comprises the minimum of *uStarTxActive* to be 900 mV.

11.1.11 Definition of communication

11.1.11.1 Matrix F (round robin test only with terminated node)

In some test instances it is necessary that every terminated node and the Active Star are the transmitter and all other terminated nodes and the Active Star are the receivers.

This matrix is used for observation of bus signals. Figure 68 depicts the communication matrix F.



Key

N_R	Receiving nodes
1	Node 1
2	Node 2
12	Node 12
23	Node 23

NOTE The receivers are all terminated nodes except the transmitter.

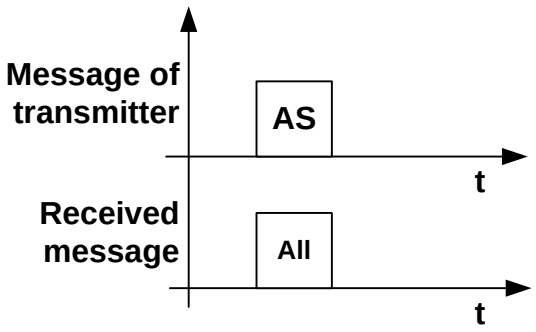
Figure 68 — Communication matrix F

Pause between the messages: 20 µs.

11.1.11.2 Active Star as transmitter

In some test instances it is necessary that the AS is the transmitter (digital interface) and all other terminated nodes are the receivers.

This communication is used for testing the digital interface. Figure 69 depicts the communication Active Star as transmitter (timing).



Key

AS	Message transmitted by the Active Star
All	Message received by all nodes

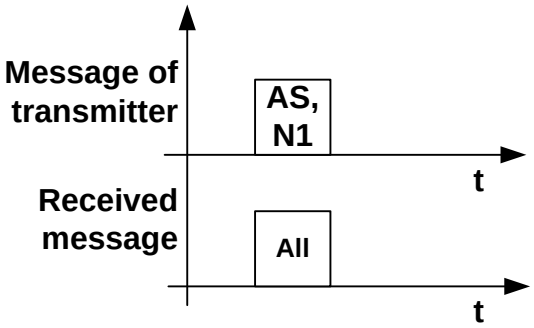
Figure 69 — Communication Active Star as transmitter (timing)

11.1.11.3 Single node

In some test cases only one transmitter (node 1 or node 2) is required to stimulate one receiving branch of the Active Star.

11.1.11.4 Node 1 and Active Star as transmitter

In some test cases node 1 and the Active Star are required for collision scenarios in the Active Star. Figure 70 depicts the communication node 1 and Active Star (timing).



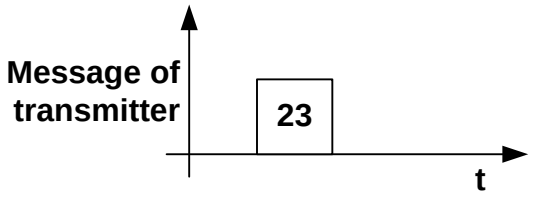
Key

AS, N1	Messages transmitted by the Active Star and node 1
All	Message(s) received by all nodes

Figure 70 — Communication node 1 and Active Star (timing)

11.1.11.5 Node 23 as transmitter

In this communication node 23 is the transmitter. Figure 71 depicts the communication with node 23 as transmitter (time diagram).



Key

23	Message transmitted by node 23

Figure 71 — Communication with node 23 as transmitter (timing)

11.1.12 Standard preamble

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure condition.

e) TxEN and TxD of all nodes shall be in logical HIGH (idle) state.

f) In case a BGE signal is available, this signal shall be in logical HIGH state at all nodes and the Active Star.

g) In case of a WAKE pin this signal shall be in logical HIGH state.

h) Stimulate Bus Drivers of all nodes via host command to enter *BD_Normal*.

i) Make sure that the Active Star is in *AS_Normal* mode when this preamble is left and the test execution is entered, e.g. by switching on the power supply of the Active Star just before the end of the preamble.

11.1.13 Sleep preamble

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure condition.

e) TxEN and TxD of all nodes shall be in logical HIGH (idle) state.

f) In case a BGE signal is available, this signal shall be in logical HIGH state at all nodes and the Active Star.

g) In case of a WAKE pin this signal shall be in logical HIGH state.

h) Stimulate Bus Drivers of all nodes via host command to enter *BD_Normal*.

i) Wait 6 400 ms to make sure that the Active Star enters *AS_Sleep*.

11.1.14 Standard postamble

a) Set ground shift to 0V.

b) Reset failures.

c) Switch off all power supplies.

11.2 Static test cases

The motivation of static test cases is to check the availability and the boundaries in the data sheet of the IUT (topology independent).

Every parameter shall be part of the data sheet and fulfill the specified boundaries. If at least one parameter does not pass this test, the result of the whole conformance test is failed.

Table 461 defines the static test cases for Active Stars with communication controller interface.

Table 461 — Static test cases for Active Stars with communication controller interface

Index	Parameter	SOVS Brace	Description	Min	Max	Unit
1.	*dStarRxAsym*	Communication. Delay	Receiver delay mismatch [a, b]		10	ns
2.	*dStarRx10*	Communication. Delay	Receiver delay, negative edge [a]		225	ns
3.	*dStarRx01*	Communication. Delay	Receiver delay, positive edge [a]		225	ns
4.	*dStarRxai*	Communication.Active Star. Timing	Idle reaction time [c]	50	550	ns
5.	*dStarRxia*	Communication.Active Star. Timing	Activity reaction time [c]	100	550	ns
6.	*dStarTxAsym*	Communication. Delay	Transmitter delay mismatch [b, d]		10	ns
7.	*dStarTx10*	Communication. Delay	Transmitter delay, negative edge [d,e]		225	ns
8.	*dStarTx01*	Communication. Delay	Transmitter delay, positive edge [d,e]		225	ns
9.	*dStarTxai*	Communication. Timing.Active Star	Propagation delay active → idle [e]		550	ns
10.	*dStarTxia*	Communication. Active Star.Timing	Propagation delay idle → active [e]		550	ns
11.	$uV_{DIG\text{-}OUT\text{-}HIGH}$	Communication. Threshold	Output voltage on a digital output, when in logical high state [f, g, h, i]	80	100	%
12.	$uV_{DIG\text{-}OUT\text{-}LOW}$	Communication. Threshold	Output voltage on a digital output, when in logical high state [f, g, h, i]		20	%
13.	$uV_{DIG\text{-}IN\text{-}HIGH}$	Communication. Threshold	Threshold for detecting a digital input as on logical high [g, h]		70	%
14.	$uV_{DIG\text{-}IN\text{-}LOW}$	Communication. Threshold	Threshold for detecting a digital input as on logical low [g, h]	30		%
15.	*uData0*	Communication. Threshold	Receiver threshold for detecting Data_0	-300 [j]	-150 [j]	mV
16.	*uData1*	Communication. Threshold	Receiver threshold for detecting Data_1	150 [j]	300 [j]	mV
17.	*uData1* - | *uData0* |	Communication. Threshold	Mismatch of receiver thresholds [k]	-30	+30	mV
18.	*uStarLogic_1*	Communication. Threshold	Threshold for detecting logical high [h]		60	%
19.	*uStarLogic_0*	Communication. Threshold	Threshold for detecting logical low [h]	40		%

Index	Parameter	SOVS Brace	Description	Min	Max	Unit
20.	*dStarRxDR15* + *dStarRxDF15*	Communication. Timing.Active Star	Sum of rise and fall time at 15 pF load [l]	—	13	ns
21.	Functional Class "Active Star – Communication controller interface"	Functional Class	Checks the complete implementation of all specified options			
22.	*dStarTxRxai*	Communication. Active Star.Timing	Idle-Loop delay	—	325	ns
23.	*C_StarTxD*	Environment	Input capacitance on TxD pin	—	10	pF
24.	$uV_{DIG\text{-}OUT\text{-}UV}$	Communication. Threshold	Output voltage on a digital output at 100 kΩ load, when VDIG in undervoltage [m]	—	500	mV
25.	*uData0_LP*	Communication. Threshold	Low power receiver threshold for detecting Data_0 [n]	-400	-100	mV
26.	$uV_{DIG\text{-}OUT\text{-}OFF}$	Communication. Threshold	Output voltage on a digital output at 100 kΩ load, when unsupplied [m] Checks the existence of this parameter in the datasheet	product specific	product specific	
27.	*dStarTSS LengthChange_TxD_Bus*	Communication. Truncation	TSS length change from TxD pin to signal on all branches [e]	-450	0	ns
28.	*dStarFES1 LengthChange_TxD_Bus*	Communication. Truncation	FES1 length change from TxD pin to signal on all branches [e]	0	450	ns
29.	*dStarSymbol LengthChange_TxD_Bus*	Communication. Truncation	Symbol length change from TxD pin to signal on all branches [e]	-300	400	ns
30.	*dStarTSS LengthChange_Bus_RxD*	Communication. Truncation	TSS length change from branch to RxD pin	-450	0	ns
31.	*dStarFES1 LengthChange_Bus_RxD*	Communication. Truncation	FES1 length change from branch to RxD pin	0	450	ns
32.	*dStarSymbol LengthChange_Bus_RxD*	Communication. Truncation	Symbol length change from branch to RxD pin	-300	400	ns
33.	*dStarActivity Detection*	Communication. Timing.Active Star	Active Star filter time for activity detection	100	250	ns
34.	*dStarIdle Detection*	Communication. Timing.Active Star	Active Star filter time for Idle detection	50	200	ns
35.	| *dStarRxDR15* - *dStarRxDF15* |	Communication. Timing.Active Star	Difference of rise and fall time at 15 pF load	—	5	ns
36.	*dStarTxActive Max*	Communication. Timing.Active Star	Maximum length of transmitter activation	650	2 600	µs
37.	*dStarTxreaction*	Communication. Timing.Active Star	TxD reaction time after TxEN HIGH	—	75	ns

Index	Parameter	SOVS Brace	Description	Min	Max	Unit

[a] To be tested with a signal according to the definitions that are done in ISO 17458-4.

[b] Shall be guaranteed for ±300 mV as well as for ±150 mV level of *uBus*.

[c] To be tested with a signal according to the definitions that are done in ISO 17458-4.

[d] TxD test signal rise and fall time shall be at least 9 ns (20 % – 80 % V_{DIG}).

[e] Load on BP/BM: 40 Ω || 100 pF

[f] Load conditions are product specific and documented in the product datasheet.

[g] In case a reference voltage for digital IO is available via a V_{IO} pin, then $uV_{DIG} = uV_{IO}$, otherwise $uV_{DIG} = uV_{CC}$

[h] Relative to V_{DIG}

[i] Condition: no undervoltage on V_{DIG} and either V_{CC} or V_{BAT} supplied (product specific supply thresholds below undervoltage thresholds, e.g. in *BD_Off* or *AS_Off* mode)

[j] Take into account the footnotes for this parameter in ISO 0 0000-4

[k] Test with (*uBP* + *uBM*)/2 = *uCM* = 2,5 V

[l] 20 % – 80 % V_{DIG}. A datasheet for the BD/CC/AS shall state maximum rise and fall time on RxD/TxD separately.

[m] Product specific supply thresholds below undervoltage thresholds, e.g. in *BD_Off* or *AS_Off* mode

[n] Prerequisite: $uV_{BAT} \geq 7$ V (if applicable, otherwise $uV_{CC} = 5$ V)

11.3 Test cases

11.3.1 Communication.Delay.dStarTx01

11.3.1.1 Transmitter delay *dStarTx01*

Table 462 defines the test case for transmitter delay dStarTx01.

Table 462 — Test case for transmitter delay dStarTx01

Name	**Transmitter delay *dStarTx01***
Test purpose	This test checks the transmitter delay *dStarTx01* from *low* to *high* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Active Star as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star according to the observation window described in 9.1.4.1. b) Observe and acquire *uBus* at *TPAS1_B2* of the active star according to the observation window described in 9.1.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Stimulate the IUT (the active star) at *TP_AS_TxD* and *TP_AS_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 10Bit High pattern, followed by one 10Bit Low pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarTx01* ≤ 225ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 463 defines the test instances for transmitter delay dStarTx01 test case defined in Table 462.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 463 — Test instances for transmitter delay *dStarTx01*

Instance		**1**	**2**	**3**	**4**	**5**	**6**
Purpose	**Stress**	none	ground shift at transmitter	ground shift at receiver	low battery	min. bus load	max. bus load
	Precondition	—	—	—	AS_VRC or AS_IVR impl.	—	—
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V	—	—
	Ground shift	—	+5,0 V at AS	+5,0 V at N23	—	—	—
	Failure	—	—	—	—	FL7 at N23	FL8 at N23
Preamble		—	—	—	—	—	—
Test execution		—	—	—	—	—	—
Pass criteria		—	—	—	—	—	—

11.3.2 Communication.Delay.dStarTx10

11.3.2.1 Transmitter delay *dStarTx10*

Table 464 defines the test case for transmitter delay dStarTx10.

Table 464 — Test case for transmitter delay *dStarTx10*

Name	**Transmitter delay *dStarTx10***
Test purpose	This test checks the transmitter delay *dStarTx10* from *high* to *low* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Active Star as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star according to the observation window described in 9.1.4.1. b) Observe and acquire *uBus* at *TPAS1_B2* of the active star according to the observation window described in 9.1.4.1. c) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. d) Stimulate the IUT (the active star) at *TP_AS_TxD* and *TP_AS_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 10Bit High pattern, followed by one 10Bit Low pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarTx10* ≤ 225ns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 465 defines the test instances for transmitter delay dStarTx10 test case defined in Table 464.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 465 — Test instances for transmitter delay *dStarTx10*

Instance		**1**	**2**	**3**	**4**	**5**	**6**
Purpose	**Stress**	none	ground shift at transmitter	ground shift at receiver	low battery	min. bus load	max. bus load
	Precondition	—	—	—	AS_VRC or AS_IVR impl.	—	—
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V	—	—
	Ground shift	—	+5,0 V at AS	+5,0 V at N23	—	—	—
	Failure	—	—	—	—	FL7 at N23	FL8 at N23
Preamble		—	—	—	—	—	—
Test execution		—	—	—	—	—	—
Pass criteria		—	—	—	—	—	—

11.3.3 Communication.Delay.dStarRx01

11.3.3.1 Receiver delay *dStarRx01*

Table 466 defines the test case for receiver delay dStarRx01.

Table 466 — Test case for receiver delay *dStarRx01*

Name	**Receiver delay *dStarRx01***
Test purpose	This test checks the receiver delay *dStarRx01* from *low* to *high* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. c) Observe and acquire *uBus* at *TPAS4_B2* of the active star according to the observation window described in 9.1.4.1. d) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star according to the observation window described in 9.1.4.1. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus driver in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 10Bit High pattern, followed by one 10Bit Low pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarRx01* ≤ 225ns.

Name	Receiver delay *dStarRx01*
	— In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 467 defines the test instances for receiver delay dStarRx01 test case defined in Table 466.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 467 — Test instances for receiver delay *dStarRx01*

Instance		1	2	3	4	5	6
Purpose	**Stress**	none	ground shift at transmitter	ground shift at receiver	low battery	min. bus load	max. bus load
	Precondition	—	—	—	AS_VRC or AS_IVR impl.	—	—
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V	—	—
	Ground shift	—	+5,0 V at N23	+5,0 V at AS	—	—	—
	Failure	—	—	—	—	FL7 at N23	FL8 at N23
Preamble		—	—	—	—	—	—
Test execution		—	—	—	—	—	—
Pass criteria		—	—	—	—	—	—

11.3.4 Communication.Delay.dStarRx10

11.3.4.1 Receiver delay *dStarRx10*

Table 468 defines the test case for receiver delay dStarRx10.

Table 468 — Test case for receiver delay *dStarRx10*

Name	**Receiver delay *dStarRx10***
Test purpose	This test checks the receiver delay *dStarRx10* from *high* to *low* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. b) Observe and acquire *uTxEN* at *TP_N23_TxD* of node 23. c) Observe and acquire *uBus* at *TPAS4_B2* of the active star according to the observation window described in 9.1.4.1. d) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star according to the observation window described in 9.1.4.1. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus driver in node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 10Bit High pattern, followed by one 10Bit Low pattern.
Postamble	Standard postamble.
Pass criteria	— *dStarRx10* ≤ 225ns.

Name	Receiver delay *dStarRx10*
	— In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 469 defines the test instances for receiver delay dStarRx10 test case defined in Table 468.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 469 — Test instances for receiver delay *dStarRx10*

Instance		1	2	3	4	5	6
Purpose	**Stress**	none	ground shift at transmitter	ground shift at receiver	low battery	min. bus load	max. bus load
	Precondition	—	—	—	AS_VRC or AS_IVR impl.	—	—
Configuration	**Power supply**	—	—	—	V_{BAT} = 5,5 V	—	—
	Ground shift	—	+5,0 V at N23	+5,0 V at AS	—	—	—
	Failure	—	—	—	—	FL7 at N23	FL8 at N23
Preamble		—	—	—	—	—	—
Test execution		—	—	—	—	—	—
Pass criteria		—	—	—	—	—	—

11.3.5 Mode.Active Star.Normal

11.3.5.1 Operation mode change to *AS_Normal* in case of power on of $V_{StarSupply}$

Table 470 defines the test case for operation mode change to AS_Normal in case of power on of VStarSupply.

Table 470 — Test case for operation mode change to *AS_Normal* in case of power on of VStarSupply

Name	Operation mode change to *AS_Normal* in case of power on of VStarSupply
Test purpose	This test checks the ability of the IUT to change from *AS_Off* mode to *AS_Standby* to *AS_Normal* due to power on $V_{StarSupply}$ according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that V_{CC} is implemented: external V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: external V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: AS as transmitter.
Preamble (setup state)	— Standard preamble. — Disable outputs of power supplies of IUT in active star from where the supply is derived.
Test execution	a) Observe and acquire *uTxD* at *TP_AS_TxD* of the AS. b) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the AS. c) Observe and acquire *uRxD* at *TP_AS_RxD* of the AS d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. e) In case of an available INH signal observe and acquire *uINH1* at *TP_AS_INH1*. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. h) Enable power supplies of IUT in active star from where the supply is derived. i) Wait 100 µs + 10 ms [a] . j) Stimulate the active star at *TP_AS_TxD* and *TP_AS_TxEN* by one TSS pattern, followed by one 50/50 pattern. k) Trigger the logic analyzer to start the observation synchronously with the stimulation of

Name	Operation mode change to *AS_Normal* in case of power on of VStarSupply
	the active star at *TP_AS_TxD* and *TP_AS_TxEN*.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uRxD* of all observed nodes and the active star shall contain the 50/50 pattern transmitted by the AS, i.e. the active star shall enter *AS_Normal* mode within 100 µs + 10 ms [a] after power on and transmit the test patterns of the AS. — In case of an available RxEN signal *uRxEN* of all nodes and the active star shall be in logical HIGH state before the active star is stimulated (falling edge of *uTxD* and *uTxEN*) and shall be in logical LOW state while *uRxD* of the corresponding node signals the received patterns. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state (*Not_Sleep*) during the observation window.
[a] Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least.	

Table 471 defines the test instances for operation mode change to AS_Normal in case of power on of VStarSupply test case defined in Table 470.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 471 — Test instances for operation mode change to *AS_Normal* in case of power on of VStarSupply

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

11.3.6 Mode.Active Star.Normal.GoToSleep

11.3.6.1 Operation mode change to *AS_Sleep* after *dStarGoToSleep*

Table 472 defines the test case for operation mode change to AS_Sleep after dStarGoToSleep.

Table 472 — Test case for operation mode change to *AS_Sleep* after *dStarGoToSleep*

Name	**Operation mode change to *AS_Sleep* after *dStarGoToSleep***
Test purpose	This test checks the ability of the active star to go to *AS_Sleep* mode if all branches are in *Branch_Idle* for longer than *dStarGoToSleep* according to ISO 17458-4 while no stress condition is present. Additionally, the behaviour at the local communication controller interface and, if available, the local bus guardian interface is verified.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Active Star as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. b) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. c) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. f) Stimulate the IUT (AS) at *TP_AS_TxD* and *TP_AS_TxEN* by one wakeup pattern, followed by one TSS pattern, followed by one 10Bit Low pattern. g) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_AS_TxEN* of the active star.

Name	Operation mode change to *AS_Sleep* after *dStarGoToSleep*
	h) Wait 6 400 ms.
Postamble	Standard postamble.
Pass criteria	The period to observe is very long in this test case. But a bit level resolution is not required. The Go-To-Sleep timeout *dStarGoToSleep* shall be measured with an error of less than 1 %. — *uRxD* of the active star shall be in logical HIGH state after the stimulation at *TP_AS_TxD* and *TP_AS_TxEN* and until the end of the test execution. — In case of an available INH1 signal *uINH1* shall initially be in logical HIGH state for at least 640 ms. Between 640 ms and 6 400 ms after the start of the observation, *uINH1* shall change to logical LOW state. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state after the stimulation at *TP_AS_TxD* and *TP_AS_TxEN* until the end of the test execution.

Table 473 defines the test instances for operation mode change to AS_Sleep after dStarGoToSleep test case defined in Table 472.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 473 — Test instances for operation mode change to *AS_Sleep* after *dStarGoToSleep*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.7 Mode.Active Star.Normal.GoToSleep_Fail

11.3.7.1 Operation mode change to *AS_Sleep* after *dStarGoToSleep* (FailSilent)

Table 474 defines the test case for operation mode change to AS_Sleep after dStarGoToSleep (FailSilent).

Table 474 — Test case for operation mode change to *AS_Sleep* after *dStarGoToSleep* (FailSilent)

Name	Operation mode change to *AS_Sleep* after *dStarGoToSleep* (FailSilent)
Test purpose	This test checks the ability of the active star to go to *AS_Sleep* mode if one branch is in *Branch_FailSilent* and all other branches are in *Branch_Idle* for longer than *dStarGoToSleep* according to ISO 17458-4 while no stress condition is present. Additionally, the behaviour at the local communication controller interface and, if available, the local bus guardian interface is verified.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: none.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of the nodes 21..24 (branch 2), node 1 (branch 1) and node 2 (branch 3).
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.6. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.6. c) Observe and acquire *uBus* at *TPAS4_B4* of the receiving branch 4 according to the observation window described in 10.2.4.6. d) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. g) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by

Name	Operation mode change to *AS_Sleep* after *dStarGoToSleep* (FailSilent)
	one babbling idiot pattern as defined in 10.2.3.1. Repeat this pattern for at least 6 400 ms + 2 600 µs. h) Trigger the logic analyzer to start the observation synchronously with the begin of the babbling idiot stimuli.
Postamble	Standard postamble.
Pass criteria	The period to observe is very long in this test case. But a bit level resolution is not required. The Go-To-Sleep timeout *dStarGoToSleep* shall be measured with an error of less than 1 %. *uBP* and *uBM* of branch 2 indicate *Data_0* state initially, i.e. the active star retransmits the babbling idiot pattern before branch 4 enters *Branch_FailSilent*. Then, branch 2 enters *Idle* state. — *uRxD* of the active star shall be in logical LOW state for at least 650 µs initially, i.e. the active star signals the babbling idiot pattern received at branch 4 on the local communication controller interface. — *uRxD* of the active star shall change to logical HIGH state between 650 µs and 2 600 µs after the start of the babbling idiot sequence and shall remain at logical HIGH state until the end of the test execution, i.e. branch 4 is excluded from communication by the active star after the noise detection timeout *dBranchRxActiveMax*. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state for at least 650 µs initially, i.e. the active star signals the babbling idiot pattern received at branch 4 on the local communication controller interface. — In case of an available RxEN signal *uRxEN* of the active star shall change to logical HIGH state between 650 µs and 2 600 µs after the start of the babbling idiot sequence and shall remain at logical HIGH state until the end of the test execution, i.e. branch 4 is excluded from communication by the active star after the noise detection timeout *dBranchRxActiveMax*. — Between 640 ms and 6 400 ms after branch 2 has entered *Idle* state, i.e. *uBP* and *uBM* of branch 2 are between 1 800 mV and 3 200 mV (*Idle*), *uBP* and *uBM* of branch 2 change to a voltage level between -200 mV and +200 mV (*Idle_LP*). — In case of an available INH1 signal *uINH1* shall be in logical HIGH state for at least 640 ms + 650 µs after the first rising edge in *uRxD* of the AS. Between 640 ms + 650 µs and 6 400 ms + 2 600 µs after this edge, *uINH1* shall change to logical LOW state, i.e. the active star shall enter *AS_Sleep* mode if all branches are in *Branch_Idle* or *Branch_FailSilent* for *dStarGoToSleep*.

Table 475 defines the test instances for operation mode change to AS_Sleep after dStarGoToSleep (FailSilent) test case defined in Table 474.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 475 — Test instances for operation mode change to *AS_Sleep* after *dStarGoToSleep* (FailSilent)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.8 Mode.Active Star.Branch.Idle

11.3.8.1 Check AS transmitter activation via TxEN (*Branch_Idle*)

Table 476 defines the test case for check AS transmitter activation via TxEN (Branch_Idle).

Table 476 — Test case for check AS transmitter activation via TxEN (*Branch_Idle*)

Name	**Check AS transmitter activation via TxEN (*Branch_Idle*)**
Test purpose	This test checks the activation of the transmitter of the active star via the TxEN signal of the local communication controller interface according to ISO 17458-4 while no stress condition is present and the branches of the active star are in *Branch_Idle* state and signal *Idle* to the central logic of the active star respectively.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Active Star as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. b) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star.

Name	Check AS transmitter activation via TxEN (*Branch_Idle*)
	h) Stimulate the IUT (AS) at *TP_AS_TxD* and *TP_AS_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall be in logical HIGH state before the IUT is stimulated to transmit. — *uRxD* of the active star shall be in logical HIGH state before the IUT is stimulated to transmit. After the IUT is stimulated *uRxD* of the active star shall contain the patterns transmitted at *uTxD* and *uTxEN* (loopback functionality). — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state before the IUT is stimulated to transmit and shall be in logical LOW state while *uRxD* of the active star signals the received pattern. — *uRxD* of all nodes shall contain the 50/50 pattern transmitted by the IUT. — In case of an available INH1 signal *uINH1* of the active star shall be in logical HIGH state during the test execution.

Table 477 defines the test instances for check AS transmitter activation via TxEN (Branch_Idle) test case defined in Table 476.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 477 — Test instances for check AS transmitter activation via TxEN (*Branch_Idle*)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.8.2 Check *dStarSetUpDelay*

Table 478 defines the test case for check dStarSetUpDelay.

Table 478 — Test case for check *dStarSetUpDelay*

Name	**Check *dStarSetUpDelay***
Test purpose	This test checks the FlexRay parameter *dStarSetUpDelay* while no stress condition is present. This test case verifies that a second incoming data stream reaching the active star (to a branch of the AS) slightly after *dStarSetUpDelay* is ignored by the active star while the CC interface receives already a data stream.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Node 1 and AS as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. b) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. c) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. d) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 1 (branch 1). f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes except node 1 (branch 1). h) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. i) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the

Name	Check *dStarSetUpDelay*
	active star. j) Stimulate the IUT (AS) at *TP_AS_TxD* and *TP_AS_TxEN* with the pattern A as defined in 10.2.4.3. k) Stimulate node 1 at *TP_N1_TxD* and *TP_N1_TxEN* with the pattern B as defined in 10.2.4.3. Start stimulation of node 1 500 ns after the start of the transmission at the CC interface of the AS.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all observed nodes and the active star shall only contain pattern A that was applied to the communication controller interface of the active star. — The pattern B that was stimulated to node 1 shall not be retransmitted by the active star because the incoming data stream at branch 1 shall be ignored after *dStarSetUpDelay*. — In case of an available INH1 signal *uINH1* of the active star shall be in logical HIGH state during the test execution.

Table 479 defines the test instances for check dStarSetUpDelay test case defined in Table 478.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 479 — Test instances for check *dStarSetUpDelay*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.9 Communication.Transmitter Activation

11.3.9.1 Check AS transmitter activation via TxEN (*Branch_Transmit*)

Table 480 defines the test case for check AS transmitter activation via TxEN (Branch_Transmit).

Table 480 — Test case for check AS transmitter activation via TxEN (*Branch_Transmit*)

Name	**Check AS transmitter activation via TxEN (*Branch_Transmit*)**
Test purpose	This test checks the activation of the transmitter of the active star via the TxEN signal of the local communication controller interface according to ISO 17458-4 while no stress condition is present. Activation shall not be possible when the branches of the active star are in *Branch_Transmit* already, i.e. it shall not be possible to disturb ongoing communication via the local communication controller interface.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: node 1 and active star as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. b) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. c) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. d) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. e) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all

Name	Check AS transmitter activation via TxEN (*Branch_Transmit*)
	nodes. i) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. j) Stimulate the bus driver in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one TSS pattern, followed by five 50/50 patterns. k) Stimulate the IUT (AS) at *TP_AS_TxD* and *TP_AS_TxEN* by one TSS pattern, followed by one 10Bit High pattern. Start the stimulation delayed by 1 µs to the stimulation of node 1, i.e. the stimulation at the local communication controller interface of the active star occurs while the branches are in *Branch_Transmit* already.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all observed nodes shall contain all 50/50 patterns transmitted by node 1, i.e. the stimulus at the local communication controller interface of the active star does not disturb ongoing communication. — *uRxD* of the active star shall contain all 50/50 patterns transmitted by node 1, i.e. the stimulus at the local communication controller interface of the active star does not disturb ongoing communication. — In case of an available INH1 signal *uINH1* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state while *uRxD* of the active star signals the patterns received from node 1 and in logical HIGH state otherwise.

Table 481 defines the test instances for check AS transmitter activation via TxEN (Branch_Transmit) test case defined in Table 480.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 481 — Test instances for check AS transmitter activation via TxEN (*Branch_Transmit*)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.9.2 Transmission enable after TxD changes to Data_0

Table 482 defines the test case for transmission enable after TxD changes to Data_0.

Table 482 — Test case for transmission enable after TxD changes to *Data_0*

Name	**Transmission enable after TxD changes to *Data_0***
Test purpose	This test checks the ability of the IUT not to start a transmission with a *Data_1* as specified in ISO 17458-4. But the transmission shall be executed as soon as TxD changes to *Data_0*.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Active star as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. b) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Observe and acquire the error signal of the host interface (*TP_N23_ERRN* or *TP_N23_INTN*) of node 23. g) Observe and acquire *uBus* at *TP_N23_BP* and *TP_N23_BM* of node 23. h) Stimulate the IUT (AS) at *TP_AS_TxD* and *TP_AS_TxEN* by six 10Bit High pattern as specified in 9.1.3.7, followed by a TSS pattern and a 50/50 pattern. i) Trigger the scope to start synchronously with the stimulation of the active star according

Name	Transmission enable after TxD changes to *Data_0*
	to the observation window described in 9.1.4.2. j) Trigger the logic analyzer to start synchronously with the stimulation of the active star.
Postamble	Standard postamble.
Pass criteria	— *uBus* at *TP_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of all nodes shall contain the 50/50 pattern sent by the active star. — In case a RxEN signal is implemented *uRxEN* of all nodes shall be in HIGH state initially. While *uRxD* of all nodes signal the 50/50 pattern sent by the active star *uRxEN* of all nodes shall be in logical LOW state. — In case of an available INH1 signal *uINH1* of the active star shall be HIGH during the test execution. — No error shall be signalled at the host interface of node 23.

Table 483 defines the test instances for transmission enable after TxD changes to Data_0 test case defined in Table 482.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 483 — Test instances for transmission enable after TxD changes to *Data_0*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.9.3 No transmission enable while TxD remains in Data_1

Table 484 defines the test case for no transmission enable while TxD remains in Data_1.

Table 484 — Test case for no transmission enable while TxD remains in *Data_1*

Name	**No transmission enable while TxD remains in *Data_1***
Test purpose	This test checks the ability of the IUT to ignore a transmission with a permanent *Data_1* at TxD while TxEN is low as specified in ISO 17458-4.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: Active star as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. b) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Observe and acquire the error signal of the host interface (*TP_N23_ERRN* or *TP_N23_INTN*) of node 23. g) Observe and acquire *uBus* at *TP_N23_BP* and *TP_N23_BM* of node 23. h) Stimulate the IUT (AS) at *TP_AS_TxD* and *TP_AS_TxEN* by six 10Bit High pattern as specified in 9.1.3.7. i) Trigger the scope to start synchronously with the stimulation of the active star according

Name	No transmission enable while TxD remains in *Data_1*
	to the observation window described in 9.1.4.2. j) Trigger the logic analyzer to start synchronously with the stimulation of the active star.
Postamble	Standard postamble.
Pass criteria	— *uBus* at *TP_N23* of node 23 shall stay within *Idle* range during the observation window, i.e. the absolute bus voltage shall not exceed 30 mV ($uBDTx_{idle}$). — *uRxD* of all nodes shall be in HIGH state during the test execution. — In case a RxEN signal is implemented *uRxEN* shall be permanently in HIGH state during the test execution. — In case of an available INH1 signal *uINH1* of the active star shall be HIGH during the test execution. — No error shall be signalled at the host interface of node 23.

Table 485 defines the test instances for no transmission enable while TxD remains in Data_1 test case defined in Table 484.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 485 — Test instances for no transmission enable while TxD remains in *Data_1*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.9.4 No transmission enable while Undervoltage V_{IO}

Table 486 defines the test case for no transmission enable while Undervoltage V_{IO}.

Table 486 — Test case for no transmission enable while Undervoltage V_{IO}

Name	No transmission enable while Undervoltage V_{IO}
Test purpose	This test checks the ability of the IUT to ignore a transmission at TxEN while undervoltage at V_{IO} is present according to ISO 17458-4 while no stress condition is present. This test case is skipped if the Functional class "Active star – logic level adaptation" is not implemented.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — external V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix F (round robin including AS).
Preamble (setup state)	— Standard preamble. — Set the external V_{IO} reference voltage of active star to $V_{IOUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 1, 2, 12 and 23. b) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 1, 2, 12 and 23. d) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of nodes 1, 2, 12 and 23. f) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of nodes 1, 2, 12 and 23. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the

Name	No transmission enable while Undervoltage V_{IO}
	active star. i) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. j) Set the external V_{IO} reference voltage of active star to VIOUndervoltage. k) Stimulate the bus drivers and the IUT (active star) according to the sequence described on matrix F at TP_Nx/AS_TxD and TP_Nx/AS_TxEN by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. Hint: the bit duration in this test case shall be gdBit=25µs, because the memory depth of the logic analyzer is much too small to acquire more than one second with a 100ns bit time. The gap between the messages in matrix F shall be 9.25ms. l) Trigger the logic analyzer to start synchronously with the stimulation of node 1.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — Latest one second after the undervoltage on V_{IO} is applied *uRxD* of all nodes shall be in logical HIGH state while the active star is stimulated to transmit. — Latest one second after the undervoltage on V_{IO} is applied *uRxD* of the active star shall be in logical LOW state and remain LOW until end of test execution. — *uRxD* of all observed nodes shall contain the 50/50 pattern applied to the communication controller interface of all nodes except the active star; i.e. the active star shall remain in *AS_Normal* mode during the test execution even when the communication controller interface is disable. — In case of an available INH1 signal *uINH1* of the active star shall be HIGH during the test execution.
a The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 487 defines the test instances for no transmission enable while Undervoltage V_{IO} test case defined in Table 486.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 487 — Test instances for no transmission enable while Undervoltage V_{IO}

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.10 Mode.Active Star.Low Power.Sleep.Wakeup

11.3.10.1 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup

Table 488 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup.

Table 488 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of *dStarWakeupReactionTime* due to remote wakeup as specified in 9.1.3.1 and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4. e) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1.

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup
	f) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. g) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. i) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. j) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern as described in 9.1.3.1. k) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*. l) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern. m) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 104 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 31 µs after the beginning of the wakeup pattern and 104 µs after the beginning of the wakeup pattern. — *uRxD* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state initially but shall change to logical LOW state for signaling the detection of a wakeup, i.e. shall contain one falling edge. While entering *AS_Normal* mode *uRxEN* of the active star shall change back to logical HIGH state.

Table 489 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup test case defined in Table 488.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 489 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.10.2 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup

Table 490 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to alternative remote wakeup.

Table 490 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup**
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of *dStarWakeupReactionTime* due to alternative remote wakeup as specified in 9.1.3.12 and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4.

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup**
	e) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. f) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. g) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. i) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. j) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one alternative wakeup pattern as described in 9.1.3.11. k) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*. l) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern. m) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 104 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 31 µs after the beginning of the wakeup pattern and 104 µs after the beginning of the wakeup pattern. — *uRxD* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state initially but shall change to logical LOW state for signaling the detection of a wakeup, i.e. shall contain one falling edge. While entering *AS_Normal* mode *uRxEN* of the active star shall change back to logical HIGH state.

Table 491 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to alternative remote wakeup test case defined in Table 490.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 491 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.10.3 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse) pattern

Table 492 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse) pattern.

Table 492 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse) pattern

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse) pattern**
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of $dStarWakeupReaction_{local}$ due to a negative local wakeup pulse and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented — the active star – wake interface is not implemented.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.10. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.10. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.10. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.10.

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse) pattern**
	e) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) Observe and acquire *uWAKE* at *TP_AS_WAKE* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. h) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. i) Apply a negative wakeup pulse of 500 µs to the active star at *TP_AS_WAKE* according to *dStarWakePulseFilter* in ISO 17458-4. j) Wait 100 µs for the active star to enter *AS_Normal* via *AS_Standby*. k) Trigger the scope to start the observation 1 µs after the falling edge of *uWAKE* at *TP_AS_WAKE* of the active star. l) Trigger the logic analyzer to start the observation synchronously with the falling edge of *uWAKE* at *TP_AS_WAKE* of the active star.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time $dStarWakeupReaction_{local}$ shall be measured with an error of less than 1 %. — *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the local wakeup event, *uBP* and *uBM* of branch 2 and 4 shall change to *Idle* state, i.e. *uBP* and *uBM* of branch 2 and 4 shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 100 µs + 500 µs after the occurrence of the local wakeup event. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event. — *uRxD* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state initially. Between 1 µs and 100 µs + 500 µs after the falling edge of *uWAKE*, *uRxEN* shall change to logical LOW state for signaling the detection of a wakeup, i.e. shall contain one falling edge. Latest 100 µs + 500 µs after the falling edge of *uWAKE*, *uRxEN* of the active star shall be in logical HIGH state, i.e. the active star is in *AS_Normal* mode.

Table 493 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse) pattern test case defined in Table 492.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 493 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse) pattern

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.10.4 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse) pattern

Table 494 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (positive pulse) pattern.

Table 494 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse) pattern

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse) pattern**
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of $dStarWakeupReaction_{local}$ due to a positive local wakeup pulse and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Functional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented — the active star – wake interface is not implemented — a positive local wakeup pulse is not supported by the IUT.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.10. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.10. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse) pattern
	the observation window described in 10.2.4.10. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.10. e) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) Observe and acquire *uWAKE* at *TP_AS_WAKE* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. h) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. i) Apply a positive wakeup pulse of 500 µs to the active star at *TP_AS_WAKE* according to *dStarWakePulseFilter* in ISO 17458-4. j) Wait 100 µs for the active star to enter *AS_Normal* via *AS_Standby*. k) Trigger the scope to start the observation 1 µs after the rising edge of *uWAKE* at *TP_AS_WAKE* of the active star. l) Trigger the logic analyzer to start the observation synchronously with the rising edge of *uWAKE* at *TP_AS_WAKE* of the active star.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time $dStarWakeupReaction_{local}$ shall be measured with an error of less than 1 %. — *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the local wakeup event, *uBP* and *uBM* of branch 2 and 4 shall change to *Idle* state, i.e. *uBP* and *uBM* of branch 2 and 4 shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 100 µs + 500 µs after the occurrence of the local wakeup event. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event. — *uRxD* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state initially. Between 1 µs and 100 µs + 500 µs after the rising edge of *uWAKE*, *uRxEN* shall change to logical LOW state for signaling the detection of a wakeup, i.e. shall contain one falling edge. Latest 100 µs + 500 µs after the rising edge of *uWAKE*, *uRxEN* of the active star shall be in logical HIGH state, i.e. the active star is in *AS_Normal* mode.

Table 495 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (positive pulse) pattern test case defined in Table 494.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 495 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse) pattern

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.10.5 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame

Table 496 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to wakeup frame.

Table 496 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of *dStarWakeupReactionTime* due to a wakeup frame payload as specified in 9.1.3.13 and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5. e) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. f) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1.

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame
	g) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. i) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. j) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup frame containing the payload as specified in 9.1.3.12. k) After the end of the wakeup frame wait at least 70 µs for the active star to enter *AS_Normal* via AS_Standby. l) Trigger the scope to start the observation 70 µs after the end of the wakeup frame; i.e. after the positive edge on *TP_N1_TxEN*. m) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle*, i.e. *uBP* and *uBM* of the observed branches shall be between 1 800 mV and 3 200 mV. — In case of an available INH1 signal *uINH1* shall be in logical LOW state (*Sleep*) before the negative edge on *TP_N1_TxEN*; i.e. the active star shall be in *AS_Sleep* mode initially. Then, latest 70 µs after the positive edge on *TP_N1_TxEN*, *uINH1* shall be in logical HIGH state (*Not_Sleep*). — *uRxD* of the active star shall be in logical HIGH state before the negative edge on *TP_N1_TxEN*. Then, latest 70 µs after the positive edge on *TP_N1_TxEN*, *uRxD* of the active star shall be in logical HIGH state. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state before the negative edge on *TP_N1_TxEN*. Then, latest 70 µs after the positive edge on *TP_N1_TxEN*, *uRxEN* of the active star shall be in logical HIGH state.

Table 497 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to wakeup frame test case defined in Table 496.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 497 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.10.6 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to shorted wakeup pattern

Table 498 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to shorted wakeup pattern.

Table 498 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to shorted wakeup pattern

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to shorted wakeup pattern**
Test purpose	This test checks the ability of the active star to wake up after a wakeup reaction time of *dStarWakeupReactionTime* due to a shorted remote wakeup as specified in 9.1.3.14 and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4.

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to shorted wakeup pattern
	e) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. h) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one shorted wakeup pattern as specified in 9.1.3.13. i) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*. j) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern. k) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 86,3 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 13,3 µs after the beginning of the wakeup pattern and 86,3 µs after the beginning of the wakeup pattern. — *uRxD* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state initially but shall change to logical LOW state for signaling the detection of a wakeup, i.e. shall contain one falling edge. While entering *AS_Normal* mode *uRxEN* of the active star shall change back to logical HIGH state.

Table 499 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to shorted wakeup pattern test case defined in Table 498.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 499 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to shorted wakeup pattern

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.11 Mode.Active Star.Branch.TxOnly

11.3.11.1 Check AS transmitter activation via TxEN (*Branch_TxOnly*)

Table 500 defines the test case for check AS transmitter activation via TxEN (Branch_TxOnly).

Table 500 — Test case for check AS transmitter activation via TxEN (*Branch_TxOnly*)

Name	**Check AS transmitter activation via TxEN (*Branch_TxOnly*)**
Test purpose	This test checks the activation of the transmitter of the active star via the TxEN signal of the local communication controller interface according to ISO 17458-4 while no stress condition is present. Activation shall be possible when the branches of the active star are in *Branch_TxOnly* state and signal *Idle* to the central logic of the active star.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: Active Star as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. b) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. h) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxEN* by one babbling idiot

Name	Check AS transmitter activation via TxEN (*Branch_TxOnly*)
	pattern as defined in 10.2.3.1. i) After 5 µs from the end of the babbling idiot pattern stimulate the IUT (AS) at *TP_AS_TxD* and *TP_AS_TxEN* by one TSS pattern, followed by one 50/50 pattern. j) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_AS_TxD* and *TP_AS_TxEN* of the active star.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all observed nodes and the active star shall contain the 50/50 pattern transmitted by the IUT (AS), i.e. activation of the transmitter of the active star via the TxEN signal of the local communication controller interface shall be possible while branch 4 is in *Branch_TxOnly* mode. — In case of an available RxEN signal *uRxEN* of all nodes and the active star shall be in logical LOW state while *uRxD* of the corresponding node signals the received patterns. — In case of an available INH1 signal *uINH1* of the active star shall be in logical HIGH state during the test execution.

Table 501 defines the test instances for check AS transmitter activation via TxEN (Branch_TxOnly) test case defined in Table 500.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 501 — Test instances for check AS transmitter activation via TxEN (*Branch_TxOnly*)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.12 Failure.Loss

11.3.12.1 TxEN unconnected

Table 502 defines the test case for TxEN unconnected.

Table 502 — Test case for TxEN unconnected

Name	TxEN unconnected
Test purpose	This test checks the behaviour of the IUT in case of an unconnected TxEN signal according to ISO 17458-4. This test case considers only the AS_Normal mode.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: TxEN unconnected. — Communication: matrix F (round robin including AS).
Preamble (setup state)	— Standard preamble. — Switch TxEN signal of the active star to unconnected according to 7.6, failure FL5.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 1, 2, 12 and 23. b) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 1, 2, 12 and 23. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of nodes 1, 2, 12 and 23. e) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. h) Stimulate the bus drivers and the IUT (active star) according to the sequence described on matrix F at *TP_Nx/AS_TxD* and *TP_Nx/AS_TxEN* by one TSS pattern, followed by

Name	TxEN unconnected
	one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— uRxD of the active star shall contain all 50/50 patterns transmitted by nodes 1, 2, 12 and 23, i.e. the active star shall signal all patterns received on all branches at the local communication controller interface. — *uRxD* of all observed nodes and the active star shall not contain the 50/50 pattern applied to the communication controller interface of the active star, i.e. the active star shall read the unconnected TxEN input as logical HIGH and shall not be able to transmit anything. — In case of an available INH1 signal uINH1 of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state while *uRxD* of the active star signals the received patterns and shall be logical HIGH state otherwise.

11.3.12.2 TxD unconnected

Table 503 defines the test case for TxD unconnected.

Table 503 — Test case for TxD unconnected

Name	TxD unconnected
Test purpose	This test checks the behaviour of the IUT in case of an unconnected TxD signal according to ISO 17458-4. This test case considers only the AS_Normal mode.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: TxD unconnected. — Communication: matrix F (round robin including AS).
Preamble (setup state)	— Standard preamble. — Switch TxD signal of the active star to unconnected according to 7.6, failure FL6.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 1, 2, 12 and 23. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 1, 2, 12 and 23. c) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of nodes 1, 2, 12 and 23. e) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. h) Stimulate the bus drivers and the IUT (active star) according to the sequence described on matrix F at *TP_Nx/AS_TxD* and *TP_Nx/AS_TxEN* by one TSS pattern, followed by one 50/50 pattern.

Name	**TxD unconnected**
Postamble	Standard postamble.
Pass criteria	— uRxD of the active star shall contain all 50/50 patterns transmitted by nodes 1, 2, 12 and 23, i.e. the active star shall signal all patterns received on all branches at the local communication controller interface. — *uRxD* of all observed nodes and the active star shall contain a logical LOW sequence with the length of the 50/50 pattern instead of the 50/50 pattern applied to the communication controller interface of the active star, i.e. the active star shall read the unconnected TxD input as logical LOW and shall transmit sequences of logical LOW if enabled to transmit. — In case of an available INH1 signal uINH1 of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state while *uRxD* of the active star signals the received patterns and shall be logical HIGH state otherwise.

11.3.12.3 BGE unconnected

Table 504 defines the test case for BGE unconnected.

Table 504 — Test case for BGE unconnected

Name	BGE unconnected
Test purpose	This test checks the behaviour of the IUT in case of an unconnected BGE signal according to ISO 17458-4. This test is skipped if the Functional class “Active star – bus guardian interface” is not implemented. This test case considers only the AS_Normal mode.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: BGE unconnected. — Communication: matrix F (round robin including AS).
Preamble (setup state)	— Standard preamble. — Switch BGE signal of the active star to unconnected according to 7.6, failure FL10.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 1, 2, 12 and 23. b) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 1, 2, 12 and 23. d) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of nodes 1, 2, 12 and 23.. f) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. h) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. i) Stimulate the bus drivers and the IUT (active star) according to the sequence described

Name	BGE unconnected
	on matrix F at *TP_Nx/AS_TxD* and *TP_Nx/AS_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— uRxD of the active star shall contain all 50/50 patterns transmitted by nodes 1, 2, 12 and 23, i.e. the active star shall signal all patterns received on all branches at the local communication controller interface. — *uRxD* of all nodes and the active star shall not contain the 50/50 pattern applied to the communication controller interface of the active star, i.e. the active star shall read the unconnected BGE input as logical LOW and shall not be able to transmit anything. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state while *uRxD* of the active star signals the received patterns and shall be logical HIGH state otherwise. — In case of an available INH1 signal uINH1 of the active star shall be in logical HIGH state during the test execution.

11.3.13 Failure.Short-circuits

11.3.13.1 Short-circuit between TxEN to GND

Table 505 defines the test case for short-circuit between TxEN to GND.

Table 505 — Test case for short-circuit between TxEN to GND

Name	**Short-circuit between TxEN to GND**
Test purpose	This test checks the behaviour of the IUT in case of TxEN is shortened to GND according to ISO 17458-4. This test case is skipped if the Functional class “Active star – host interface” is implemented.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: short-circuit TxEN to GND. — Communication: active star as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. b) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of the active star. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Short-circuit TxEN and GND of the IUT (AS) according to 7.6, failure FL4. g) Beginning with the falling edge of *uTxEN* of the active star, stimulate the IUT (AS) at *TP_AS_TxD* by a logical LOW state sequence of at least 2 600 µs.
Postamble	Standard postamble.
Pass criteria	For *dBranchRxActiveMax* timeout measurement, a trigger event on the falling edge of *uTxEN* is required.

Name	Short-circuit between TxEN to GND
	— *uRxD* of all nodes and the active star shall be in logical HIGH state before the falling edge of *uTxEN* of the active star. After the falling edge of *uTxEN* of the active star, *uRxD* of all nodes and the active star shall change to logical LOW state and shall remain in logical LOW state for at least 650 µs and not more than 2 600 µs. After this logical LOW state phase, *uRxD* of all IUTs shall return to and remain in logical HIGH state. — In case of an available INH1 signal uINH1 of the active star shall be in logical HIGH state during the test execution.

11.3.14 Communication.Truncation

11.3.14.1 Path truncation

Table 506 defines the test case for path truncation.

Table 506 — Test case for path truncation

Name	Path truncation
Test purpose	This test checks the overall channel truncation if no stress condition is present according to the sum of all allowed truncation effects specified in ISO 17458-4. This test shall verify, that only the transmission start sequence is affected by truncation effects and that a protocol controller would decode the following data properly.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix F (round robin including AS).
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 1, 2, 12 and 23. b) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 1, 2, 12 and 23. d) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of nodes 1, 2, 12 and 23. f) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. i) In case of an available RxEN signal observe and acquire uRxEN at TP_Nx_RxEN of

Name	Path truncation
	nodes 1, 2, 12 and 23. j) Stimulate the bus drivers and the IUT (active star) according to the sequence described on matrix F at *TP_Nx/AS_TxD* and *TP_Nx/AS_TxEN* by one TSS pattern, followed by one 10/90 pattern.
Postamble	Standard postamble.
Pass criteria	The maximum allowed truncation depends on the presence or not of the inter star interface in the communication path; i.e. between the communication controller interface of the active star and the transmitter/receiver node. — The width of the received TSS pattern transmitted by the active star (logical LOW phase from the falling edge of the received TSS pattern to the rising edge of the first bit of the following 10/90 pattern) in *uRxD* of all observed nodes shall be as follow: — If the receiver node is connected to the same active star device where the communication controller interface is connected, then the received TSS pattern should be at least 700 ns and not lengthen more than 50 ns, i.e. the channel truncation shall be within the allowed range. — If the receiver node is not connected to the same active star device where the communication controller interface is connected, then the received TSS pattern should be at least 250 ns and not lengthen more than 50 ns, i.e. the channel truncation shall be within the allowed range. — The width of all received TSS patterns transmitted by nodes 1, 2, 12 and 23 (logical LOW phase from the falling edge of the received TSS pattern to the rising edge of the first bit of the following 10/90 pattern) in *uRxD* of the active star shall be as follow: — If the transmitter node is connected to the same active star device where the communication controller interface is connected, then the received TSS pattern should be at least 700 ns and not lengthen more than 50 ns, i.e. the channel truncation shall be within the allowed range. — If the receiver node is not connected to the same active star device where the communication controller interface is connected, then the received TSS pattern should be at least 250 ns and not lengthen more than 50 ns, i.e. the channel truncation shall be within the allowed range. — In case of an available INH1 signal *uINH1* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state while *uRxD* of the active star signals the received patterns and shall be logical HIGH state otherwise.

Table 507 defines the test instances for path truncation test case defined in Table 506.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 507 — Test instances for path truncation

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

11.3.15 Environment.Ground Shift.Dynamic Ground Shift

11.3.15.1 Active star receives pattern during ground shift at transmitter

Table 508 defines the test case for active star receives pattern during ground shift at transmitter.

Table 508 — Test case for active star receives pattern during ground shift at transmitter

Name	**Active star receives pattern during ground shift at transmitter**
Test purpose	This test checks the ability of the IUT to receive a test pattern while dynamic ground shift is present at the transmitting node.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: dynamic at node 23. — Failure: None. — Communication: Node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uGS_dyn* at *TP_N23_UGS* of node 23 according to the observation window described in 9.1.4.3. b) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23. c) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23. d) Observe and acquire *uRxD* at *TP_AS_RxD* of the AS. e) Stimulate node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1, followed by one TSS pattern, followed by nine 50/50 patterns, followed by one 10Bit High pattern. Trigger the dynamic ground shift curve synchronously with the first rising edge after the TSS pattern.
Postamble	Standard postamble.
Pass criteria	*uRxD* of the AS shall contain all patterns transmitted by node 23, i.e. the dynamic ground shift at node 23 shall not disturb the communication.

11.3.15.2 Active star transmits pattern during ground shift at AS

Table 509 defines the test case for active star transmits pattern during ground shift at AS.

Table 509 — Test case for active star transmits pattern during ground shift at AS

Name	Active star transmits pattern during ground shift at AS
Test purpose	This test checks the ability of the IUT to transmit a test pattern while dynamic ground shift is present at the AS.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: dynamic at the AS. — Failure: None. — Communication: AS as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uGS_dyn* at *TP_AS_UGS* of the active star according to the observation window described in 9.1.4.3. b) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. c) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. d) Observe and acquire *uRxD* at *TP_N23_RxD* of node 23. e) Stimulate the AS at *TP_AS_TxD* and *TP_AS_TxEN* by one wakeup pattern as described in 9.1.3.1, followed by one TSS pattern, followed by nine 50/50 patterns, followed by one 10Bit High pattern. Trigger the dynamic ground shift curve synchronously with the first rising edge after the TSS pattern.
Postamble	Standard postamble.
Pass criteria	*uRxD* of node 23 shall contain all patterns transmitted by the AS, i.e. the dynamic ground shift at the AS shall not disturb the communication.

11.3.15.3 Active star receives pattern during ground shift at AS

Table 510 defines the test case for active star receives pattern during ground shift at AS.

Table 510 — Test case for active star receives pattern during ground shift at AS

Name	**Active star receives pattern during ground shift at AS**
Test purpose	This test checks the ability of the IUT to receive a test pattern while dynamic ground shift is present at the AS.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: dynamic at the AS. — Failure: None. — Communication: Node 23 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uGS_dyn* at *TP_AS_UGS* of the active star according to the observation window described in 9.1.4.3. b) Observe and acquire *uTxD* at *TP_N23_TxD* of node 23 c) Observe and acquire *uTxEN* at *TP_N23_TxEN* of node 23 d) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. e) Stimulate node 23 at *TP_N23_TxD* and *TP_N23_TxEN* by one wakeup pattern as described in 9.1.3.1, followed by one TSS pattern, followed by nine 50/50 patterns, followed by one 10Bit High pattern. Trigger the dynamic ground shift curve synchronously with the first rising edge after the TSS pattern.
Postamble	Standard postamble.
Pass criteria	*uRxD* of the AS shall contain all patterns transmitted by node 23, i.e. the dynamic ground shift at the AS shall not disturb the communication.

11.3.15.4 Active star transmits pattern to shifted receiver

Table 511 defines the test case for active star transmits pattern to shifted receiver.

Table 511 — Test case for active star transmits pattern to shifted receiver

Name	Active star transmits pattern to shifted receiver
Test purpose	This test checks the ability of the IUT to transmit a test pattern while dynamic ground shift is present at the receiving node.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: dynamic at node 23. — Failure: None. — Communication: AS as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uGS_dyn* at *TP_N23_UGS* of node 23 according to the observation window described in 9.1.4.3. b) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. c) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. d) Observe and acquire *uRxD* at *TP_N23_RxD* of node 23. e) Stimulate the AS at *TP_AS_TxD* and *TP_AS_TxEN* by one wakeup pattern as described in 9.1.3.1, followed by one TSS pattern, followed by ten 50/50 patterns. Trigger the dynamic ground shift curve synchronously with the first rising edge after the TSS pattern.
Postamble	Standard postamble.
Pass criteria	*uRxD* of node 23 shall contain all 50/50 patterns transmitted by the AS, i.e. the dynamic ground shift at node 23 shall not disturb the communication.

11.3.16 Dynamic Low Battery Voltage

11.3.16.1 Dynamic low battery voltage

Table 512 defines the test case for dynamic low battery voltage.

Table 512 — Test case for dynamic low battery voltage

Name	Dynamic low battery voltage
Test purpose	This test checks the behaviour of the IUT after a dynamic low battery voltage pulse according to 7.4 in *AS_Normal* mode. Additionally, the behaviour at the local communication controller interface and, if available, the local bus guardian interface is verified. This test case intends to test the capability of the active star to stay in *AS_Normal* mode during the dynamic low battery pulse. This test case is applicable to all IUTs, even if no V_{BAT} supply input is implemented. In this case, the input voltage of the V_{CC} voltage regulator (the battery voltage) is stressed by the dynamic low battery voltage pulse.
Configuration	— Topology: as specified in previous configuration see 11.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: 11,6 V. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: 11,6 V. — Ground shift: 0 V. — Failure: none. — Communication: matrix F (round robin including AS). — Test signal: U_S/t_{f1} as specified in 7.4.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 1, 2, 12 and 23. b) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 1, 2, 12 and 23. d) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of nodes 1, 2, 12 and 23. f) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star.

Name	Dynamic low battery voltage
	h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of nodes 1, 2, 12 and 23. i) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. j) Stimulate the bus drivers and the IUT (active star) according to the sequence described on matrix F at *TP_Nx/AS_TxD* and *TP_Nx/AS_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low battery voltage pulse. The bit duration in this test case shall be *gdBit*=25 µs, because the memory depth of the logic analyzer is much too small to acquire 10 seconds with a 100 ns bit time. The gap between the messages in matrix F shall be 9,25 ms. k) After the first communication round trigger the dynamic low battery pulse.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all observed nodes and the active star shall contain all 50/50 patterns applied to the local communication controller interface of the active star (according to *uTxD* and *uTxEN* of the active star), i.e. all data shall be transmitted by the active star. — *uRxD* of the active star shall contain all 50/50 patterns transmitted by nodes 1, 2, 12, 23 and the active star (according to *uTxD* and *uTxEN* of the corresponding node), i.e. the active star shall signal all patterns received on all branches to the local communication controller interface. — In case of an available INH1 signal *uINH1* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state while *uRxD* of the active star signals the received patterns and shall be logical HIGH state otherwise.

11.3.17 Dynamic Low Supply

11.3.17.1 Mode change back to *AS_Normal* after dynamic low supply voltage

Table 513 defines the test case for mode change back to AS_Normal after dynamic low supply voltage.

Table 513 — Test case for mode change back to *AS_Normal* after dynamic low supply voltage

Name	**Mode change back to *AS_Normal* after dynamic low supply voltage**
Test purpose	This test checks the behaviour of the IUT after a dynamic low supply voltage pulse according to 7.5 occuring in *AS_Normal* mode.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: 11,6 V. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: 11,6 V. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix F (round robin including AS). — Test signal: Case 1.1 as specified in 7.5.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 1, 2, 12 and 23. b) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 1, 2, 12 and 23. d) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of nodes 1, 2, 12 and 23. f) Observe and acquire *uRxD* at *TP_AS_RxD* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of

Name	Mode change back to *AS_Normal* after dynamic low supply voltage
	nodes 1, 2, 12 and 23. i) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. j) Start the dynamic low supply voltage pulse at the power supply of the active star. k) Wait until the power supply voltage(s) rise(s) above the specific undervoltage thresholds. l) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern as described in 9.1.3.1. m) Stimulate the bus drivers and the IUT (active star) according to the sequence described on matrix F at *TP_Nx/AS_TxD* and *TP_Nx/AS_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low supply voltage pulse. n) Trigger the logic analyzer to start synchronously with the first falling edge of *uTxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The observation window shall start with the first falling edge of *uTxEN* of node 1. Adaptation of the thresholds for digital signals may be required. — *uRxD* of all observed nodes and the active star shall contain all 50/50 patterns applied to the local communication controller interface of the active star (according to *uTxD* and *uTxEN* of the active star) at least after the first communication round, i.e. all data shall be transmitted by the active star. — *uRxD* of the active star shall contain all 50/50 patterns transmitted by nodes 1, 2, 12, 23 and the active star (according to *uTxD* and *uTxEN* of the corresponding node) at least after the first communication round, i.e. the active star shall signal all patterns received on all branches to the local communication controller interface. — In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical HIGH state latest 104 µs after the beginning of the first wakeup pattern until the end of the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state while *uRxD* of the active star signals the received patterns and shall be logical HIGH state otherwise.

Table 514 defines the test instances for mode change back to AS_Normal after dynamic low supply voltage test case defined in Table 513.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 514 — Test instances for mode change back to *AS_Normal* after dynamic low supply voltage

Instance		1	2	3	4
Purpose	**Stress**	—	—	—	—
	Precondition	—	—	—	—
Configuration	**Power supply**	Test signal: Case 1.1 as specified in 7.5	Test signal: Case 1.2 as specified in 7.5	Test signal: Case 2.1 as specified in 7.5	Test signal: Case 2.2 as specified in 7.5
	Ground shift	—	—	—	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

12 Test Cases for Active Stars with host interface

12.1 Configuration

12.1.1 Topology

The topology corresponds to 10.2.1.

12.1.2 Test planes

12.1.2.1 Analog signals

The test planes for analog signals correspond to 10.2.2.1.

12.1.2.2 Digital signals

The following test planes at the IUT for digital signals are specified as depicted in Table 515.

Table 515 — Test planes at the Active Star host interface

Test plane	Signal	Input	Description
TP_AS_INTN	INTN	V_{IO}/V_{CC}	Interrupt Not output signal of the IUT
TP_AS_SCSN	SCSN	V_{IO}/V_{CC}	The SCSN input signal of the SPI
TP_AS_SCK	SCK	V_{IO}/V_{CC}	The clock signal of the SPI
TP_AS_SDI	SDI	V_{IO}/V_{CC}	The Serial Data Input signal of the SPI
TP_AS_SDO	SDO	V_{IO}/V_{CC}	The Serial Data Output signal of the SPI

12.1.2.3 Test planes for the oscilloscope

The oscilloscope observes the following test planes:

— *TPAS1_By_BM*

— *TPAS1_By_BP*

NOTE For illustration of the location of these test planes see 10.2.2.4.

12.1.2.4 Test planes for the logic analyzer

The logic analyzer observes the following test planes:

— *TP_AS_INTN*

— *TP_AS_SCSN*

— *TP_AS_RxD*

— *TP_AS_RxEN*

— *TP_AS_TxD*

— *TP_AS_TxEN*

— *TP_AS_INH1*

— *TP_AS_WAKE*

12.1.2.5 Test planes for the pattern generator

The pattern generator stimulates the following test planes:

— *TP_AS_TxD*

— *TP_AS_TxEN*

— *TP_AS_WAKE*

— *TP_AS_SCSN*

— *TP_AS_SDI*

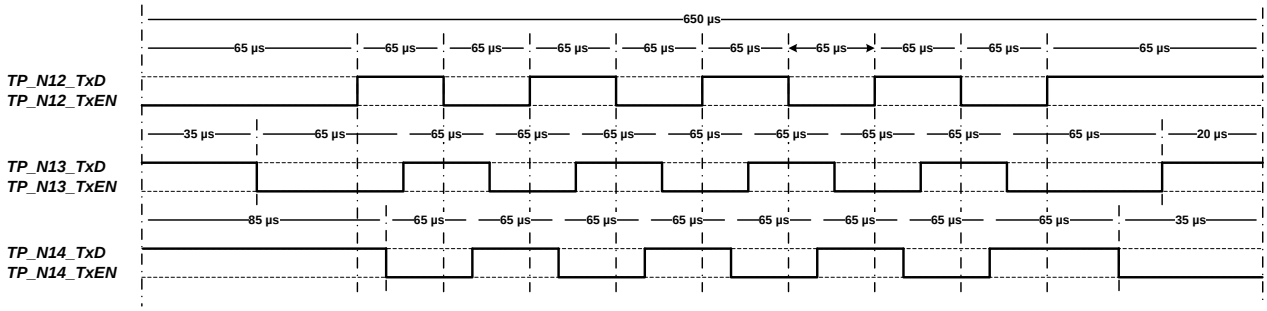
12.1.3 Test Patterns

There is only one additional test patterns for the Active Star host interface specified. The other used test patterns are specified in subclauses 10.2.3 and 9.1.3.

12.1.3.1 Starting Babbling Idiot

This test signal simulates the start of a babbling idiot, it is as long as the minimum value of *dBranchRxActiveMax*, i.e. 650 µs.

Figure 72 depicts the test pattern for a starting babbling idiot simulation.



Key

TP_N12_TxD	Transmit Data input signal of the IUT at node 12
TP_N12_TxEN	Transmit Data Enable Not input signal of the IUT at node 12
TP_N13_TxD	Transmit Data input signal of the IUT at node 13
TP_N13_TxEN	Transmit Data Enable Not input signal of the IUT at node 13
TP_N14_TxD	Transmit Data input signal of the IUT at node 14
TP_N14_TxEN	Transmit Data Enable Not input signal of the IUT at node 14

Figure 72 — Test pattern for a starting babbling idiot simulation

12.1.4 Observation windows

This subclause corresponds to 10.2.4.

12.1.5 Operation modes of the Active Star

This subclause corresponds to 10.2.5. The autonomous power moding flag (APM flag) may be reset via the host interface.

12.1.6 Power supplies

This subclause corresponds to 10.2.6.

12.1.7 Stress

This subclause corresponds to 10.2.7.

12.1.8 Failures

The failures are located as shown in Figure 19.

12.1.9 Mandatory features

12.1.9.1 Functional class "Active Star – host interface"

This functional class requires the implementation of an Active Star – host interface as described in ISO 17458-4.

12.1.10 Optional features

12.1.10.1 General

The following features are optional as specified in ISO 17458-4 and shall be tested in the test cases if available in the IUT.

12.1.10.2 Functional class "Active Star – voltage regulator control"

This functional class requires the following optional features to be implemented in coexistence:

— Signal INH1

— Power supply input V_{BAT}

— Power supply input V_{CC}

— Active Star – wake interface (optional within this functional class)

12.1.10.3 Functional class "Active Star – internal voltage regulator"

This functional class requires the following optional features to be implemented in coexistence:

— Power supply input V_{BAT}

— Signal INH1 (optional within this functional class)

— Active Star – wake interface (optional within this functional class)

This Functional class requires that no V_{CC} supply input is present

12.1.10.4 Functional class "Active Star – logic level adaptation"

This functional class requires the implementation of a logic level-shift interface and requires that the thresholds of all digital inputs are controlled by this voltage as well as all digital outputs are related to this level.

12.1.10.5 Functional class "Active Star – communication controller interface"

This functional class requires the following optional features to be implemented in coexistence:

— Signal RxD

— Signal TxD

— Signal TxEN

12.1.10.6 Functional class "Active Star increased voltage amplitude transmitter"

This functional class comprises the minimum of $uStarTx_{Active}$ to be 900 mV.

12.1.11 Definition of communication and control

There are no definitions of communication and control for the Active Star host interface specified.

12.1.12 Standard preamble

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure condition.

e) TxEN and TxD of all nodes shall be in logical HIGH (idle) state.

f) In case a BGE signal is available, this signal shall be in logical HIGH state at all nodes and the Active Star.

g) In case of a VDIG input this voltage shall be supplied by the voltage used in the implementation of the conformance test.

h) In case of a WAKE pin this signal shall be in logical HIGH state.

i) Stimulate Bus Drivers of all nodes via host command to enter *BD_Normal*.

j) Unset the APM flag via host command.

k) Wait 100 µs

l) Stimulate the Active Star via host command to enter *AS_Normal*.

m) Wait 100 µs.

12.1.13 Standby preamble

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure condition.

e) TxEN and TxD shall be in logical HIGH (idle) state.

f) In case of a BGE signal this signal shall be in logical HIGH state at all nodes and the Active Star.

g) In case of a V_{DIG} input this voltage shall be supplied by the voltage used in the implementation of the conformance test.

h) In case of a WAKE pin this signal shall be in logical HIGH state.

i) Stimulate all IUTs via the host interface to enter *BD_Normal*.

j) Unset the APM flag via host command.

k) Wait 100 µs

l) Stimulate the Active Star via host command to enter *AS_Standby*.

m) Wait 100 µs.

12.1.14 Sleep preamble

a) Switch on power supplies and initialize them according to the values defined for each test case in the configuration.

b) Set ground shift and initialize it according to the values defined for each test case in the configuration.

c) Set failure according to the values defined for each test case in the configuration.

d) Wait for 500 ms in order to have a stable failure condition.

e) TxEN and TxD of all nodes shall be in logical HIGH (idle) state.

f) In case a BGE signal is available, this signal shall be in logical HIGH state at all nodes and the Active Star.

g) In case of a VDIG input this voltage shall be supplied by the voltage used in the implementation of the conformance test.

h) In case of a WAKE pin this signal shall be in logical HIGH state.

i) Stimulate Bus Drivers of all nodes via host command to enter *BD_Normal*.

j) Unset the APM flag via host command.

k) Wait 100 µs

l) Stimulate the Active Star via host command to enter *AS_Sleep*.

m) Wait 100 µs.

12.1.15 Standard postamble

a) Set ground shift to 0 V.

b) Set to faultless configuration (reset failures).

c) Switch off power supplies.

12.2 Static test cases

The motivation of static test cases is to check the availability and the boundaries in the data sheet of the IUT (topology independent).

Every parameter shall be part of the data sheet and fulfill the specified boundaries. If at least one parameter does not pass this test, the result of the whole conformance test is failed.

Table 516 defines the static test cases for Active Stars with host interface.

Table 516 — Static test cases for Active Stars with host interface

Index	Parameter	SOVS Brace	Description	Min	Max	Unit
1.	*dStarMode Change$_{SPI}$*	Host Interface. Active Star. SPI	*Mode transition time after (SPI) host command*		100	µs
2.	*dStarReaction Time$_{SPI}$*	Host Interface. Active Star. SPI	*Time from detection of an event to falling edge of INTN*		200	µs
3.	*uV$_{DIG-OUT-HIGH}$*	Communication. Threshold	Output voltage on a digital output, when in logical high state [a, b, c, d]	80 [b]	100 [b]	%
4.	*uV$_{DIG-OUT-LOW}$*	Communication. Threshold	Output voltage on a digital output, when in logical high state [a, b, c, d]		20 [b]	%
5.	*uV$_{DIG-IN-HIGH}$*	Communication. Threshold	Threshold for detecting a digital input as on logical high [b, c]		70 [b]	%
6.	*uV$_{DIG-IN-LOW}$*	Communication. Threshold	Threshold for detecting a digital input as on logical low [b, c]	30 [b]		%
7.	Functional class “Active Star – host interface”	Functional Class	Checks the complete implementation of all specified options			-
8.	SPI	Host Interface. Active Star	Characteristics of the optional SPI Bus Driver to host interface [e, f]	0,01	1	Mbit/s
9.	*uV$_{DIG-OUT-UV}$*	Communication. Threshold	*Output voltage on a digital output at 100 k*Ω load, when V_{DIG} in undervoltage [a, b, c, d]	—	500	mV
10.	*uV$_{DIG-OUT-OFF}$*	Communication. Threshold	Output voltage on a digital output at 100 kΩ load, when unsupplied [g] Checks the existence of this parameter in the datasheet	product specific	product specific	
11.	Behaviour in case of SCK unconnected	Simulation	SCK shall have pull-down behaviour in case it is unconnected			
12.	Behaviour in case of SDI unconnected	Simulation	SDI (if implemented) shall have pull-down behaviour in case it is unconnected			
13.	Behaviour in case of SCSN unconnected	Simulation	SCSN (if implemented) shall have pull-up behaviour in case it is unconnected			

[a] Load conditions are product specific and documented in the product datasheet.

Index	Parameter	SOVS Brace	Description	Min	Max	Unit
b In case a reference voltage for digital IO is available via a V_{IO} pin, then $uV_{DIG} = uV_{IO}$, otherwise $uV_{DIG} = uV_{CC}$						
c Relative to V_{DIG}						
d Condition: no undervoltage on V_{DIG} and either V_{CC} or V_{BAT} supplied (product specific supply thresholds below undervoltage thresholds, e.g. in *BD_Off* or *AS_Off* mode)						
e The values represent the range of the transfer speed which shall be guaranteed by the IUT.						
f The device shall meet at least the range as given in ISO 17458-4, but may be better than the minimum and maximum values.						
g Product specific supply thresholds below undervoltage thresholds, e.g. in *BD_Off* or *AS_Off* mode.						

12.3 Test cases

12.3.1 Mode.Active Star.Normal

12.3.1.1 Operation mode change from *AS_Sleep* to *AS_Normal* due to host command

Table 517 defines the test case for operation mode change from AS_Sleep to AS_Normal due to host command.

Table 517 — Test case for operation mode change from *AS_Sleep* to *AS_Normal* due to host command

Name	**Operation mode change from *AS_Sleep* to *AS_Normal* due to host command**
Test purpose	This test checks the ability of the IUT to change from mode *AS_Sleep* to *AS_Normal* due to host command according to ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	Sleep preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 2. d) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all

Name	Operation mode change from *AS_Sleep* to *AS_Normal* due to host command
	nodes. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. h) Stimulate the active star via the host interface to enter *AS_Normal*. i) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. j) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all observed nodes shall contain the 50/50 pattern transmitted by node 2, i.e. the active star shall be in *AS_Normal* mode within 100 µs after the stimulation at the host interface and retransmit the test patterns of node 2. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state (*Not_Sleep*) during the observation. — In case of an available RxD signal *uRxD* at *TP_AS_RxD* shall contain the 50/50 pattern transmitted by node 2. — In case of an available RxEN signal *uRxEN* at *TP_AS_RxEN* of the active star shall be in logical LOW state while node 2 is stimulated and shall be in logical HIGH state otherwise.

Table 518 defines the test instances for operation mode change from AS_Sleep to AS_Normal due to host command test case defined in Table 517.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 518 — Test instances for operation mode change from *AS_Sleep* to *AS_Normal* due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.1.2 Operation mode change from *AS_Standby* to *AS_Normal* due to host command

Table 519 defines the test case for operation mode change from AS_Standby to AS_Normal due to host command.

Table 519 — Test case for operation mode change from *AS_Standby* to *AS_Normal* due to host command

Name	**Operation mode change from *AS_Standby* to *AS_Normal* due to host command**
Test purpose	This test checks the ability of the IUT to change from mode *AS_Standby* to *AS_Normal* due to host command according to ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	Standby preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 2. d) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star.

Name	Operation mode change from *AS_Standby* to *AS_Normal* due to host command
	h) Stimulate the active star via the host interface to enter *AS_Normal*. i) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. j) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all observed nodes shall contain the 50/50 pattern transmitted by node 2, i.e. the active star shall be in *AS_Normal* mode and retransmit the test patterns of node 2. — In case of an available INH signal *uINH1* shall be in logical HIGH state (*Not_Sleep*) during the test execution. — In case of an available RxD signal *uRxD* at *TP_AS_RxD* shall contain the 50/50 pattern transmitted by node 2. — In case of an available RxEN signal *uRxEN* at *TP_AS_RxEN* of the active star shall be in logical LOW state during the stimulation of node 2.

Table 520 defines the test instances for operation mode change from AS_Standby to AS_Normal due to host command test case defined in Table 519.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 520 — Test instances for operation mode change from *AS_Standby* to *AS_Normal* due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.1.3 AS remains in *AS_Normal* after *dStarGoToSleep*

Table 521 defines the test case for AS remains in AS_Normal after dStarGoToSleep.

Table 521 — Test case for AS remains in *AS_Normal* after *dStarGoToSleep*

Name	**AS remains in *AS_Normal* after *dStarGoToSleep***
Test purpose	This test checks the ability of the active star to remain in *AS_Normal* mode if all branches are in *Branch_Idle* for longer than *dStarGoToSleep* according to ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. e) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. h) After at least 6 400 ms stimulate the bus driver of node 2 at *TP_N2_TxD* and

Name	AS remains in *AS_Normal* after *dStarGoToSleep*
	TP_N2_TxEN by one TSS pattern, followed by one 50/50 pattern. i) Trigger the logic analyzer to start the observation synchronously with the stimulation of node 2.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical HIGH state during the test execution. — *uRxD* of all observed nodes shall signal the pattern transmitted by node 2. — In case of an available RxD signal *uRxD* at *TP_AS_RxD* of the active star shall contain all 50/50 patterns transmitted at *uTxD* and *uTxEN* of node 2. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical HIGH state before the stimulation of node 2 (falling edge of *uTxD* and *uTxEN*) and shall be in logical LOW state while *uRxD* of the active star signals the received patterns.

Table 522 defines the test instances for AS remains in AS_Normal after dStarGoToSleep test case defined in Table 521.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 522 — Test instances for AS remains in *AS_Normal* after *dStarGoToSleep*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.2 Mode.Active Star.Low Power.Sleep

12.3.2.1 Operation mode change from *AS_Normal* to *AS_Sleep* due to host command

Table 523 defines the test case for operation mode change from AS_Normal to AS_Sleep due to host command.

Table 523 — Test case for operation mode change from *AS_Normal* to *AS_Sleep* due to host command

Name	Operation mode change from *AS_Normal* to *AS_Sleep* due to host command
Test purpose	This test checks the ability of the IUT to change from *AS_Normal* mode to *AS_Sleep* due to host command according to ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.7. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.7. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.7. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.7.

Name	Operation mode change from *AS_Normal* to *AS_Sleep* due to host command
	e) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. f) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. g) In case of an available INH1 signal observe and acquire INH1 signal *uINH1* at *TP_AS_INH1* of the active star. h) Stimulate the active star via the host interface to enter *AS_Sleep*. i) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 10Bit Low pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2. k) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical LOW state during the observation window. — *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode.

Table 524 defines the test instances for operation mode change from AS_Normal to AS_Sleep due to host command test case defined in Table 523.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 524 — Test instances for operation mode change from *AS_Normal* to *AS_Sleep* due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.2.2 Operation mode change from *AS_Standby* to *AS_Sleep* due to host command

Table 525 defines the test case for operation mode change from AS_Standby to AS_Sleep due to host command.

Table 525 — Test case for operation mode change from AS_Standby to AS_Sleep due to host command

Name	**Operation mode change from *AS_Standby* to *AS_Sleep* due to host command**
Test purpose	This test checks the ability of the IUT to change from *AS_Standby* mode to *AS_Sleep* due to host command according ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standby preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.

Table 525 — *(continued)***)**

Name	Operation mode change from *AS_Standby* to *AS_Sleep* due to host command
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.7. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.7. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.7. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.7. e) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. f) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. g) In case of an available INH1 signal observe and acquire INH1 signal *uINH1* at *TP_AS_INH1* of the active star. h) Stimulate the active star via the host interface to enter *AS_Sleep*. i) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. j) Trigger the scope to start the observation synchronously with the stimuli at the host interface of the active star. k) Trigger the logic analyzer to start the observation synchronously with the stimuli at the host interface of the active star.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical LOW state during the observation window. — *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode.

Table 526 defines the test instances for mode change from AS_Standby to AS_Sleep due to host command test case defined in Table 525.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 526 — Test instances for mode change from *AS_Standby* to *AS_Sleep* due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.2.3 Operation mode change from *AS_Normal* to *AS_Sleep* after dStarGoToSleep (undervoltage V_{IO} sets APM flag)

Table 527 defines the test case for operation mode change from AS_Normal to AS_Sleep after dStarGoToSleep (undervoltage V_{IO} sets APM flag).

Table 527 — Test case for operation mode change from *AS_Normal* to *AS_Sleep* after *dStarGoToSleep* (undervoltage V_{IO} sets APM flag)

Name	**Operation mode change from *AS_Normal* to *AS_Sleep* after *dStarGoToSleep* (undervoltage V_{IO} sets APM flag)**
Test purpose	This test checks the ability of the active star to set the autonomous power moding flag (APM flag) automatically due to undervoltage condition at V_{IO}, i.e. to go to *AS_Sleep* mode if all branches are in *Branch_Idle* for longer than *dStarGoToSleep* according to ISO 17458-4 while no other stress condition is present. This test case if skipped if the Functional class “Active Star – logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.

Table 527 — *(continued)*

Name	**Operation mode change from *AS_Normal* to *AS_Sleep* after *dStarGoToSleep* (undervoltage V_{IO} sets APM flag)**
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.7. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.7. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.7. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.7. e) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. f) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. h) Set V_{IO} reference voltage to: VIOUndervoltage. i) Wait 6 400 ms + 1 000ms for the AS to enter *AS_Sleep*. j) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2. l) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode. — In case of an available INH1 signal *uINH1* shall be in logical LOW state during the test execution.

Table 528 defines the test instances for operation mode change from AS_Normal to AS_Sleep after *dStarGoToSleep* (undervoltage V_{IO} sets APM flag) test case defined in Table 527.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 528 — Test instances for operation mode change from *AS_Normal* to *AS_Sleep* after *dStarGoToSleep* (undervoltage V_{IO} sets APM flag)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.3 Mode.Active Star.Low Power.Sleep.Wakeup

12.3.3.1 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern

Table 529 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern.

Table 529 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern**
Test purpose	This test checks the ability of the active star to signal the remote wakeup event to the host and to wake up after a wakeup reaction time of *dStarWakeupReactionTime*, i.e. to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4. e) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. f) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1 g) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. h) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the

Name	Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern
	active star. i) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. j) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. k) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one remote wakeup pattern as described in 9.1.3.1. l) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern. m) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N1_TxD* and *TP_N1_TxEN* of node 1. n) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*.
Postamble	Standard postamble.
Pass criteria	The wakeup reaction time *dStarWakeupReactionTime* shall be measured with an error of less than 1 %. The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 104 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 31 µs after the beginning of the wakeup pattern and 104 µs after the beginning of the wakeup pattern. — *uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 1. Between 31 µs after the beginning of the wakeup pattern and 104 µs + 200 µs after the beginning of the wakeup pattern *uINTN* at *TP_AS_INTN* of the active star shall change to logical LOW state. — In case of an available RxD signal *uRxD* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state initially but shall change to logical LOW state for signaling the detection of a wakeup, i.e. shall contain one falling edge. While entering *AS_Normal* mode *uRxEN* of the active star shall change back to logical HIGH state.

Table 530 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern test case defined in Table 529.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 530 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.3.2 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse)

Table 531 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse).

Table 531 — Test case for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse)

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse)**
Test purpose	This test checks the ability of the active star to signal the local wakeup event (negative pulse) to the host and to wake up after a wakeup reaction time of $dStarWakeupReaction_{local}$, i.e. to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the active star – wake interface is not implemented — neither the Functional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.10. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.10. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.10. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.10.

Name	**Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse)**
	e) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. f) Observe and acquire uWAKE at TP_AS_WAKE of the active star. g) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. h) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. i) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. j) Apply a negative wakeup pulse of 500 µs to the active star at *TP_AS_WAKE* according to *dStarWakePulseFilter* in ISO 17458-4. k) Trigger the scope to start the observation 1 µs after the falling edge of *uWAKE* at *TP_AS_WAKE* of the active star. l) Trigger the logic analyzer to start the observation synchronously with the falling edge of *uWAKE* at *TP_AS_WAKE* of the active star. m) Wait 100 µs.
Postamble	Standard postamble.
Pass criteria	The period to observe is very long in this test case. But a bit level resolution is not required. The wakeup reaction time $dStarWakeupReaction_{local}$ shall be measured with an error of less than 1 %. — *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the local wakeup event, *uBP* and *uBM* of branch 2 and 4 shall change to *Idle* state, i.e. *uBP* and *uBM* of branch 2 and 4 shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 100 µs + 500 µs after the occurrence of the local wakeup event. — In case of an available INH1 signal *uINH1* shall be in logical LOW state initially. *uINH1* shall change to logical HIGH state between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event. — *uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. Between 1 µs after the occurrence of the local wakeup event and 500 µs + 200 µs after the occurrence of the local wakeup event *uINTN* at *TP_AS_INTN* of the active star shall change to logical LOW state. — In case of an available RxD signal *uRxD* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state initially. Between 1 µs and 100 µs + 500 µs after the falling edge of *uWAKE*, *uRxEN* shall change to logical LOW state for signaling the detection of a wakeup, i.e. shall contain one falling edge. Latest 100 µs + 500 µs after the falling edge of *uWAKE*, *uRxEN* of the active star shall be in logical HIGH state, i.e. the active star is in *AS_Normal* mode.

Table 532 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse) test case defined in Table 531.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 532 — Test instances for operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.3.3 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to remote wakeup pattern (with APM)

Table 533 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (with APM).

Table 533 — Test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (with APM)

Name	**Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (with APM)**
Test purpose	This test checks the ability of the active star to signal the remote wakeup event to the host and to wake up after a wakeup reaction time of *dStarWakeupReactionTime*, i.e. to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is enabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Set the APM flag via host command. — Wait 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. b) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. c) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. d) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern as described in 9.1.3.1. e) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*.

Name	**Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (with APM)**
Postamble	Standard postamble.

Table 533 — *(continued)*

Name	**Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (with APM)**
Pass criteria	*uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 1. Between 31 µs after the beginning of the wakeup pattern and 104 µs + 200 µs after the beginning of the wakeup pattern *uINTN* at *TP_AS_INTN* of the active star shall change to logical LOW state.

Table 534 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (with APM) test case defined in Table 533.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 534 — Test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to remote wakeup pattern (with APM)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} /not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.3.4 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to alternative remote wakeup (with APM)

Table 535 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to alternative remote wakeup (with APM).

Table 535 — Test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to alternative remote wakeup (with APM)

Name	**Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to alternative remote wakeup (with APM)**
Test purpose	This test checks the ability of the active star to signal the alternative remote wakeup event to the host and to wake up after a wakeup reaction time of *dStarWakeupReactionTime*, i.e. to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is enabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Set the APM flag via host command. — Wait 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. b) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. c) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. d) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one alternative wakeup pattern as described in 9.1.3.11. e) After 4 µs from the end of the second *Data_0* phase in the wakeup pattern wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*.

Name	**Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to alternative remote wakeup (with APM)**
Postamble	Standard postamble.
Pass criteria	*uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 1. Between 31 µs after the beginning of the wakeup pattern and 104 µs + 200 µs after the beginning of the wakeup pattern *uINTN* at *TP_AS_INTN* of the active star shall change to logical LOW state.

Table 536 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to alternative remote wakeup (with APM) test case defined in Table 535.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 536 — Test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to alternative remote wakeup (with APM)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.3.5 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (negative pulse, with APM)

Table 537 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse, with APM).

Table 537 — Test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse, with APM)

Name	**Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse, with APM)**
Test purpose	This test checks the ability of the active star to signal the local wakeup event (negative pulse) to the host and to wake up after a wakeup reaction time of $dStarWakeupReaction_{local}$, i.e. to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is previously disabled. This test case is skipped if — the active star – wake interface is not implemented — neither the Functional class “Active Star – voltage regulator control” nor the Functional class “Active Star – internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	Sleep preamble.
Test execution	a) Observe and acquire *uWAKE* at *TP_AS_WAKE* of the active star. b) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. c) Apply a negative wakeup pulse of 500 µs to the active star at *TP_AS_WAKE* according to *dStarWakePulseFilter* in ISO 17458-4. d) Wait 100 µs.
Postamble	Standard postamble.
Pass criteria	*uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. Between 1 µs after the occurrence of the local wakeup event and 500 µs +

Name	Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse, with APM)
	100 µs + 200 µs after the occurrence of the local wakeup event *uINTN* at *TP_AS_INTN* of the active star shall change to logical LOW state.

Table 538 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse, with APM) test case defined in Table 537.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 538 — Test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (negative pulse, with APM)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.3.6 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to LWU (positive pulse, with APM)

Table 539 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (positive pulse, with APM).

Table 539 — Test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (positive pulse, with APM)

Name	**Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (positive pulse, with APM)**
Test purpose	This test checks the ability of the active star to signal the local wakeup event (positive pulse) to the host and wake up after a wakeup reaction time of $dBDWakeupReaction_{local}$, i.e. to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is previously disabled. This test case is skipped if — the active star – wake interface is not implemented — neither the Functional class “Active Star – voltage regulator control” nor the Functional class “Active Star – internal voltage regulator” is implemented — a positive local wakeup pulse is not supported by the IUT.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{BAT} and V_{CC} are both implemented: V_{BAT} power supply of active star: default. V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Sleep preamble. — Set the APM flag via host command. — Wait 100 µs.
Test execution	a) Observe and acquire *uWAKE* at *TP_AS_WAKE* of the active star. b) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. c) Apply a positive wakeup pulse of 500 µs to the active star at *TP_AS_WAKE* according to

Name	Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (positive pulse, with APM)
	dStarWakePulseFilter in ISO 17458-4. d) Wait 100 µs.
Postamble	Standard postamble.
Pass criteria	*uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state at least until 1 µs after the rising edge of *uWAKE*. Between 1 µs after the occurrence of the wakeup pulse and 500 µs + 100 µs + 200 µs after the occurrence of the wakeup pulse *uINTN* at *TP_AS_INTN* of the active star shall change to logical LOW state.

Table 540 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (positive pulse, with APM) test case defined in Table 539.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 540 — Test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to LWU (positive pulse, with APM)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.3.7 Operation mode change from *AS_Sleep* via *AS_Standby* to *AS_Normal* due to wakeup frame (with APM)

Table 541 defines the test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to wakeup frame (with APM).

Table 541 — Test case for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to wakeup frame (with APM)

Name	**Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to wakeup frame (with APM)**
Test purpose	This test checks the ability of the active star to signal the remote wakeup event (wakeup frame) to the host, to wake up after a wakeup reaction time of *dStarWakeupReactionTime* and to change the operation mode from *AS_Sleep* via *AS_Standby* to *AS_Normal* according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is enabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Set the APM flag via host command. — Wait 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. b) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. c) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. d) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup frame containing the payload as specified in 9.1.3.12. e) After 4 µs from the end of the second *Data_0* phase in the wakeup frame payload wait 70 µs for the active star to enter *AS_Normal* via *AS_Standby*.

Name	**Operation mode change from AS_Sleep via AS_Standby to AS_Normal due to wakeup frame (with APM)**
Postamble	Standard postamble.
Pass criteria	*uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state before the negative edge on *TP_N1_TxEN*. Then, latest 70 µs + 200 µs after the positive edge on *TP_N1_TxEN*, *uINTN* at *TP_AS_INTN* of the active star shall be in logical LOW state.

Table 542 defines the test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to wakeup frame (with APM) test case defined in Table 541.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 542 — Test instances for operation mode change from AS_Sleep via AS_Standby to AS_Normal due to wakeup frame (with APM)

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.4 Mode.Active Star.Low Power.Standby

12.3.4.1 Operation mode change from *AS_Normal* to *AS_Standby* due to host command

Table 543 defines the test case for operation mode change from AS_Normal to AS_Standby due to host command.

Table 543 — Test case for operation mode change from AS_Normal to AS_Standby due to host command

Name	Operation mode change from AS_Normal to AS_Standby due to host command
Test purpose	This test checks the ability of the IUT to change from *AS_Normal* mode to *AS_Standby* due to host command according to ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.7. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.7. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.7. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.7.

Name	Operation mode change from AS_Normal to AS_Standby due to host command
	e) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. f) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. h) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. i) Stimulate the active star via the host interface to enter *AS_Standby*. j) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten 50/50 patterns. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2. l) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical HIGH state during the test execution. — *uRxD* of all observed nodes except node 2 shall not contain the 50/50 pattern transmitted by node, i.e. *uRxD* of all observed nodes except node 2 shall be in logical HIGH state during the test execution. — *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode. — In case of an available RxD signal *uRxD* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state during the test execution.

Table 544 defines the test instances for operation mode change from AS_Normal to AS_Standby due to host command test case defined in Table 543.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 544 — Test instances for operation mode change from AS_Normal to AS_Standby due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.4.2 Operation mode change from *AS_Sleep* to *AS_Standby* due to host command

Table 545 defines the test case for operation mode change from AS_Sleep to AS_Standby due to host command.

Table 545 — Test case for operation mode change from AS_Sleep to AS_Standby due to host command

Name	Operation mode change from AS_Sleep to AS_Standby due to host command
Test purpose	This test checks the ability of the IUT to change from *AS_Sleep* mode to *AS_Standby* due to host command ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Sleep preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.7. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.7. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.7. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.7. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the active star via the host interface to enter *AS_Standby*.

Name	Operation mode change from AS_Sleep to AS_Standby due to host command
	g) Wait 100 µs for the active star to enter *AS_Standby*. h) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten 50/50 pattern. i) Trigger the scope and the logic analyzer to start the observation synchronously with the stimulation of node 2.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical HIGH state during the test execution. — *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode.

Table 546 defines the test instances for operation mode change from AS_Sleep to AS_Standby due to host command test case defined in Table 545.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 546 — Test instances for operation mode change from AS_Sleep to AS_Standby due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.4.3 Operation mode change *AS_Normal* to *AS_Standby* due to undervoltage $V_{StarSupply}$

Table 547 defines the test case for operation mode change AS_Normal to AS_Standby due to undervoltage VStarSupply.

Table 547 — Test case for operation mode change AS_Normal to AS_Standby due to undervoltage VStarSupply

Name	Operation mode change AS_Normal to AS_Standby due to undervoltage VStarSupply
Test purpose	This test checks the ability of the IUT to change from *AS_Normal* mode to *AS_Standby* due to undervoltage condition occurring at $V_{StarSupply}$ according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{CC} is implemented: external V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: external V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	While setting $V_{StarSupply}$ at the active star to undervoltage, potential voltages at all implemented supplies, i.e. V_{BAT}, V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.7. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.7. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.7. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.7. e) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. f) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. h) Set $V_{StarSupply}$ power supply of the active star to undervoltage: depends on

Name	Operation mode change AS_Normal to AS_Standby due to undervoltage VStarSupply
	implementation. i) After 1 ms [a] stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten [b] 50/50 patterns. j) Trigger the scope and the logic analyzer to start the observation synchronously with the stimulation at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case of an available RxD signal *uRxD* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state during the test execution. — *uINTN* at *TP_AS_INTN* of the active star shall be in logical LOW state during the observation window. — *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode.
[a] Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least. [b] The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 548 defines the test instances for operation mode change AS_Normal to AS_Standby due to undervoltage VStarSupply test case defined in Table 547.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 548 — Test instances for operation mode change AS_Normal to AS_Standby due to undervoltage VStarSupply

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

12.3.4.4 AS remains in *AS_Standby* after *dStarGoToSleep*

Table 549 defines the test case for AS remains in AS_Standby after dStarGoToSleep.

Table 549 — Test case for AS remains in AS_Standby after dStarGoToSleep

Name	AS remains in AS_Standby after dStarGoToSleep
Test purpose	This test checks the ability of the active star to remain in *AS_Standby* mode if all branches are in *Branch_Idle* for longer than *dStarGoToSleep* according to ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standby preamble. — Interrupt BP and BM of the nodes 21..24 (branch 2) and 11..14 (branch 4).
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.7. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.7. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.7. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.7. e) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star.

Name	AS remains in AS_Standby after dStarGoToSleep
	h) Wait at least 6 400 ms. i) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten 50/50 pattern. j) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2. k) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical HIGH state during the test execution. — *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode. — In case of an available RxD signal *uRxD* at *TP_AS_RxD* of the active star shall be in logical HIGH state during the test execution. — In case of an available RxEN signal *uRxEN* at *TP_AS_RxEN* of the active star shall be in logical HIGH state during the test execution.

Table 550 defines the test instances for AS remains in AS_Standby after dStarGoToSleep test case defined in Table 549.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 550 — Test instances for AS remains in AS_Standby after dStarGoToSleep

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.5 Mode.Active Star.Low Power.Standby.Wakeup

12.3.5.1 Operation mode change from *AS_Standby* to *AS_Normal* due to remote wakeup

Table 551 defines the test case for operation mode change from AS_Standby to AS_Normal due to remote wakeup.

Table 551 — Test case for operation mode change from AS_Standby to AS_Normal due to remote wakeup

Name	**Operation mode change from AS_Standby to AS_Normal due to remote wakeup (retransmission of wakeup symbols)**
Test purpose	This test checks the ability of the IUT to change its operation mode from *AS_Standby* mode to *AS_Normal* mode due to remote wakeup event according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standby preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.4. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.4. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.4. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.4.

Name	**Operation mode change from AS_Standby to AS_Normal due to remote wakeup (retransmission of wakeup symbols)**
	e) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. f) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. g) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. h) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. i) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. j) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. k) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern. l) Trigger the scope to start the observation 1 µs after the end of the second *Data_0* phase in the wakeup pattern. m) Trigger the logic analyzer to start the observation synchronously with the stimulation at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The verification of *uBP* and *uBM* shall be performed only in branches connected to the same active star device that receives the remote wakeup. — *uBP* and *uBM* of the observed branches that are connected to the same active star device that receives the remote wakeup shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* shall be between -200 mV and +200 mV (*Idle_LP*). After the detection of the remote wakeup event, *uBP* and *uBM* shall change to *Idle* state, i.e. *uBP* and *uBM* shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*) within 104 µs after the beginning of the wakeup pattern. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution. — *uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state at least until 31 µs after the first falling edge of *uTxD* or *uTxEN* of node 1. Between 31 µs after the beginning of the wakeup pattern and 104 µs + 200 µs after the beginning of the wakeup pattern *uINTN* at *TP_AS_INTN* of the active star shall change to logical LOW state. — In case of an available RxD signal *uRxD* of the active star shall be in logical HIGH state permanently. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state initially and shall change to logical LOW state for signaling the detection of a wakeup, i.e. shall contain one falling edge. While entering *AS_Normal* mode *uRxEN* of the active star shall change back to logical HIGH state.

Table 552 defines the test instances for operation mode change from AS_Standby to AS_Normal due to remote wakeup test case defined in Table 551.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 552 — Test instances for operation mode change from AS_Standby to AS_Normal due to remote wakeup

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.5.2 Operation mode change from *AS_Standby* to *AS_Normal* due to LWU (negative pulse)

Table 553 defines the test case for operation mode change from AS_Standby to AS_Normal due to LWU (negative pulse).

Table 553 — Test case for operation mode change from AS_Standby to AS_Normal due to LWU (negative pulse)

Name	Operation mode change from AS_Standby to AS_Normal due to LWU (negative pulse)
Test purpose	This test checks the ability of the IUT to change its operation mode from *AS_Standby* mode to *AS_Normal* mode due to a negative local wakeup pulse according to ISO 17458-4 while no stress condition is present. This test case is skipped if — the active star – wake interface is not implemented — neither the Functional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standby preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.10. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.10. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.10. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.10. e) Observe and acquire *uWAKE* at *TP_AS_WAKE* of the active star.

Name	Operation mode change from AS_Standby to AS_Normal due to LWU (negative pulse)
	f) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. g) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. h) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. i) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. j) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. k) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. l) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. m) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. n) Apply a negative wakeup pulse of 500 µs to the active star at *TP_AS_WAKE* according to *dStarWakePulseFilter* in ISO 17458-4. o) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. p) Trigger the scope to start the observation 1 µs after the falling edge of *uWAKE* at *TP_AS_WAKE* of the active star. q) Trigger the logic analyzer to start the observation synchronously with the falling edge of *uWAKE* at *TP_AS_WAKE* of the active star.
Postamble	Standard postamble.
Pass criteria	— *uBP* and *uBM* of branch 2 and 4 shall indicate *Idle_LP* initially, i.e. *uBP* and *uBM* of branch 2 and 4 shall be between -200 mV and +200 mV (*Idle_LP*). After the wakeup event is detected (between 1 µs after the occurrence of the local wakeup event and 100 µs + 500 µs after the occurrence of the local wakeup event), *uBP* and *uBM* of branch 2 and 4 shall change to *Idle* state, i.e. *uBP* and *uBM* of branch 2 and 4 shall change to a voltage level between 1 800 mV and 3 200 mV (*Idle*). — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution. — *uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state at least until 1 µs after the falling edge of *uWAKE*. Between 1 µs after the occurrence of the wakeup event and 100 µs + 500 µs + 200 µs after the occurrence of the wakeup event *uINTN* at *TP_AS_INTN* of the active star shall change to logical LOW state. — In case of an available RxD signal *uRxD* of the active star shall be in logical HIGH state permanently. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical HIGH state initially and shall change to logical LOW state for signaling the detection of the local wakeup, i.e. shall contain one falling edge. While entering *AS_Normal* mode *uRxEN* of the active star shall change back to logical HIGH state.

Table 554 defines the test instances for operation mode change from AS_Standby to AS_Normal due to LWU (negative pulse) test case defined in Table 553.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 554 — Test instances for operation mode change from AS_Standby to AS_Normal due to LWU (negative pulse)

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	—
Configuration	**Power supply**	—	—	V_{BAT} = 7,0 V (if V_{CC} impl.) V_{BAT} = 5,5 V (if V_{CC} not impl.)
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.6 Mode.Active Star.Branch.FailSilent

12.3.6.1 Operation state change from *Branch_TxOnly* to *Branch_FailSilent*

Table 555 defines the test case for operation state change from Branch_TxOnly to Branch_FailSilent.

Table 555 — Test case for operation state change from Branch_TxOnly to Branch_FailSilent

Name	Operation state change from Branch_TxOnly to Branch_FailSilent
Test purpose	This test checks the parameter *dBranchRxActiveMax* and the ability of the active star to change its branch state from *Branch_TxOnly* to *Branch_FailSilent* according to ISO 17458-4 and to signal an error to the host due to babbling idiot while no stress condition is present. Additionally, the transitions 5, 6 and 11 are indirectly tested.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Set the APM flag via host command. — Wait 100 µs.
Test execution	a) Observe and acquire *uBus* at *TPAS1_B2* of the transmitting branch 2 according to the observation window described in 9.1.4.2. b) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. c) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 2, 11, 12, 13 and 14. d) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 2, 11, 12, 13 and 14. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by

Name	Operation state change from Branch_TxOnly to Branch_FailSilent
	one babbling idiot pattern as defined in 10.2.3.1. g) 100 ms[a] after the end of the babbling idiot pattern short-circuit BP to BM (failure FL21) of the AS at *TPAS1_B4.* h) Stimulate the bus driver of node 2 by one TSS pattern, followed by eight 50/50 patterns. i) 300 ms[b] after the end of the babbling idiot pattern disable the short-circuit of BP to BM (failure FL21) of the AS at *TPAS1_B4.* j) Stimulate the bus driver of node 11 by one TSS pattern, followed by one 50/50 pattern. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N11_TxEN* of node 11.
Postamble	Standard postamble.
Pass criteria	— While the bus driver of node 11 is being stimulated the active star shall switch branch 4 back to *Branch_TxOnly*, i.e. the absolute value of *uBus* at branch 2 shall be between 0 mV and 30mV ($uStarTx_{idle}$) when node 11 is being stimulated. That means that the active star shall have detected that the bus error has been disabled before the stimulation of the bus driver of node 11 and shall not receive the pattern sent by node 11. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution. — *uINTN* shall change to logical LOW state latest 200 µs after the rising edge of *uTxEN* at *TP_N2_TxEN* of node 2.
a Space time for measurement and reaction of the IUT, i.e. idle detection time, error detection time, etc. b Space time for measurement and reaction of the IUT, i.e. idle detection time, error detection time, etc.	

Table 556 defines the test instances for operation state change from Branch_TxOnly to Branch_FailSilent test case defined in Table 555.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 556 — Test instances for operation state change from Branch_TxOnly to Branch_FailSilent

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.7 Mode.Active Star.Branch.Disabled

12.3.7.1 Branch operation state transition from *Branch_Transmit* to *Branch_Disabled* due to host command

Table 557 defines the test case for branch operation state transition from Branch_Transmit to Branch_Disabled due to host command.

Table 557 — Test case for branch operation state transition from Branch_Transmit to Branch_Disabled due to host command

Name	**Branch operation state transition from Branch_Transmit to Branch_Disabled due to host command**
Test purpose	This test checks the ability of the active star to switch its branch operation state from *Branch_Transmit* to *Branch_Disabled* due to host command according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: babbling idiot.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 12, 13 and 14. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 12, 13 and 14. c) Observe and acquire *uSCSN* at *TP_AS_SCSN* of the active star. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except nodes 12, 13 and 14. e) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star.

Name	Branch operation state transition from Branch_Transmit to Branch_Disabled due to host command
	g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. h) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by one starting babbling idiot pattern as defined in 12.1.3.1. i) Latest 100 µs + 10 µs (safety margin for measurement) before the end of the "starting babbling idiot pattern" stimulate branch 1 of the active star via the host interface to enter *Branch_Disabled*. j) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N12_TxD* and *TP_N12_TxEN* of node 12.
Postamble	Standard postamble.
Pass criteria	— *uRxD* at *TP_Nx_RxD* of all observed nodes except node 1 shall be in logical LOW state while the transmission of the "starting babbling idiot pattern". — *uRxD* at *TP_N1_RxD* of node 1 shall be in logical LOW state initially. After branch 1 has been stimulated to enter *Branch_Disabled*, i.e. latest 100 µs after the positive edge of *uSCSN* at *TP_AS_SCSN* of the active star, *uRxD* at *TP_N1_RxD* of node 1 shall be in logical HIGH state. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution. — In case of an available RxD signal *uRxD* of the active star shall be in logical LOW state while the transmission of the "starting babbling idiot pattern", i.e. *uRxD* of the active star shall signal the pattern transmitted by the stimulated nodes. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state while *uRxD* of the active star signals the received pattern, i.e. *uRxEN* of the active star shall signal the pattern transmitted by the stimulated nodes.

Table 558 defines the test instances for branch operation state transition from Branch_Transmit to Branch_Disabled due to host command test case defined in Table 557.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 558 — Test instances for branch operation state transition from Branch_Transmit to Branch_Disabled due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.7.2 Branch operation state transition from *Branch_Idle* to *Branch_Disabled* due to host command

Table 559 defines the test case for branch operation state transition from Branch_Idle to Branch_Disabled due to host command.

Table 559 — Test case for branch operation state transition from Branch_Idle to Branch_Disabled due to host command

Name	Branch operation state transition from Branch_Idle to Branch_Disabled due to host command
Test purpose	This test checks the ability of the active star to switch its branch operation state from *Branch_Idle* to *Branch_Disabled* due to host command according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of the active star. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. g) Stimulate branch 2 of the active star via the host interface to enter *Branch_Disabled*. h) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.

Name	Branch operation state transition from Branch_Idle to Branch_Disabled due to host command
	i) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of nodes 21 .. 24 shall be in logical HIGH state during the test execution, i.e. branch 2 of the active star have entered *Branch_Disabled.* — *uRxD* of all nodes except nodes 21 .. 24 shall contain the 50/50 pattern transmitted by node 2. — In case of an available INH1 signal *uINH1* of the active star shall be in logical HIGH state during the test execution.

Table 560 defines the test instances for branch operation state transition from Branch_Idle to Branch_Disabled due to host command test case defined in Table 559.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 560 — Test instances for branch operation state transition from Branch_Idle to Branch_Disabled due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.7.3 Branch operation state transition from *Branch_Receive* to *Branch_Disabled* due to host command

Table 561 defines the test case for branch operation state transition from Branch_Receive to Branch_Disabled due to host command.

Table 561 — Test case for branch operation state transition from Branch_Receive to Branch_Disabled due to host command

Name	**Branch operation state transition from Branch_Receive to Branch_Disabled due to host command**
Test purpose	This test checks the ability of the active star to switch its branch operation state from *Branch_Receive* to *Branch_Disabled* due to host command according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: starting babbling idiot.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 12, 13 and 14. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 12, 13 and 14. c) Observe and acquire *uSCSN* at *TP_AS_SCSN* of the active star. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except nodes 12, 13 and 14. e) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. h) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by

Name	Branch operation state transition from Branch_Receive to Branch_Disabled due to host command
	one starting babbling idiot pattern as defined in 12.1.3.1. i) Latest 100 µs + 10 µs (safety margin for measurement) before the end of the "starting babbling idiot pattern" stimulate branch 4 of the active star via the host interface to enter *Branch_Disabled*. j) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N12_TxD* and *TP_N12_TxEN* of node 12.
Postamble	Standard postamble.
Pass criteria	— *uRxD* at *TP_Nx_RxD* of all observed nodes shall be in logical LOW state initially. After branch 4 has been stimulated to enter *Branch_Disabled*, i.e. latest 100 µs after the positive edge of *uSCSN* at *TP_AS_SCSN* of the active star, *uRxD* at *TP_Nx_RxD* of all observed nodes shall be in logical HIGH state. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution. — In case of an available RxD signal *uRxD* of the active star shall be in logical LOW state initially, i.e. *uRxD* of the active star shall signal the pattern transmitted by the stimulated nodes. After branch 4 has been stimulated to enter *Branch_Disabled*, i.e. latest 100 µs after the positive edge of *uSCSN* at *TP_AS_SCSN* of the active star *uRxD* of the AS shall be in logical HIGH state. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state initially, i.e. *uRxEN* of the AS shall signal the pattern transmitted by the stimulated nodes. After branch 4 has been stimulated to enter *Branch_Disabled*, i.e. latest 100 µs after the positive edge of *uSCSN* at *TP_AS_SCSN* of the active star *uRxEN* of the active star shall be in logical HIGH state.

Table 562 defines the test instances for branch operation state transition from Branch_Receive to Branch_Disabled due to host command test case defined in Table 561.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 562 — Test instances for branch operation state transition from Branch_Receive to Branch_Disabled due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.7.4 Operation state change from *Branch_FailSilent* to *Branch_Disabled* due to host command

Table 563 defines the Test case for operation state change from Branch_FailSilent to Branch_Disabled due to host command.

Table 563 — Test case for operation state change from *Branch_FailSilent* to *Branch_Disabled* due to host command

Name	Operation state change from *Branch_FailSilent* to *Branch_Disabled* due to host command
Test purpose	This test checks the ability of the active star to switch its branch operation state from *Branch_FailSilent* to *Branch_Disabled* due to host command according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. b) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 2, 12, 13 and 14. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 2, 12, 13 and 14. d) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star.

Name	Operation state change from *Branch_FailSilent* to *Branch_Disabled* due to host command
	h) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1. i) After the end of the babbling idiot pattern stimulate branch 4 of the active star via the host interface to enter *Branch_Disabled*. j) After 100 µs stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten [a] 50/50 patterns. k) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2. l) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution. — *uRxD* at *TP_Nx_RxD* of all nodes except nodes 11..14 shall contain the 50/50 pattern transmitted by node 2. — In case of an available RxD signal *uRxD* of the active star shall contain the 50/50 pattern transmitted by node 2. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state during the observation window, i.e. *uRxEN* of the active star shall signal the pattern transmitted by node 2.
[a] The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 564 defines the test instances for operation state change from Branch_FailSilent to Branch_Disabled due to host command test case defined in Table 563.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 564 — Test instances for operation state change from *Branch_FailSilent* to *Branch_Disabled* due to host command

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.7.5 Operation state change from *Branch_TxOnly* to *Branch_Disabled* due to host command

Table 565 defines the test case for operation state change from Branch_TxOnly to Branch_Disabled due to host command.

Table 565 — Test case for operation state change from *Branch_TxOnly* to *Branch_Disabled* due to host command

Name	Operation state change from *Branch_TxOnly* to *Branch_Disabled* due to host command
Test purpose	This test checks the ability of the active star to switch its branch operation state from *Branch_TxOnly* to *Branch_Disabled* due to host command according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Set the APM flag via host command. — Wait 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 2, 12, 13 and 14. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 2, 12, 13 and 14. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the

Name	Operation state change from *Branch_TxOnly* to *Branch_Disabled* due to host command
	active star. h) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1. i) Wait 5 µs for the active star to detect *Idle* on the bus. j) After the end of the babbling idiot pattern stimulate branch 4 of the active star via the host interface to enter *Branch_Disabled*. k) After 100 µs stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten [a] 50/50 patterns. l) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution. — *uRxD* at *TP_Nx_RxD* of all nodes except nodes 11..14 shall contain the 50/50 pattern transmitted by node 2. — In case of an available RxD signal *uRxD* of the active star shall contain the 50/50 pattern transmitted by node 2. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state during the observation window, i.e. *uRxEN* of the active star shall signal the pattern transmitted by node 2.
[a] The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 566 defines the test instances for operation state change from Branch_TxOnly to Branch_Disabled due to host command test case defined in Table 565.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 566 — Test instances for operation state change from *Branch_TxOnly* to *Branch_Disabled* due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	— AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.7.6 Branch remain in state *Branch_Disabled* while undervoltage V_{IO}

Table 567 defines the test case for branch remain in state Branch_Disabled while undervoltage V_{IO}.

Table 567 — Test case for branch remain in state *Branch_Disabled* while undervoltage V_{IO}

Name	Branch remain in state *Branch_Disabled* while undervoltage V_{IO}
Test purpose	This test checks the ability of the active star to remain its branch in *Branch_Disabled* in case of undervoltage at V_{IO} according to ISO 17458-4 while no stress condition is present. This test case is skipped if the Functional class "Active star – logic level adaptation" is not implemented.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — external V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Stimulate branch 2 of the active star via the host interface to enter *Branch_Disabled*. — Wait 100 µs.
Test execution	a) Observe and acquire *uTxD* at *TP_N1_TxD* of node 1. b) Observe and acquire *uTxEN* at *TP_N1_TxEN* of node 1. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. e) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. g) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN*

Name	Branch remain in state *Branch_Disabled* while undervoltage V_{IO}
	of all nodes. h) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. i) Set the external V_{IO} reference voltage of active star to $V_{IOUndervoltage}$. j) Stimulate the IUT in node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one TSS pattern, followed by a 50/50 pattern. Repeat this sequence for longer than 1 100 ms. The bit duration in this test case shall be gdBit=25 µs, because the memory depth of the logic analyzer is much too small to acquire more than one second with a 100 ns bit time. The gap between the messages shall be 9,25 ms. k) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution. — *uRxD* at *TP_Nx_RxD* of all nodes except nodes 21 .. 24 shall contain the 50/50 pattern transmitted by node 1. — In case of an available RxD signal *uRxD* of the active star shall be in logical LOW state latest 1 second after the undervoltage on V_{IO} is applied. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state latest 1 second after the undervoltage on V_{IO} is applied. — *uINTN* at *TP_AS_INTN* of the active star shall be in logical LOW state after the undervoltage on V_{IO} is detected.
a The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 568 defines the test instances for branch remain in state Branch_Disabled while undervoltage V_{IO} test case defined in Table 567.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 568 — Test instances for branch remain in state *Branch_Disabled* while undervoltage V_{IO}

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.8 Mode.Active Star.Branch.LowPower

12.3.8.1 Operation state change from *Branch_Disabled* to *Branch_LowPower* due to undervoltage $V_{StarSupply}$

Table 569 defines the test case for operation state change from Branch_Disabled to Branch_LowPower due to undervoltage VStarSupply.

Table 569 — Test case for operation state change from *Branch_Disabled* to *Branch_LowPower* due to undervoltage VStarSupply

Name	**Operation state change from *Branch_Disabled* to *Branch_LowPower* due to undervoltage VStarSupply**
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_Disabled* to *Branch_LowPower* due to undervoltage condition occurring at $V_{StarSupply}$ according to ISO 17458-4 while no stress condition is present.

Configuration	— Topology: as specified in previous configuration see 12.1.
	— In case that V_{CC} is implemented:
	  — External V_{CC} power supply of active star: +5,0 V
	  — In case that the $V_{StarSupply}$ power supply of the active star depends on V_{CC}: external V_{CC} power supply of active star: +5,0 V.
	— In case that V_{BAT} is implemented:
	  — External V_{BAT} power supply of active star: default
	  — In case that the $V_{StarSupply}$ power supply of the active star depends on V_{BAT}: external V_{BAT} power supply of active star: default.
	— In case that V_{IO} is implemented:
	External V_{IO} reference voltage of active star: depends on implementation.
	— Ground shift: 0 V.
	— Failure: none.
	— Communication: single node.

Preamble (setup state)	— Standard preamble. — Stimulate the branches 1, 2 and 4 of the active star via host command to enter *Branch_Disabled*. — Wait 100 µs for the active star to switch its branches to *Branch_Disabled*. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	While setting $V_{StarSupply}$ at the active star to undervoltage, potential voltages at all implemented supplies, i.e. V_{BAT}, V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to

Name	Operation state change from *Branch_Disabled* to *Branch_LowPower* due to undervoltage VStarSupply
	the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5. e) Set $V_{StarSupply}$ power supply of the active star to undervoltage: depends on implementation. f) 1 ms [a] after the undervoltage is set stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten [b] 50/50 patterns. g) Trigger the scope to start the observation 1 ms before the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode.
[a] Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least. [b] The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms.	

Table 570 defines the test instances for operation state change from Branch_Disabled to Branch_LowPower due to undervoltage VStarSupply test case defined in Table 569.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 570 — Test instances for operation state change from *Branch_Disabled* to *Branch_LowPower* due to undervoltage VStarSupply

Instance		**1**	**2**
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

12.3.8.2 Operation state change from *Branch_FailSilent* to *Branch_LowPower* due to undervoltage $V_{StarSupply}$

Table 571 defines the test case for operation state change from Branch_FailSilent to Branch_LowPower due to undervoltage VStarSupply.

Table 571 — Test case for operation state change from *Branch_FailSilent* to *Branch_LowPower* due to undervoltage VStarSupply

Name	**Operation state change from *Branch_FailSilent* to *Branch_LowPower* due to undervoltage VStarSupply**
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_FailSilent* to *Branch_LowPower* due to undervoltage condition occurring at $V_{StarSupply}$ according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{CC} is implemented: external V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: external V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: external V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	While setting $V_{StarSupply}$ at the active star to undervoltage, potential voltages at all implemented supplies, i.e. V_{BAT}, V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5. e) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1. f) After the end of the babbling idiot pattern set $V_{StarSupply}$ power supply of the active star to undervoltage: depends on implementation. g) 1 ms [a] after the undervoltage is set stimulate the IUT in node 2 at *TP_N2_TxD* and

Name	Operation state change from *Branch_FailSilent* to *Branch_LowPower* due to undervoltage VStarSupply
	TP_N2_TxEN by one TSS pattern, followed by ten [b] 50/50 patterns. h) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode.
[a] Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device's datasheet at least. [b] The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 572 defines the test instances for operation state change from Branch_FailSilent to Branch_LowPower due to undervoltage VStarSupply test cease defined in Table 571.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 572 — Test instances for operation state change from *Branch_FailSilent* to *Branch_LowPower* due to undervoltage VStarSupply

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

12.3.8.3 Operation state change from *Branch_Idle* to *Branch_LowPower* due to undervoltage $V_{StarSupply}$

Table 573 defines the test case for operation state change from Branch_Idle to Branch_LowPower due to undervoltage VStarSupply.

Table 573 — Test case for operation state change from *Branch_Idle* to *Branch_LowPower* due to undervoltage VStarSupply

Name	**Operation state change from *Branch_Idle* to *Branch_LowPower* due to undervoltage VStarSupply**
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_Idle* to *Branch_LowPower* due to undervoltage condition occurring at $V_{StarSupply}$ according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{CC} is implemented: In case that the $V_{StarSupply}$ power supply of the active star depends on V_{CC}: external V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} is implemented: In case that the $V_{StarSupply}$ power supply of the active star depends on V_{BAT}: external V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: External V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	While setting $V_{StarSupply}$ at the active star to undervoltage, potential voltages at all implemented supplies, i.e. V_{BAT}, V_{CC} and $V_{StarSupply}$ shall be discharged, e.g. via a resistor to GND. a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.7. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.7. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.7. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.7. e) Set $V_{StarSupply}$ power supply of the active star to undervoltage: depends on implementation. f) After 1 ms stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS

Name	Operation state change from *Branch_Idle* to *Branch_LowPower* due to undervoltage VStarSupply
	pattern, followed by ten 50/50 patterns. g) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode.

Table 574 defines the test instances for operation state change from Branch_Idle to Branch_LowPower due to undervoltage VStarSupply test case defined in Table 573.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 574 — Test instances for operation state change from *Branch_Idle* to *Branch_LowPower* due to

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

12.3.8.4 Operation state change from *Branch_FailSilent* to *Branch_LowPower* due to mode change to *AS_Standby*

Table 575 defines the test case for operation state change from Branch_FailSilent to Branch_LowPower due to mode change to *AS_Standby*.

Table 575 — Test case for operation state change from *Branch_FailSilent* to *Branch_LowPower* due to mode change to *AS_Standby*

Name	**Operation state change from *Branch_FailSilent* to *Branch_LowPower* due to mode change to *AS_Standby***
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_FailSilent* to *Branch_LowPower* due to the mode change from *AS_Normal* to *AS_Standby* by host command according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 2, 12, 13 and 14. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 2, 12, 13 and 14. c) Observe and acquire *uSCSN* at *TP_AS_SCSN* of the active star. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 2. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1. g) After the end of the babbling idiot pattern stimulate the active star via the host interface

Name	Operation state change from *Branch_FailSilent* to *Branch_LowPower* due to mode change to *AS_Standby*
	to enter *AS_Standby*. h) After 100 µs stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten [a] 50/50 patterns. i) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 12.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution. — *uRxD* of all observed nodes shall be in logical HIGH state after the end of the babbling idiot pattern, i.e. the active star shall be in *AS_Standby* mode.
[a] The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 576 defines the test instances for operation state change from Branch_FailSilent to Branch_LowPower due to mode change to *AS_Standby* test case defined in Table 575.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 576 — Test instances for operation state change from *Branch_FailSilent* to *Branch_LowPower* due to mode change to *AS_Standby*

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.8.5 Operation state change from *Branch_Idle* to *Branch_LowPower* due to mode change to *AS_Standby*

Table 577 defines the test case for operation state change from Branch_Idle to Branch_LowPower due to mode change to *AS_Standby*.

Table 577 — Test case for operation state change from *Branch_Idle* to *Branch_LowPower* due to mode change to *AS_Standby*

Name	**Operation state change from *Branch_Idle* to *Branch_LowPower* due to mode change to *AS_Standby***
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_Idle* to *Branch_LowPower* due to host command according to ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of the nodes 21..24 (branch 2) and 11..14 (branch 4).
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.7. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.7. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.7. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.7. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star.

Name	**Operation state change from *Branch_Idle* to *Branch_LowPower* due to mode change to *AS_Standby***
	f) Stimulate the active star via the host interface to enter *AS_Standby*. g) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Trigger the scope and the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2.
Postamble	— Standard postamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Pass criteria	— *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode. — In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical HIGH state during the test execution.

Table 578 defines the test instances for operation state change from Branch_Idle to Branch_LowPower due to mode change to *AS_Standby* test case defined in Table 577.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 578 — Test instances for operation state change from *Branch_Idle* to *Branch_LowPower* due to mode change to *AS_Standby*

Instance		**1**	**2**	**3**
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.8.6 Operation state change from *Branch_Disabled* to *Branch_LowPower* due to mode change to *AS_Standby*

Table 579 defines the test case for operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Standby.

Table 579 — Test case for operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Standby

Name	**Operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Standby**
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_Disabled* to *Branch_LowPower* due to host command according to ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Stimulate the branches 1, 2 and 4 of the active star via host command to enter *Branch_Disabled*. — Wait 100 µs for the active star to switch its branches to *Branch_Disabled*. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to

Name	Operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Standby
	the observation window described in 10.2.4.5. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the active star via the host interface to enter *AS_Standby*. g) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Trigger the scope and the logic analyzer to start the observation synchronously the first stimuli at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode. — In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical HIGH state during the test execution.

Table 580 defines the test instances for operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Standby test case defined in Table 579.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 580 — Test instances for operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Standby

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.8.7 Operation state change from *Branch_FailSilent* to *Branch_LowPower* due to mode change to *AS_Sleep*

Table 581 defines the test case for operation state change from Branch_FailSilent to Branch_LowPower due to mode change to AS_Sleep.

Table 581 — Test case for operation state change from Branch_FailSilent to Branch_LowPower due to mode change to AS_Sleep

Name	**Operation state change from Branch_FailSilent to Branch_LowPower due to mode change to AS_Sleep**
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_FailSilent* to *Branch_LowPower* due to the mode change from *AS_Normal* to *AS_Sleep* by host command according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of nodes 2, 12, 13 and 14. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of nodes 2, 12, 13 and 14. c) Observe and acquire *uSCSN* at *TP_AS_SCSN* of the active star. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes except node 2. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1. g) After the end of the babbling idiot pattern stimulate the active star via the host interface

Name	Operation state change from Branch_FailSilent to Branch_LowPower due to mode change to AS_Sleep
	to enter *AS_Sleep*. h) After 100 µs stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by ten [a] 50/50 patterns. i) Trigger the scope and the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— In case of an available INH1 signal *uINH1* shall be logical HIGH state at the beginning of the test execution, then latest 100 µsafter the positive edge on SCSN INH1 shall be in logical LOW state — uRxD of all observed nodes shall be in logical HIGH state after the end of the babbling idiot pattern, i.e. the active star shall be in *AS_Standby* mode.
[a] The low phase shall be long enough to allow the logic analyzer to detect each received low phase in an observation period of at least 1 000 ms	

Table 582 defines the test instances for operation state change from Branch_FailSilent to Branch_LowPower due to mode change to AS_Sleep test case defined in Table 581.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 582 — Test instances for operation state change from Branch_FailSilent to Branch_LowPower due to mode change to AS_Sleep

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.8.8 Operation state change from *Branch_Idle* to *Branch_LowPower* due to mode change to *AS_Sleep*

Table 583 defines the test case for operation state change from Branch_Idle to Branch_LowPower due to mode change to AS_Sleep.

Table 583 — Test case for operation state change from Branch_Idle to Branch_LowPower due to mode change to AS_Sleep

Name	**Operation state change from Branch_Idle to Branch_LowPower due to mode change to AS_Sleep**
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_Idle* to *Branch_LowPower* due to the mode change from *AS_Normal* to *AS_Sleep* by host command according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the

Name	Operation state change from Branch_Idle to Branch_LowPower due to mode change to AS_Sleep
	active star. f) Stimulate the active star via the host interface to enter *AS_Sleep*. g) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Trigger the scope and the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode. — In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical LOW state during the test execution.

Table 584 defines the Test instances for operation state change from Branch_Idle to Branch_LowPower due to mode change to AS_Sleep test case defined in Table 583.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 584 — Test instances for operation state change from Branch_Idle to Branch_LowPower due to mode change to AS_Sleep

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.8.9 Operation state change from *Branch_Disabled* to *Branch_LowPower* due to mode change to *AS_Sleep*

Table 585 defines the test case for operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Sleep.

Table 585 — Test case for operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Sleep

Name	**Operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Sleep**
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_Disabled* to *Branch_LowPower* due to the mode change from *AS_Normal* to *AS_Sleep* by host command according to ISO 17458-4 while no stress condition is present and autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Stimulate the branches 1, 2 and 4 of the active star via host command to enter *Branch_Disabled*. — Wait 100 µs for the active star to switch its branches to *Branch_Disabled*. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5.

Name	Operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Sleep
	d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5. e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Stimulate the active star via the host interface to enter *AS_Sleep*. g) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) Trigger the scope and the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode. — In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical LOW state during the test execution.

Table 586 defines the test instances for operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Sleep test case defined in Table 585.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 586 — Test instances for operation state change from Branch_Disabled to Branch_LowPower due to mode change to AS_Sleep

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.8.10 Operation state change from *Branch_Disabled* to *Branch_LowPower* after *dStarGoToSleep*

Table 587 defines the test case for operation state change from Branch_Disabled to Branch_LowPower after dStarGoToSleep.

Table 587 — Test case for operation state change from Branch_Disabled to Branch_LowPower after dStarGoToSleep

Name	Operation state change from Branch_Disabled to Branch_LowPower after dStarGoToSleep
Test purpose	This test checks the ability of the IUT to change the state of the branch from *Branch_Disabled* to *Branch_LowPower* after *dStarGoToSleep* according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Stimulate the branches of the active star via the host interface to enter *Branch_Disabled*. — Wait 100 µs for the active star to switch its branches to *Branch_Disabled*. — Interrupt BP and BM of branch 2 and branch 4 at the active star; i.e. no termination shall be connected to these branches.
Test execution	a) Observe and acquire *uBP* at *TPAS1_B2_BP* of the transmitting branch 2 according to the observation window described in 10.2.4.5. b) Observe and acquire *uBM* at *TPAS1_B2_BM* of the transmitting branch 2 according to the observation window described in 10.2.4.5. c) Observe and acquire *uBP* at *TPAS1_B4_BP* of the transmitting branch 4 according to the observation window described in 10.2.4.5. d) Observe and acquire *uBM* at *TPAS1_B4_BM* of the transmitting branch 4 according to the observation window described in 10.2.4.5.

Name	Operation state change from Branch_Disabled to Branch_LowPower after dStarGoToSleep
	e) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. f) Set the APM flag via host command. g) Wait 6 400 ms + 100 µs for the AS to enter *AS_Sleep*. h) Stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. i) Trigger the scope to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2. j) Trigger the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	The period to observe is very long in this test case. But a bit level resolution is not required. The Go-To-Sleep timeout *dStarGoToSleep* shall be measured with an error of less than 1 %. — *uBP* and *uBM* of branch 2 and 4 shall be within a voltage level between -200 mV and +200 mV (*Idle_LP*) during the observation window, i.e. the active star stall stay in a low power mode. — In case of an available INH1 signal *uINH1* shall be in logical LOW state during the observation window.

Table 588 defines the test instances for operation state change from Branch_Disabled to Branch_LowPower after dStarGoToSleep test case defined in Table 587.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 588 — Test instances for operation state change from Branch_Disabled to Branch_LowPower after dStarGoToSleep

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.9 Mode.Active Star.Branch.Idle

12.3.9.1 Branch operation state transition from *Branch_Disabled* to *Branch_Idle* due to host command

Table 589 defines the test case for Branch operation state transition from Branch_Disabled to Branch_Idle due to host command.

Table 589 — Test case for Branch operation state transition from Branch_Disabled to Branch_Idle due to host command

Name	Branch operation state transition from Branch_Disabled to Branch_Idle due to host command
Test purpose	This test checks the ability of the active star to switch its branch operation state from *Branch_Disabled* to *Branch_Idle* due to host command according to ISO 17458-4 while no stress condition is present.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Stimulate branch 3 of the active star via the host interface to enter *Branch_Disabled*. — Wait 100 µs for the active star to switch the branch to *Branch_Disabled*.
Test execution	a) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. b) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_AS_RxEN* of the active star. c) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. d) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. e) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes.

Name	Branch operation state transition from Branch_Disabled to Branch_Idle due to host command
	f) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. g) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. h) Stimulate branch 3 of the active star via the host interface to enter *Branch_Idle*. i) After 100 µs stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. j) Trigger the scope and the logic analyzer to start the observation synchronously with the stimuli at *TP_N2_TxD* and *TP_N2_TxEN* of node 2.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes shall indicate the 50/50 pattern sent by node 2. — In case of an available RxEN signal *uRxEN* of all nodes shall be in logical LOW state while the signal *uRxD* of the corresponding node signals the received pattern and shall be in logical HIGH state otherwise. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution. — In case of an available RxD signal *uRxD* of the active star shall indicate the 50/50 pattern sent by node 2. — In case of an available RxEN signal *uRxEN* of the active star shall be in logical LOW state while node 2 is being stimulated.

Table 590 defines the test instances for operation state transition from Branch_Disabled to Branch_Idle due to host command test case defined in Table 589.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 590 — Test instances for operation state transition from Branch_Disabled to Branch_Idle due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.10 Mode.Active Star.Branch.TxOnly

12.3.10.1 Operation state change from *Branch_FailSilent* to *Branch_TxOnly* due to host command

Table 591 defines the test case for operation state change from Branch_FailSilent to Branch_TxOnly due to host command.

Table 591 — Test case for operation state change from Branch_FailSilent to Branch_TxOnly due to host command

Name	Operation state change from Branch_FailSilent to Branch_TxOnly due to host command
Test purpose	This test checks the ability of the active star to switch its branch operation state from *Branch_FailSilent* to *Branch_TxOnly* due to host command according to ISO 17458-4 while no stress condition is present and the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: babbling idiot. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* and *TP_Nx_TxEN* of nodes 2, 11, 12, 13 and 14. b) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. c) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. d) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. e) Stimulate the bus drivers of nodes 12, 13 and 14 at *TP_Nx_TxD* and *TP_Nx_TxEN* by one babbling idiot pattern as defined in 10.2.3.1. f) After the end of the babbling idiot pattern stimulate branch 4 of the active star via the

Name	Operation state change from Branch_FailSilent to Branch_TxOnly due to host command
	host interface to enter *Branch_TxOnly*. g) Stimulate the IUT in node 11 at *TP_N11_TxD* and *TP_N11_TxEN* by one TSS pattern, followed by one 50/50 pattern. h) After 5,0 µs stimulate the IUT in node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern. i) After 5,0 µs stimulate the IUT in node 11 at *TP_N11_TxD* and *TP_N11_TxEN* by one TSS pattern, followed by one 50/50 pattern. j) Trigger the logic analyzer to start the observation synchronously with the first falling edge of *uTxEN* at *TP_N11_TxEN* of node 11.
Postamble	Standard postamble.
Pass criteria	— *uRxD* of all nodes except nodes 11, 12, 13 and 14 shall not contain the 50/50 pattern transmitted by node 11 at the first stimulation, i.e. the active star has switched branch 4 from *Branch_FailSilent* to *Branch_TxOnly* and receiving on this branch is not possible. — *uRxD* of the nodes 11, 12, 13 and 14 shall contain the 50/50 pattern transmitted by node 2 after the end of the babbling idiot sequence, i.e. the active star has switched branch 4 from *Branch_FailSilent* to *Branch_TxOnly* after *Idle* on all branches is detected. — *uRxD* of all nodes shall contain the 50/50 pattern transmitted by node 11 at the second stimulation, i.e. the active star has switched branch 4 from *Branch_Idle* to *Branch_Receive*. — In case of an available INH1 signal *uINH1* shall be in logical HIGH state during the test execution.

Table 592 defines the test instances for operation state change from Branch_FailSilent to Branch_TxOnly due to host command test case defined in Table 591.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 592 — Test instances for operation state change from Branch_FailSilent to Branch_TxOnly due to host command

Instance		1	2	3
Purpose	**Stress**	none	ground shift	low battery
	Precondition	—	—	AS_VRC or AS_IVR implemented
Configuration	**Power supply**	—	—	V_{BAT} = 5,5 V
	Ground shift	—	+5,0 V at AS	—
	Failure	—	—	—
Preamble		—	—	—
Test execution		—	—	—
Pass criteria		—	—	—

12.3.11 Failure.Error Indication

12.3.11.1 Short-circuit bus wires to GND

Table 593 defines the test case for short-circuit bus wires to GND.

Table 593 — Test case for short-circuit bus wires to GND

Name	**Short-circuit bus wires to GND**
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit of the bus wire to GND while the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to GND. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. d) Short-circuit BP (failure FL11) of the AS to GND at *TPAS1_B2_BP*. e) Stimulate the IUT of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern according to 9.1.3.2 followed by eight 50/50 patterns according to 9.1.3.3. f) Wait 200 µs.
Postamble	Standard postamble.
Pass criteria	*uINTN* at TP_AS_INTN of the active star shall be in logical LOW state latest 200 µs after the stimulation of node 2.

Table 594 defines the test instances for short-circuit bus wires to GND test case defined in Table 593.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 594 — Test instances for short-circuit bus wires to GND

Instance		1	2
Purpose	**Stress**	S/C BP to GND at AS	S/C BM to GND at AS
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	—	—
Preamble		—	—
Test execution		… Short-circuit BP (failure FL11) of the AS to GND at *TPAS1_B2_BP*. … Switch off short-circuit BP (failure FL11) of the AS at *TPAS1_B2_BP*. …	… Short-circuit BM (failure FL12) of the AS to GND at *TPAS1_B2_BM* … Switch off short-circuit BM (failure FL12) of the AS at *TPAS1_B2_BM*. …
Pass criteria		—	—

12.3.11.2 Short-circuit bus wires to V_{ANY}

Table 595 defines the test case for short-circuit bus wires to V_{ANY}.

Table 595 — Test case for short-circuit bus wires to V_{ANY}

Name	**Short-circuit bus wires to V_{ANY}**
Test purpose	This test checks the ability of the active star to signal the occurrence of an error in case of a short-circuit of the bus wire to +48 V [a] while the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to +48 V [a]. — Communication: Node 1 and 2 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. d) Short-circuit BP (failure FL13) of the AS to +48 V [a] at *TPAS1_B2_BP*. e) Stimulate the IUT of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern according to 9.1.3.2 followed by eight 50/50 patterns according to 9.1.3.3. f) Wait 200 µs.
Postamble	Standard postamble.
Pass criteria	*uINTN* at TP_AS_INTN of the active star shall be in logical LOW state latest 200 µs after the stimulation of node 2.
[a] In case the IUT does not support 42 V systems the V_{BAT} shall be +27 V	

Table 596 defines the test instances for short-circuit bus wires to V_{ANY} test case defined in Table 595.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 596 — Test instances for short-circuit bus wires to V_{ANY}

Instance		1	2
Purpose	**Stress**	S/C BP to +48 V at AS	S/C BM to +48 V at AS
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to +48 V[a]	S/C BM to +48 V [a]
Preamble		—	—
Test execution		… Short-circuit BP (failure FL13) of the AS to +48 V [a] at *TPAS1_B2_BP*. … Switch off short-circuit BP (failure FL13) of the AS at *TPAS1_B2_BP*. …	… Short-circuit BM (failure FL14) of the AS to +48 V [a] at *TPAS1_B2_BM.* … Switch off short-circuit BM (failure FL14) of the AS at *TPAS1_B2_BM*. …
Pass criteria		—	—

[a] In case the IUT does not support 42 V systems the V_{BAT} shall be +27 V

12.3.11.3 Short-circuit bus wires to -5 V

Table 597 defines the test case for short-circuit bus wires to -5 V.

Table 597 — Test case for short-circuit bus wires to -5 V

Name	**Short-circuit bus wires to -5 V**
Test purpose	This test checks the ability of the active star to signal the occurrence of an error in case of a short-circuit of the bus wire to -5 V while the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to -5 V. — Communication: Node 1 and 2 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. d) Short-circuit BP (failure FL19) of the AS to -5 V at *TPAS1_B2_BP*. e) Stimulate the IUT of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern according to 9.1.3.2 followed by eight 50/50 patterns according to 9.1.3.3. f) Wait 200 µs.
Postamble	Standard postamble.
Pass criteria	*uINTN* at TP_AS_INTN of the active star shall be in logical LOW state latest 200 µs after the stimulation of node 2.

Table 598 defines the test instances for short-circuit bus wires to -5 V test case defined in Table 597.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 598 — Test instances for short-circuit bus wires to -5 V

Instance		**1**	**2**
Purpose	**Stress**	S/C BP to -5 V at AS	S/C BM to -5 V at AS
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to -5 V	S/C BM to -5 V
Preamble		—	—
Test execution		… Short-circuit BP (failure FL19) of the AS to -5 V at *TPAS1_B2_BP*. … Switch off short-circuit BP (failure FL19) of the AS at *TPAS1_B2_BP*. …	… Short-circuit BM (failure FL20) of the AS to -5 V at *TPAS1_B2_BM.* … Switch off short-circuit BM (failure FL20) of the AS at *TPAS1_B2_BM*. …
Pass criteria		—	—

12.3.11.4 S/C BP to BM at AS

Table 599 defines the test case for S/C BP to BM at AS.

Table 599 — Test case for S/C BP to BM at AS

Name	S/C BP to BM at AS
Test purpose	This test checks the ability of the active star to signal the occurrence of an error in case of a short-circuit between both bus wires while the autonomous power moding flag (APM flag) is disabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to BM. — Communication: Node 1 and 2 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. d) Short-circuit BP to BM (failure FL21) of the AS at *TPAS1_B1*. e) Stimulate the IUT of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern according to 9.1.3.2 followed by eight 50/50 patterns according to 9.1.3.3. f) Wait 200 µs.
Postamble	Standard postamble.
Pass criteria	*uINTN* at TP_AS_INTN of the active star shall be in logical LOW state latest 200 µs after the stimulation of node 2.

12.3.11.5 Short-circuit between TxEN to GND

Table 600 defines the test case for short-circuit between TxEN to GND.

Table 600 — Test case for short-circuit between TxEN to GND

Name	Short-circuit between TxEN to GND
Test purpose	This test checks the ability of the active star to signal the occurrence of an error in case of TxEN is shortened to GND according to ISO 17458-4 while the autonomous power moding flag (APM flag) is disabled. This case is skipped if the Functional class “Active star – communication controller interface” is not implemented.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: short-circuit TxEN to GND. — Communication: active star as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. b) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. c) Short-circuit TxEN and GND of the IUT (AS) according to 7.6, failure FL4. d) Beginning with the falling edge of *uTxEN* of the active star, stimulate the IUT (AS) at *TP_AS_TxD* by a logical LOW state sequence of at least 2 600 µs.
Postamble	Standard postamble.
Pass criteria	*uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state initially. After activating the failure, i.e. between 650 µs and 2 600 µs +200 µs after the falling edge of *uTxD* at *TP_AS_TxD* of the active star, *uINTN* at *TP_AS_INTN* of the active star shall switch to logical LOW state.

12.3.11.6 Short-circuit bus wires to GND (without APM)

Table 601 defines the test case for short-circuit bus wires to GND (without APM).

Table 601 — Test case for short-circuit bus wires to GND (without APM)

Name	**Short-circuit bus wires to GND (without APM)**
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit of the bus wire to GND. Additionally it is checked that the IUT is not permanently damaged by the short-circuit.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to GND. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uSCSN* at *TP_AS_SCSN* of the active star. b) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 1 and 2. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 1 and 2. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 1 and 2. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 1 and 2. f) Observe and acquire $iBP_{GNDShortMax}$ at $TP\_AS\_B2\_R_{iBP}$ of the AS (shall be at *TPAS1_B2_BP*). g) Stimulate the bus driver of the transmitting node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by a current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples were taken by the data acquisition unit. h) At least 500 ns after the start of transmission short-circuit BP (failure FL11) of the AS to

Name	Short-circuit bus wires to GND (without APM)
	GND at *TPAS1_B2_BP*. i) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at node 2. Acquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*. j) Switch off the short-circuit BP (failure FL11) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds. k) Stimulate node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. l) Stimulate node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— $\|iBP_{GNDShortMax}\| \leq 60$ mA. — After switching off the failure node 1 shall receive the patterns and signal them accordingly: — *TP_N1_RxD* of node1 as stimulated at *TP_N2_TxD* at node 2. — In case RxEN is implemented *TP_N1_RxEN* of node 1 as stimulated at *TP_N2_TxEN* at node 2. — After switching off the failure node 2 shall receive the patterns and signal them accordingly: — *TP_N2_RxD* of node2 as stimulated at *TP_N1_TxD* at node 1. — In case RxEN is implemented *TP_N2_RxEN* of node 2 as stimulated at *TP_N1_TxEN* at node 1.

Table 602 defines the test instances for short-circuit bus wires to GND (without APM) test case defined in Table 601.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 602 — Test instances for short-circuit bus wires to GND (without APM)

Instance		**1**	**2**
Purpose	**Stress**	S/C BP to GND at AS	S/C BM to GND at AS
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	—	—
Preamble		—	—
Test execution		… Observe and acquire $iBP_{GNDShortMax}$ at $TP\_AS\_B2\_R_{iBP}$ of the AS (shall be at *TPAS1_B2_BP*). Short-circuit BP (failure FL11) of the AS to GND at *TPAS1_B2_BP*. … Switch off short-circuit BP (failure FL11) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds. …	… Observe and acquire $iBM_{GNDShortMax}$ at $TP\_AS\_B2\_R_{iBM}$ of the AS (shall be at *TPAS1_B2_BM*). Short-circuit BM (failure FL12) of the AS to GND at *TPAS1_B2_BM.* … Switch off short-circuit BM (failure FL12) of the AS at *TPAS1_B2_BM*. Wait at least 12 seconds. …
Pass criteria		—	—

12.3.11.7 Short-circuit bus wires to V_{ANY} (without APM)

Table 603 defines the test case for short-circuit bus wires to V_{ANY} (without APM).

Table 603 — Test case for short-circuit bus wires to V_{ANY} (without APM)

Name	Short-circuit bus wires to V_{ANY} (without APM)
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit of the bus wire to +48 V [a] . Additionally it is checked that the IUT is not permanently damaged by the short-circuit.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to +48 V [a] according to Figure 19 and Table 26, failure FL13. — Communication: Node 1 and 2 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire uSCSN at TP_AS_SCSN of the active star. b) Observe and acquire uTxD at TP_Nx_TxD of node 1 and 2. c) Observe and acquire uTxEN at TP_Nx_TxEN of node 1 and 2. d) Observe and acquire uRxD at TP_Nx_RxD of node 1 and 2. e) In case of an available RxEN signal observe and acquire uRxEN at TP_Nx_RxEN of node 1 and 2. f) Observe and acquire iBPBAT48ShortMaxb or iBPBAT27ShortMaxc at TP_AS_B2_RiBP of the AS (shall be at TPAS1_B1). g) Stimulate the bus driver of the transmitting node 2 at TP_N2_TxD and TP_N2_TxEN by a current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples were taken by the data acquisition unit. h) At least 500 ns after the start of transmission short-circuit BP (failure FL13) of the AS to +48 V a at TPAS1_B2_BP.

Name	Short-circuit bus wires to V_{ANY} (without APM)
	i) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at node 2. Acquire at least 500 samples, while the IUT transmits Data_0, Idle and Data_1. j) Switch off short-circuit BP (failure FL13) of the AS at TPAS1_B2_BP. Wait at least 12 seconds. k) Stimulate node 1 at TP_N1_TxD and TP_N1_TxEN by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. l) Stimulate node 2 at TP_N2_TxD and TP_N2_TxEN by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— In case the IUT does not support 42 V systems: $\|iBP_{BAT27ShortMax}\| \leq 60$ mA. — In case the IUT does support 42 V systems: $\|iBP_{BAT48ShortMax}\| \leq 72$ mA. — After switching off the failure node 1 shall receive the patterns and signal them accordingly: — *TP_N1_RxD* of node1 as stimulated at *TP_N2_TxD* at node 2. — In case RxEN is implemented *TP_N1_RxEN* of node 1 as stimulated at *TP_N2_TxEN* at node 2. — After switching off the failure node 2 shall receive the patterns and signal them accordingly: — *TP_N2_RxD* of node2 as stimulated at *TP_N1_TxD* at node 1. — In case RxEN is implemented *TP_N2_RxEN* of node 2 as stimulated at *TP_N1_TxEN* at node 1.

a In case the IUT does not support 42 V systems the V_{BAT} shall be +27 V

b In case the IUT does support 42 V systems

c In case the IUT does not support 42 V systems

Table 604 defines the test instances for short-circuit bus wires to V_{ANY} (without APM) test case defined in Table 603.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 604 — Test instances for short-circuit bus wires to V_{ANY} (without APM)

Instance		1	2
Purpose	**Stress**	S/C BP to +48 V at AS	S/C BM to +48 V at AS
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to +48 V [a]	S/C BM to +48 V [a]
Preamble		—	—
Test execution		… Observe and acquire *$iBP_{BAT48ShortMax}$* [b] or *$iBP_{BAT27ShortMax}$* [c] at *$TP\_AS\_B2\_R_{iBP}$* of the AS (shall be at *TPAS1_B1*). Short-circuit BP (failure FL13) of the AS to +48 V [a] at *TPAS1_B2_BP*. … Switch off short-circuit BP (failure FL13) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds. …	… Observe and acquire *$iBM_{BAT48ShortMax}$* [b] or *$iBM_{BAT27ShortMax}$* [c] at *$TP\_AS\_B2\_R_{iBM}$* of the AS (shall be at *TPAS1_B1*). Short-circuit BM (failure FL14) of the AS to +48 V [a] at *TPAS1_B2_BM.* … Switch off short-circuit BM (failure FL14) of the AS at *TPAS1_B2_BM*. Wait at least 12 seconds. …
Pass criteria		—	—

[a] In case the IUT does not support 42 V systems the V_{BAT} shall be +27 V

[b] In case the IUT does support 42 V systems

[c] In case the IUT does not support 42 V systems

12.3.11.8 Short-circuit bus wires to -5 V (without APM)

Table 605 defines the test case for short-circuit bus wires to -5 V (without APM).

Table 605 — Test case for short-circuit bus wires to -5 V (without APM)

Name	**Short-circuit bus wires to -5 V (without APM)**
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit of the bus wire to -5 V. Additionally it is checked that the IUT is not permanently damaged by the short-circuit.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure S/C BP to -5 V according to Figure 19 and Table 26, failure FL19. — Communication: Node 1 and 2 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uSCSN* at *TP_AS_SCSN* of the active star. b) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 1 and 2. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 1 and 2. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 1 and 2. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 1 and 2. f) Observe and acquire $iBP_{-5VshortMax}$ at *TP_AS_B2_*R_{iBP} of the AS (shall be at *TPAS1_B1*). g) Stimulate the bus driver of the transmitting node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by a current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples were taken by the data acquisition unit. h) At least 500 ns after the start of transmission short-circuit BP (failure FL19) of the AS to -5 V at *TPAS1_B2_BP*.

Name	Short-circuit bus wires to -5 V (without APM)
	i) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at node 2. Acquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*. j) Switch off short-circuit BP (failure FL19) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds. k) Stimulate node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. l) Stimulate node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— $\|iBP_{-5VshortMax}\| \leq 60$ mA. — After switching off the failure node 1 shall receive the patterns and signal them accordingly: — *TP_N1_RxD* of node1 as stimulated at *TP_N2_TxD* at node 2. — In case RxEN is implemented *TP_N1_RxEN* of node 1 as stimulated at *TP_N2_TxEN* at node 2. — After switching off the failure node 2 shall receive the patterns and signal them accordingly: — *TP_N2_RxD* of node2 as stimulated at *TP_N1_TxD* at node 1. — In case RxEN is implemented *TP_N2_RxEN* of node 2 as stimulated at *TP_N1_TxEN* at node 1.

Table 606 defines the test instances for short-circuit bus wires to -5 V (without APM) test case defined in Table 605.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 606 — Test instances for short-circuit bus wires to -5 V (without APM)

Instance		**1**	**2**
Purpose	**Stress**	S/C BP to -5 V at AS	S/C BM to -5 V at AS
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	—
	Failure	S/C BP to -5 V	S/C BM to -5 V
Preamble		—	—
Test execution		… Observe and acquire $iBP_{-5VshortMax}$ at $TP\_AS\_B2\_R_{iBP}$ of the AS (shall be at *TPAS1_B1*). Short-circuit BP (failure FL19) of the AS to -5 V at *TPAS1_B2_BP*. … Switch off short-circuit BP (failure FL19) of the AS at *TPAS1_B2_BP*. Wait at least 12 seconds. …	… Observe and acquire $iBM_{-5VshortMax}$ at $TP\_AS\_B2\_R_{iBM}$ of the AS (shall be at *TPAS1_B1*). Short-circuit BM (failure FL20) of the AS to -5 V at *TPAS1_B2_BM.* … Switch off short-circuit BM (failure FL20) of the AS at *TPAS1_B2_BM*. Wait at least 12 seconds. …
Pass criteria		—	—

12.3.11.9 S/C BP to BM at AS (without APM)

Table 607 defines the test case for S/C BP to BM at AS (without APM).

Table 607 — Test case for S/C BP to BM at AS (without APM)

Name	S/C BP to BM at AS (without APM)
Test purpose	This test checks the ability of the IUT to limit the absolute current in case of a short-circuit between both bus wires. Additionally it is checked that the IUT is not permanently damaged by the short-circuit and that the active star to signal the occurrence of an error in this case while the autonomous power moding flag (APM flag) is enabled.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: S/C BP to BM. — Communication: Node 1 and 2 as transmitter.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uSCSN* at *TP_AS_SCSN* of the active star. b) Observe and acquire *uTxD* at *TP_Nx_TxD* of node 1 and 2. c) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of node 1 and 2. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of node 1 and 2. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of node 1 and 2. f) Observe and acquire $iBM_{BPShortMax}$ at *TP_AS_B2_*R_{iBM} of the AS (shall be at *TPAS1_B1*). g) Stimulate the bus driver of the transmitting node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by a current measurement pattern according to 9.1.3.8. Repeat this sequence until at least 500 samples were taken by the data acquisition unit. h) At least 500 ns after the start of transmission short-circuit BP to BM (failure FL21) of the AS at *TPAS2_B1* 9.1.4.3. i) Trigger the data acquisition unit to start the measurement 100 µs after the stimuli at

Name	S/C BP to BM at AS (without APM)
	node 2. Aquire at least 500 samples, while the IUT transmits *Data_0*, *Idle* and *Data_1*. j) Switch off short-circuit BP to BM (failure FL21) of the AS at *TPAS1_B1*. Wait at least 12 seconds. k) Stimulate node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one TSS pattern, followed by one 50/50 pattern. Wait 500 µs. l) Stimulate node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	— $\|iBM_{BPShortMax}\| \leq 60$ mA. — After switching off the failure node 1 shall receive the patterns and signal them at *TP_N1_RxD* and *TP_N1_RxEN* that are stimulated at *TP_N2_TxD* and *TP_N2_TxEN* of node 2. — After switching off the failure node 2 shall receive the patterns and signal them at *TP_N2_RxD* and *TP_N2_RxEN* that are stimulated at *TP_N1_TxD* and *TP_N1_TxEN* of node 1.

12.3.11.10 Short-circuit between TxEN to GND (with APM)

Table 608 defines the test case for short-circuit between TxEN to GND (with APM).

Table 608 — Test case for short-circuit between TxEN to GND (with APM)

Name	Short-circuit between TxEN to GND (with APM)
Test purpose	This test checks the ability of the active star to signal the occurrence of an error in case of TxEN is shortened to GND according to ISO 17458-4 while the autonomous power moding flag (APM flag) is enabled. This case is skipped if the Functional class “Active star – communication controller interface” is not implemented.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: short-circuit TxEN to GND. — Communication: active star as transmitter.
Preamble (setup state)	— Standard preamble. — Set the APM flag via host command. — Wait 100 µs.
Test execution	a) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. b) Observe and acquire *uTxD* at *TP_AS_TxD* of the active star. c) Observe and acquire *uTxEN* at *TP_AS_TxEN* of the active star. d) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. e) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. f) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. g) Short-circuit TxEN and GND of the IUT (AS) according to 7.6, failure FL4.

Name	Short-circuit between TxEN to GND (with APM)
	h) Beginning with the falling edge of *uTxEN* of the active star, stimulate the IUT (AS) at *TP_AS_TxD* by a logical LOW state sequence of at least 2 600 µs.
Postamble	Standard postamble.
Pass criteria	For *dBranchRxActiveMax* timeout measurement, a trigger event on the falling edge of *uTxEN* is required. — *uRxD* of all nodes shall and the active star be in logical HIGH state before the falling edge of *uTxEN* of the active star. After the falling edge of *uTxEN* of the active star, *uRxD* of all nodes and the active star shall change to logical LOW state and shall remain in logical LOW state for at least 650 µs and not more than 2 600 µs. After this logical LOW state phase, *uRxD* of all nodes and the active star shall return to and remain in logical HIGH state. — In case of an available INH1 signal *uINH1* of the active star shall be in logical HIGH state during the test execution. — *uINTN* at *TP_AS_INTN* of the active star shall be in logical HIGH state initially. Latest 2 600 µs + 200 µs after the falling edge of *uTxEN* at *TP_AS_TxEN* of the active star, *uINTN* at *TP_AS_INTN* of the active star shall switch to logical LOW state.

12.3.11.11 Undervoltage V_{BAT}

Table 609 defines the test case for undervoltage V_{BAT}.

Table 609 — Test case for undervoltage V_{BAT}

Name	**Undervoltage V_{BAT}**
Test purpose	This test checks the ability of the active star to signal the occurrence of an error in case of an undervoltage at V_{BAT} while the autonomous power moding flag (APM flag) is disabled. This test case is skipped if neither the Functional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{BAT} and V_{CC} are both implemented: — external V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: external V_{BAT} power supply of active star: default. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_N2_TxD* of node 2. b) Observe and acquire *uTxEN* at *TP_N2_TxEN* of node 2. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) In case of an available RxD signal observe and acquire *uRxD* at *TP_AS_RxD* of the active star. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. g) Set V_{BAT} power supply of active star to $V_{BATUndervoltage}$. h) After 1 000 ms stimulate the bus driver of node 2 at *TP_N2_TxD* and *TP_N2_TxEN* by one TSS pattern, followed by one 50/50 pattern.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. — *uINTN* at *TP_AS_INTN* of the active star shall be in logical LOW state latest 200 µs after the

Name	Undervoltage V_{BAT}
	beginning of the observation window. — In case that V_{CC} is implemented: *uRxD* of all observed nodes and the active star shall contain the 50/50 sequence transmitted by node 2, i.e. the active star shall stay in *AS_Normal* mode and shall retransmit all patterns received on branch 3. — In case that V_{CC} is not implemented and V_{IO} is implemented: *uRxD* of the active star and all observed nodes except node 2 shall not contain the 50/50 sequence transmitted by node 2, i.e. the active star shall change to *AS_Standby* mode and shall not retransmit any patterns received on branch 3. — In case that V_{CC} and V_{IO} are not implemented: — *uRxD* of all observed nodes except node 2 shall not contain the 50/50 sequence transmitted by node 2, i.e. the active star shall change to *AS_Standby* mode and shall not retransmit any patterns received on branch 3. — *uRxD* of the active star shall be in logical LOW state during observation window.

Table 610 defines the test instances for undervoltage V_{BAT} test case defined in Table 609.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 610 — Test instances for undervoltage V_{BAT}

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

12.3.11.12 Error recovery after undervoltage V_{BAT}

Table 611 defines the test case for error recovery after undervoltage V_{BAT}.

Table 611 — Test case for error recovery after undervoltage V_{BAT}

Name	Error recovery after undervoltage V_{BAT}
Test purpose	This test checks the ability of the active star to signal the recovery of an error in case of an undervoltage at V_{BAT} while the autonomous power moding flag (APM flag) is disabled. Additionally it is tested that the INTN may not be reset due any host command. This test case is skipped if — neither the Functional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented — the Functional class “Active star – logic level adaptation” is not implemented.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{BAT} and V_{CC} are both implemented: — external V_{BAT} power supply of active star: default. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: external V_{BAT} power supply of active star: default. — V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: single node.
Preamble (setup state)	— Standard preamble. — Set V_{BAT} power supply of active star to $V_{BATUndervoltage}$. — After 1 000 ms + 200 µs reset the SPI interrupt line of the active star via *uSCSN* at *TP_AS_SCSN* of the active star.
Test execution	a) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. b) Set V_{BAT} power supply of active star to default. c) Wait at least 10 ms + 200 µs for the active star to recover the undervoltage. Additionally, a possible product specific delay shall be considered. If such a delay is implemented a way to calculate this delay shall be provided by the device’s datasheet at least. d) Stimulate the active star at the host interface to enter *AS_Normal*. e) Wait at least 200 µs because *uINTN* may change the logical state during this time. f) Trigger the logic analyzer to start the observation synchronously with the stimulation at

Name	Error recovery after undervoltage V_{BAT}
	the host interface of the active star.
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. *uINTN* at *TP_AS_INTN* of the active star shall be in logical LOW state during the observation window.

Table 612 defines the test instances for error recovery after undervoltage V_{BAT} test case defined in Table 611.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 612 — Test instances for error recovery after undervoltage V_{BAT}

Instance		1	2
Purpose	**Stress**	none	ground shift
	Precondition	—	—
Configuration	**Power supply**	—	—
	Ground shift	—	+5,0 V at AS
	Failure	—	—
Preamble		—	—
Test execution		—	—
Pass criteria		—	—

12.3.12 Dynamic Low Supply

12.3.12.1 Mode change back to *AS_Normal* (host interface) after dynamic low supply voltage

Table 613 defines the test case for mode change back to AS_Normal (host interface) after dynamic low supply voltage.

Table 613 — Test case for mode change back to AS_Normal (host interface) after dynamic low supply

Name	**Mode change back to AS_Normal (host interface) after dynamic low supply voltage**
Test purpose	This test checks the behaviour of the IUT after a dynamic low supply voltage pulse according to 7.5 occurring in *AS_Normal* mode.
Configuration	— Topology: as specified in previous configuration see 9.1. — In case that only V_{CC} is implemented: V_{CC} power supply of active star: +5,0 V. — In case that V_{BAT} and V_{CC} are both implemented: — V_{BAT} power supply of active star: 11,6 V. — V_{CC} power supply of active star: +5,0 V. — In case that only V_{BAT} is implemented: V_{BAT} power supply of active star: 11,6 V. — In case that V_{IO} is implemented: V_{IO} reference voltage of active star: depends on implementation. — Ground shift: 0 V. — Failure: none. — Communication: matrix A (round robin test). — Test signal: Case 1.1 as specified in 7.5.
Preamble (setup state)	Standard preamble.
Test execution	a) Observe and acquire *uTxD* at *TP_Nx_TxD* of all nodes. b) Observe and acquire *uTxEN* at *TP_Nx_TxEN* of all nodes. c) Observe and acquire *uRxD* at *TP_Nx_RxD* of all nodes. d) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. e) In case of an available RxEN signal observe and acquire *uRxEN* at *TP_Nx_RxEN* of all nodes. f) In case of an available INH1 signal observe and acquire *uINH1* at *TP_AS_INH1* of the active star. g) Start the dynamic low supply voltage pulse at the power supply of the active star. h) Wait until the power supply voltage(s) rise(s) above the specific undervoltage thresholds.

Name	Mode change back to AS_Normal (host interface) after dynamic low supply voltage
	i) Stimulate the bus driver of node 1 at *TP_N1_TxD* and *TP_N1_TxEN* by one wakeup pattern as described in 9.1.3.1. j) Stimulate the bus drivers of the transmitting nodes according to the sequence described on matrix A at *TP_Nx_TxD* and *TP_Nx_TxEN* by one TSS pattern, followed by one 50/50 pattern. Repeat this sequence. At least one more sequence shall be transmitted after the end of the dynamic low supply voltage pulse. k) Trigger the logic analyzer to start synchronously with the first falling edge of *uTxEN* of node 1.
Postamble	Standard postamble.
Pass criteria	The observation window shall start with the first falling edge of *uTxEN* of node 1. Adaptation of the thresholds for digital signals may be required. — *uRxD* of all nodes shall contain all 50/50 patterns transmitted by all nodes (according to *uTxD* and *uTxEN* of all nodes) at least after the first communication round, i.e. all data shall be retransmitted by the active star after the wakeup has been detected. — In case of an available INH1 signal *uINH1* at *TP_AS_INH1* of the active star shall be in logical HIGH state latest 104 µs after the beginning of the first wakeup pattern until the end of the test execution. — *uINTN* at *TP_AS_INTN* of the active star shall be in logical LOW state during the observation window.

Table 614 defines the test instances for mode change back to AS_Normal (host interface) after dynamic low supply voltage test case defined in Table 613.

The test case shall be executed for each test instance, whereas each test instance defines variations of the corresponding test configuration under different stress conditions. The variations with respect to the test case table are disclosed in the test instances table.

Table 614 — Test instances for mode change back to *AS_Normal* (host interface) after dynamic low supply voltage

Instance		1	2	3	4
Purpose	**Stress**	—	—	—	—
	Precondition	—	—	—	—
Configuration	**Power supply**	Test signal: Case 1.1 as specified in 7.5	Test signal: Case 1.2 as specified in 7.5	Test signal: Case 2.1 as specified in 7.5	Test signal: Case 2.2 as specified in 7.5
	Ground shift	—	—	—	—
	Failure	—	—	—	—
Preamble		—	—	—	—
Test execution		—	—	—	—
Pass criteria		—	—	—	—

12.3.13 Power supply Undervoltage V_{BAT}

12.3.13.1 Reset SPI interrupt line after undervoltage of V_{BAT}

Table 615 defines the test case for reset SPI interrupt line after undervoltage of V_{BAT}.Table 615 — Test case for reset SPI interrupt line after undervoltage of V_{BAT}

Name	**Reset SPI interrupt line after undervoltage of V_{BAT}**
Test purpose	This test checks the behaviour of the IUT when the SPI interrupt line is been reset due to host command according to ISO 17458-4 while no stress condition is present. This test case is skipped if — neither the Funtional class “Active star – voltage regulator control” nor the Functional class “Active star – internal voltage regulator” is implemented.
Configuration	— Topology: as specified in previous configuration see 12.1. — In case that V_{BAT} and V_{CC} are both implemented: — External V_{BAT} power supply of the active star: default. — V_{CC} power supply of the active star: +5,0 V. — In case that only V_{BAT} is implemented: — V_{BAT} power supply of the active star: default. — In case that V_{IO} is implemented: — V_{IO} reference voltage of the active star: depends on implementation — Ground shift: 0 V. — Failure: none. — Communication: none.
Preamble (setup state)	— Standby preamble. — Set the external V_{BAT} power supply of the active star to $V_{BATUndervoltage}$. — Wait 1 000 ms.
Test execution	a) Observe and acquire *uINTN* at *TP_AS_INTN* of the active star. b) Observe and acquire *uSCSN* at *TP_AS_SCSN* of the active star. c) After at least 10 ms reset the SPI interrupt line of the active star via *uSCSN* at *TP_AS_SCSN* of the active star (i.e. valid reset access). d) Trigger the logic analyzer to start the observation synchronously with the stimuli at the host interface of the active star, i.e. with the first falling edge of *uSCSN* signal at *TP_AS_SCSN* of the active star. e) After at least 200µs set the external VBAT power supply of the active star to the default implementation value.

Name	Reset SPI interrupt line after undervoltage of V_{BAT}
Postamble	Standard postamble.
Pass criteria	Adaptation of the thresholds for digital signals may be required. *uINTN* at *TP_AS_INTN* of the active star shall be in logical LOW state initially. Latest 100 us after *uSCSN* at *TP_AS_SCSN* (after valid reset access) of the active star returns to high *uINTN* at *TP_AS_INTN* of the active star shall change to logical HIGH state. Latest 10,2ms after Vbat recovery uINTN at TP_AS_INTN of the active star shall change to logical LOW state.

Annex A
(normative)

FlexRay parameters

Table A.1 defines the FlexRay parameters.

Table A.1 — FlexRay parameters

FlexRay Parameter	Description	Min	Max	Unit
gdBit	Nominal duration of one bit time	100 [a]	—	ns
gdTSSTransmitter	Overall truncation with one AS See also ISO 17458-4 and ISO 17458-2.	100	1 600 [b]	ns
gdWakeupTxActive	Length of the low part of the wakeup symbol	—	60	gdBit
gdWakeupTxIdle	Length of the idle part of the wakeup symbol	—	180	gdBit
$dPropagationDelay_{M,N}$	Propagation delay from TP1_BD of node module M to TP4_BD of node module N	—	2 450	ns
$dFrameTSSLengthChange_{M,N}$	Length change on path from node module M to node module N	-1 300	50	ns
R_{DCLoad}	DC bus load	40	55	Ω
uData1	Receiver threshold for detecting *Data_1*	150	300	mV
uData0	Receiver threshold for detecting *Data_0*	-300	-150	mV
uData1 - |uData0|	Mismatch of receiver thresholds	-30	+30	mV
dBDIdleDetection	Idle detection time	50	200	ns
dBDActivityDetection	Activity detection time	100	250	ns
dBDRxai	Idle reaction time	50	275	ns
dBDRxia	Activity reaction time	100	325	ns
uRx	*uBus* at TP4	425	435	mV
dBusRxia	Transition time *Idle* → *Data_0*	18	22	ns
dBusRxai	Transition time *Data_0* → *Idle*	18	22	ns
dBDRx10	Receiver delay, negative edge	—	75	ns
dBDRx01	Receiver delay, positive edge	—	75	ns
dBDRxAsym	Receiver delay mismatch	—	5	ns
$uBDTx_{active}$	Absolute differential voltage, while sending [c]	600	2000	mV

Table A.1 — *(continued)*

FlexRay Parameter	Description	Min	Max	Unit
$uBDTx_{idle}$	Absolute differential voltage, while idle	0	30	mV
$iBP_{GNDShortMax}$	Maximum output current when shorted to GND	—	60	mA
$iBM_{GNDShortMax}$	Maximum output current when shorted to GND	—	60	mA
$iBP_{BAT27ShortMax}$	Absolute maximum output current when shorted to 27 V	—	60	mA
$iBM_{BAT27ShortMax}$	Absolute maximum output current when shorted to 27 V	—	60	mA
$iBP_{BAT48ShortMax}$	Absolute maximum output current when shorted to 48 V	—	72	mA
$iBM_{BAT48ShortMax}$	Absolute maximum output current when shorted to 48 V	—	72	mA
$iBP_{BAT60ShortMax}$	Absolute maximum output current when shorted to 60 V	—	90	mA
$iBM_{BAT60ShortMax}$	Absolute maximum output current when shorted to 60 V	—	90	mA
$iBM_{BPShortMax}$	Absolute maximum output current when BM shorted to BP	—	60	mA
$iBP_{BMShortMax}$	Absolute maximum output current when BP shorted to BM	—	60	mA
$iBM_{-5VshortMax}$	Absolute maximum output current when shorted to -5 V	—	60	mA
$iBP_{-5VshortMax}$	Absolute maximum output current when shorted to -5 V	—	60	mA
dBDTx10	Transmitter delay, negative edge	—	75	ns
dBDTx01	Transmitter delay, positive edge	—	75	ns
dBDTxAsym	Transmitter delay mismatch [d]	—	4	ns
dBusTx10	Fall time differential bus voltage	6	18,75	ns
dBusTx01	Rise time differential bus voltage	6	18,75	ns
dBDTxia	Propagation delay idle to active	—	75	ns
dBDTxai	Propagation delay active to idle	—	75	ns
dBusTxia	Signal slope idle to active (BD and AS)	—	30	ns
dBusTxai	Signal slope active to idle (BD and AS)	—	30	ns
$dTxEN_{Low}$	Time span of bus activity	550	650	ns
$dWU_{0Detect}$	Time for detection of a *Data_0* phase in WU symbol	1	4	µs
$dWU_{IdleDetect}$	Time for detection of a *Idle* phase in WU symbol	1	4	µs
$dWU_{Timeout}$	Acceptance timeout for WU recognition	48	140	µs
dBDWakePulseFilter	Duration of the wake pulse filter time	1	500	µs

Table A.1 — *(continued)*

FlexRay Parameter	Description	Min	Max	Unit
$dBDUVV_{BAT}$	Undervoltage detection filter time for Bus Driver with undervoltage on V_{BAT}	—	1 000	ms
$dBDUVV_{CC}$	Undervoltage detection filter time for Bus Driver with undervoltage on V_{CC}	—	1 000	ms
dStarDelay10	Propagation delay trough an Active Star	0	150	ns
dStarDelay01	Propagation delay trough an Active Star	*0*	150	ns
dStarAsym	Asymmetric propagation delay for monolithic devices	0	8	ns
dStarAsym2	Asymmetric propagation delay for non-monolithic devices	0	10	ns
dStarGoToSleep	Go-to-Sleep timeout	640	6 400	ms
dStarWakeupReaction Time	Active Star wakeup reaction time (time to enter *AS_Normal* after wakeup)	—	70	µs
dBranchRxActiveMax	Noise detection time	650	2 600	µs
dStarSetUpDelay	Set up delay	—	500	ns
$uV_{DIG-IN-HIGH}$	Threshold for detecting a digital input as on logical high [e]	—	70	%
$uV_{DIG-IN-LOW}$	Threshold for detecting a digital input as on logical low [e]	30	—	%
$uV_{DIG-OUT-HIGH}$	Output voltage on a digital output, when in logical HIGH state [e]	80	100	%
$uV_{DIG-OUT-LOW}$	Output voltage on a digital output, when in logical LOW state [e]	—	20	%
R_{CM1}, R_{CM2}	Common mode input resistance	10	40	kΩ
uCM	Common mode voltage range that does not disturb the receive function	-10	+15	V
SPI speed	Characteristics of the optional SPI Bus Driver to host interface	0,01	1	Mbit/s
uBias – BD_Normal	Voltage at BP & BM during bus state *Idle*	1 800	3 200	mV
uBias – Low Power	Voltage at BP & BM during bus state *Idle_LP*	-200	+200	mV
uBias – Idle	Nominal voltage of *uBias* in *BD_Normal* or *AS_Normal* mode.	—	2 500	mV
$uV_{BAT-WAKE}$	Minimum battery voltage required for wakeup detector operation in case that V_{CC} is implemented	—	7	V
$uV_{BAT-WAKE}$	Minimum battery voltage required for wakeup detector operation in case that V_{CC} is not implemented	—	5,5	V
$uBDUV_{BAT}$	Undervoltage detection threshold for Bus Driver with undervoltage on V_{BAT}	4	5,5	V

Table A.1 — *(continued)*

FlexRay Parameter	Description	Min	Max	Unit
$dBDUVV_{IO}$	Undervoltage detection filter time for Bus Driver with undervoltage on V_{IO}	—	1 000	ms
$uBDUV_{CC}$	Undervoltage detection threshold for Bus Driver with undervoltage on V_{CC}	4	—	V
$uBDUV_{IO}$	Undervoltage detection threshold for Bus Driver with undervoltage on V_{IO}	2	—	V
iBP_{Leak}	Leakage current when all supplies are switched off	—	25	µA
iBM_{Leak}	Leakage current when all supplies are switched off	—	25	µA
$iBP_{LeakGND}$	Absolute leakage current in case of loss of GND	—	1 600	µA
$iBM_{LeakGND}$	Absolute leakage current in case of loss of GND	—	1 600	µA
T_{AMB_Class0}	Ambient temperature for class 0	-40	+150	°C
T_{AMB_Class1}	Ambient temperature for class 1	-40	+125	°C
T_{AMB_Class2}	Ambient temperature for class 2	-40	+105	°C
T_{AMB_Class3}	Ambient temperature for class 3	-40	+85	°C
dBDTxDM	Idle-active transmitter delay mismatch |*dBDTxia* - *dBDTxai*|	-50	50	ns
$dSymbolLength Change_{M,N}$	Change of length of a symbol on path from node module M to node module N	-925	1 125	ns
dStarTxia	Propagation delay idle → active	—	550	ns
dStarTxai	Propagation delay active → idle	—	550	ns
$dBusRx0_{BD}$	Transition span *Data_0* for Bus Driver	70	4 330	ns
$dBusRx1_{BD}$	Transition span *Data_1* for Bus Driver	70	4 330	ns
$dBusRx0_{Star}$	Transition span *Data_0* for Active Star	80	4 320	ns
$dBusRx1_{Star}$	Transition span *Data_1* for Active Star	80	4 320	ns
dBusRxia	Transition time *Idle → Data_0*	18	22	ns
dBusRxai	Transition time *Data_0 → Idle*	18	22	ns
dBusActive	Minimum time *Data_0*	590	610	ns
dBusIdle	Minimum time *Idle*	590	610	ns
dBDModeChange	Mode transition time after (hard-wired) host command	—	100	µs
$dBDModeChange_{SPI}$	Mode transition time after (SPI) host command	—	100	µs
$dBDReactionTime_{SPI}$	Time from detection of an event to falling edge of INTN	—	200	µs
$dStarModeChange_{SPI}$	Mode transition time after (SPI) host command	—	100	µs
$dStarReactionTime_{SPI}$	Time from detection of an event to falling edge of INTN	—	200	µs

Table A.1 — *(continued)*

FlexRay Parameter	Description	Min	Max	Unit
$dBDWakeupReaction_{local}$	Bus Driver reaction time on a local wakeup event	—	100	µs
dStarTxAsym	Transmitter delay mismatch	—	10	ns
dStarRxAsym	Receiver delay mismatch	—	10	ns
dStarRx10	Receiver delay, negative edge	—	225	ns
dStarRx01	Receiver delay, positive edge	—	225	ns
dStarTx10	Transmitter delay, negative edge	—	225	ns
dStarTx01	Transmitter delay, positive edge	—	225	ns
dBDTxActiveMax	Maximum length of transmitter activation	650	2 600	µs
Z_0	Differential mode impedance at 10 MHz	80	110	Ω
T'_0	Specific line delay	3,4	10	ns/m
$R_{DCContact}$	Contact resistance (including crimps)	—	50	mΩ
$Z_{Connector}$	Impedance of connector	70	200	Ω
$l_{Couling}$	Length coupling connection	—	150	mm
$d_{ContactInterruption}$	Contact resistance RDCContact > 1 Ω	—	100	ns
R_{CMC}	Resistance (per line)	—	2	Ω
dBDTxRxai	Idle-Loopdelay	—	325	ns
$dBDRxD_{R15}$ + $dBDRxD_{F15}$	Sum of rise and fall time at 15 pF load [f]	—	13	ns
C_BDTxD	Input capacitance on TxD pin	—	10	pF
uBDLogic_1	Threshold for detecting logical high [e]	—	60	%
uBDLogic_0	Threshold for detecting logical low [e]	40	—	%
uStarLogic_1	Threshold for detecting logical high [e]	—	60	%
uStarLogic_0	Threshold for detecting logical low [e]	40	—	%
$uINH1_{Not\_Sleep}$	Voltage on inhibit pin, when signaling *Not_Sleep* at 200 µA load	uV_{BAT} – 1 V	—	V
$iINH1_{Leak}$	Absolute leakage current while signaling *Sleep*	—	10	µA
uData0_LP	Low power receiver threshold for detecting *Data_0*	-400	-100	mV
$dWU_{Interrupt}$	Acceptance timeout for interruptions	0,13 [g]	1	µs
$dBDWakeupReacton_{remote}$	Bus Driver reaction time on a remote wakeup event	—	100	µs
slV_{BAT}	Absolute slope of V_{BAT} voltage	0,02	1,52	V/ms
dVoltageRampSkew	Time skew in reaching end of dynamic low supply voltage slope	0	65	ms
dStarTSSLength Change	Frame TSS length change caused by Active Star (= $dTSS_B$ – $dTSS_A$)	-450	0	ns

Table A.1 — *(continued)*

FlexRay Parameter	Description	Min	Max	Unit
dStarFES1Length Change	Prolongation of last bit of a frame (=$dFES1_B$ – $dFES1_A$)	0	450	ns
dStarSymbolLength Change	Symbol length change (only static portion) = $dSymbol_B$ - $dSymbol_A$	-300	450	ns
$uStarTx_{active}$	Absolute value of uBus, while sending [c]	600	2 000	mV
$uStarTx_{idle}$	Absolute value of uBus, while Idle	0	30	mV
dStarRxai	Active Star idle reaction time	50	550	ns
dStarRxia	Active Star activity reaction time	100	550	ns
dStarTxRxai	Idle-Loopdelay	—	325	ns
$dStarUVV_{Supply}$	Supply undervoltage reaction time	—	1	ms
$dStarRV_{Supply}$	Supply undervoltage recovery time	—	10	ms
$uStarUVV_{Supply}$	Supply undervoltage detection threshold	4	—	V
$uV_{DIG-OUT-UV}$	Output voltage on a digital output at 100 kΩ load to GND, when VDIG in undervoltage	—	500	mV
$uV_{DIG-OUT-OFF}$	Output voltage on a digital output at 100 kΩ load, when unsupplied	product specific	product specific	—
$dBDERRN_{Stable}$	Error signaling time on ERRN pin	1	10	µs
$dReactionTime_{ERRN}$	Reaction time on ERRN pin	—	100	µs
$uStarUVV_{BAT}$	Transition to low power when voltage falls below product specific threshold	4	5,5	V
$uStarUVV_{CC}$	Transition to low power when voltage falls below product specific threshold	4	—	V
$uStarUVV_{IO}$	Transition to low power when voltage falls below product specific threshold	2	—	V
$dStarUVV_{CC}$	Undervoltage detection filter time for Active Star with undervoltage on V_{CC}	—	1 000	ms
$dStarUVV_{BAT}$	Undervoltage detection filter time for Active Star with undervoltage on V_{BAT}	—	1 000	ms
$dStarUVV_{IO}$	Undervoltage detection filter time for Active Star with undervoltage on V_{IO}	—	1 000	ms
$dBDRV_{CC}$	V_{CC} Undervoltage recovery time for Bus Drivers	—	10	ms
$dBDRV_{BAT}$	V_{BAT} Undervoltage recovery time for Bus Drivers	—	10	ms
$dBDRV_{IO}$	V_{IO} Undervoltage recovery time for Bus Drivers	—	10	ms
$dStarRV_{BAT}$	V_{BAT} Undervoltage recovery time for Active Star	—	10	ms
$dStarRV_{CC}$	V_{CC} Undervoltage recovery time for Active Star	—	10	ms
$dStarRV_{IO}$	V_{IO} Undervoltage recovery time for Active Star	—	10	ms

Table A.1 — *(continued)*

FlexRay Parameter	Description	Min	Max	Unit
dStarTSSLength Change_TxD_Bus	TSS length change from TxD pin to signal on all branches	-450	0	ns
dStarFES1Length Change_TxD_Bus	FES1 length change from TxD pin to signal on all branches	0	450	ns
dStarSymbolLength Change_TxD_Bus	Symbol length change from TxD pin to signal on all branches	-300	400	ns
dStarTSSLength Change_Bus_RxD	TSS length change from branch to RxD pin	-450	0	ns
dStarFES1Length Change_Bus_RxD	FES1 length change from branch to RxD pin	0	450	ns
dStarSymbolLength Change_Bus_RxD	Symbol length change from branch to RxD pin	-300	400	ns
$dStarRxD_{R15}$ + $dStarRxD_{F15}$	Sum of rise and fall time at 15 pF load [f]	—	13	ns
| $dStarRxD_{R15}$ – $dStarRxD_{F15}$ |	Difference of rise and fall time at 15 pF load	—	5	ns
$dCCRxAsymAccept_{15}$	Acceptance of asymmetry at receiving CC with 15 pF load	-31,5	+44,0	ns
$dCCRxAsymAccept_{25}$	Acceptance of asymmetry at receiving CC with 25 pF load	-30,5	+43,0	ns
C_StarTxD	Input capacitance on TxD pin	—	10	pF
$uESD_{EXT}$	ESD protection on pins that lead to ECU terminals	6	—	kV
$uESD_{INT}$	ESD on all other pins	2	—	kV
$uESD_{IEC}$	ESD protection on BP and BM	6	—	kV
| $dBDRxD_{R15}$ – $dBDRxD_{F15}$ |	Difference of rise and fall time at 15 pF load	—	5	ns
$R_{BDTransmitter}$	Bus Driver - Bus interface simulation resistor	product specific	product specific	—
dFrameTSSLength Change1$AS_{M,N}$	Frame TSS length change on a path with one Active Star from node module M to node module N	-850	50	ns
$dStarPower_{ONOFF}$	Reaction time of the Active Star on power-on/power-off event	—	100	µs
RxD signal sum of rise and fall time at TP4_CC	between 20 % and 80 % VDIG at 10 pF load at the end of a 50 Ω, 1 ns microstripline	—	16,5	ns
dStarWakeup $Reaction_{local}$	Active Star reaction time on a local wakeup event	—	100	µs
dStarWakePulseFilter	Duration of the wake pulse filter time	1	500	µs
dStarActivityDetection	Activity detection time for Active Star	100	250	ns
dStarIdleDetection	Idle detection time for Active Star	50	200	ns
$dBDRxD_{R25}$ + $dBDRxD_{F25}$	Sum of rise and fall time at 25 pF load [f]	—	16,5	ns

Table A.1 — *(continued)*

FlexRay Parameter	Description	Min	Max	Unit
$\lvert dBDRxD_{R25} - dBDRxD_{F25} \rvert$	Difference of rise and fall time at 25 pF load	—	5	ns
dStarTxActiveMax	Maximum length of transmitter activation	650	2 600	µs
dBusTxDif	Difference between differential rise and all time | dBusTx10 - dBusTx01 |	—	3	ns
$R_{StarTransmitter}$	Active Star - Bus interface simulation resistor	product specific	product specific	—
$dStarTx_{reaction}$	TxD reaction time after TxEN HIGH	—	75	ns
dStarSymbolEndLengthChange	Prolongation of symbol at symbol end	0	450	ns
RxD signal difference of rise and fall time at TP4_CC	between 20 % and 80 % VDIG at 10 pF load at the end of a 50 Ω, 1 ns microstripline	—	5	ns
dFrameTSSLength Change0$AS_{M,N}$	Frame TSS length change on a path with without active stars from node module M to node module N	-400	50	ns

[a] Currently there is only one data rate specified: 10 Mbit/s

[b] In the conformance test, the maximum truncation is limited because there is only one Active Star in the topology.

[c] In case the functional class “Bus Driver increased voltage amplitude transmitter” or the functional class “Active Star increased voltage amplitude transmitter” is implemented, the minimum of *uBDTxActive* or *uStarTxAcive* shall be shifted to 900 mV.

[d] For all TxD signals with a sum of rise and fall time (20 % - 80 % V_{DIG}) of up to 9 ns.

[e] Relative to V_{DIG}

[f] 20 % – 80 % V_{DIG}. A datasheet for the BD/CC/AS shall state maximum rise and fall time on RxD/TxD separately.

[g] The minimum value is only guaranteed, when the phase that is interrupted was continuously present for at least 870 ns.

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