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FOREWORD

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Draft International Standards adopted by the Technical Committees are circulated to the Member Bodies for approval before their acceptance as International Standards by the ISO Council.

International Standard ISO 3563 was drawn up by Technical Committee ISO/TC 97, *Computers and Information processing*, and was circulated to the Member Bodies in March 1975.

It has been approved by the Member Bodies of the following countries :

Belgium	Mexico	Switzerland
Czechoslovakia	New Zealand	United Kingdom
France	Netherlands	U.S.S.R.
Germany	Poland	Yugoslavia
Hungary	Romania	
Italy	South Africa, Rep. of	

The Member Body of the following country expressed disapproval of the document on technical grounds :

Japan

Printed in Switzerland

Information processing — Interchangeable magnetic single-disk cartridge (top loaded) — Track format

1 SCOPE AND FIELD OF APPLICATION

This International Standard specifies the track format characteristics for the single-disk cartridge (top loaded) to be used for data interchange (see ISO 3562). The 7-bit coded character set specified in ISO 646 has been adopted, though, by agreement between the interchange parties, the 7-bit or 8-bit code extensions specified in ISO 2022 may be used.

However, it should be noted that in this International Standard plain binary numbers in 8-bit bytes are used in the control field to define the control information.

2 GENERAL REQUIREMENTS

2.1 Rotation speed and clock period

The total tolerance on rotation speed and clock period shall not exceed ± 3 % (see annex A).

2.2 Mode of recording

The mode of recording shall be double frequency where the start of every bit cell is a clock transition. A ONE is represented by a transition between two clock transitions.

At the nominal rotation speed of 2 400 rev/min the all-ZERO pattern consists of $2{,}50 \times 10^6$ transitions per second nominally, and the all-ONES pattern consists of $5{,}0 \times 10^6$ transitions per second nominally.

2.3 Index

The index is a point which defines the beginning and the end of a track. Its location is specified as a true position in 5.2.5 of ISO 3562.

2.4 Track capacity

The capacity of a track is $62\ 500 \begin{smallmatrix} +1\ 933 \\ -1\ 821 \end{smallmatrix}$ bits.

2.5 Track layout

Figure 1 shows the general track layout (see also annex B).

3 DEFINITIONS

3.1 sector : A track is divided into sectors. A sector may be further subdivided.

3.2 sector 0 : The Sector 0 contains information which defines the physical location and characteristics of a track.

3.3 data sectors : Each data sector is composed of an identifier and a data block.

3.4 identifier : The identifier contains information which defines the physical location and characteristics of a sector.

3.5 data block : Part of a sector in which information is recorded.

3.6 gap : The space between the various divisions of a track.

3.7 byte (or octet) : Eight serial bits, identified B8 to B1 with B8 as the most significant and recorded first.

3.8 hexadecimal notation :

$(00)_{16}$ denotes a byte (or octet) with B8 to B1 = 00000000

$(FF)_{16}$ denotes a byte (or octet) with B8 to B1 = 11111111

$(CC)_{16}$ denotes a byte (or octet) with B8 to B1 = 11001100

$(09)_{16}$ denotes a byte (or octet) with B8 to B1 = 00001001

$(0B)_{16}$ denotes a byte (or octet) with B8 to B1 = 00001011

$(0F)_{16}$ denotes a byte (or octet) with B8 to B1 = 00001111

$(F2)^*_{16}$ denotes a byte (or octet) with B8 to B1 = 11110010

For $(F2)^*_{16}$ the clock transitions of B6 and B5 are missing.

3.9 cyclic redundancy check (CRC) : This consists of two bytes which are the remainder formed by dividing the relevant bytes defined later in this specification by the polynomial

$$x^{16} + x^{15} + x^2 + 1$$

(See annex E.)

They can be used for error checking when reading.

4 DETAILED DESCRIPTION OF TRACK LAYOUT

4.1 Secteur 0

The first sector following index is unique in that it contains a track identifier and will therefore be described separately. Figure 2 shows the Sector 0 layout.

4.1.1 *Index gap*

This is a gap preceding the track identifier and shall be written so that the start of the track identifier is located within 65 ± 12,5 bytes from index. It is also a requirement that, when this gap is initially written, 65 bytes of $(FF)_{16}$ shall precede the track identifier. The first 25 bytes of $(FF)_{16}$ may, as a result of interchange, be unreadable (see annex C).

4.1.2 *Track identifier*

The track identifier consists of 16 bytes as follows :

4.1.2.1 Synchronization (8 bytes) as follows :

$(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(FF)_{16}$ $(F2)^*_{16}$ $(F2)^*_{16}$ $(09)_{16}$

4.1.2.2 F — Flag (1 byte). This is used to indicate defective and alternative tracks. The significance of the bits in this byte is as follows :

The first two bits (B8 and B7) are always ZERO. B6 to B3 are reserved for future standardization and are all ZERO.

B2 B1 = 00 indicates good original track.

B2 B1 = 01 indicates good alternative track.

B2 B1 = 10 indicates defective track, alternative has been allocated.

B2 B1 = 11 indicates defective track, no alternative has been allocated.

4.1.2.3 C — Cylinder (2 bytes). These specify in binary the address of the cylinder.

4.1.2.4 H — Head (1 byte). This specifies in binary the address of a track within a cylinder. The byte can have the values 0 or 1.

4.1.2.5 NS — Number of sectors (1 byte). This specifies in binary the number of data sectors in a track. For interchange purposes the value contained in this byte will be 20.

4.1.2.6 Cyclic redundancy check. These two bytes are formed as specified in 3.9 from the bytes defined in 4.1.2.2 to 4.1.2.5.

4.1.2.7 The track identifier ends with one byte $(CC)_{16}$.

4.1.3 *Track identifier gap*

A 36-byte gap of $(FF)_{16}$ is initially recorded between the end of the track identifier and the start of Sector 1. The contents of this gap may subsequently become undefined because of repeated writing operations.

4.2 Data sector

4.2.1 *Identifier*

The identifier is composed of 18 bytes. Figure 3 shows the identifier layout. The identifier is as follows :

4.2.1.1 Synchronization (8 bytes) as follows :

$(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(FF)_{16}$ $(F2)^*_{16}$ $(F2)^*_{16}$ $(OB)_{16}$

4.2.1.2 F — Flag (1 byte). This is used in each identifier for certain control and checking operations and can be used to indicate defective and alternative tracks. The significance of the bits in this byte is as follows :

B8 = 1 for the first sector following Sector 0 and alternate sectors thereafter, and

B8 = 0 for the other sectors.

B7 to B3 are reserved for future standardization and are all ZERO.

B1 and B2 : see 4.1.2.2.

4.2.1.3 C and H — Cylinder and Head (3 bytes). These bytes are identical to those in Sector 0 except when appearing on defective or alternative tracks. On a defective track, cylinder and head bytes C and H contain the cylinder and head number of the alternative track if the flag bits B1 and B2 are 1, 0 respectively. On an alternative track, C and H contain cylinder and head number of the defective track which it replaces.

4.2.1.4 S — Sector (1 byte). This is used to identify sectors on the track. The first sector after Sector 0 will have S = 1, and the subsequent sectors will be numbered consecutively.

4.2.1.5 DL — Data length (2 bytes). These specify in binary the number of information bytes in the data sector. For interchange purposes the data length will be 256 bytes.

4.2.1.6 Cyclic redundancy check. These two bytes are formed as specified in 3.9 from the bytes defined in 4.2.1.2 to 4.2.1.5.

4.2.1.7 The identifier ends with one byte $(CC)_{16}$.

4.2.2 *Identifier gap*

A 34-byte gap of $(FF)_{16}$ is initially recorded between the end of the identifier block and the start of the data block. The contents of this gap may subsequently become undefined because of repeated writing operations.

4.2.3 *Data block*

The data block consists of (DL + 12) bytes, where DL is the number of information bytes (see 4.2.1.5). Figure 4 shows the data block layout.

The data block is as follows :

4.2.3.1 Synchronization (8 bytes) as follows :

$(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(FF)_{16}$ $(F2)^*_{16}$ $(F2)^*_{16}$ $(OF)_{16}$

4.2.3.2 Information. This consists of a number of information bytes as specified in the DL portion of the identifier. The data in these bytes shall be recorded in the 7-bit coded character set in accordance with ISO 646. However, by agreement between the interchange parties, data in some other 7-bit or 8-bit code structured in accordance with ISO 2022 may be recorded.

A 7-bit coded character shall be recorded so that bits b7 to b1 of the coded character appear in positions B7 to B1 respectively (see 3.7); B8 shall always be ZERO. An 8-bit coded character shall be recorded so that bits a8 to a1 of the coded character are recorded in positions B8 to B1 respectively.

4.2.3.3 DF — Data flag byte. This is used in each data field and B8 = 1 indicates that the information in this data field is continued in the following sector.

B7 to B1 are reserved for future standardization and are all ZERO.

4.2.3.4 Cyclic redundancy check. These two bytes are formed as specified in 3.9 from the bytes defined in 4.2.3.2 and 4.2.3.3.

4.2.3.5 The data block ends with one byte $(CC)_{16}$.

4.2.4 *Data block gap*

The gap between the end of the data block and the start of the next sector is initially recorded with $(FF)_{16}$.

Its initial length is :

$$36 + \frac{1}{16} \text{DL bytes}$$

Any fraction is truncated.

DL is the number of information bytes in the data block.

The contents of this gap may subsequently become undefined because of repeated writing operations.

The length of the gap may vary due to repeated writing operations; however, a minimum of 36 bytes shall always be present.

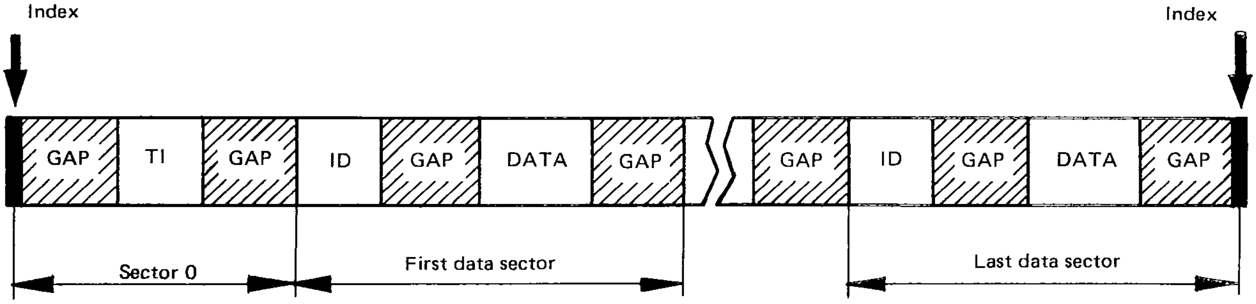
NOTE — For interchange purposes the length of this gap is initially 52 bytes.

4.2.5 *Last data block gap*

The gap following the last sector will be initially recorded as $(FF)_{16}$ to within ± 12,5 bytes of index.

It is also a requirement that the end of the last sector is located 23,5 ± 12,5 bytes before index when the track is recorded to the maximum capacity (see annex B) under worst-case conditions of disk speed and clock period (see also annex C).

For the interchange standard of 20 sectors of 256 bytes this gap is increased by 44 bytes.



TI — Track identifier
ID — Identifier
DATA — Data block

FIGURE 1 — **General track layout**

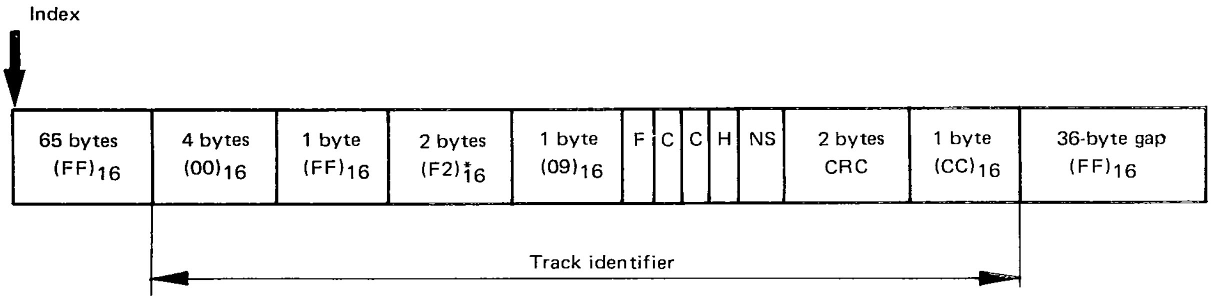


FIGURE 2 — **Sector 0 layout**

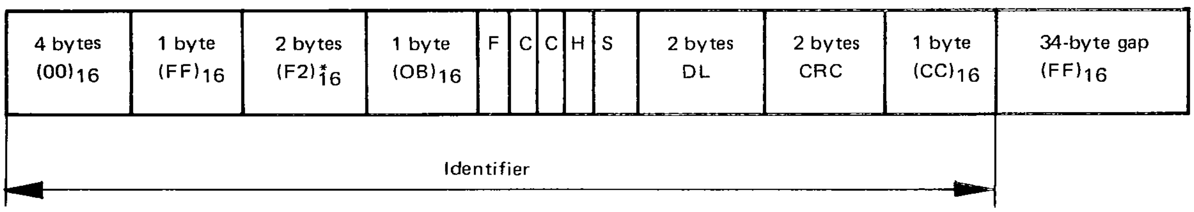


FIGURE 3 — **Identifier layout (data sector)**

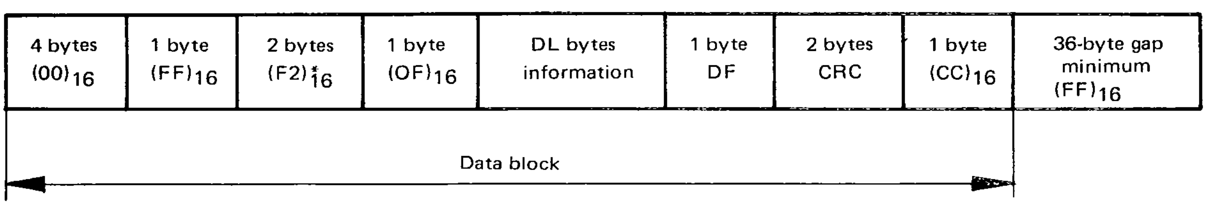


FIGURE 4 — **Data block layout**

ANNEX A
(not part of the standard)

ROTATION SPEED AND CLOCK PERIOD TOLERANCE

If the nominal record length is L, the minimum record length is L_1, the maximum record length is L_2 and the tolerance is x :

From 4.2.4 :

$$\frac{L_2}{L_1} = 1 + \frac{1}{16}$$

$$L_1 = L - x$$

$$L_2 = L + x$$

therefore

$$\frac{L + x}{L - x} = \frac{17}{16}$$

$$16\,L + 16\,x = 17\,L - 17\,x$$

$$33\,x = L$$

$$\frac{x}{L} = \frac{1}{33} = 3{,}03\ \%$$

Hence, 3,0 % is used.

ANNEX B
(not part of the standard)

TRACK DATA CAPACITY

The data capacity of a track may be calculated as follows :

The track capacity under worst-case conditions is 7 585 bytes.

This capacity is allocated as follows :

Index gap 65 bytes Track identifier 16 bytes Track identifier gap 36 bytes	117 bytes
Identifier 18 bytes Identifier gap 34 bytes Data block 12 + DL bytes Data block gap $\left(36 + \frac{1}{16}\text{DL}\right)$ bytes	$n\left(100 + \frac{17}{16}\text{DL}\right)$

where n is the number of data sectors in the track.

The following formula gives the maximum number of equal-length sectors that can be accommodated on a track :

$$n\left(100 + \frac{17}{16}\,\text{DL}\right) - \frac{1}{16}\,\text{DL} \leqslant 7\ 468$$

where the term $\frac{1}{16}$ DL compensates for the last data block gap.

Any fraction is truncated.

For data interchange purposes where DL = 256, the formula gives $n = 20$.

ANNEX C
(not part of the standard)

INDEX SLOT DETECTION TOLERANCES

A tolerance is given for the location of the start of the track identifier with respect to index to allow for equipment adjustment of the index slot detection system.

Figure 5 shows the effect, on the index gap and the gap after the last sector, of the tolerance on index slot detection under worst-case conditions of disk speed and clock period, with maximum data capacity.

The following cases are covered :

A. This shows the location of the start of the track identifier and the end of the last sector with respect to index when the index slot is detected at its nominal position.

B. As case A but with the index slot detected early.

C. As case A but with the index slot detected late.

D. This shows a track which was formatted as in case B being read by equipment which detects the index slot late. For this equipment the index gap is shortened to 40 bytes while the gap after the last sector is increased to 61 bytes.

E. This shows a track which was formatted as in case C being read by equipment which detects the index slot early. For this equipment the index gap is lengthened to 90 bytes. The gap after the last sector is shortened to 11 bytes.

In the above only the extreme cases are shown; intermediate values of the tolerance on index slot detection result in a situation where the first 25 bytes, read after the index slot has been detected, cannot be guaranteed. It is therefore recommended that these 25 bytes should be treated as undefined.

A further case is included which shows the conditions under which a minimum length gap after the last sector is written.

F. This shows a track which was partially formatted as in case C having the format completed, under worst-case conditions of disk speed and clock period with maximum data capacity, by equipment which detects the index slot early. The index gap is lengthened to 90 bytes leaving only 11 bytes after the last sector before the index slot is detected.

It should be noted that in all the above cases the minimum gap between the end of the last sector and the start of the track identifier is 101 bytes.

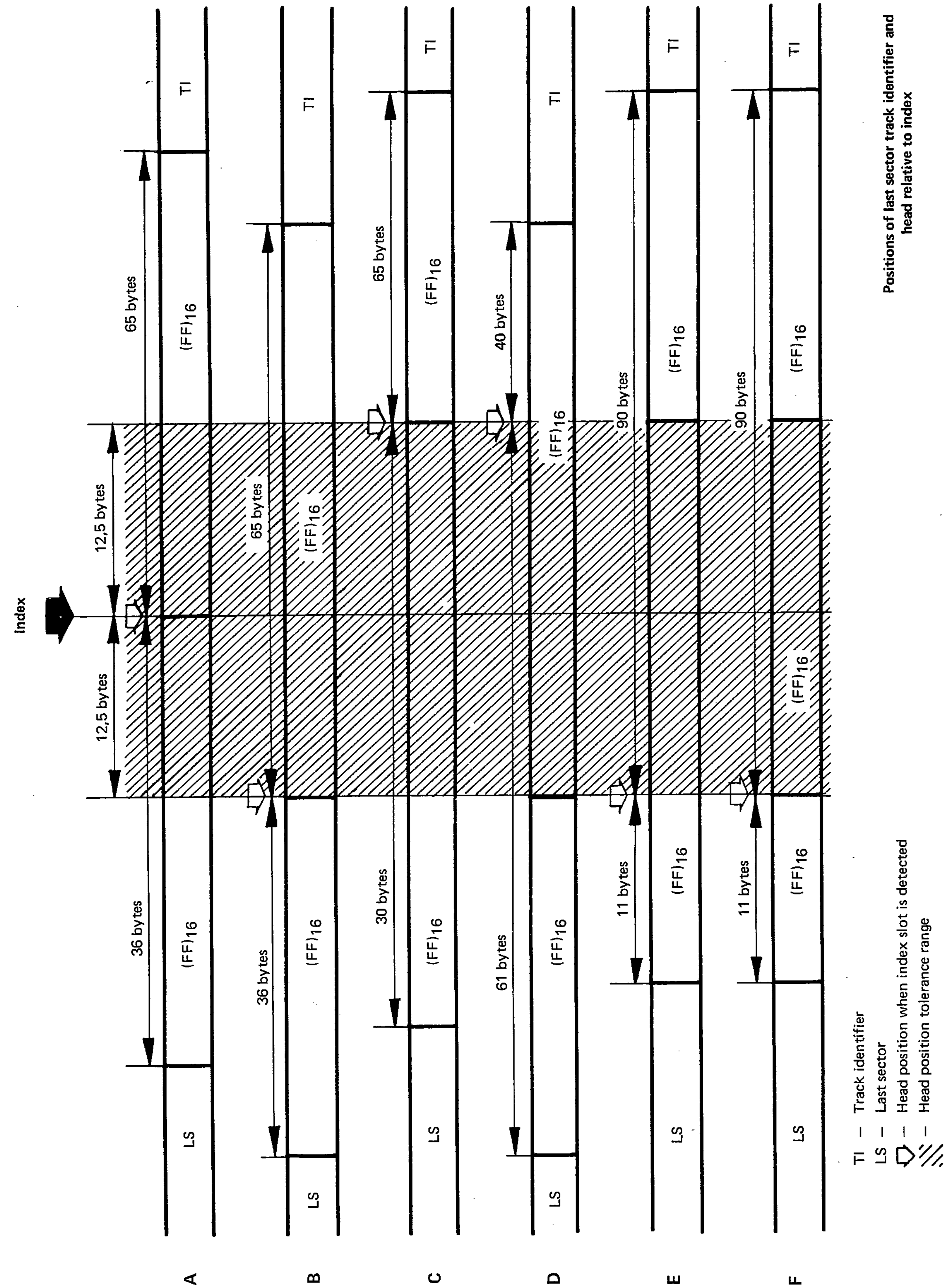


FIGURE 5 — Positions of last sector track identifier and head relative to index

ANNEX D

(not part of the standard)

FACTORS AFFECTING DATA INTERCHANGE

This annex provides some guidelines on the use of the format for data interchange.

D.1 SYNCHRONIZATION BYTES

These are bytes at the start of the track identifier, identifiers and data blocks; their purpose is to enable equipment reading the information on the track to identify the start of the above areas. The synchronization bytes are special in that they contain a unique pattern of flux reversals which would not normally be encountered elsewhere on the track. This enables equipment reading the information on the track to locate the synchronization bytes without reference to index.

D.2 UNDEFINED GAP CONTENTS

If information that lies within a track is updated, then at the point at which writing is started and terminated the information may be corrupted. Writing must be started and terminated such that the track identifier, identifiers and data blocks remain as defined in the body of this document. To allow for flexibility in equipment design and to allow for disk speed tolerances, the point of switching from reading to writing and vice versa has not been precisely defined. This means that after a number of update operations a number of bytes in the gap may be corrupted and for example an $(F2)^*_{16}$ pattern may be generated. However, the gaps are initially defined in such a way that the chance of a complete set of synchronization bytes being generated is negligible.

ANNEX E
(not part of the standard)

CRC IMPLEMENTATION

Figure 6 shows the feedback connections of a shift register which may be used to generate the CRC bytes.

Prior to the operation, the shift register is set to ZERO. Input data are added (exclusive OR) to the contents of bit 15 of the register to form a feedback.

This feedback is in its turn added (exclusive OR) to the contents of bit 1 and bit 14.

On shifting, the outputs of the exclusive OR gates are entered respectively into positions C0, C2 and C15.

After the last data bit has been added, the register is shifted once more as specified above.

The register then contains the CRC bytes.

If further shifting is to take place during the writing of the CRC bytes, the control signal inhibits exclusive OR operations. To check for errors when reading, the data bits are entered into the shift register in exactly the same manner as they were during writing. After the data the CRC bytes are also entered into the shift register as if they were data. After this operation the shift register contents will be all ZERO if the record does not contain errors.

The error burst detection characteristics of this method are detailed below.

For data lengths of 4 096 bytes or less it will detect :

- all errors in a single burst of 16 bits or less;
- 99,997 0 % of errors in a single burst of 17 bits;
- 99,998 5 % of errors in a single burst greater than 17 bits.

This method will also detect any odd number of bits in error.

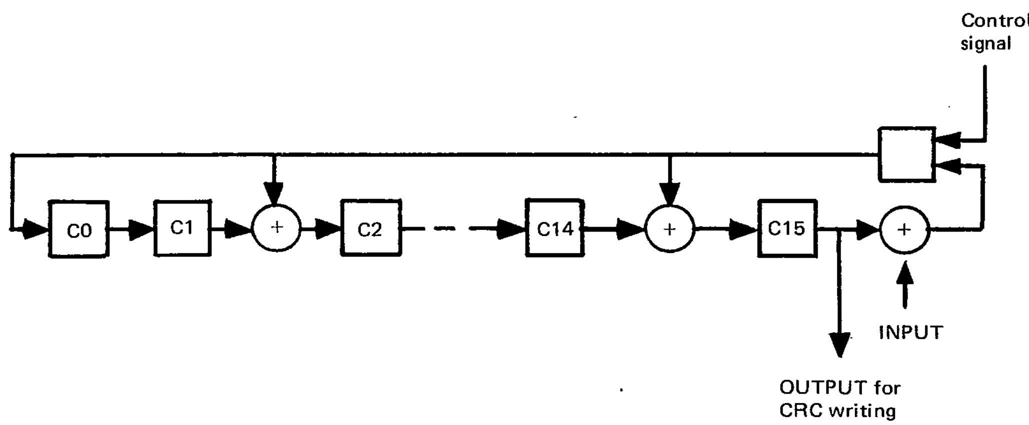


FIGURE 6 — **CRC shift register**