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BSI Standards Publication

Device embedded substrate

Part 2-1: Guidelines — General description of technology

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A list of organizations represented on this committee can be obtained on request to its secretary.

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SPECIFICATION TECHNIQUE

Device embedded substrate –
Part 2-1: Guidelines – General description of technology

Substrat avec appareil(s) intégré(s) –
Partie 2-1: Directives – Description générale de la technologie

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DEVICE EMBEDDED SUBSTRATE –

Part 2-1: Guidelines – General description of technology

FOREWORD

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- the subject is still under technical development or where, for any other reason, there is the future but no immediate possibility of an agreement on an International Standard.

Technical Specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC TS 62878-2-1, which is a Technical Specification, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this Technical Specification is based on the following documents:

Enquiry draft	Report on voting
91/1142/DTS	91/1163A/RVC

Full information on the voting for the approval of this Technical Specification can be found in the report on voting indicated in the above table.

A list of all parts in the IEC 62878 series, published under the general title *Device embedded substrate*, can be found on the IEC website.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

This part of IEC 62878 provides guidance with respect to device embedded substrate, fabricated by embedding discrete active and passive electronic devices into one or multiple inner layers of a substrate with electric connections by means of vias, conductor plating, conductive paste, and printing. Within the IEC 62878 series,

- IEC 62878-1-1 specifies the test methods,
- IEC TS 62878-2-1 gives a general description of the technology,
- IEC TS 62878-2-3 provides guidance on design, and
- IEC TS 62878-2-4 specifies the test element groups.

The device embedded substrate may be used as a substrate to mount SMDs to form electronic circuits, as conductor and insulator layers may be formed after embedding electronic devices.

The purpose of the IEC 62878 series is to achieve a common understanding with respect to structures, test methods, design and fabrication processes and the use of the device embedded substrate in industry.

DEVICE EMBEDDED SUBSTRATE –
Part 2-1: Guidelines – General description of technology

1 Scope

This part of IEC 62878 describes the basics of device embedding substrate.

This part of IEC 62878 is applicable to device embedded substrates fabricated by use of organic base material, which include for example active or passive devices, discrete components formed in the fabrication process of electronic wiring board, and sheet formed components.

The IEC 62878 series neither applies to the re-distribution layer (RDL) nor to the electronic modules defined as an M-type business model in IEC 62421.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

IEC 61189 (all parts), *Test methods for electrical materials, printed boards and other interconnection structures and assemblies*

3 Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 apply.

3.2 Abbreviations

BGA	ball grid array
I/O	in/out
IPD	integrated passive device
LGA	land grid array
LTCC	low temperature co-fired ceramic
MEMS	micro electro mechanical systems
PoP	package on package
QFN	quad flat no-lead package
QFP	quad flat package
SMD	surface mount device
SOJ	small outline J-leaded package
WLP	wafer level package

4 Technology of device embedded substrate

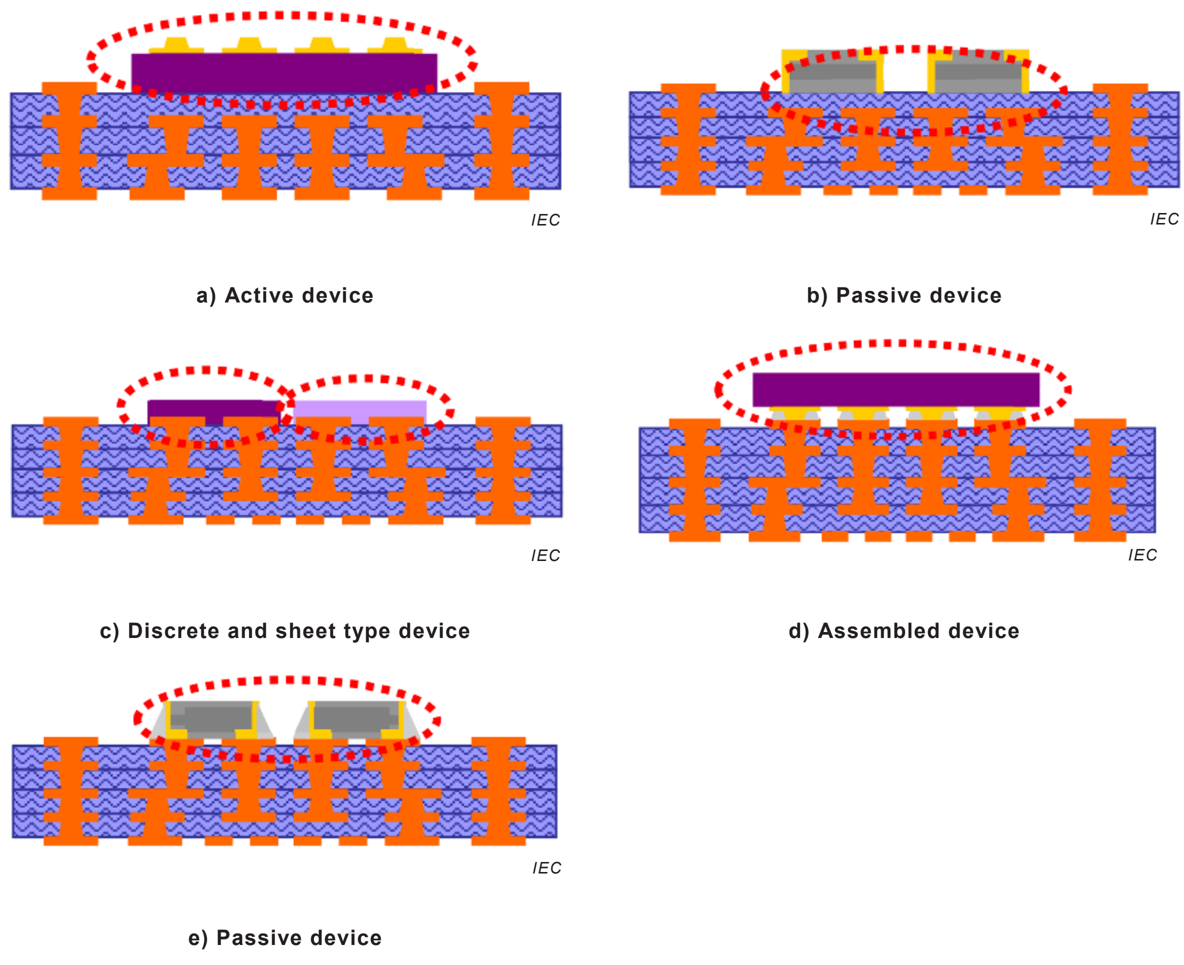
4.1 Basic structures

Figure 1 shows an example of device embedding structures in the fabrication process of a device embedded substrate. Active and passive devices are connected to each other by interlayer vias and/or conductor patterns. Insulating layers are formed using insulating materials

with vias for connection of inside conductor patterns to the conductor patterns formed on the surface(s) of the substrate. Figure 2 shows the substrate with connections using pads. Figure 3 shows the board using via connections.

The insulating layer includes rigid and flexible insulating resins such as phenol resin, epoxy resin, polyimide resin and modified polyimide resin, which may be reinforced with glass cloth, aramid cloth or paper. Interconnections include conventional interconnections to terminals of an embedded device and to a land for SMD, and formation of terminals by copper plating or vias using conductive paste.

This part of IEC 62878 does not specify a specific fabrication process of a device embedded substrate, via diameter/land diameter, conductor width/conductor spacing or a conductor line density.



a) Active device

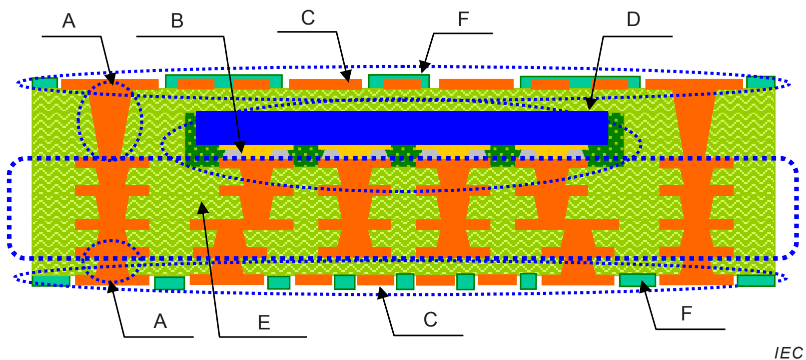
b) Passive device

c) Discrete and sheet type device

d) Assembled device

e) Passive device

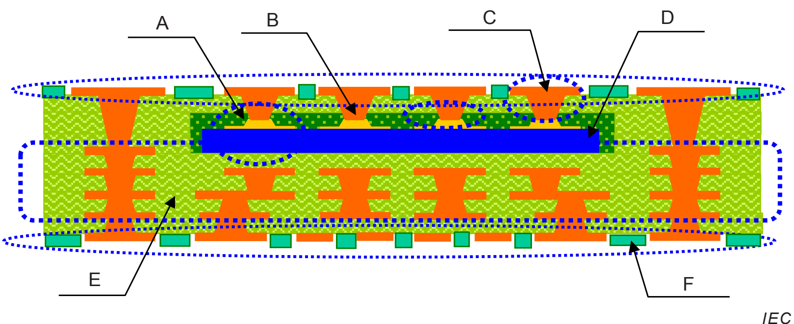
Figure 1 – Examples of device embedded substrate



Key

A	Layer connection (via)
B	Solder connection
C	Pattern formation
D	Embedded active device
E	Base
F	Solder resist

Figure 2 – Completed device embedded substrate (pad connection)



Key

A	Embedded with terminals upward
B	Copper plated connection
C	Copper plated via
D	Embedded active device
E	Base
F	Solder resist

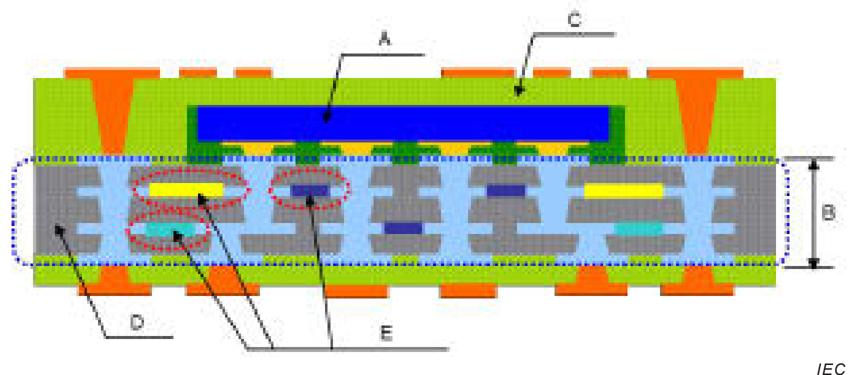
Figure 3 – Completed device embedded substrate (via connection)

4.2 Technology of device embedded substrate

There are two types of device embedded substrates. One type consists of mounting active and/or passive devices on a base substrate, then covering with organic resin; the other type consists of forming a device on a substrate and then covering it with organic resin.

Figure 4 shows the structure of a pad connection type substrate in which the active device is connected by pad onto the passive device embedded ceramics base. The device embedded substrate also includes composite type substrates which consist of mass produced inorganic

ceramics, including LTCC (low temperature co-fired ceramics, hereafter referred to as ceramics) substrates.

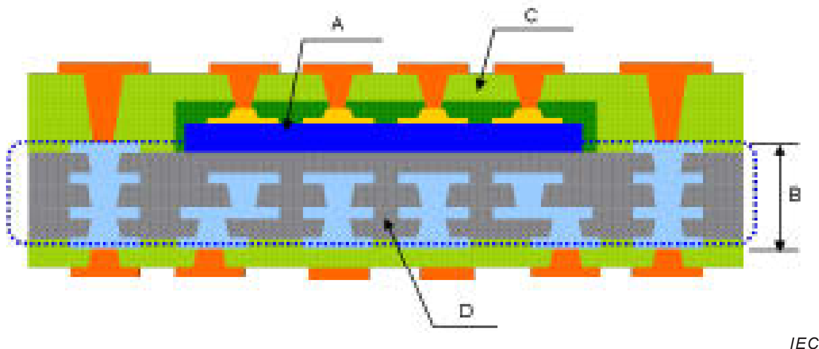


Key

A	Active device
B	Base
C	Embedding using resin
D	Ceramic substrate
E	Embedded devices in ceramic

Figure 4 – Structure of a pad connection type substrate on a passive device embedded ceramics base

In the via structure type, as shown in Figure 5, the ceramic substrate is used as a base on which active and passive devices are mounted and the entire body is covered with organic resin. However, details of inorganic ceramic substrates are not specified in this part of IEC 62878. Such a ceramic substrate is treated just as a base of a device embedded substrate.



Key

A	Active device
B	Base
C	Resin embedding
D	Ceramic substrate

Figure 5 – Structure of a device embedded substrate using a ceramic board as the base (via connection type)

Classification of device embedding is given in Table 1. Active devices include for example bare die, wafer level package (WLP), ball grid array (BGA), land grid array (LGA), quad flat no lead package (QFN), small outline J-leaded package (SOJ) and quad flat package (QFP).

Passive devices include a chip component, a complex chip component like an array and an integrated passive device (IPD). Module and MEMS may be embedded into the substrate after

packaging and molding. The components formed during substrate formation are not covered by this specification and are not included in Table 2.

There are two types of embedding formed passive components. The first type consists of forming passive components using thick film or thin film technology on the base of silicon or compound semiconductor and/or on the stacked chip at the wafer level or on package-on-package (PoP). The second type consists of using a sheet-type passive device on an organic substrate followed by the embedding of other devices.

Table 1 – Classification of device embedding

Classification	Item	Embedding	Device terminals	Bonding	Schematics
Active device	Bare die	Die bonding	Peripheral	Wire bonding	
		Flip chip bonding	Peripheral area array	Flip chip bonding	
		Die bonding	Peripheral area array	Via connection (Plating, paste)	
	Wafer level package	Mounting	Peripheral area array	Soldering Conductive paste	
		Die bonding	Peripheral area array	Via connection (Plating, paste)	
	Package	Mounting	BGA, LGA, QFN	Soldering Conductive paste	
		Mounting	BGA, LGA, QFN	Via connection (Plating, paste)	
Passive device	Chip component	Mounting	Rectangular chip Rod type chip	Through hole	
		Mounting	Rectangular chip Rod type chip	Soldering Conductive paste	
		Mounting	Rectangular chip	Via connection (Plating, paste)	
	Module chip component	Mounting	Rectangular chip	Soldering Conductive paste	
		Mounting	Rectangular chip	Via connection (Plating, paste)	
	Integrated passive device	Mounting	IPD	Soldering Conductive paste	
		Mounting	IPD	Via connection (Plating, paste)	
Module	Packaging and molding	Mounting	Arbitrary	Soldering Conductive paste	

Classification	Item	Embedding	Device terminals	Bonding	Schematics
		Mounting	Arbitrary	Via connection (Plating, paste)	
MEMS	Packaging and molding	Mounting	Arbitrary	Soldering Conductive paste	
		Mounting	Arbitrary	Via connection (Plating, paste)	

Table 2 – Formed embedded device into the substrate

Classification	Item	Embedding	Device terminals	Bonding	Schematics
Active device	Formed	Thin film sputtering	Silicon	Via connection (Plating, paste)	
		Thick film screen printing	Semiconducting polymer		
Passive device	Formed	Double through hole	Copper plating		
		Etching	Laminate material		
		Etching	Film		
		Screen printing	Polymer		
		Transfer	Ferromagnetic ceramics		
		Lamination	Seeding		
		Spin coating	Polymer		

4.3 Structures of device embedded substrates and terms used in this specification

Structures and fabrication processes of device embedded substrates are illustrated in Table 3. A base substrate is necessary for a device embedded substrate to embed active and passive devices. Most of the base substrates are multilayer substrates and/or build-up substrates which are made of insulating resin board; insulating sheet, metal sheet and film carrier can also be used. Table 3 shows the methods to embed active or passive devices and then connect devices to the surface conductor by plated through hole vias and/or conductive paste, and checking items during the fabrication process.

This specification, however, does not cover active devices formed on silicon interposer, compound semiconductor substrates or a printed wiring board and formed passive device (resistor, capacitor or inductor). On the other hand it covers an inductor formed together with the formation of conductor pattern and the capacitor with via-in-via structure.

Table 3 – Embedded device structure and fabrication process

Process	Item	Structure		To check
		Pad bonding	Via connection	
1	Base			Opening, short-circuiting
2	Mounting			Position accuracy
3	Pad bonding		-	Connection, conduction
4	Embedding			Microvoid Board thickness Flatness
5	Via forming			Hole position Terminal position Resistance to chemicals
6	Via connection	-		Thicknesses of copper plating and conductive paste Microvoid
7	Pattern formation (multi-layer)			Open, short
8	Surface treatment (Solder mask, etc.)			Visual inspection

5 Jisso mounting and interconnection

5.1 General

There are two types of terminal connection. One type consists of connecting the terminals of an embedded device to connecting pads formed on the base, and the other consists of forming connecting vias on the device after embedding. The device is connected to pads on the base using conventional semiconductor and SMD mounting techniques and then the device is embedded. In the second type, the device is connected to a conductor pattern after it has been embedded by copper plating or conductive paste. Both device mounting types can be classified into die-bonding and mounting methods, as shown in Table 4.

Table 4 – Jisso mounting and interconnection of device embedded substrate

Jisso mounting		Device	Interconnection		Structure
			Process	Interconnection	
Pad bonding	Die bonding	Chip	Wire bonding		
			Flip-chip bonding	Metal bonding Contact connection	Metal bonding Contact
	Mounting	Wafer level package (WLP)	Reflow polymer bonding	Soldering conductive paste	Soldering Conductive paste
		Package			
		Rectangular chip			Soldering Conductive paste
		Rod-type chip			
		Module			Soldering Conductive paste
		MEMS			

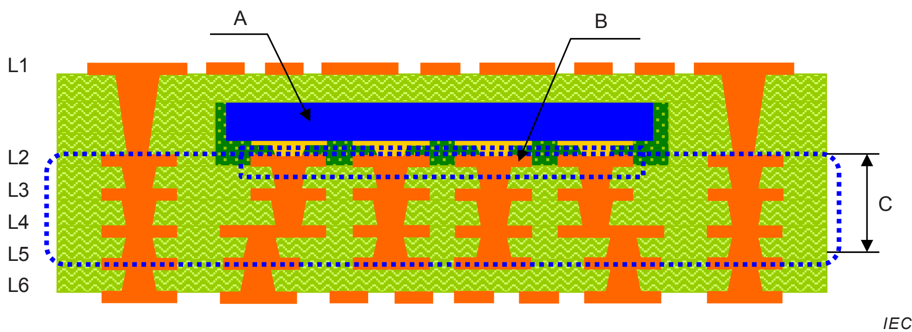
<table>
<tr><th colspan="2" rowspan="2">Jisso mounting</th><th rowspan="2">Device</th><th colspan="2">Interconnection</th><th rowspan="2">Structure</th></tr>
<tr><th>Process</th><th>Interconnection</th></tr>
<tr><td rowspan="7">Via bonding</td><td rowspan="2">Die bonding</td><td>Chip</td><td rowspan="6">Via connection</td><td rowspan="6">Copper plating conductive paste</td><td rowspan="3">Copper plating
Conductive paste</td></tr>
<tr><td>Wafer level package (WLP)</td></tr>
<tr><td rowspan="5">Mounting</td><td>Package</td></tr>
<tr><td>Rectangular chip</td><td rowspan="4">Copper plating
Conductive paste</td></tr>
<tr><td>Rod-type chip</td></tr>
<tr><td>Module</td></tr>
<tr><td>MEMS</td><td>Via connection</td><td>Copper plating
Conductive paste</td></tr>
</table>

Shape and surface treatment of terminals of the device to be embedded should be agreed between user and supplier of the device.

5.2 Interconnections and structures of device embedded substrate

Figure 6 shows each section of a device embedded substrate and its name. See IEC 60194 for the terms used in this part of IEC 62878. Additions to IEC 60194 for the terms specific to device embedding technology are being reviewed. The number of layers is counted after device embedding is complete as L1, L2 to L6 (in case of 6 layers) counting from the top layer.

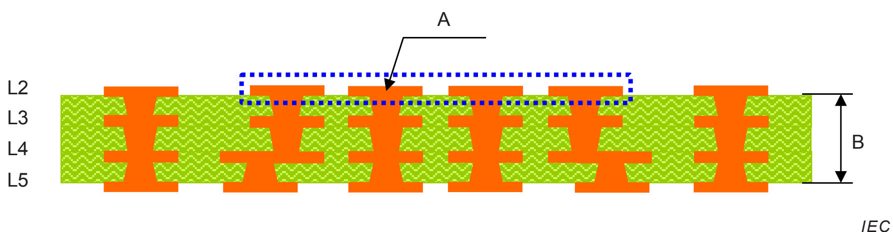
The structure of the device embedded substrate is illustrated by means of the structure of the build-up substrate. Figure 7 shows a typical base structure and Figure 8 a cavity structure. Figure 9 shows the structure for an insulating base and Figure 10 for a base using a conductive carrier or metal sheet. Use of ceramic substrate in device embedding is stated here for technical information. Figure 11 and Figure 12 show ceramic board as the wiring board base and ceramic board used as base, respectively.



Key

A	Active device
B	Embedded device connecting pad
C	Base

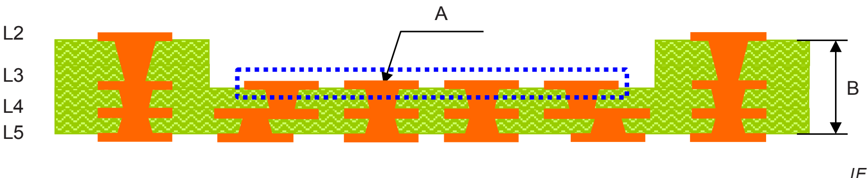
Figure 6 – Entire structure of device embedded substrate



Key

A	Embedded device connecting pad
B	Base

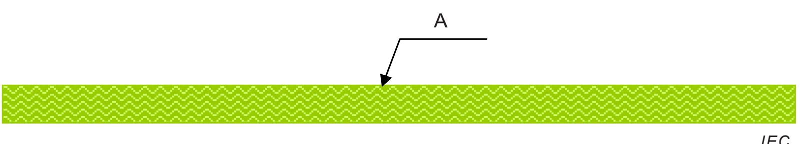
Figure 7 – Base (typical structure)



Key

A	Embedded device connecting pad
B	Base

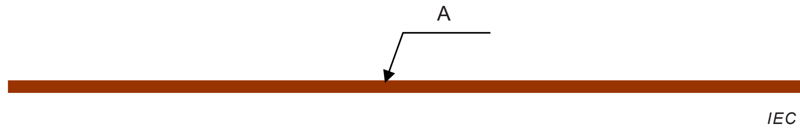
Figure 8 – Base (cavity structure)



Key

A	Insulating material (base, prepreg, etc.)

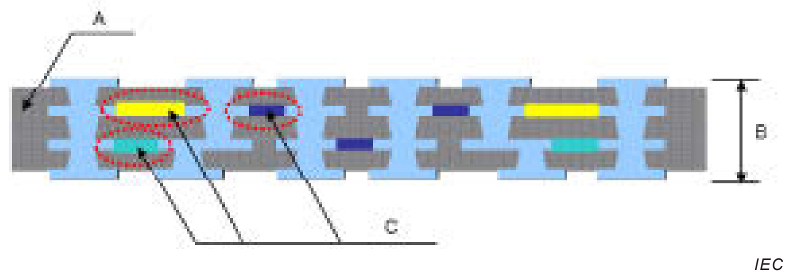
Figure 9 – Base (insulator)



Key

A	Copper foil

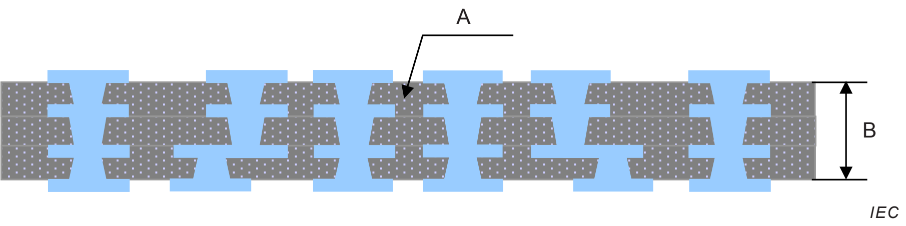
Figure 10 – Base (Conductive carrier – metal plate)



Key

A	Ceramic wiring board
B	Base
C	Embedded component in ceramic board

Figure 11 – Passive device embedded ceramic board used as a base



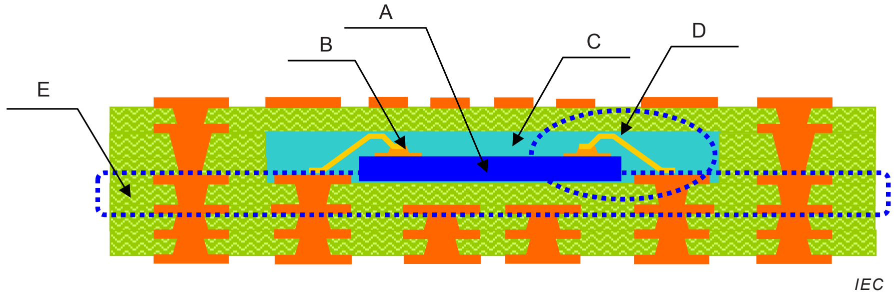
Key

A	Ceramic wiring board
B	Base

Figure 12 – Ceramic board used as base (ceramic)

5.3 Device embedding by conventional process

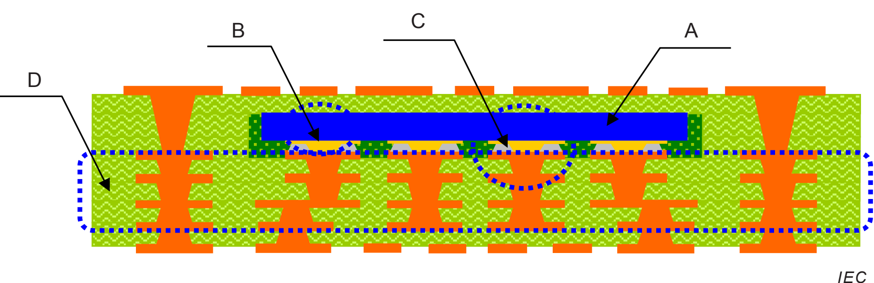
Figure 13 to Figure 18 show various cases of device embedding in conventional mounting techniques, electric connection after embedding of various types of devices, embedding device to more than one layer, device embedding with a resin base, and also the use of a conductor layer and metal sheet/copper foil.



Key

A	Active device
B	Embedded with upward terminal
C	Encapsulant
D	Bonding wire
E	Base

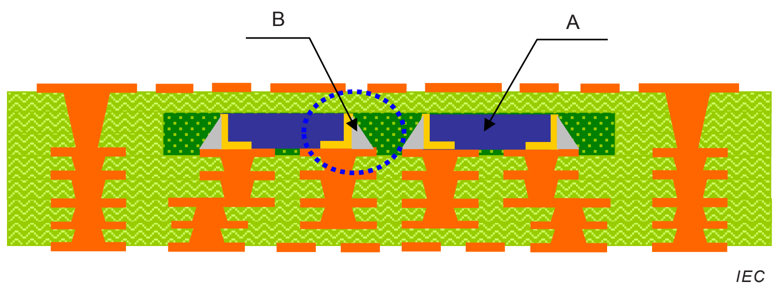
Figure 13 – Wire bonding connection and embedding of active device bare die



Key

A	Active device
B	Embedded with downward terminal
C	Soldering
D	Base

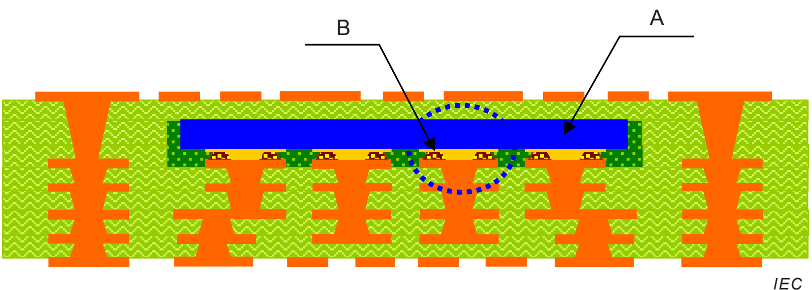
Figure 14 – Soldering connection and embedding of active device



Key

A	Passive device
B	Soldering

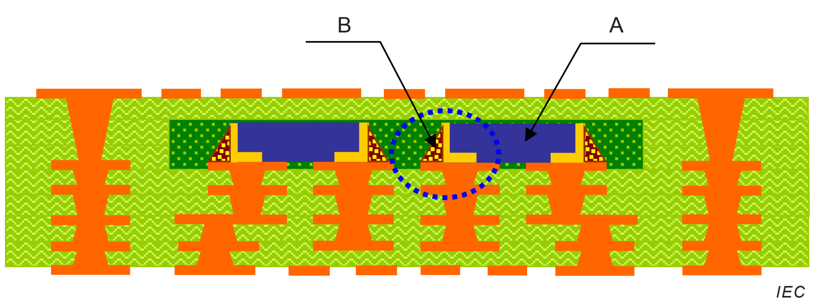
Figure 15 – Soldering connection of square type passive device



Key

A	Active device
B	Conductive adhesive

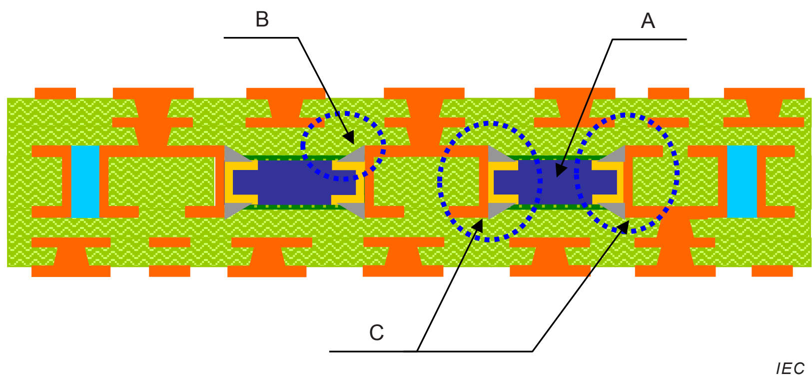
Figure 16 – Conductive resin connection and embedding of active device



Key

A	Passive device
B	Conductive adhesive

Figure 17 – Conductive resin connection and embedding of square type passive device



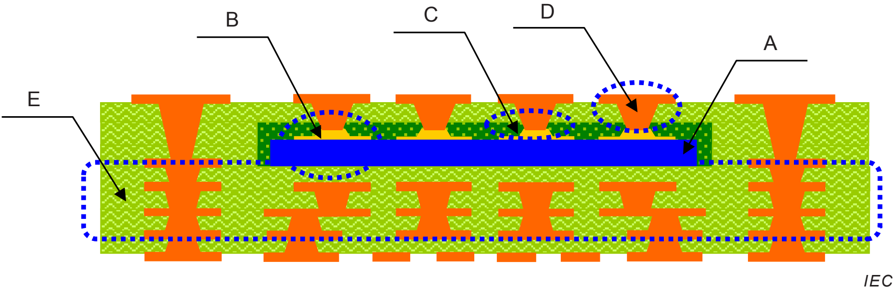
Key

A	Passive device
B	Soldering
C	Two through holes

Figure 18 – Soldering connection into through hole and embedding of passive device

5.4 Device embedding using vias

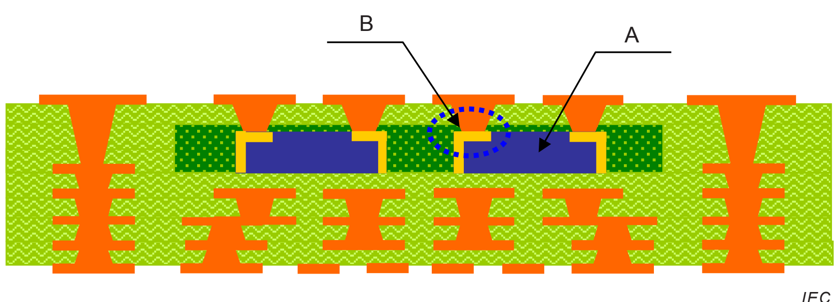
Figure 19 to Figure 27 show various cases of device embedding using vias.



Key

A	Active device
B	Embedded with upward terminals
C	Copper plating connection
D	Copper plated via
E	Base

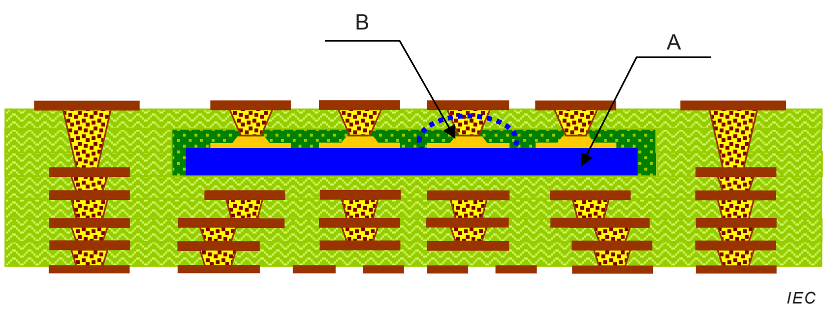
Figure 19 – Connection by copper plating after embedding of active device



Key

A	Passive device
B	Copper plating connection

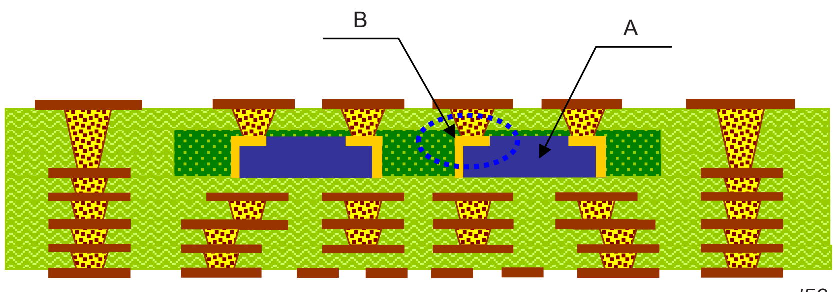
Figure 20 – Connection by copper plating after embedding of square type passive device



Key

A	Active device
B	Conductive paste connection

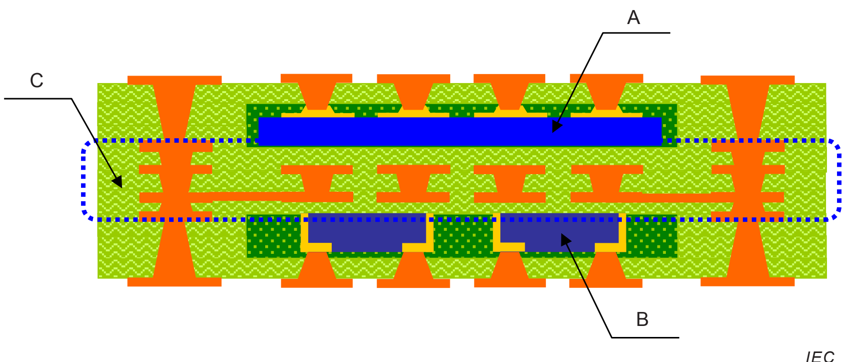
Figure 21 – Conductive paste connection after embedding of active device package



Key

A	Passive device
B	Conductive paste connection

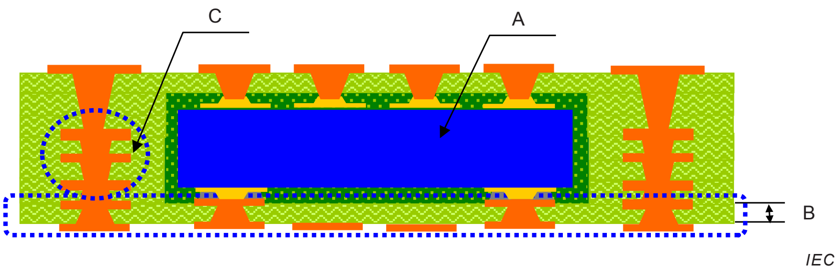
Figure 22 – Conductive paste connection after embedding of square type passive device chip



Key

A	Active device
B	Passive device
C	Base

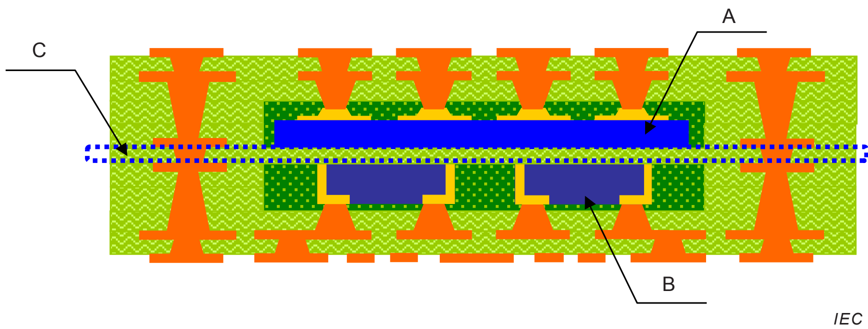
Figure 23 – Device embedded substrate for device embedding in multi-layers



Key

A	Active device
B	Base
C	Conductive layer in embedding layer

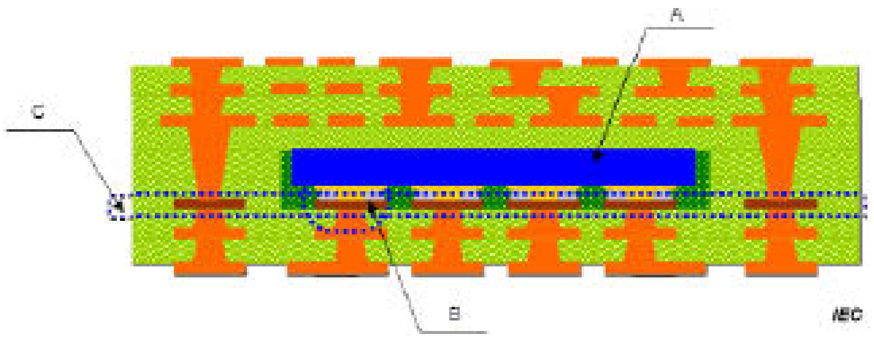
Figure 24 – Embedding of devices over multiple layers



Key

A	Active device
B	Passive device
C	Base (insulator)

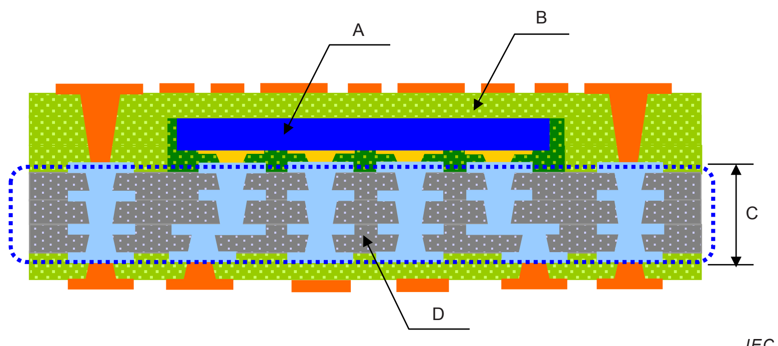
Figure 25 – Resin base substrate



Key

A	Active device
B	Soldering
C	Base (Copper foil)

Figure 26 – Conductor and metal sheet/copper foil as base substrate



Key

A	Active device
B	Molding compound
C	Ceramic substrate
D	Base

Figure 27 – Device embedded substrate using passive device embedded ceramic substrates as base substrate – Second type

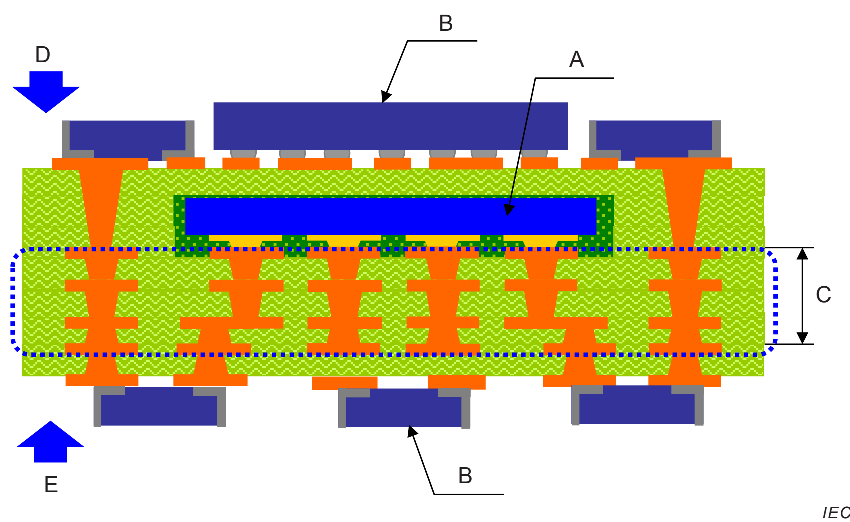
6 Naming of each section

6.1 General

The structure of a device embedded board is described in 5.2. Positions and names of the parts of a board are specified here to technically understand the construction and structure of a device embedded board and to establish a common understanding in design and/or production of boards.

6.2 General definition of top and bottom surfaces

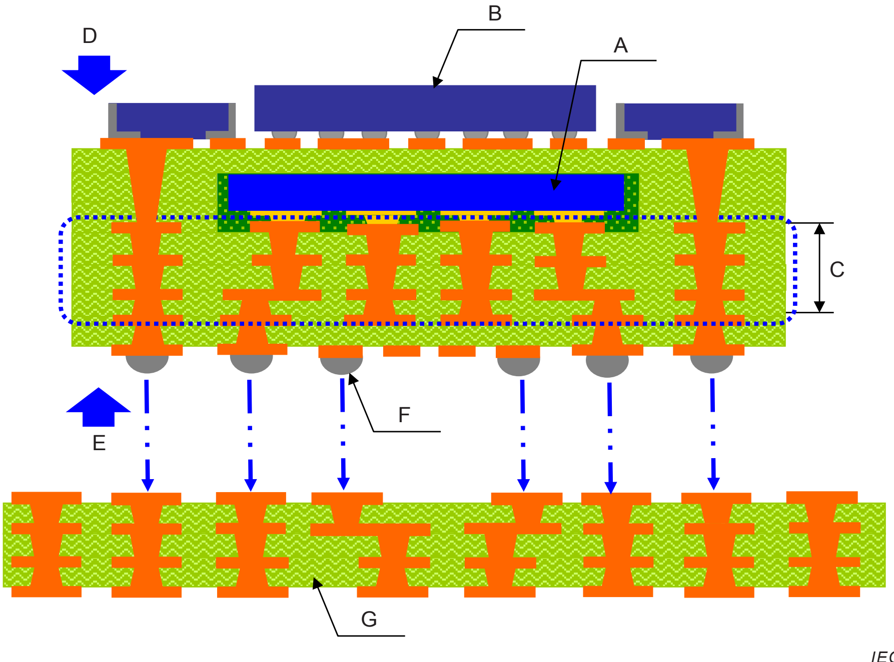
The top surface of a device embedded board is defined as the side where more electrical terminals (pads) exist. The bottom surface is defined as the side to which a board is connected to a printed wiring board (hereafter called mother board) and this is shown as Figure 29. Although the bottom surface may have more I/O terminals (pads) than the top surface, this side is still defined as the bottom surface. Figure 28 shows structure of a completed device embedded board and Figure 29 shows cross section of the completed device embedded board mounted on a mother board. User and supplier may define the top and bottom surfaces otherwise even when different from the definition given here.



Key

A	Embedded component	D	Top surface
B	Surface mounted device	E	Bottom surface
C	Base		

Figure 28 – Definition of top and bottom surfaces



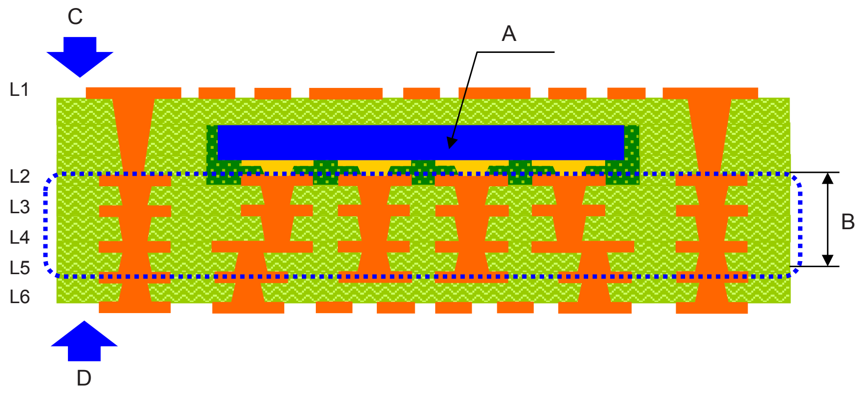
Key

A	Embedded component	E	Bottom surface
B	Surface mounted device	F	Connecting terminal (BGA or LGA)
C	Base	G	Printed wiring board (mother board)
D	Top surface		

Figure 29 – Definition of top and bottom surfaces (mounting of a mother board)

6.3 Naming of layers and interconnection position

Names and symbols of layers in a device embedded board are illustrated in Figure 30. Each layer is numbered as L1, L2 to L6 (in case of 6 layers) from the top surface. The number indicates the order of the layer with respect to the top surface.



Key

A	Embedded component	C	Top surface
B	Base	D	Bottom surface

Figure 30 – Names of layers in pad connection

In the case of via connection, the position of connecting terminals of the embedded device is different from the surrounding layer number. The component symbol and connecting position(s) are defined as illustrated in Figure 31 in order to clarify the interconnecting positions of the embedded device and of its electrical terminals with respect to construction design, pattern design, board fabrication and jisso (assembly).

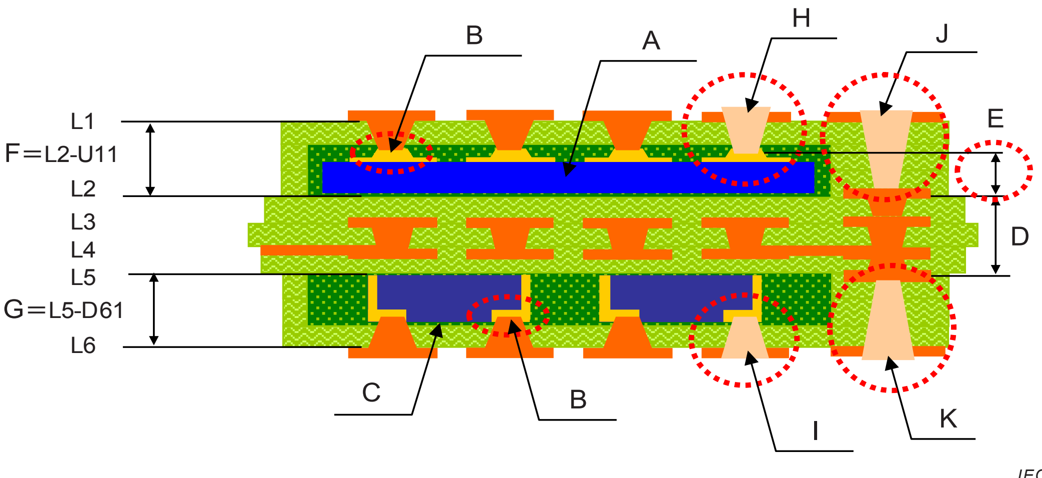
It is recommended to use the component symbols and names as shown in a circuit diagram to use 2 to 4 indications. The position of interconnection in the case of die-bonding or mounting of a device embedded device may be expressed using another name in addition to the name of the layer in which the device is embedded.

The surface of a device is upward facing. Use upward (U) when connecting terminals are in the upward facing surface, and downward (D) when the terminals are in the downward facing surface.

A three digit number is used if multiple components are embedded and/or multiple connection terminals are in the same layer. The left side number indicates the interconnecting layer number and the right side number indicates the layer position of the embedded component. If there are multiple layers involved, numbers 1, 2 indicate the layers from the top for upward and numbers 1, 2 indicate the layers from the bottom for downward. The second number may be omitted if there is only one embedded component in a layer. See the example in Figure 31.

Figure 31 shows additional information on the interconnection position. The active device is mounted on the L2 layer and connected to the first layer with upward direction. In this case, the name of the interconnection layer is expressed as L2-U11. The last digit 1 indicates the number of the embedded component. Passive components mounted on the L5 layer are connected to L6 with downward direction. In this case, the name of the interconnection layer is expressed as L5-D61.

A virtual layer is used as a virtual conductor layer and as the connecting points. The terminal connection design of an embedded device is carried out by first establishing the connection and hole machining data A and B, then the connection and hole machining data C and D for L2 and L5 (in the case of the above structure). The terminal setting may be omitted if a via connection and the positions of embedded device terminals and the conduction layer are the same.

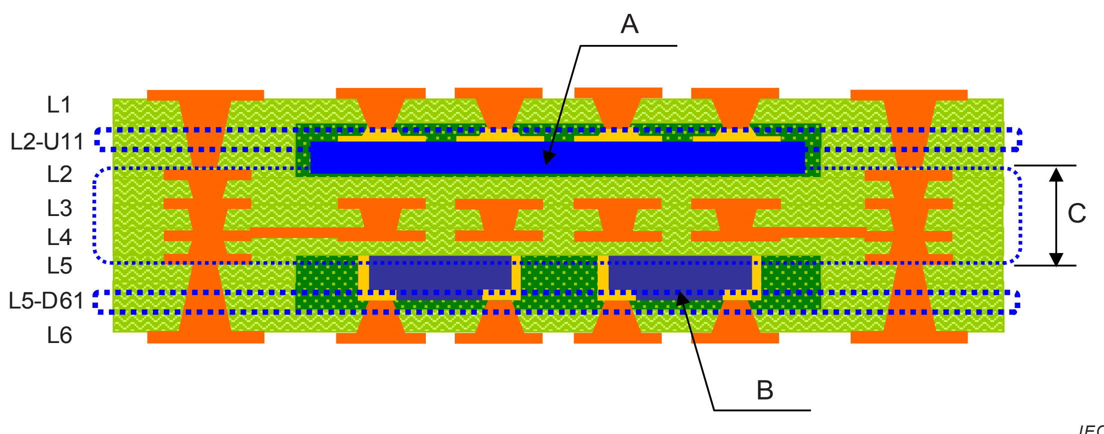


Key

A	Embedded active device	G	Name of the layer between L5 and L6
B	Connecting terminal	H	Connection and machining data from L1 to a virtual layer (L2-U11)
C	Embedded passive device	I	Connection and machining data from L1 to L2
D	Base	J	Connection and machining data from L6 to virtual layer (L5-D61)
E	Terminal position	K	Connection and machining data from L6 to L5
F	Name of the layer between L1 and L2		

Figure 31 – Additional information concerning the interconnection position

Figure 32 shows the interconnection position. Active device (xxxx) is mounted on the L2 layer and connected to the first layer with upward direction. In this case, the name of the interconnection position is expressed as xxxx-L2-U11. Passive components (yyyy) mounted on the L5 layer are connected to L6 with downward direction. In this case, the name of the interconnection position is expressed as yyyy-L5-D61.



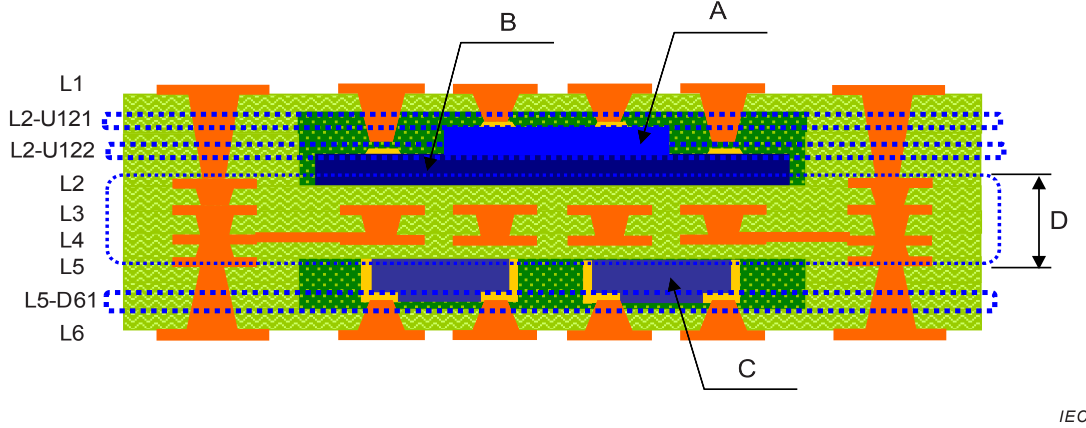
Key

A	Embedded active device
B	Embedded passive device
C	Base

Figure 32 – Names of layers in via connection [I]

Figure 33 shows a chip-stacked case. Active device 2 (xxx2) is mounted on the L2 layer and active device 1 (xxx1) is stacked on active device 2. Both are connected to the L1 layer with

upward direction. In this case, the name of the interconnection position of active device 2 is expressed as xxx2-L2-U122. The name of the interconnection position of active device 1 is expressed as xxx1-L2-U121. The second digit from the right (2) shows the number of the embedded device.

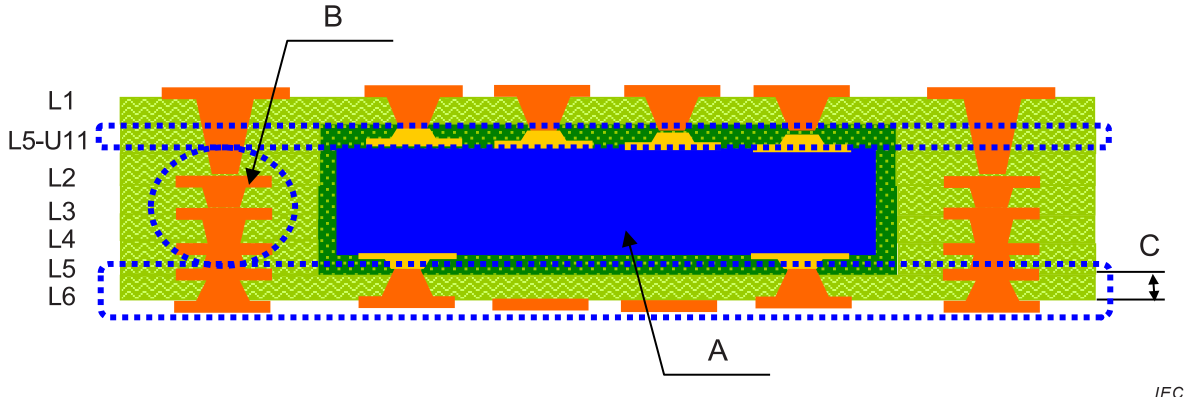


Key

A	Embedded active device 1	C	Embedded passive device
B	Embedded active device 2	D	Base

Figure 33 – Names of layers in via connection [II]

Figure 34 shows the interconnection position of an active device having multilayer connecting pads. Active device (xxxx) is mounted and connected to the L5 layer and pads on the other side are connected to the L1 layer with upward direction. Therefore, in this case, the name of the interconnection position of the active device is expressed as xxxx-L5-U11.



Key

A	Embedded active device
B	Conductor layer in embedding layer
C	Base

Figure 34 – Names of layers in via connection [III]

The content of Figure 31 to Figure 34 is summarized in Table 5.

Table 5 – Names of layers of device embedded board

Example	Embedded device				Embedding and connection of embedded device					
	Device	Hyphen	Compo-nent number	Hyphen	Layer	Hyphen	Terminal direction	Layer	No. of components	
									No.	Layer
Figure 31	Active	-	A12	-	L2	-	U	1	1	Omit
	Passive	-	1	-	L5	-	D	6	1	Omit
Figure 32	Active	-	A13	-	L2	-	U	1	1	Omit
	Passive	-	2	-	L5	-	D	6	1	Omit
Figure 33	Active	-	A13	-	L2	-	U	1	2	1
	IPD	-	4	-	L2	-	U	1	2	2
	Capacitor	-	1	-	L5	-	D	6	1	Omit
Figure 34	IPD, etc.	-	12	-	L2	-	U	1	1	Omit
		-	B1	-	L6	-	D	6	1	Omit

Information on embedded components is necessary in embedded board design.
For example, in Figure 31 the interconnection position of active device A12 is expressed as A12-L2-U11.

6.4 Definitions of insulation layer thickness, conductor gap and connection distance between terminal and conductor

6.4.1 General

The insulating layer thickness and conductor gap in each layer are specified based on the thickness of each layer.

a) The insulation layer thickness is defined as the thickness of one layer. The insulation thickness is not the thickness of each insulation layer made but the thickness of all layers used (or made).

b) The conductor gap is the thickness of the insulator between the conductor layer (pattern) and the facing conductor layer.

c) The distance between the electrode and the conductor is the thickness of an insulating layer existing between the terminals of an embedded component and the facing conductor, applicable to a via interconnection.

d) The following names are used for each section:

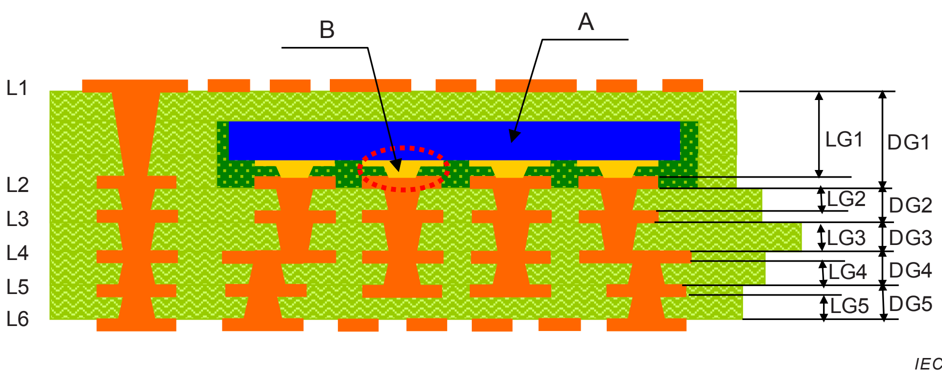
1) insulation layer thickness DG1 (dielectric gap);
2) conductor gap LG1 (layer gap);
3) electrode/conductor gap EG11 (device embedded gap).

The numbers in 1) and 2) indicate the numbers of layers; in 3) the left number is for conductor layer and the right number is for embedded components in the first layer and the second layer. See 6.3 for the definition of steps (layers).

Insulation layer thickness, conductor gap, and electrode/conductor gap are illustrated in Figure 35 and Figure 36. Additional information for the insulation layer thickness and conductor gap, and electrode/conductor gap are shown in Figure 37 and Figure 38.

6.4.2 Insulation layer thickness, conductor gap and electrode/conductor gap in pad connection

Figure 35 shows the definition of insulation layer thickness, conductor gap, and electrode/conductor gap. Conductor gap and dielectric gap from the corresponding insulation layer are expressed as LG and DG, respectively. And, the numbers following the abbreviations indicate the layer number.



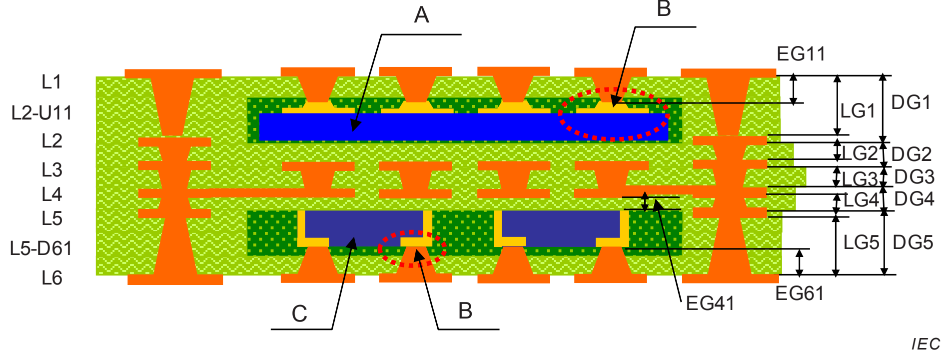
Key

A	Embedded device	B	Electrode (connecting terminal)

Figure 35 – Definition of insulating layer thickness and conductor gap in pad connection

6.4.3 Insulation layer thickness, conductor gap and electrode/conductor gap in a via connection

Figure 36 shows the definition of electrode gap in via connection. Electrode gap is expressed as EG and the numbers following the abbreviations indicate the connection to conductor layer 1 from one embedded component.



Key

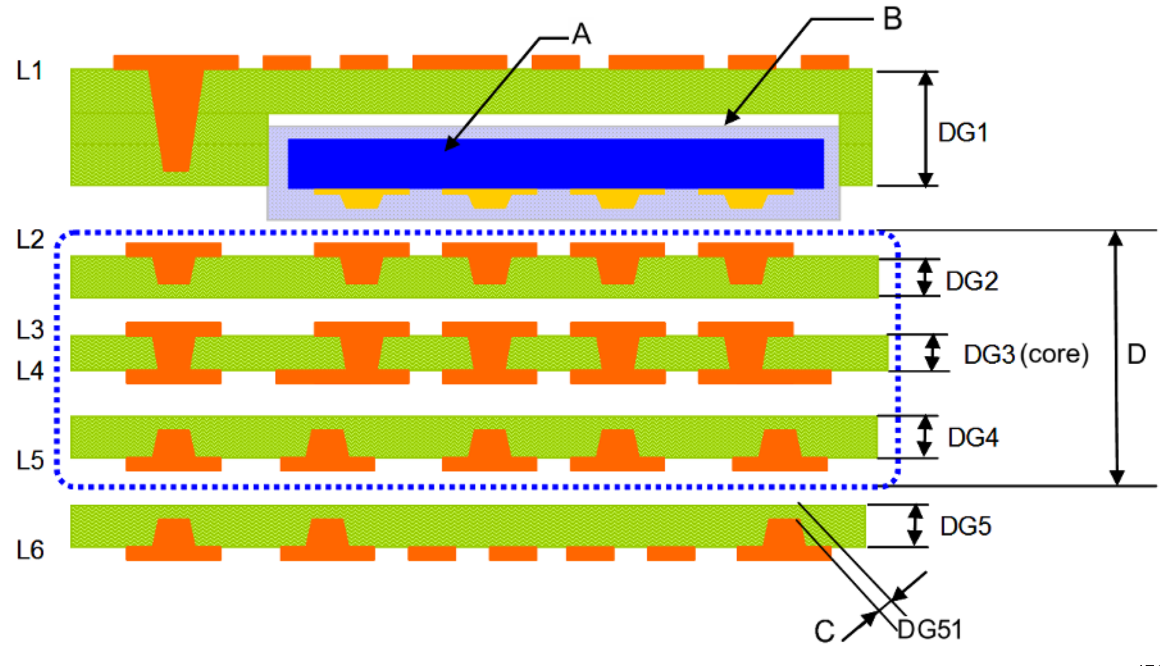
A	Embedded active device	C	Embedded passive device
B	Electrode (connecting terminal)		

Figure 36 – Definition of electrode gap in via connection

6.5 Additional information

6.5.1 Additional information for the insulation layer

Figure 37 illustrates the structure of the insulation layer prior to lamination. The active device is embedded in the insulation layer DG1. DG51 indicates the minimum thickness of the insulation layer in DG5.



Key

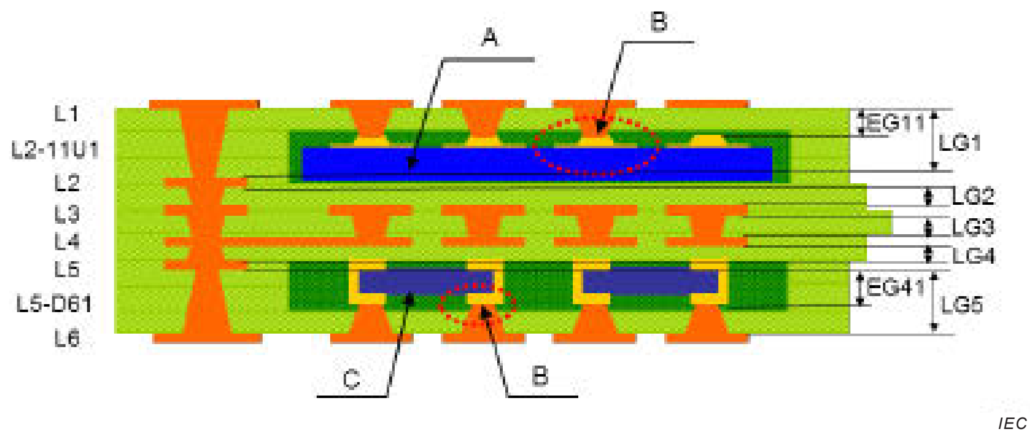
A	Embedded active device	C	Embedding of conductor in the insulation layer, DG51
B	Embedding in the insulation layer, DG1	D	Base

Figure 37 – Additional illustration of insulating layer thickness

6.5.2 Additional information for conductor gap and electrode/conductor gap

Figure 38 illustrates conductor gap and electrode/connector gap. EG11 indicates the insulation gap between non-attached pads of active devices embedded in the conductor of the outer-layer.

EG41 indicates the insulation gap between L4 and L5.



Key

A	Embedded active device	C	Embedded passive device
B	Electrode (connecting terminal)		

Figure 38 – Additional illustration for conductor gap and electrode/connector gap

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[1] To be published.

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