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BSI Standards Publication

Power electronics systems and equipment — Operation conditions and characteristics of active infeed converter (AIC) applications including design recommendations for their emission values below 150 kHz

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The UK participation in its preparation was entrusted to Technical Committee PEL/22, Power electronics.

A list of organizations represented on this committee can be obtained on request to its secretary.

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colour inside

Power electronics systems and equipment – Operation conditions and characteristics of active infeed converter (AIC) applications including design recommendations for their emission values below 150 kHz

Systèmes et équipements électroniques de puissance – Conditions de fonctionnement et caractéristiques des convertisseurs à alimentation active (AIC), y compris les recommandations de conception pour leurs valeurs d'émission inférieures à 150 kHz

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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POWER ELECTRONICS SYSTEMS AND EQUIPMENT –

Operation conditions and characteristics of active infeed converter (AIC) applications including design recommendations for their emission values below 150 kHz

FOREWORD

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Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC TS 62578, which is a technical specification, has been prepared by IEC technical committee TC 22: Power electronic systems and equipment.

This second edition cancels and replaces the first edition published in 2009. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) IEC TS 62578, in its revised version includes observed values out of practical applications for emission values below 150 kHz.
b) Therefore the document has been extended compared to the first edition, several detailed analysis results are given in the extended Annexes.
c) Design recommendations have been derived from the international working group by an assessment of the power supply impedances between 2 kHz and 9 kHz, a comprehensive analysis of the withstand capability of power capacitors against harmonic currents injected by AIC, immunity tests of equipment and considerations about shifted resonances in the power supply network with increased population of undamped filter capacitors.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
22/235/DTS	22/239/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

The French version of this technical specification has not been voted upon.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

This revision of the technical specification IEC TS 62578 is necessary because active infeed converters (AIC) are a state of the art technology in power electronic products and will be of major importance in order to realize the "smart grid" and the "energy efficiency" initiatives.

AICs in industrial and domestic use are necessary to feedback energy from an energy source (e.g. solar panels, fuel cells or wind turbines) or from a motor load to the power supply network and make it available for other consumers instead of dissipating it as a waste-heat to the environment.

Dispersed power generating equipment uses AICs to synchronise their voltages and currents to the power supply network or to exchange electrical energy between energy storage devices such as batteries and consumers.

Utilities will require information on how to correctly apply the AICs in order to mitigate harmonics in the power supply network.

AICs can also be used to mitigate pre-existing harmonics in the supply system – information on this is of interest to utilities.

Different possible topologies of AICs are described together with their specific advantages.

Warning: The recommendations of maximum emission values for conducted emissions <150 kHz defined in this document are based on observations and experience gained from state of the art AICs operating today in most power supply networks together with other equipment without creating intolerable interference and should lead to an increased acceptance of using AICs.

Nevertheless it has to be highlighted that electromagnetic environment is subject to changes e.g. because of smart grid deployment and that emission limits that are currently under development by the IEC EMC Committees may be different to the maximum emission values recommended in this document.

This document is being issued in the Technical Specification series of publications (according to the ISO/IEC Directives, Part 1, 3.1.1.1) as a “prospective standard for provisional application” in the field of power electronics because there is an urgent need for guidance on the design and use of active infeed converters (AIC) today and in “smart grid environments”.

It remains unclear during revision of this document, how and when the smart grid vision will be realized and to what extent in the future. AICs will be the "key link components" if several electrical energy storage devices or storage technologies and energy users are to be connected together and will interact under "smart grid behaviour" conditions. The power supply network may adapt its future characteristics compared to the state of the art while increasing the installed density of AIC.

POWER ELECTRONICS SYSTEMS AND EQUIPMENT –

Operation conditions and characteristics of active infeed converter (AIC) applications including design recommendations for their emission values below 150 kHz

1 Scope

This Technical Specification IEC TS 62578 describes the operation conditions and typical characteristics of active infeed converters (AIC) of all technologies and topologies which can be connected between the electrical power supply network (lines) a.c. side and a constant current or voltage type d.c. side and which can convert electrical power (active and reactive) in both directions (generative or regenerative).

Applications with active infeed converters are commonly used with the d.c. sides of adjustable speed power drive systems (PDS), uninterruptible power systems (UPS), active filters, photovoltaic systems, wind turbine systems, battery backed power management systems etc. of all voltages and power ratings.

Active infeed converters are generally connected between the electrical power supply network (a.c. side) and a current or voltage d.c. side, with the objective to avoid emitting low frequency harmonics (e.g. less than 1 kHz) by synthesizing a sinusoidal a.c. current. Some of them can additionally compensate the pre-existing harmonic distortion of a given supply side voltage. They are moreover able to control the power factor of a power supply network section by moving the electrical power (active and reactive) in both directions (generative or regenerative), which enables energy saving in the system and stabilizes the power supply voltage or enables coupling of renewable energy sources or electrical energy storage devices to the supply.

A practical and analytical approach for emission values for AICs in power supply networks is given, which is based on the latest results for line impedance values between 2 kHz and 9 kHz and withstand capability of capacitors connected directly to the supply.

This results in design recommendations for emission values below 150 kHz.

The following is excluded from the scope.

- Requirements for the design, development or further functionality of active infeed applications.
- Probability of interactions or influences of the AIC with other equipment caused by parasitic elements in an installation or caused by poor electronic design as well as their mitigations.
- "Overhead line" power supply networks because of lack of information (measurements) of their three phase impedances. This could be the subject for future editions.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050 (all parts), *International Electrotechnical Vocabulary* (available at www.electropedia.org)

IEC TR 60725:2012, *Consideration of reference impedances and public supply network impedances for use in determining the disturbance characteristics of electrical equipment having a rated current ≤75 A per phase*

IEC 61800-3, *Adjustable speed electrical power drive systems – Part 3: EMC requirements and specific test methods*

IEC 61800-5-1, *Adjustable speed electrical power drive systems – Part 5-1: Safety requirements – Electrical, thermal and energy*

IEC 62040-1, *Uninterruptible power systems (UPS) – Part 1: General and safety requirements for UPS*

IEC 62103, *Electronic equipment for use in power installations*

IEC 61000-4-7:2002, *Electromagnetic compatibility (EMC) – Part 4-7: Testing and measurement techniques – General guide on harmonics and interharmonics measurements and instrumentation, for power supply systems and equipment connected thereto*
IEC 61000-4-7:2002/AMD1:2008

CISPR 16-1-1, *Radio disturbance and immunity measuring apparatus – Measuring apparatus*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60500 and the following apply

3.1
active equalization of the power supply network
AEP
ability of an AIC to enable and combine smart grid functionalities with a specific main application

Note 1 to entry: Specific main applications include:

- reduce or avoid emitting low frequency harmonics (e.g. less than 2 kHz) from the power supply network by synthesizing a sinusoidal line current
- contributes to controlling the reactive power of a power supply network
- exchanging the electrical power (active and reactive) in generative or regenerative modes
- stabilization of the power supply voltage and energy saving in the supply system
- exchanging electrical energy between power supply networks or other power generations applications like fuel cells and electrical energy storage devices
- coupling of decentralized power sources (e.g. from renewable energy) to the power supply network.

3.2
a.c. filter
filter consisting of passive components, such as inductors, capacitors and resistors connected to the a.c. side of a converter, designed to reduce the circulation of harmonic currents in the associated system

3.3
active filter
AIC operating as a filter to control the specific a.c. side harmonic and interharmonics voltages or currents usually without active power flow

3.4
active infeed application
application using the properties of an active infeed converter

3.5
active infeed converter
AIC
self-commutated electronic power converters of all technologies, topologies, voltages and sizes which are connected between to the a.c. power supply network (lines) and usually a stiff d.c. side (current source or voltage source) and which can convert electric power in both directions (generative or regenerative) and which can control the reactive power or the power factor

Note 1 to entry: Some of them can additionally control the harmonics to reduce the distortion of an applied voltage or current.

Note 2 to entry: Basic topologies may be realized as a Voltage Source Converter (VSC) or a Current Source Converter (CSC).

Note 3 to entry: In IEC 60050-551 these terms (VSC and CSC) are defined as voltage stiff a.c./d.c. converter (551-12-03) and current stiff a.c./d.c. converter (551-12-04). Most of the AICs are bi-directional converters and have sources on the d.c. side. So, they are known as voltage source converters and current source converters in this TS.

Note 4 to entry: Some kind of AIC might be realized without a stiff d.c. side (a.c. matrix converter). Also a.c. conversion equipment could be included.

3.6
controlled free-wheeling arm
by-pass arm constructed with controllable valve device(s)

3.7
controllable harmonics or interharmonics
set of harmonics or interharmonics which can be influenced directly by the control strategy of the AIC

3.8
conventional converter
converter based on line commutation technology, that cannot control power factor or harmonics

3.9
converter topology
different possible arrangements of semiconductor valves and their connections

3.10
d.c. filter
filter on the d.c. side of a converter, designed to reduce the ripple in the associated system

3.11
d.c. side load
electrical device consuming or generating power connected to the d.c. side

3.12
effective supply-side filter impedance
effective impedance of the supply-side filter of the AIC for frequencies in the range of the controllable harmonics or interharmonics

3.13
evidential per unit supply side impedance of the AIC
$u_{scv,equ}$
per unit short-circuit voltage drop value of the hardware inductance which is connected between the AIC and the power supply network

$u_{scv,equ} = Z_{choke} / (U_{LN} / I_{equ})$

3.14
fundamental and harmonic components
defined in IEC 60050:101, IEC 60050:161 and IEC 60050:551, respectively and are dedicated for the AIC in this document

3.15
F3E-infeed
fundamental frequency front end infeed
fundamental frequency front end voltage source converter with its commutation capacitor on the a.c. side which uses line-frequency switched semiconductor valve devices and has regenerative capability

Note 1 to entry: The d.c.-link capacitor which is normally an electrolytic capacitor is basically replaced by an a.c. line side filter, designed to limit the voltage distortion caused by the PWM currents of the inverter stage

3.16
generated harmonics or interharmonics
set of harmonics or interharmonics which result from the pulse frequency and the pulse pattern

3.17
in-plant point of coupling
IPC
point on a network inside a system or an installation, electrically nearest to the AIC, at which other apparatus are, or could be, connected

Note 1 to entry: The IPC is usually the point for which electromagnetic compatibility is to be considered. In case of connection to the public supply system the IPC is equivalent to the PCC (Point of Common Coupling).

3.18
k_{zred}
ratio of the power supply impedance according to 5.2.4 (95 % values) related to the frequency proportional extrapolated reference impedance according IEC 60725

3.19
line impedance of phase x
$Z_{Lx, h}$
line impedance of phase x at harmonic order h

Note 1 to entry: The impedance at a harmonic frequency between the star point of the equivalent power supply and one of the phase terminals at a defined point on a network. The point on a network could be defined to be for example the terminals of the AIC or the in-plant point of coupling.

3.20

long-time energy storage device
device connected to the d.c.-link directly or by a semiconductor valve device, or a converter, providing rated power for typically seconds to minutes

3.21
neutral impedance at harmonic order h
$Z_{N,\,h}$
impedance between the star point of the equivalent power supply and neutral terminal at a defined point on a network

Note 1 to entry: The point on a network could be defined to be for example the terminals of the AIC or the in-plant point of coupling.

3.22
PWM controlled converter
converter using a pulse-width modulation technique in order to control the switching of its semiconductor valve devices

3.23
pulse frequency
frequency, resulting from the switching frequency and the converter topology, which characterizes, together with the selected pulse pattern, the lowest frequency of non-controllable harmonics or interharmonics at the IPC (in-plant point of coupling)

Note 1 to entry: The switching frequency itself may not be present as a harmonic or interharmonics

3.24
pulse pattern
pattern of the switched voltages or currents, measurable at the terminal of the converter, resulting from pulse frequency and modulation schemes used

3.25
rated apparent power of equipment
S_{equ}
value calculated from the rated r.m.s. line current I_{equ} of the piece of equipment stated by the manufacturer and dependent on the rated interphase voltage U_{LL}

$S_{equ} = \sqrt{3} \times U_{LL} \times I_{equ}$ for balanced three phase equipment

$S_{equ} = U_{LL} \times I_{equ}$ for interphase equipment

$S_{equ} = U_{LN} \times I_{equ}$ for single phase equipment

3.26
reactive power converter
converter for reactive power compensation that generates or consumes reactive power without the flow of active power except for the power losses in the converter

[SOURCE: IEC 60050-551:1998, 551-12-15]

3.27
short-circuit power
S_{SC}
value of the three-phase short-circuit power calculated from the nominal line to line system voltage U_{LL} and the impedance $Z_{Lx,1}$ of the system at the point of common coupling (PCC)

Note 1 to entry: In this case the U_{LL} is the nominal line to line voltage of the power supply network.

$S_{SC} = (U_{LL})^2 / Z_{Lx,1}$

where

$Z_{Lx,1}$ is the supply impedance at the fundamental frequency.

3.28
short-circuit ratio
R_{SCe}
characteristic value for the application of a single equipment derived from the Ratio of short-circuit power of the supply to the rated apparent power of the AIC of the single equipment (S_{equ})

$R_{SCe} = S_{SC} / S_{equ}$ for balanced three phase equipment

$R_{SCe} = S_{SC} /(2* S_{equ})$ for interphase equipment

$R_{SCe} = S_{SC} /(3* S_{equ})$ for single phase equipment

3.29
short-time energy storage device
one or more inductors or capacitors providing rated power for about 1 ms to 10 ms and directly connected to the d.c. side

Note 1 to entry: Short time energy storage is used to have a stiff voltage or current characteristic or operate the AIC continually in short time a.c. voltage dip, and time could be more than 10 ms.

Note 2 to entry: Long-time energy storage is used to provide energy to a.c. power system.

3.30
switching frequency
frequency with which the semiconductor valve devices of a PWM converter are operated

Note 1 to entry: In some converters the switching frequency may not be the same for all semiconductor valve devices.

3.31
total impedance
resulting impedance consisting of the supply impedance and the supply-side filter impedance of the AIC

3.32
$U_{LL, 1}$
fundamental frequency line to line voltage rms value of the power supply network

3.33
$U_{LL, h}$
harmonic line to line voltage rms value of the power supply network

3.34
$U_{LN, h} / U_{LN, 1}$
relative voltage (line to neutral voltage) at order h

Note 1 to entry: ratio of a harmonic line to neutral voltage amplitude to the fundamental frequency line to neutral voltage amplitude

3.35
$U_{LL, h} / U_{LL, 1}$
relative harmonic voltage (line to line) at order h

3.36
$X_{L, h}$
actual resulting reactance of the power supply network at the IPC

Note 1 to entry: The index “h” means in any case that the dedicated reactance is considered at a certain harmonic order.

3.37
$Z_{L,h}$
actual resulting impedance of the power supply network at the IPC

Note 1 to entry: For harmonic calculation for a single phase load: $Z_L = Z_{Lx} + Z_{LN}$ is used. For a three phase load: $Z_L = Z_{Lx}$ is used. The index "h" means in any case that the dedicated impedance is considered at a certain harmonic order.

4 General system characteristics of PWM active infeed converters connected to the power supply network

4.1 General

In this clause, the voltage source AIC, which is used in large numbers, is chosen as the example.

4.2 Basic topologies and operating principles

4.2.1 General

Active Infeed Applications are mainly available with capacitive (VSC) or inductive (CSC) smoothing on the d.c. side. Some converter concepts use no or nearly no d.c.-side smoothing. The majority of installed units utilize capacitive smoothing.

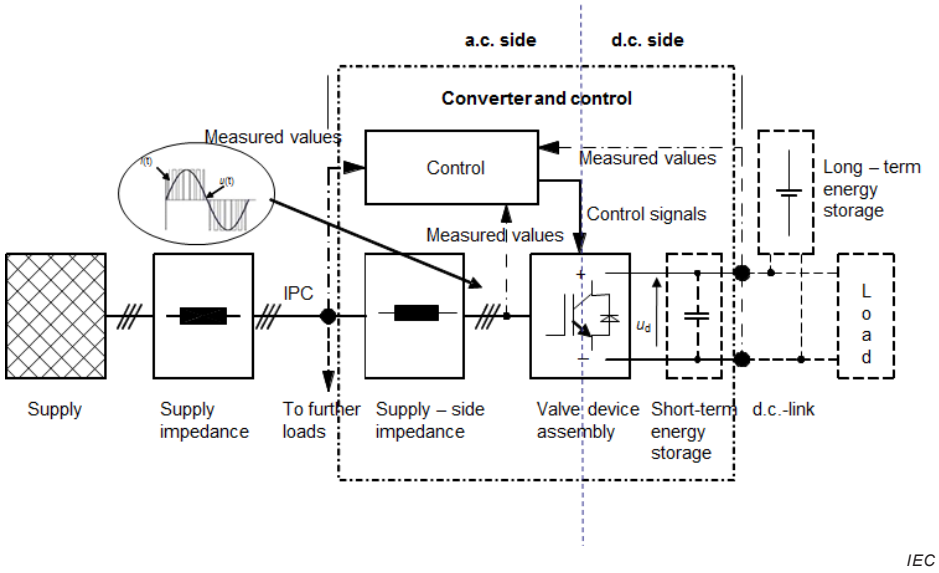
Depending on the rated power and the power supply network availability the connection to the power supply network may be single-phase or three-phase. The three-phase version is selected for the examples.

4.2.2 Operating principles

The main operating principle is to switch the d.c.-side potentials or the d.c.-side currents to the a.c. side conductors with a pulse frequency of normally between 300 Hz and 20 kHz. In this way the desired voltages or currents on the a.c. side are realised as mean values. The pulse frequency is normally high compared to the line frequency and allows quick and accurate control of the voltages and currents on the a.c. side. However, switching between fixed potentials or currents generates undesirable distortions in the high frequency range. Passive a.c-side filters might be required to mitigate those.

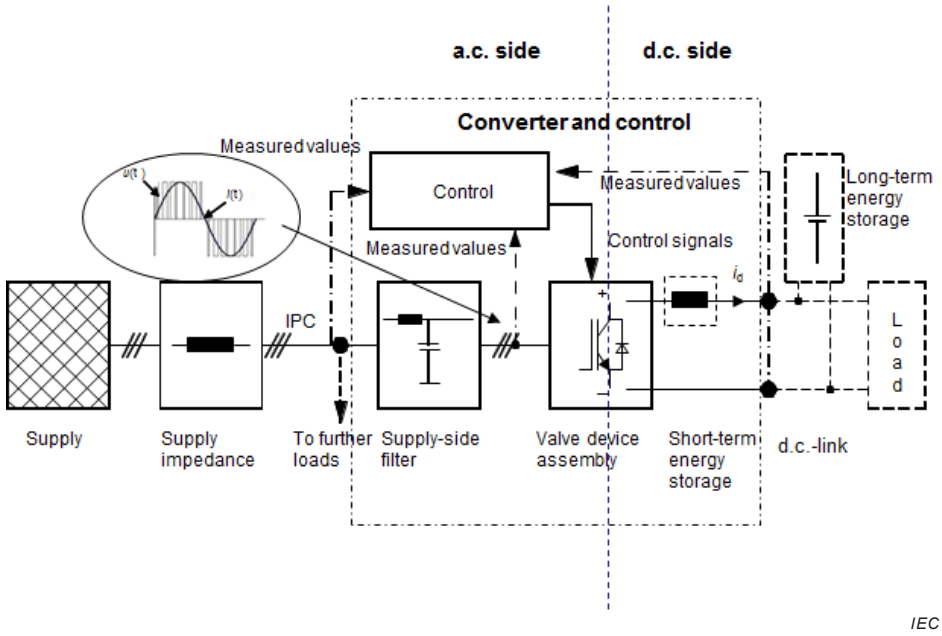
A control system allows a precise control of the fundamental and additional harmonic components. The frequency up to which harmonics can be controlled is determined by the pulse frequency of the converter.

The usual structure of VSC and CSC systems is shown in Figure 1 and Figure 2, respectively:



NOTE The valve device symbols are used merely for illustration.

Figure 1 – AIC in VSC topology, basic structure



NOTE The valve device symbols are used merely for illustration.

Figure 2 – AIC in CSC topology, basic structure

Figure 1 and Figure 2 show that the structure of voltage and current source converter systems is very similar. The main differences can be found on the d.c. side, the a.c. side filters and in the type of semiconductors used for the valve device part of the converter. Details can be found in the sections covering the different topologies.

The structure can be separated into three parts.

- Supply impedance at the internal point of coupling (IPC) (see Figure 2) which is mainly inductive.
- Converter and control up to the d.c. side. This part usually contains an a.c. side filter, typically realized as supply side inductance or an LCL-filter with a T-structure. A converter

transformer, if used, is part of (or designed to be used as) the supply-side filter choke. Next in the chain is the valve device part, which may vary in structure – see the following subclause on different topologies as well as on the d.c.-side load characteristic (capacitive smoothing or inductive smoothing). The control typically uses pulse width modulation principles like space vector modulation, optimised synchronous pulse patterns or hysteresis or sliding mode control for pulse pattern generation. In case of space vector modulation the pulse frequency is fixed. In case of optimised synchronous pulse patterns the pulse pattern normally has a fixed shape and is synchronous with respect to the line frequency.

- Load side. The majority of equipment connected are various energy sources or PWM-converter-fed machines. Another typical application are converters to feed passive or mixed loads, as for example in uninterruptible power systems (UPS). If the AIC is used for power factor compensation or harmonic control the load is not required, but can be included. In case of voltage source converters long-term energy storage units may easily be connected in parallel with the d.c.-side smoothing capacitor. In typical applications the d.c.-side smoothing capacitor supplies the rated power for about 1 ms to 10 ms without tripping of the converter. The long-term storage may typically provide rated power for seconds to minutes.

4.2.3 Equivalent circuit of an AIC

The stationary behaviour of AICs is best described using the equivalent circuit consisting of equivalent sources and impedances given in Figure 3.

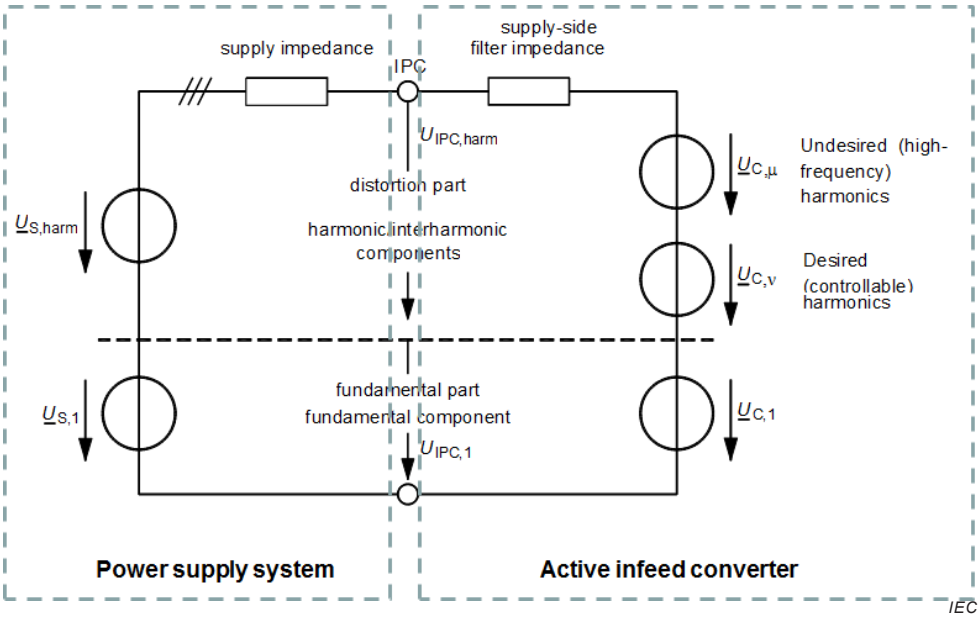


Figure 3 – Equivalent circuit for the interaction of the power supply network with an AIC

For better understanding it is advantageous to separate the power supply network voltages and the converter voltages into their fundamentals and the remaining harmonics. For the converter voltages, two sets of harmonic voltages may be distinguished.

- One set of harmonics which can be controlled directly. This set is defined as controllable or desired harmonics and characterised by the index ν.
- One set of harmonics results from the pulse frequency and the pulse pattern. This set is defined as undesired (generated) harmonics and characterised by the index μ.

The voltage $U_{s,\,h}$ is the superposition of all (desired and undesired) harmonics caused by all loads.

NOTE Similar conclusions can be drawn concerning current source AICs. In this case the set of voltages in Figure 3 has to be replaced by a set of currents.

4.2.4 Filters

The supply side filter is usually designed to let the desired harmonics pass through the filter and to mitigate the undesired harmonics to a value prescribed by the EMC specifications of the environment. If necessary, additional filter measures may be applied.

Additional design criteria may result from the power-supply system conditions at the IPC as well as from economic constraints.

It should be noted that the frequency of the undesired harmonics is mainly from pulse frequency on upward. The specification of the converter-side filter inductor has to take these high frequencies into account, otherwise the inductor will overheat.

The d.c.-side filter, if used, has to attenuate the ripple of the d.c. voltage or current so that the converter and the possibly connected devices function properly. The specification of the d.c.-link filter has to take the amount of harmonics into account, otherwise it may overheat

In some cases the energy-storage capability of the d.c.-side filter is adapted to the dynamic requirements of the application. One application is the ride-through (continue operation during and after a short interruption of the power supply network). Rapid changes of the energy flow in the power supply network or the load during power transients also need larger d.c. side energy storage elements otherwise the characterising d.c.-link quantity (voltage or current) may leave the tolerance band in which proper operation of the PWM converter is guaranteed. An overshoot of voltage or current, even for a very short time, may destroy the semiconductor valve devices of the converter.

For the fundamental frequency and the controllable harmonics, the supply-side filter may be regarded as purely inductive. Depending on the topology and the chosen control principle, the voltage drop across the total impedance drives the supply-side current.

The total impedance should be limited to allow proper dynamic control of the supply side current.

4.2.5 Pulse patterns

The selected pulse pattern generation scheme greatly influences the characteristics of the converter. The three main basic pattern generation schemes are space vector modulation, optimized synchronous pulse-width modulation and line flux guidance.

NOTE Space vector modulation and symmetric pulse width modulation lead to identical pulse patterns.

In case of space-vector modulation a sequence of zero states and non-zero voltage space vectors is selected in such a way that the voltage space vector requested by the control results as a mean value of the sequence. The zero states selected have to be of equal duration.

In case of symmetric pulse-width modulation, a set-point curve is compared to a triangular reference function. Two ways of treating the set-point curve are known:

- natural sampling directly compares the (analogue) curve to the triangular reference function;
- regular sampling samples values of the set point curve at the extreme values of the triangular function and compares these sampled values to the reference function.

Digital controllers normally use regular sampling. The difference between the two methods is small but leads to slightly different generated harmonics.

A suitable instantaneously defined zero-sequence component added to the reference values assures equal zero-state duration. This is sometimes called “addition of multiple of third order harmonic". If the half value of the mean of the three phase signal is added to all signals, the result is identical to space vector modulation.

4.2.6 Control methods

A basic introduction into control methods is described in Clause A.1. More detailed description can be found in the references.

4.2.7 Control of current components

The AIC gives the possibility to adjust the fundamental and controllable harmonic components fed into or taken from the line. This feature effectively can be used for mitigation purposes. As a secondary effect, high frequency distortion is generated, which might have to be mitigated by a suitable filter.

The line voltage given by Figure 3 is normally unknown, as is the line impedance that may change without notice, depending on the actual line configuration, including other loads attached. Therefore, control schemes are usually based on the measurable voltage at the IPC (see Figure 1 and Figure 2). In addition, d.c. link quantities are measured.

The flexibility of AICs and associated control schemes offer a large variety of applications and associated control schemes. The main objectives are, however, control of active power and control of reactive power or non-active (vector sum of reactive plus harmonics) power. The desired behaviour can be achieved by controlling the currents caused by the AIC. References for the active, reactive, non-active and purely harmonic currents have to be derived from the line voltages.

One possibility to define the reference for the current is to use resistive load emulation. Energy is then fed to the d.c. link from every available supply voltage component, thus adding damping for undesirable components. If the voltages at the IPC are non-sinusoidal, the line currents will be consequently non-sinusoidal, too.

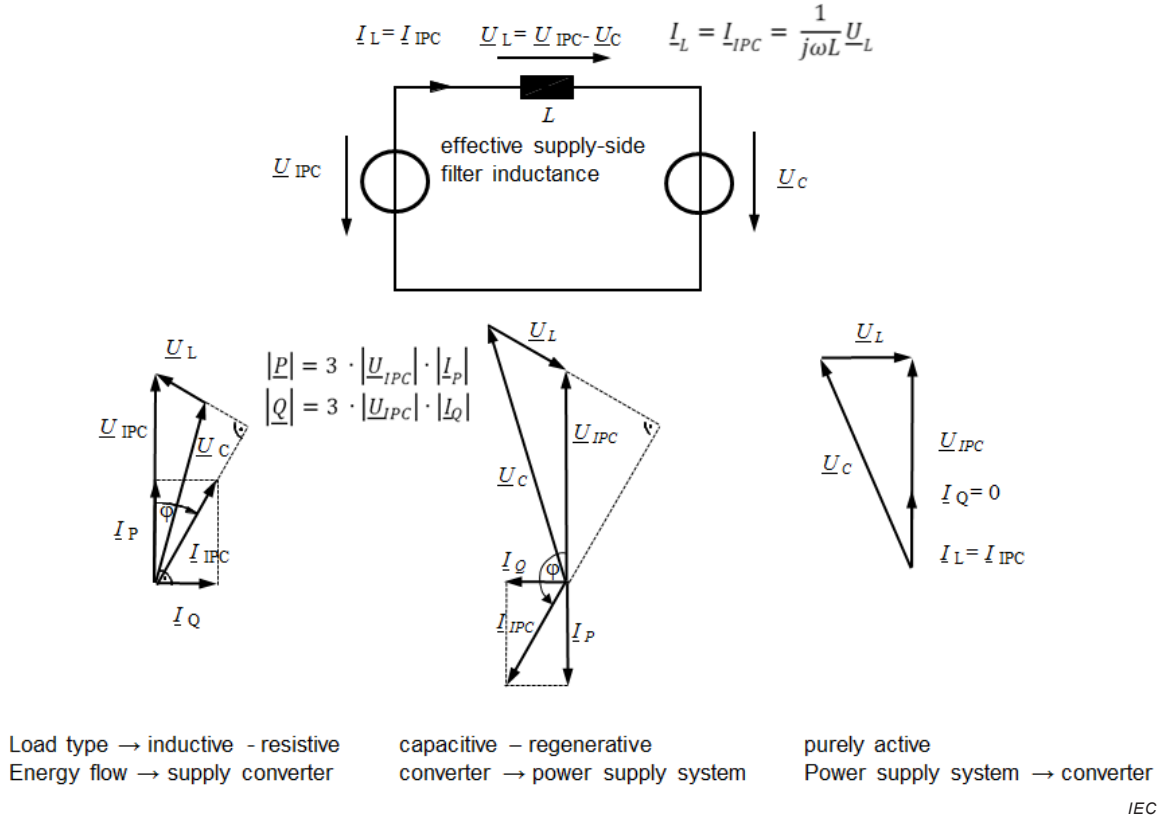
The drawback of resistive load emulation is that it may become unstable and increase harmonics if an attempt is made to feed energy to the supply from the d.c. link. In this case energy should be delivered to the supply only via the fundamental component of the current.

4.2.8 Active power factor correction

This consideration is based on fundamental frequency components described by vectors.

Adequate control of the line-side converter voltage $\underline{U}_C$ allows the voltage $\underline{U}_L$ across the effective supply-side filter impedance to be adjusted to a desired value. This voltage then causes the desired line current $\underline{I}_L$ to flow. In this way the AIC is able to impress any desired amount of reactive current, including zero – and cause any desired amount of reactive power, including zero – inside its specifications. The converter can thus be used as a compensator to maintain a certain voltage level in the a.c. side supply by additionally impressing capacitive or inductive currents.

For an ideal active power factor correction the currents of the filter inductances are orthogonal (they lag or lead by 90°) to the respective supply voltages. Examples of vector diagrams are shown in Figure 4.



NOTE PCC in this case can also be replaced by IPC.

Figure 4 – Voltage and current vectors of line and converter at fundamental frequency for different load conditions

It is obvious that the line-side converter voltage has to be larger than the voltage at the IPC in many cases, depending on the operation point. This has to be taken into account when specifying rated values for the converter. As mentioned above, further reserves are needed for dynamics.

4.3 AIC rating

4.3.1 General

The required AIC ratings are an accumulation of requirements of several origins like sinusoidal conditions, harmonic currents and dynamic conditions.

4.3.2 Converter rating under sinusoidal conditions

The worst-case condition for operation is with rated current, purely capacitive, at the maximum allowed level of the voltage at the IPC. In this case the converter still has to deliver the peak value of line-side converter voltage required instantaneously. Otherwise the amount of capacitive current has to be limited or the line currents will not be as desired.

4.3.3 Converter rating in case of harmonic currents

In addition to the rating discussed for sinusoidal condition in the preceding section, further requirements follow from harmonic currents control. The equivalent circuit diagram (Figure 4) remains valid.

Each desired current harmonic requires an additional voltage at the effective supply-side filter impedance. The superposition principle is applicable. Therefore, all required voltages can be

added. Depending on the phase angle of the harmonic current, the instantaneously required peak value of the converter voltage varies. As a worst-case rating, all peak values of voltage resulting from the fundamental and all desired harmonics have to be added to the peak value of the voltage at the IPC for maximal instantaneous converter voltage. If the rating of the converter does not allow handling this voltage, line currents will not be generated as desired.

In special cases, where the voltage at the IPC contains many harmonics, the peak value of the voltage at the IPC including worst-case superposition of harmonics has to be used for the rating of the converter.

4.3.4 Converter rating under dynamic conditions

The equivalent circuit (Figure 4) still remains valid. However, now the currents in the effective supply-side impedances have to be changed dynamically. This requires a certain amount of voltage across these impedances. This voltage has to be supplied by the converter. Depending on the desired dynamic performance the rating of the converter has to be matched to allow large enough instantaneous values of the AIC voltages.

5 Electromagnetic compatibility (EMC) considerations for the use of AICs

5.1 General

In this clause a selection of EMC aspects is covered. The selection is done in order to choose the appropriate AIC functionality with the provision that there should be no disturbing interference at the power supply network with other equipment.

Moreover the active equalization of the power supply network by using an AIC will be described as well as the typical side effects by using an AIC.

The determination of the power supply impedance in the range between 2 kHz and 20 kHz, the typical withstand capability of power capacitors and other equipment and the displacement of resonance frequencies in the power supply network are considered. This leads to the recommendation of design guidelines for emission values of AICs in the range of 2 kHz up to 150 kHz.

Emission and immunity are given in the relevant product standards e.g. IEC 61800-3 in the case of Power Drive Systems or IEC 62040-2 for Uninterruptible Power Systems.

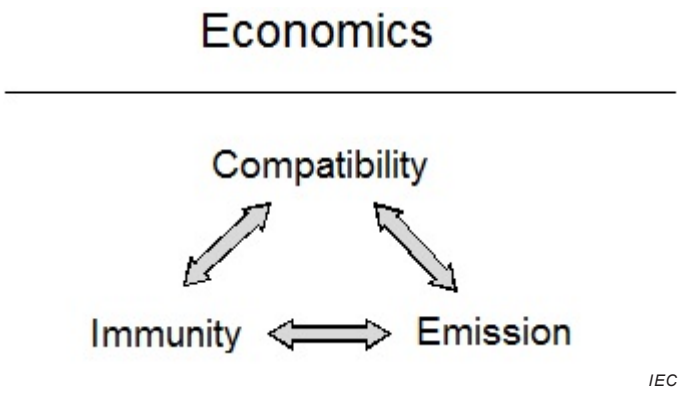


Figure 5 – The basic issues of EMC as tools of economics

The minimum required immunity of electric apparatus, the compatibility levels in the power supply network and the maximum allowed emission of disturbances are directly related to each other. All of them are subject to economic considerations (see Figure 5).

The acceptance of the recommended design guidelines for emission values between 2 kHz and 150 kHz will allow widespread use of AICs in multiple applications for the control of electrical energy in the context of the Smart Grid and Energy Efficiency initiatives.

In the frequency range between 2 kHz to 9 kHz a system of multiple AICs can be designed to meet the emission values at the PCC. This allows the use of cancellation techniques when multiple AICs are used together.

This approach might also be considered above 9 kHz. However, it may be less valid near 150 kHz, due to radiated effects.

5.2 Low-frequency phenomena (<150 kHz)

5.2.1 General

Low-frequency EMC phenomena mainly occur due to conductive, inductive and capacitive coupling of the power supply network to the neighbouring networks and also due to interference between devices connected to the supply network.

Harmonics, voltage fluctuations, voltage dips and commutation notches are part of the low-frequency power supply related phenomena. However, voltage fluctuations and commutation notches are significantly reduced compared to conventional converters.

AICs generate distortion with frequencies originating from the switching of the semiconductor valve devices which have to be sufficiently mitigated by the supply-side filter of the AIC (see Figure B.2).

The power supply network's impedance and short-circuit ratio R_{SCe} have a decisive impact (see 5.2.3.2) on the filter performance. The supply system, its configuration and the load have to be considered together in the evaluation. Thus technical possibilities for the limitation of emissions have to be analysed individually for each application.

If several AICs are connected to the same supply system it has to be noted that the resulting voltage distortion will be lower or equal to the distortion caused by one big equivalent AIC due to the random superposition.

It has to be noted that non-sinusoidal input current is not only generated by distortion of the AIC, but as well by non-sinusoidal supply voltage, causing parasitic currents flowing through applied capacitive input filters.

Measuring quantities at the d.c.-side connections and/or at the supply-side filter is a challenging task. Measuring equipment with a bandwidth of ten to twenty times the pulse frequency is required in case harmonics need to be measured.

See additional information in Annex B.

5.2.2 Emerging converter topologies and their advantages for the power supply network

Figure 7 and Figure 8 show the technological progress and the main milestones of different topologies (see Figure 6) with impact on the power supply network by presenting their typical wave shapes for power supply current distortions and voltages.

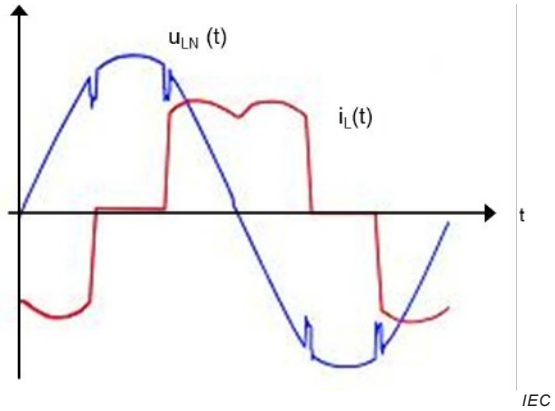


Figure 6 – Typical power supply network current i_L(t) and voltage u_{LN}(t) of a phase controlled converter with d.c. output and inductive smoothing

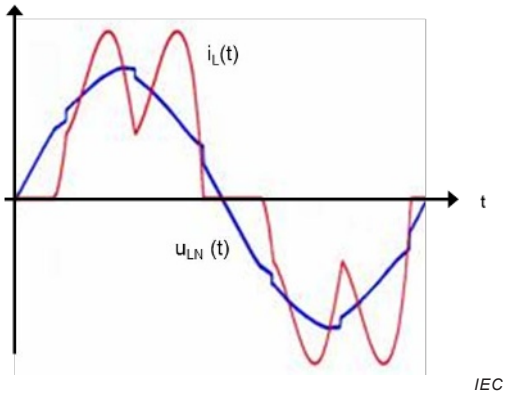


Figure 7 – Typical power supply network current i_L(t) and voltage u_{LN}(t) of an uncontrolled converter with d.c. output and capacitive smoothing

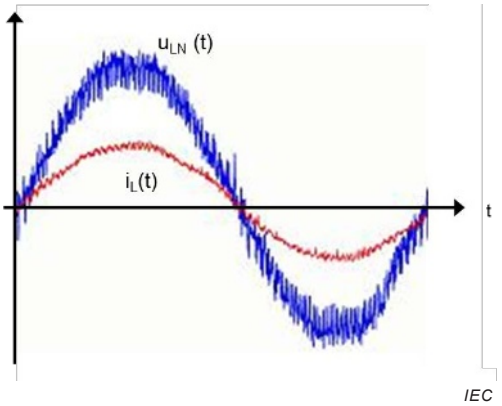


Figure 8 – Typical power supply network current i_L(t) and voltage u_{LN}(t) of an AIC realized by a PWM Converter with capacitive smoothing without additional filters

With the emerging technology development, the approach towards an ideal sinusoidal wave shape of the equipment input current (which had been a goal since long time) has been more closely achieved.

5.2.3 Active equalizing of the power supply network

5.2.3.1 General

An AIC is able to supply active and reactive power (capacitive or inductive) in both directions (4-quadrant operation). Thus if the AIC is correctly rated the user can apply a dynamic reactive power compensation without additional compensator facilities. Figure 9 shows an example of attainable active and reactive power of the AIC at different line voltages.

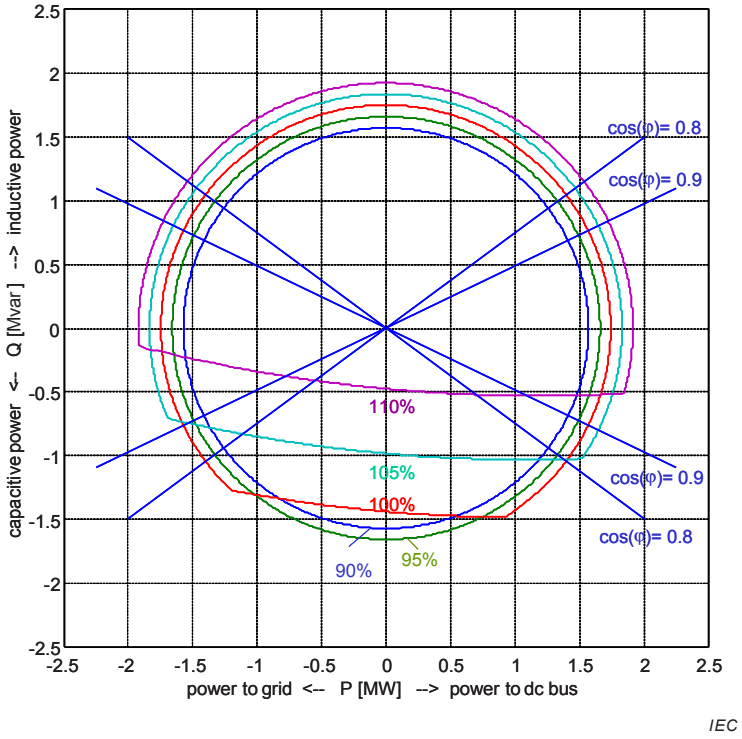


Figure 9 – Example of attainable active and reactive power of the AIC (VSC-type) at different line to line voltages in per unit (with 10 % combined transformer and filter inductor short-circuit voltage, X/R ratio = 10/1, d.c. voltage = 6,5 kV)

For an AIC based on PWM technology, virtually no harmonic current distortion occurs below the pulse frequency unless they are generated intentionally for the purpose of eliminating particular harmonic components (see 4.2.7).

In this case the converter will generally improve the quality of the power supply network (active equalizing of the power supply network) by compensating low frequency harmonics to a desired extent. Further, pre-existing disturbances may be even mitigated by such converters equipped with an appropriate control system and/or higher order filters. A significant portion of harmonic currents at the IPC may be caused by the background distortion of the power supply network voltage.

The different harmonics can be calculated using Fourier analysis and reduced or compensated by separate controllers. An example of a so called active filter is shown in Figure 11 for three phase loads but the method is also applicable to single phase cases.

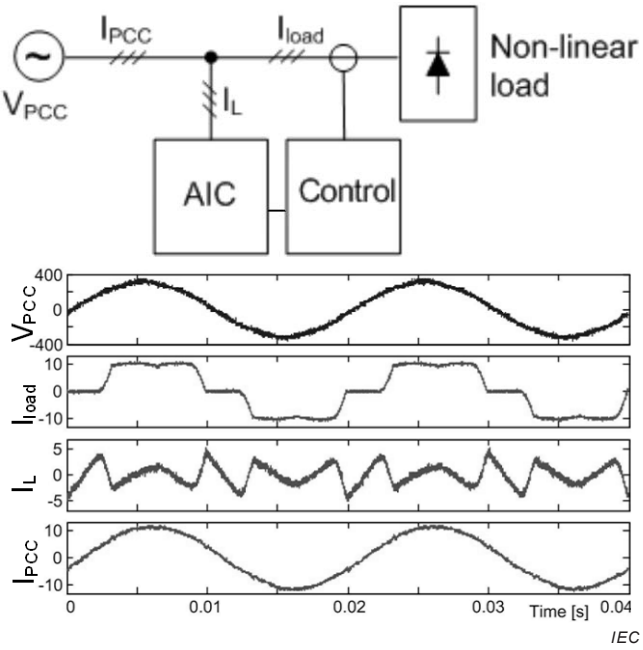


Figure 10 – Principle of compensating given harmonics in the power supply system by using an AIC and suitable control simultaneously

5.2.3.2 Typical side effects

As a typical side effect of the active compensation with the switching action of the semiconductor valves in the AIC, harmonic distortion may occur near the pulse frequency and at integer multiples of it.

NOTE 1 The following text refers to two-level topology according to Clause 6. In case of the application of three-level or multilevel technology, the voltage distortions are substantially lower.

Contrary to a phase controlled bridge with current source characteristic (conventional converters), the voltage waveform of an AIC (VSC) on the supply side of the bridge is determined by the switching action of the semiconductor valves and the voltage of the d.c. link capacitor, see Figure 10. Furthermore, the pulse pattern is fairly independent of the load of the converter.

Due to this characteristic the voltage distortion caused in the power supply network depends on the pulse pattern applied and the voltage sharing between the impedance of the power supply network and the impedance of the supply-side filter of the AIC. When a simple L-filter is used and the capacitances and resistances of the supply system are ignored, this causes the highest distortion. Figure 11 and formulae (1), (2) and (3) show the formation principle of the distortion in the line-to-line and line-to-neutral voltage generated by an AIC with an L-filter and assuming that the supply impedance is inductive.

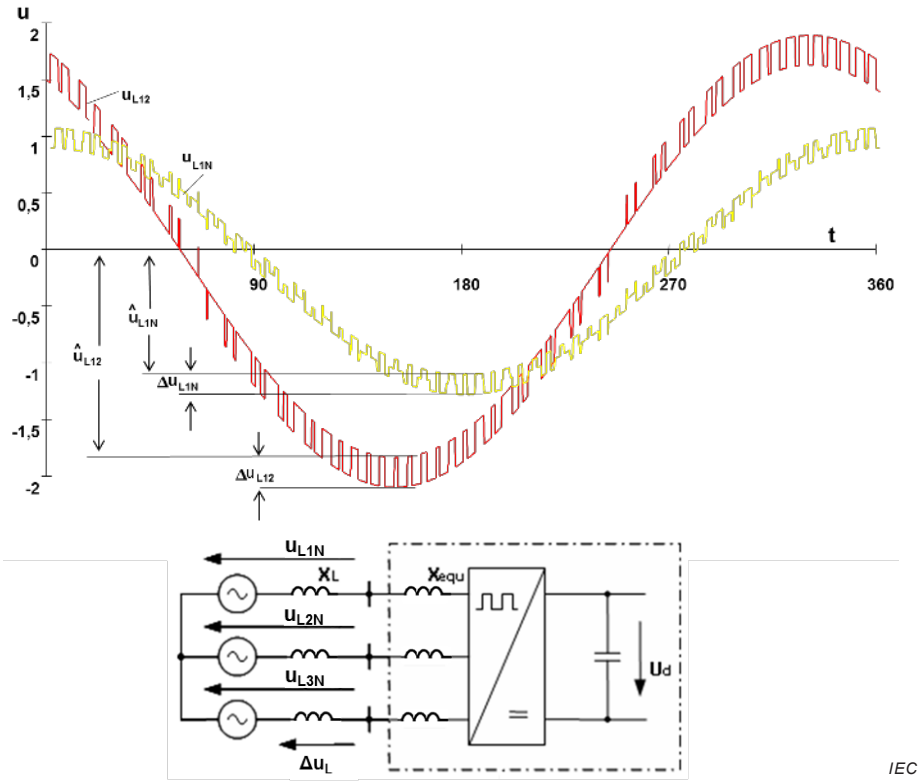


Figure 11 – Typical Voltage Distortion in the Line-to-Line and Line-to-Neutral Voltage generated by an AIC without additional filters (u in % and t in degrees)

$$\frac{\Delta U_{\mathrm{L1N}}}{2 \cdot \hat{U}_{\mathrm{L1N}}} = \frac{1}{3} \cdot \frac{U_{\mathrm{d}}}{\hat{U}_{\mathrm{L1N}}} \cdot \frac{X_{\mathrm{L}}}{X_{\mathrm{L}} + X_{\mathrm{equ}}} \tag{1}$$

$$\frac{\Delta U_{\mathrm{L12}}}{2 \cdot \hat{U}_{\mathrm{L12}}} = \frac{1}{2} \cdot \frac{U_{\mathrm{d}}}{\hat{U}_{\mathrm{L12}}} \cdot \frac{X_{\mathrm{L}}}{X_{\mathrm{L}} + X_{\mathrm{equ}}} \tag{2}$$

typically:

$$\frac{U_{\mathrm{d}}}{\hat{U}_{\mathrm{L12}}} \approx 1{,}1 \text{ and } \frac{U_{\mathrm{d}}}{\hat{U}_{\mathrm{L1N}}} \approx 1{,}1 \cdot \sqrt{3} \tag{3}$$

Taking into account the frequency dependency of the network impedance according to Figure 27, Formula (2) changes to Formula (4). In order to evaluate the expected distortion in the supply system, it is advisable to use the short-circuit power ratio R_{SCe} for calculation.

$$\frac{\Delta U_{(\mathrm{L1–L2})}}{2 \cdot \hat{U}_{(\mathrm{L1–L2})}} \approx \frac{1}{2} \cdot 1{,}1 \cdot \frac{X_{\mathrm{h}}}{X_{\mathrm{h}} + u_{\mathrm{scv,equ}} \cdot R_{\mathrm{sce}} \cdot h \cdot X_{\mathrm{L1}}} \tag{4}$$

Using the formula for k_{Zred} according to 3.18:

$$k_{\mathrm{Zred}} = \frac{X_{\mathrm{h}}}{h \cdot X_{\mathrm{L1}}} \tag{5}$$

The formula changes to:

$$\frac{\Delta U_{(L1–L2)}}{2 \cdot \hat{U}_{(L1–L2)}} \approx \frac{1}{2} \cdot 1{,}1 \cdot \frac{X_h}{X_h + u_{scv,equ} \cdot R_{sce} \cdot \frac{X_h}{k_{Zred}}} \tag{6}$$

Dividing by X_h leads to:

$$\frac{\Delta U_{(L1–L2)}}{2 \cdot \hat{U}_{(L1–L2)}} \approx \frac{k}{1 + u_{scv,equ} \cdot R_{sce} \frac{1}{k_{Zred}}} = f\left(k; u_{scv,equ}; R_{SCe}; k_{Zred}\right) \tag{7}$$

In the example given in Figure 11 the pulse frequency is 3 kHz, short-circuit power ratio of R_{SCe} = 100 and the supply-side L-filter inductor $u_{SCV,equ}$ = 6 % (referenced to the base impedance of AIC $Z_B = U^2_{nominal}/S_{equ}$, thus X_{equ} = 0,06 R_{SCe} X_L).

With these values the amplitude of the 3 kHz-ripple in the line-to-line voltage is approximately 1,3 %. Figure 12 shows the typical pulse frequency voltage distortion in the power supply network depending on R_{SCe} and $u_{SCV,equ}$ for an AIC (PWM type; 2-Level) with a pulse frequency of 3 kHz and passive mitigation provided by an L-filter.

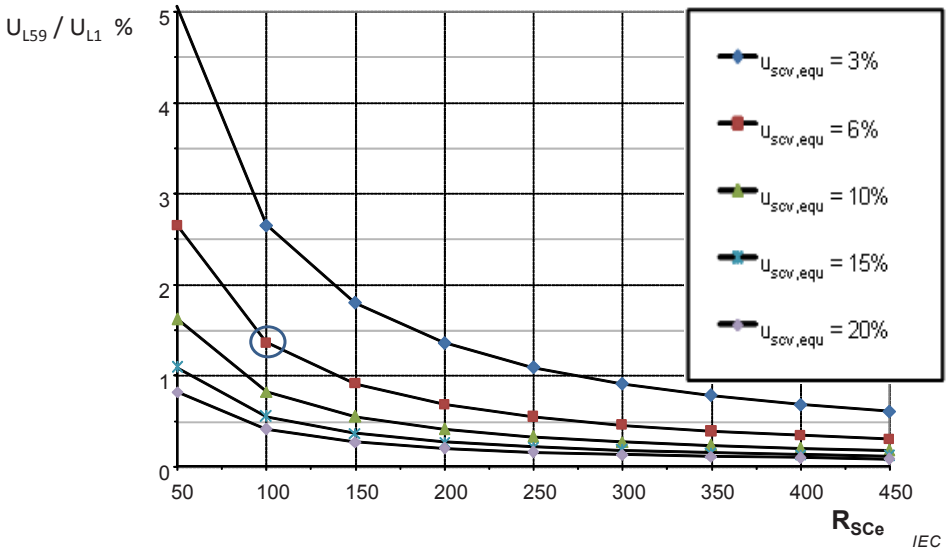


Figure 12 – Basic characteristic of the relative voltage distortion (59th harmonic) of one AIC operated at a pulse frequency of 3 kHz versus R_{SCe} with the line impedance according to 5.2.4

Regarding the side effects on the power supply network it is furthermore remarkable for AICs that the supply impedance plays a more important role in the harmonic current distortion than it does with the conventional converters. The impact is greater with smaller filter reactances. An example of this is shown in Figure 13 for the L-filter case.

The consequence of this characteristic is that harmonic current distortion of the equipment is lower with a weak power supply network than with a stronger one. Therefore calculations based on the current distortion of the equipment measured in a strong power supply network may exaggerate the estimated voltage distortion in a weak power supply network.

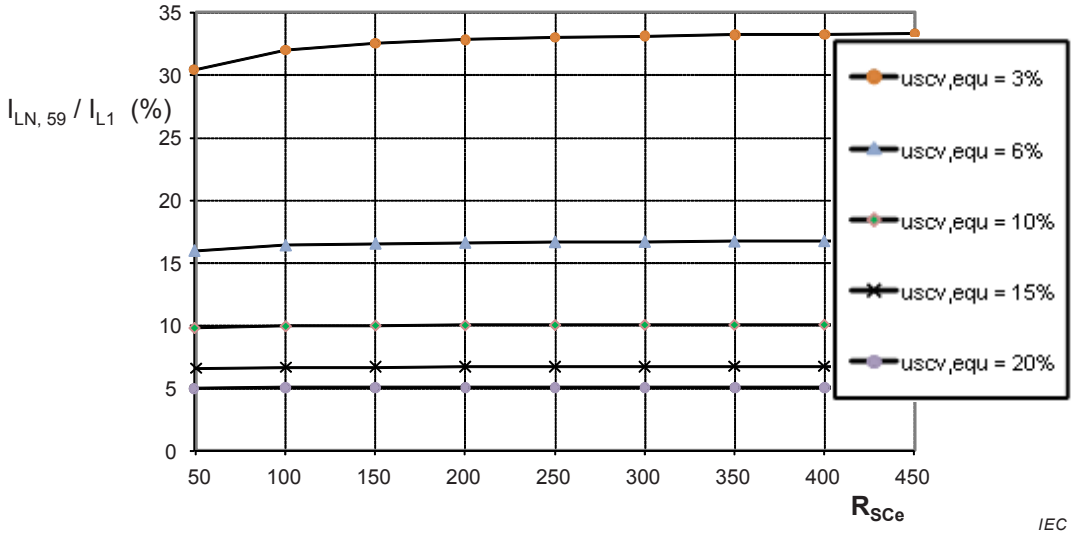


Figure 13 – Basic characteristic of the relative current emission (59th harmonic) of one AIC at a pulse frequency of 3 kHz versus R_{SCe} with the line impedance according to 5.2.4

However, in spite of the fact that the harmonic current distortion decreases with higher supply impedance the impact of the more unfavourable voltage sharing ratio predominates and may result in an excessive voltage distortion level. Therefore additional filter measures might be needed when AICs are connected in particular to the public power supply network.

Several different filter configurations can be applied, all with the aim to reduce the voltage distortion at the pulse frequency and its side bands. Figure 14 shows the three most used state of the art differential mode line filter solutions for VSC. The simplest filter is the L-filter, as described before. An alternative with better filter efficiency and less line frequency voltage drop is the LCL filter. As a power supply network side inductor L_2, the stray inductance of a transformer may be used. If no active damping in the control is implemented, a passive damping as shown in the damped trapped LCL-filter topology of Figure 14 might be necessary. To increase the damping of a constant pulse frequency ripple further, a trapped LCL filter may be used. With a third inductor a series resonant circuit for the pulse frequency is built. A decrease of the filter performance for pulse frequency multiples should be considered.

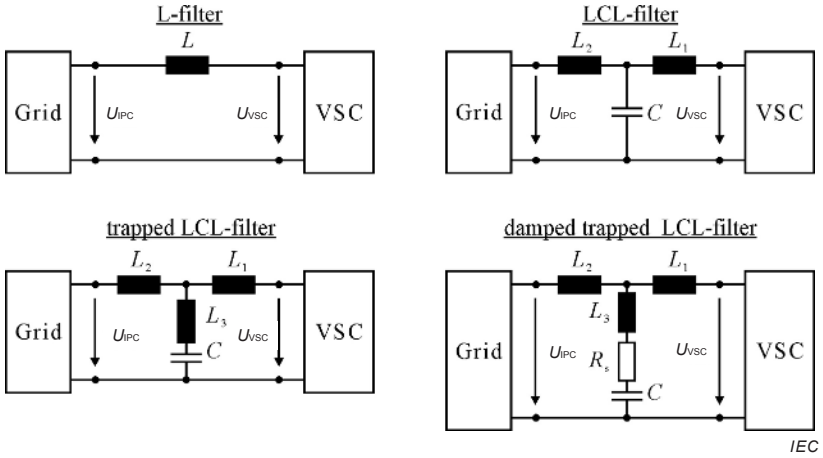


Figure 14 – Single phase electric circuit of the three commonly used differential mode passive line filter topologies for VSC and one example for passive damping

As an example, Figure 15 shows the attenuation of the VSC line to line voltage to the line to line voltage at the IPC. The power supply network is hereby assumed to be resistive-inductive with R_{line}=40 mΩ and L_{line}=100 µH. The filter characteristics are

- L-Filter: L = 4mH
- LCL-Filter: L_1=1mH; L_2=1mH; C=4,7µF
- LCL-Filter (trapped): L_1=1mH; L_2=1mH; L_3=54µH; C=4,7µF
- LCL-Filter (damped and trapped): L_1=1mH; L_2=1mH; L_3=54µH; C=4,7µF; R_S=10Ω

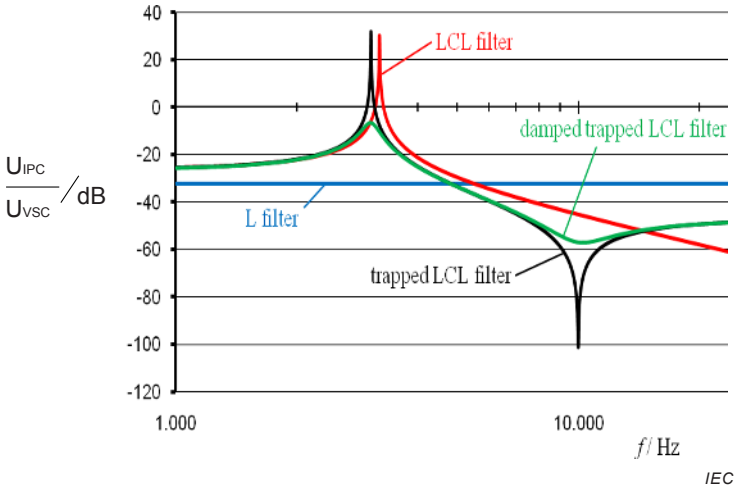


Figure 15 – Example of the attenuation of the VSC line to line voltage to the line to line voltage at the IPC with state of the art differential mode passive line filter topologies

NOTE 2 Especially for L-filters the across the lines (X-) capacitors of any additional EMI filters might be taken into account in the filter design, because they may have a considerable effect on the filter performance.

The design of filter circuits for an AIC has to take into consideration that an undesirable resonance with the power supply network's impedance may appear below the tuned resonance frequency of the filter arrangement which may lead to an unintentional increase of the supply impedance in the lower frequency range. An example of this can be seen in Figure 15 around 2 kHz. As a result of this effect, resonances may arise if conventional converters with significant harmonic distortion at lower frequency are connected on the same power supply network with an AIC.

A practical example is shown in Clause A.7.

In such cases it may be necessary to add damping circuits to the additional filter arrangements. In this way the effect of this resonance is reduced, see Figure 15, green curve. Instead of passive damping circuits, that increase losses and decrease the filter effect, a damping function may be included in the AIC control. However, this kind of active damping requires that the filter resonance frequencies are less than half of the pulse frequency.

5.2.4 Measured power supply network impedances in the range between 2 kHz to 20 kHz

The values of the power supply network impedances in the range of the pulse frequency of an AIC and its harmonics might have significant influence on the conducted emissions of an electric or electronic device.

In a dedicated research project, the power supply network impedances at the IPC in various industrial and public supply systems in Central Europe have been examined. The aim was to determine the statistical distribution of the power supply network impedances up to 20 kHz.

On the one hand this will help to design robust and affordable supply side filters for the AIC and on the other hand the results are useful for the definition of emission levels of AICs.

The studies were performed at several sites in North, Central and South Germany and Northern France over three years. At each measurement location, the power supply network impedances were determined in intervals of one hour. In general, each determination required a whole day measurement (see [1][1]). For explanations of different possible methods see A.8.

All examined networks had a rated voltage of 400 V and all were cable networks. The following results are not valid for overhead lines.

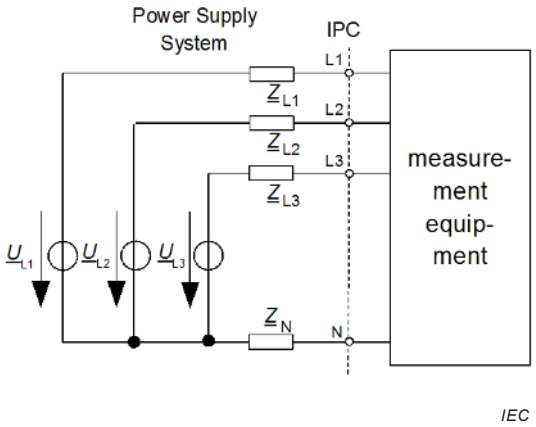


Figure 16 – Connection of the power supply network impedance measurement equipment

Figure 16 shows the connection of the measurement equipment to the power supply network. The measurement equipment provides measurements of up to 20 kHz of:

- the complex line to neutral impedance $\underline{Z}_{L1N}$ to $\underline{Z}_{L3N}$ and their mean value
- the complex line to line impedances $\underline{Z}_{L12}$ to $\underline{Z}_{L31}$
- the complex positive-sequence impedances Z_{pos}

Figure 17 shows the impedance characteristic of a low-voltage transformer under no load condition. This basically corresponds to the leakage reactance.

1 Numbers in square brackets refer to the bibliography.

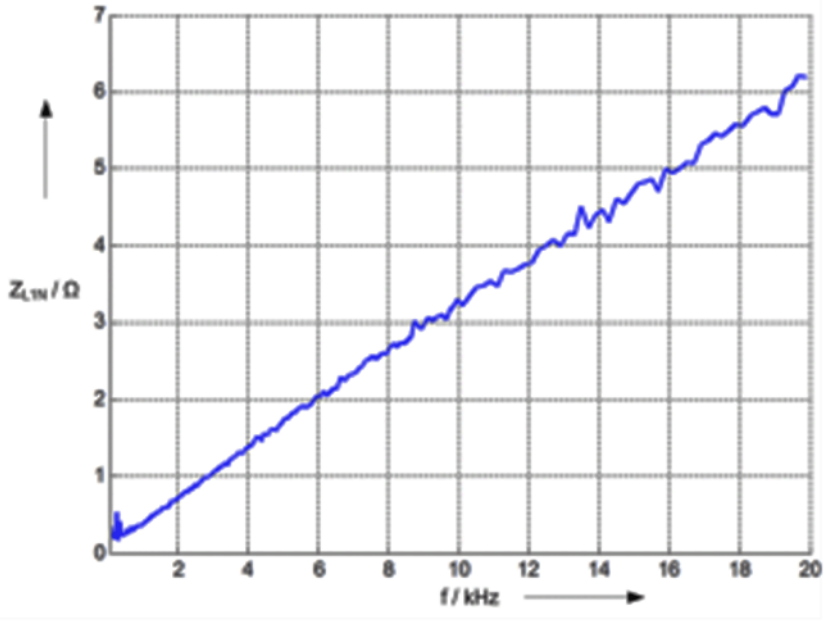


Figure 17 – Example of the measured impedance of a low-voltage transformer under no load condition S = 630 kVA, u_k = 6,08 %

In Figure 18 an example of a power supply network impedance measurement over a whole day is given where the variation of the impedance can be examined.

In the daytime hours when many loads are connected to the power supply network, the impedance is considerably low. During the night, the impedance tends to increase. It can be seen that the power supply network impedances sometimes doubles during the night as a result of loads being switched off. Significant differences between day and night were found in nearly half of all the measured supply systems. The differences are more significant at higher frequencies (> 6 kHz) than at lower frequencies.

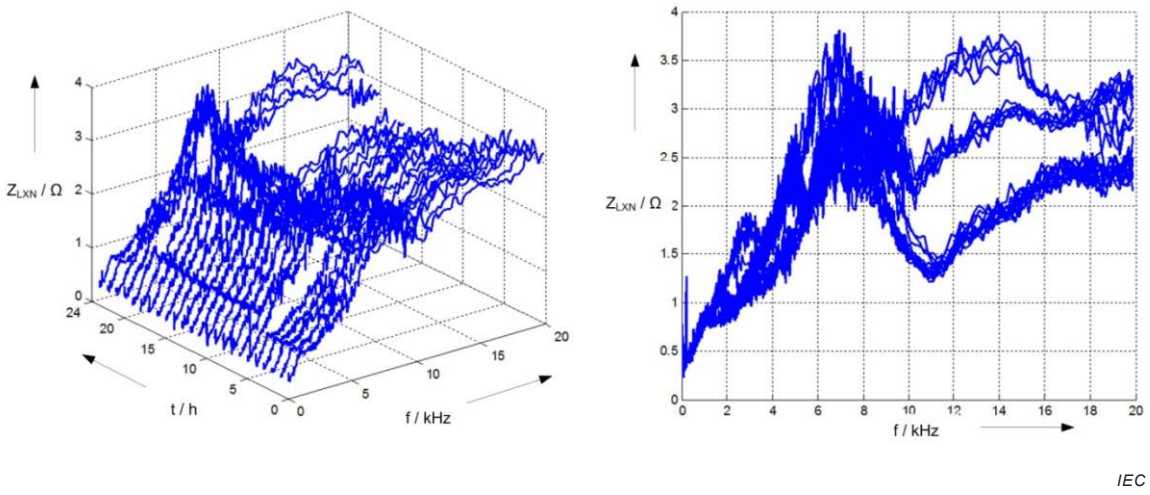


Figure 18 – Measured variation of the power supply network impedance over the course of a day at one location

Especially loads with power-electronic circuits on the supply side and corresponding capacitive filtering influence the system impedance. In Figure 19, a supply system with a

negative imaginary part is shown i.e. the power supply network behaves capacitive for a certain frequency range.

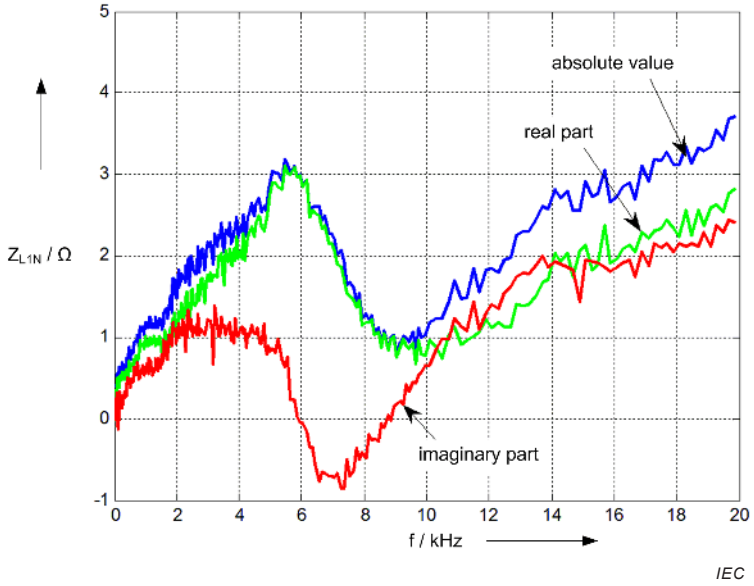


Figure 19 – Power supply network impedance with partly negative imaginary part

Approximately 20 % of the measured power supply networks showed a capacitive (negative) imaginary part of the power supply network impedance for the inspected frequency range.

The impedances shown in Figure 18 and Figure 19 were measured between the phase and the neutral conductor and are representative examples only. Therefore an evaluation of the statistical distribution of the power system impedance for the respective frequency is presented in Figure 20. For this purpose, measurements have been carried out at 25 different measurement locations (North, Central and South Germany and Northern France) and, from them, over 1 300 graphs were recorded.

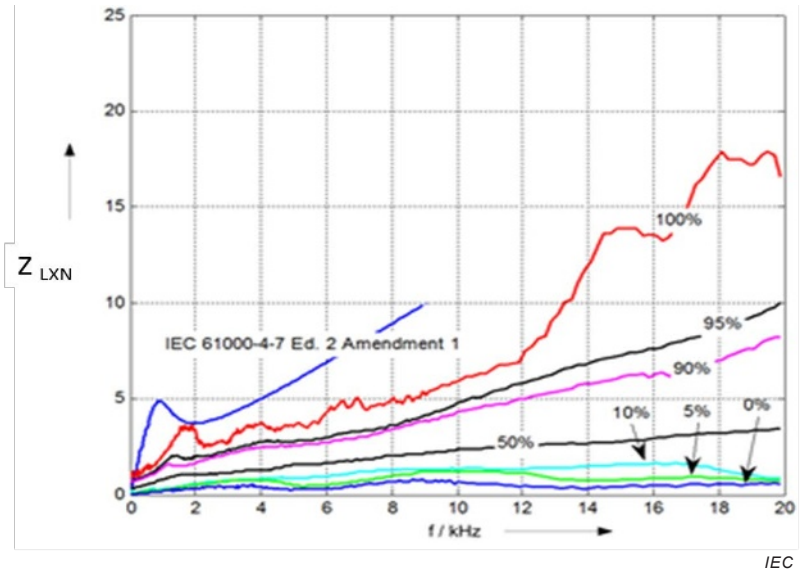


Figure 20 – Distribution of power system impedance (measured between phase and neutral conductor) in low-voltage systems versus frequency

The displayed 100 % curve in Figure 20 is the envelope over all power system impedance curves. It is composed of all maximum values for each frequency control point. The 0 % curve is composed of all minimum values for each frequency. The 50 % curve, for example, shows the impedance value for every frequency; whereby 50 % of the measured power systems have higher impedance and 50 % lower impedance.

The impedance curve of the LISN (Line Impedance Stabilization Network) derived from IEC 61000-4-7 for harmonics and interharmonics measurement is also shown in Figure 20.

According to Figure 20, the measured impedances are considerably below the impedance curve given in IEC 61000-4-7:2008 which demonstrates that using this impedance curve for frequencies up to 9 kHz would lead to overestimation of distortion.

Above 9 kHz the standardized impedance according to CISPR 16-1-1 applies.

The impedance between phase and neutral conductor is mainly important for single-phase loads, whereas for balanced three-phase loads, without a connected neutral conductor, the impedance at the individual phases is relevant.

A measure of this is the impedance in the positive-sequence system. This positive-sequence system and the negative sequence system are identical in most power systems. This had been confirmed by [2] as well as by the measurements carried out.

The positive-sequence impedance is the ratio of voltage to current in the positive-sequence system.

The impedance in the zero system is irrelevant for these specific analyses and in the case of three-phase devices without a connected neutral conductor.

In the case of symmetrical impedance values, the following applies:

$$\underline{Z}_{\mathrm{pos}}(j\omega) = \underline{Z}_{\mathrm{L1}}(j\omega) = \underline{Z}_{\mathrm{L2}}(j\omega) = \underline{Z}_{\mathrm{L3}}(j\omega) = \underline{Z}_{\mathrm{L}}(j\omega) \tag{8}$$

NOTE 1 In the case of asymmetrical impedance values, the impedance matrix contains secondary elements [2]. In typical supply systems these elements can be ignored, because they are much lower than the diagonal elements, and only the diagonal elements can be used to calculate the positive sequence impedance.

The statistical evaluation of the positive-sequence impedance values resulted in the following.

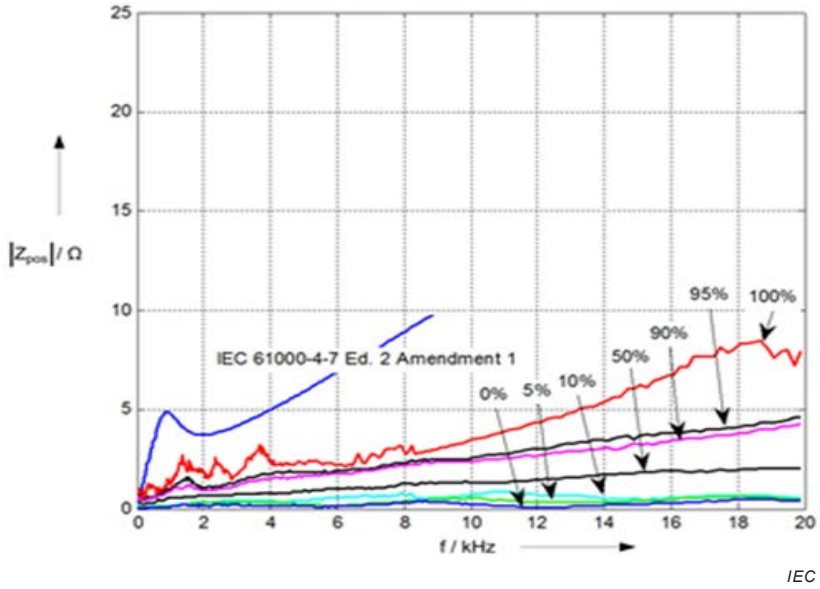


Figure 21 – Statistical distribution of positive-sequence impedance versus frequency in low-voltage power supply networks

Figure 20 and Figure 21 show, that on the average, the levels in the positive-sequence system $|Z_{pos}|$ are about 50 % lower than the impedance $|Z_{LxN}|$ between phase and neutral.

In IEC 61000-4-7+, the impedance of the neutral conductor has been set to zero, which would mean that $Z_{pos} = Z_{LxN}$; which is nearly twice the value of the line impedance.

The impedances of the LISN IEC 61000-4-7+ displayed in Figure 20 and Figure 21 are higher than all measured impedance levels between a phase and the neutral conductor and are also considerably higher than all measured levels of the positive sequence impedance.

There are also significant differences of the power system impedance with respect to public and industrial power supply networks.

In addition, it shall be noted that resonances occur more frequently in the range below 10 kHz. Due to the network impedance most resonances are expected in the range between 1 kHz and 4 kHz.

As the measuring results show, the system impedance curves do not have a proportional increase with the frequency whereas they display a steep increase in the range below 2 kHz. Above 2 kHz, the slope decreases considerably. The power system impedance in the frequency range from 2 kHz to 9 kHz is therefore not to be approximated by means of linear extrapolation with the 50 Hz impedance.

NOTE 2 As an example: The 50 Hz impedance value of the 90 % curve in Figure 21 is about 0,75 Ω. The impedance value at 9 kHz is about 3,1 Ω or 4,2 times 0,75 Ω. A former linear approximation of the 50 Hz impedance to 9 kHz would have led to a value of 10 Ω which is inadequately too high.

5.2.5 Proposal of an appropriate line impedance stabilisation network (LISN) from 2 kHz to 9 kHz

5.2.5.1 General

In order to predict system perturbations by means of simulations, analytical models of power system impedance are necessary. In this subclause a model that can be used for simulation is shown in Figure 22.

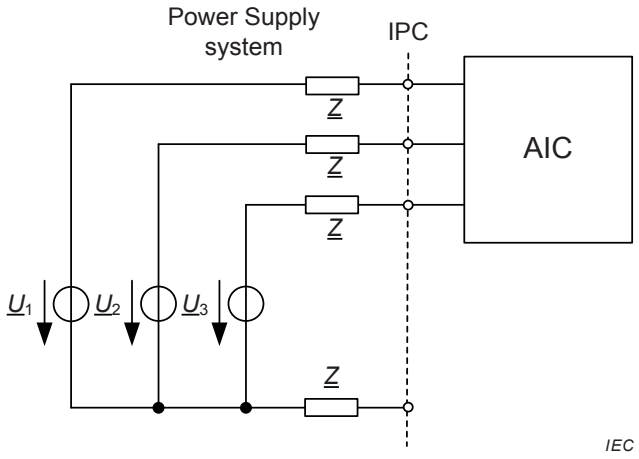


Figure 22 – Equivalent circuit describing the power supply network impedance

The impedance values Z need to be each simulated by components. The more components are used for Z, the more accurately the impedance may be simulated but the greater the computing power needed for the simulation and the less practical is the realization of such a network.

As a consequence, a useful compromise between accurate simulation of the measured curves and the computing power needed for this has been found in the topology according to Figure 23.

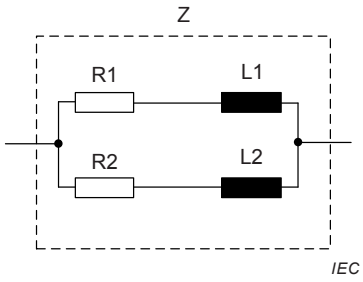


Figure 23 – Circuit topology for power system simulation

The impedance Z is calculated as follows:

$$\underline{Z}(\omega; R_1; L_1; R_2; L_2) = \frac{1}{\frac{1}{(R_1 + j\omega L_1)} + \frac{1}{(R_2 + j\omega L_2)}} \quad (9)$$

Formula (9) represents the trial function in the sense of regression analysis. It can be seen that the trial function is non-linear and complex.

Table 1 – Parameters of line impedance stabilisation network for different power system impedance curves

Curve	R_1 / Ω	R_2 / Ω	L_1 / µH	L_2 / µH
10 %	0,10	0,55	12,0	0,5
50 %	0,49	2,55	30,9	13,0
90 %	1,07	7,07	51,0	21,1
NOTE The parameters in Table 1 were verified by means of matching with the corresponding impedance curves such as the one in Figure 20 for the 50 % curve.				

The approximated impedance curves are shown in Figure 24 together with the measured 50 % impedance curves and the curves are in good agreement in the frequency range between 2 kHz and 9 kHz.

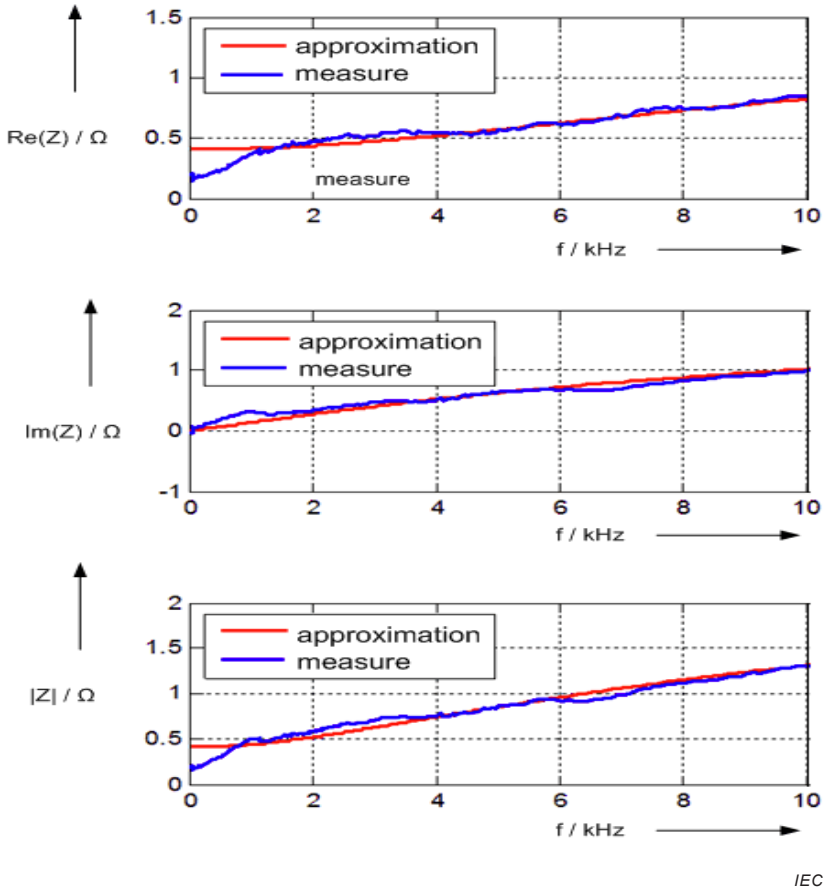


Figure 24 – Approximated and measured 50 % impedance curve

5.2.5.2 Single Phase LISN for the 2 kHz to 9 kHz frequency range

For measurements of distortion, LISNs are necessary, whereas for currents above 200 A the availability might be very limited. In contrast to a simulation model, real LISNs do not only provide defined power system impedance but also form the link to the power system for the fundamental and ensure decoupling from the power system for all harmonics.

IEC 61000-4-7 proposes the following circuit topology for a LISN.

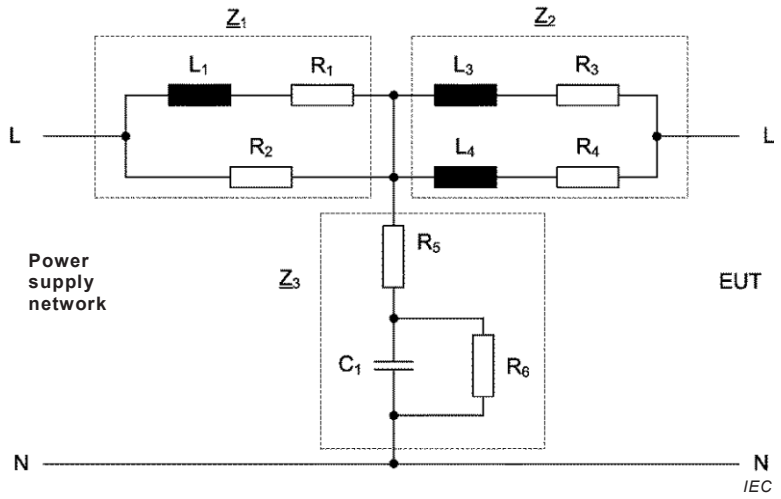


Figure 25 – Single phase circuit topology according to IEC 61000-4-7+ used for line impedance stabilisation network

The line impedance stabilisation network shown in Figure 25 is only applicable to single-phase application and it provides considerable high impedance values which do not match the practical power system impedance values.

Table 2 – Parameters of the LISN described in Figure 25 and Figure 26

R_1 / Ω	R_2 / Ω	R_3 / Ω	R_4 / Ω	R_5 / Ω	R_6 / kΩ	L_1 / µH	L_3 / µH	L_4 / µH	C_1 /µF
0,02	0,8	0,38	7,03	1	10	100	44,2	22,1	50

To be able to practically realize a LISN, the component tolerances must be specified. Resistors usually have a 1 % tolerance and are not critical.

Magnetic components and capacitors usually have tolerances of 5 % to 10 %, which can obviously influence the impedance curve. Because of the high damping of the proposed LISN, resonance effects are not expected.

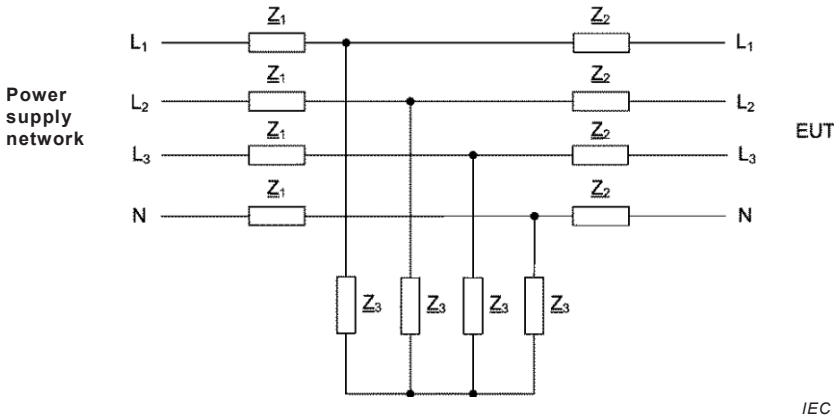
In worst case, with a tolerance of 10 % (Cs and Ls), the deviation from the curve of Figure 27 is 7,5 %. This can lead to 0,6 dB higher or lower distortion levels. With a tolerance of 5 % the deviation would be just 0,3 dB.

The associated impedance curves are shown in Figure 20 and Figure 21. The components R_1, L_1, R_2 , R_5, R_6 and C_1 are used for coupling and decoupling purposes and only have a minor influence on the impedance of the line impedance stabilisation network, whereas L_3, R_3, L_4 and R_4 provide the defined power system impedance for the 2 kHz to 9 kHz frequency range considered here.

5.2.5.3 Three-phase LISN for the 2 kHz to 9 kHz frequency range

To extend its use to three-phase devices and to distribute the impedances to the three phases and the neutral conductor, the following topology is therefore proposed in Figure 26, the verification is given in Figure 27. The assigned values of Z_1, Z_2 and Z_3 are taken from Figure 25 and Table 2.

For AICs with a rated current above 100 A, the inductance values of L_1, R_1, L_3, R_3, R_4 and L_4 may be reduced by the factor I_{equ} / 100 A.



NOTE The assigned values of Z_1, Z_2 and Z_3 are taken from Figure 25 and Table 2.

Figure 26 – Three-phase circuit topology for the line impedance stabilisation network

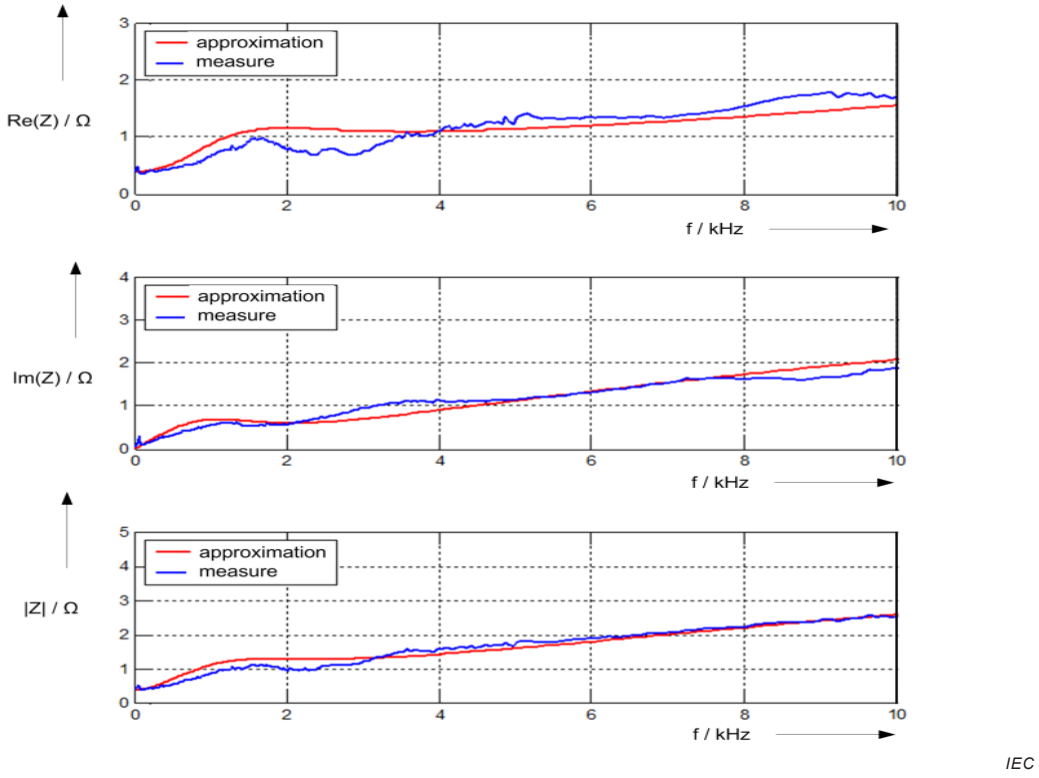


Figure 27 – Impedance variation in the 90 % curve of the LISN described in Figure 26

5.2.6 Effects on industrial equipment in the frequency band 2 kHz to 9 kHz

5.2.6.1 General

In order to determine the immunity of industrial equipment in the frequency band 2 kHz to 9 kHz, various equipment has been tested with a 2 kHz, 5 kHz or 9 kHz voltage superimposed on the fundamental frequency with amplitude of 2 %, 5 % and 10 % of the fundamental.

The following equipment has been investigated:

- industrial power supplies with following topologies: single phase industrial power supply 230 Va.c./24 Vd.c., without PFC; single phase industrial power supply 230 Va.c./24 Vd.c., with PFC; three phase industrial power supply 400 Va.c./24 Vd.c.;

- EMI filters (common-mode and differential mode);
- transformers;
- power drive systems with following topologies: no inductors and large d.c. capacitance; line inductors: d.c. inductors.

The immunity against disturbances in the 2 kHz to 9 kHz range was observed from a functional and thermal point of view. The effect of resonances was not considered in industrial power supply networks.

Distortion in the 2 kHz to 9 kHz frequency band cause additional currents caused by the EMI filter capacitors. At 9 kHz and 10 % amplitude the current can reach values up to ten times the rated current of the power supply. This can cause tripping of the internal or branch fuses. The internal thermal losses in the capacitors have not been found significant, although this cannot be generally ruled out (see B.1.3).

Increase of the d.c. link voltage is possible in resonant conditions. The control of the voltage is not affected by distortion in this frequency band. No significant changes in the efficiency of the power supply have been observed.

Multiple zero-crossing commutations can be observed in the diode rectifier. These may lead to temperature increase at amplitudes of 5 % or 10 %.

5.2.6.2 EMI filters

The capacitors used in EMI filters may cause additional capacitive currents if distortion in the frequency band 2 kHz to 9 kHz is present. The amplitude of the capacitive currents can reach values that exceed the nominal current of the installed equipment. This may cause tripping of fuses or circuit breakers (see also B.1.3).

Resonances may also occur but these have not been investigated because various EMI filters have different resonance frequencies.

5.2.6.3 Transformers

The transformer in the test was not susceptible to disturbances in the inspected frequency band between 2 kHz to 9 kHz with amplitudes up to 10 %. No significant additional iron losses could be measured. No significant acoustic noise could be measured. This cannot be generally ruled out, because the behavior of the transformer depends on its design. Some audible noise emissions in other transformers have been noticed even with low amplitude between 2kHz and 9kHz due to mechanical resonances (see 5.4).

5.2.6.4 Power drive systems

Three different power drive system (PDS) topologies using IGBT semiconductor switches have been investigated:

- PDS with large d.c. capacitance (Figure 28),
- PDS with large d.c. capacitance and line inductors (Figure 29),
- PDS with large d.c. capacitance and inductors in the d.c.link (Figure 30).

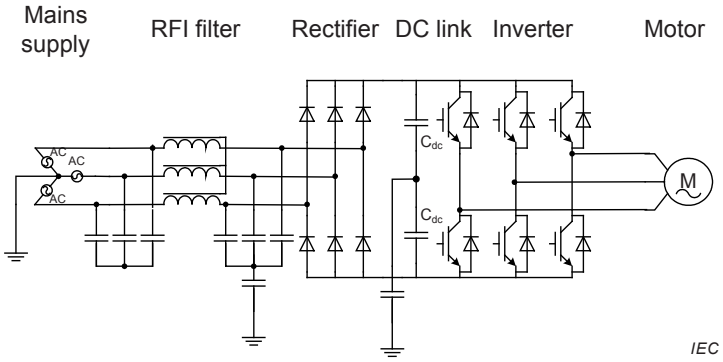


Figure 28 – PDS with large d.c. capacitance

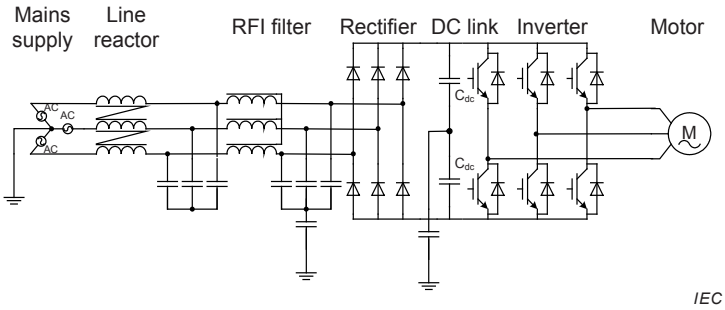


Figure 29 – PDS with large capacitance and line inductor

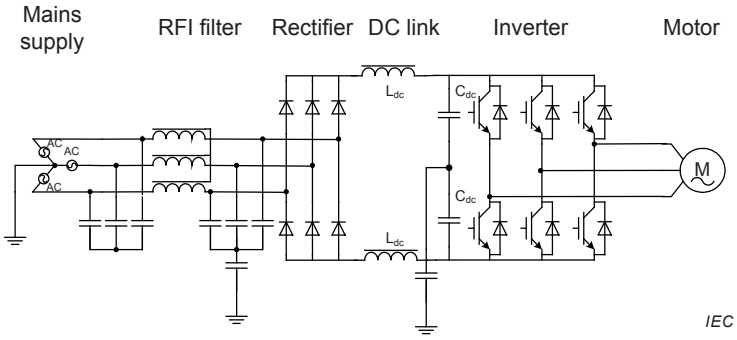


Figure 30 – PDS with a large d.c. capacitance and inductors in the d.c. link

5.2.6.5 PDS with a large capacitance

The d.c. link voltage can be slightly boosted, the maximum boost being observed at 2 kHz and 10 % amplitude: 9 % boost of the d.c.-link voltage.

Multiple zero crossing commutation of the rectifier is observed. This effect is attenuated at higher frequencies and is not observed anymore at 9 kHz.

The current through the capacitors of the EMI filter is increased by the disturbance, as explained in Clause A.6.

5.2.6.6 PDS with a large capacitance and line inductors

When line inductors are used the immunity of the PDS is increased in loaded conditions. However, for the measured example in stand-by mode the d.c.-link voltage was boosted by the distortions in the 2 kHz to 9 kHz frequency band. The worst case was observed at 2 kHz

with 10 % distortion. In these conditions the d.c.-link voltage is boosted by 28 %. At 2 % distortion the d.c.-link voltage has been boosted by 4,8 % (see also Clause A.5).

5.2.6.7 PDS with a large capacitance and d.c.-link inductors

In the case of the observed PDS with a large capacitance and d.c.-link inductors the d.c.-link voltage is slightly boosted.

The worst-case has been observed in this special case at 2 kHz and 10 % amplitude. In this case the d.c.-link voltage has been boosted by 5,9 %.

5.3 High-frequency phenomena (> 150 kHz)

5.3.1 General

To reduce interference (differential/symmetrical mode and common mode/asymmetrical mode), the choice of adequate components and methods should be used in order to find an economical solution.

5.3.2 Mitigation of distortion

The reduction of the common mode distortion of AICs is similar to the distortion suppression of switch mode power supplies. However, due to the bigger size of the AICs the capacitive currents are higher and thus adequately sized mitigation components are required. Further, correct grounding and shielding of the supply cables is important.

The mitigation of the differential mode high frequency interferences may be incorporated with the harmonic filter components (see Figure 32). However, care has to be taken in the design of the filter components in order to preserve their low frequency properties in the high frequency range.

5.3.3 Immunity

The radio frequency filtering or protection has to be constructively provided at the input of the device, in the device itself and at the output towards the load. Usually the distortion inside the AIC is much higher than the distortion from external sources. Thus the cross-coupling from internal power cabling to signal cabling should be avoided. Signal inputs and outputs should be protected by galvanic separation or separated power supplies.

5.3.4 EMI filters

In the absence of EMI filters, the high frequency distortion levels can reach values that exceed 120 dBμV. EMI filtering is necessary in most applications in order to comply with the required limits.

NOTE The use of EMI filters can have an incompatibility effect with residual current device (RCD) protection devices because of increased leakage currents.

In order to achieve an EMC-reasonable solution, the combination of following mitigation techniques is needed: filtering, grounding and shielding. Figure 31 and Figure 32 show a basic EMI filter topology and block diagram which are commonly used for those applications.

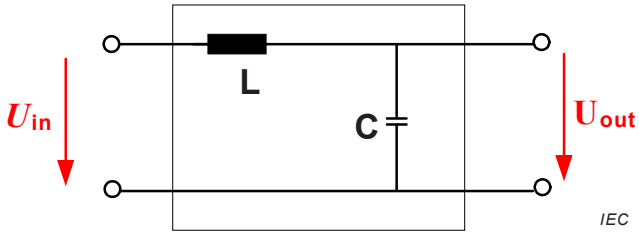
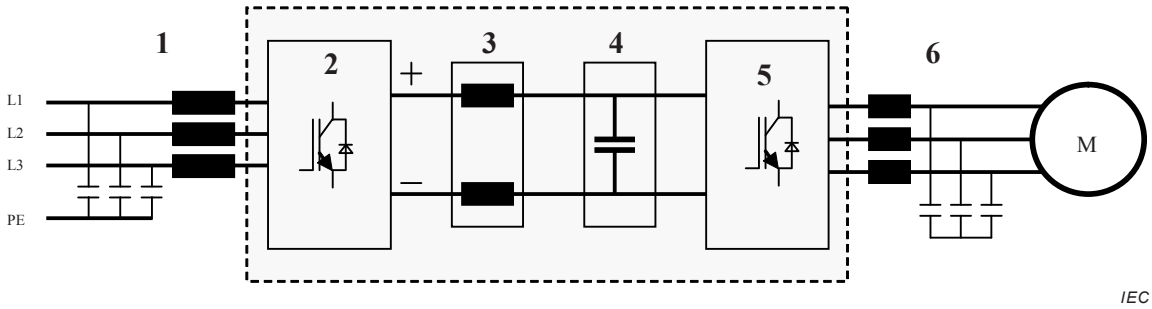


Figure 31 – Basic EMI filter topology



1. EMI-filter or choke
2. Supply-side converter (AIC)
3. common mode chokes
4. d.c.-link capacitors smooth the d.c.-voltage
5. Motor-side converter
6. Output chokes or filter

Figure 32 – Block diagram of a PDS with high frequency EMI filter system

5.4 Audible noise effects

Due to the voltage distortion, an increase in audible noise of different electrical equipment (i.e. small plug in power supplies, chokes in fluorescent lamps, incandescent lamps, glass-ceramic cooker tops) connected to the same power supply networks may occur.

Together with implementing of appropriate filtering measures to mitigate the voltage distortion, the filtering measures would come along with decreasing the audible noise.

NOTE The audible noise emission is often a consequence from amplification of solid bodies like of resonances in musical instruments even at very low levels of excitation. Noise problems can be mostly solved by improvement of mechanical issues. In PDS this problem had been solved just by adapting the switching frequency.

5.5 Leakage currents

Because of impedances between energized parts and earth, such as capacitors connected between the power supply network conductors and earth in EMI filters, or stray capacitances between power supply networks conductors and earth in shielded power cables, the leakage currents might be above 3,5 mA. Therefore fixed and redundant earth connection might be required (see IEC 61800-5-1 for PDS).

Residual current devices (RCD) are usually not compatible with non-residential equipment.

5.6 Aspects of system integration and dedicated tests

The electrical and thermal safety of converters of this type is tested according to the relevant product standards.

In view of the requirements for AICs with regard to protection against electric shock it has to be considered that VSCs in particular are usually equipped with large d.c.-link capacitors which store the electric energy even after disconnection from the supply. Therefore appropriate measures have to be provided in order to discharge the capacitors after switching off the AIC. Performance of the discharge should be checked by recalculation of the stored energy, or measurement of the capacitors voltage at 1 s to 5 s after switching off of the AIC.

For aspects of system integration, IEC 62103 applies.

The following type tests are recommended to be made for AICs additionally to established tests for uncontrolled rectifiers:

- operational behaviour at asymmetrical line voltages;
- turn-off in case of supply over and under voltage;
- operational behaviour in the case of single-phase and three-phase supply voltage interruptions and short dips;
- short-circuit at the AIC power ports equipment to turn-off in case of over- current);
- turn-off with maximum current and highest reference value of the d.c.-link voltage (d.c.-link voltage shall not rise to inadmissible values);
- disconnection from the electrical power supply network during energy recovery.

Further tests may be required but are under consideration.

6 Characteristics of a PWM active infeed converter of voltage source type and two level topology

6.1 General

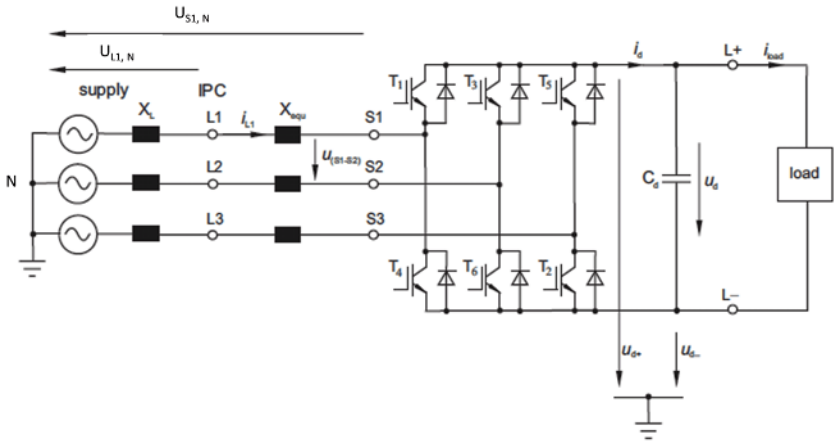
This clause is about the special properties of two level PWM voltage source AIC.

6.2 General function, basic circuit topologies

Two level PWM voltage source AICs usually use pulse frequencies between 1,5 kHz and 16 kHz. They are capable of four-quadrant operation and can control a sinusoidal line current of any phase angle. Active and reactive power can be controlled independently of each other. Active filters can also be realized with the same circuit. Because of the generative power ability, the good control possibilities as well as the small line interference they are used with frequency converters for drives, wind-power systems as well as an improved technology alternative to uncontrolled rectifiers.

Figure 33 shows the basic topology of a two level PWM voltage source AIC. It consists of a supply side reactance X_{equ}, the electronic valve devices and the d.c. link capacitor C_{d}. The load can be any circuit with d.c. voltage input, e.g. a chopper or a machine-side converter. Active filters normally do not have load. The electronic valve devices connect the d.c. voltage U_{d} to the supply phases L1 to L3. Reactances X_{equ} separate the instantaneous values of the supply and the converter input voltages.

A minimum value of the reactance ($X_{\mathrm{L}} + X_{\mathrm{equ}}$) between supply voltage and converter input is required for proper function. Additional filter components (see 5.2.3.2 and 5.2.6.2) are necessary to limit the distortion to permissible values.



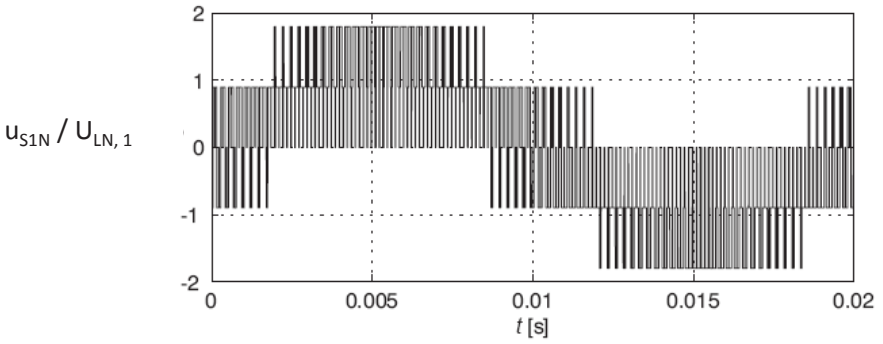
IEC

Figure 33 – Basic illustration of a topology of a two level PWM voltage source AIC

As the d.c. link of a two level PWM voltage source AICs has no connection to the neutral of the supply, the phase-to-phase voltage at the converter input is +/- U_d or zero and the d.c.-link has a common mode voltage to ground.

$$u_{CM} = \frac{u_{d+} + u_{d-}}{2}$$

Figure 34 shows typical waveforms of the phase-to-phase voltage u_{S1} and the phase-to-neutral voltage u_{S1N} related to $U_{LN,\,1}$ ($U_{LN,\,1}$: fundamental of the line to neutral voltage). The common mode voltage u_{CM} of the d.c. link is shown in Figure 35.



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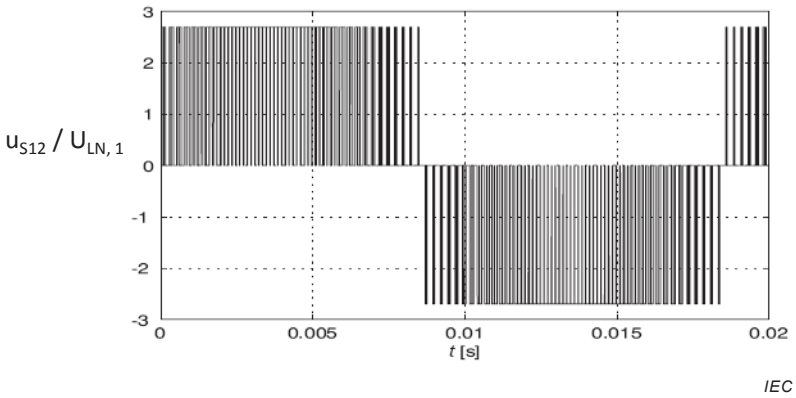
NOTE Power supply frequency is 50 Hz.

a) – Typical waveform of the voltage u_{S1N} / $U_{LN,1}$ at pulse frequency of 4 kHz



NOTE Power supply frequency is 50 Hz.

b) – Typical waveform of the voltage u_{S12} / $U_{LN,1}$ at pulse frequency of 4 kHz

Figure 34 – Typical waveforms of voltages u_{S1N} / $U_{LN,1}$ and voltage u_{S12} / $U_{LN,1}$ at pulse frequency of 4 kHz

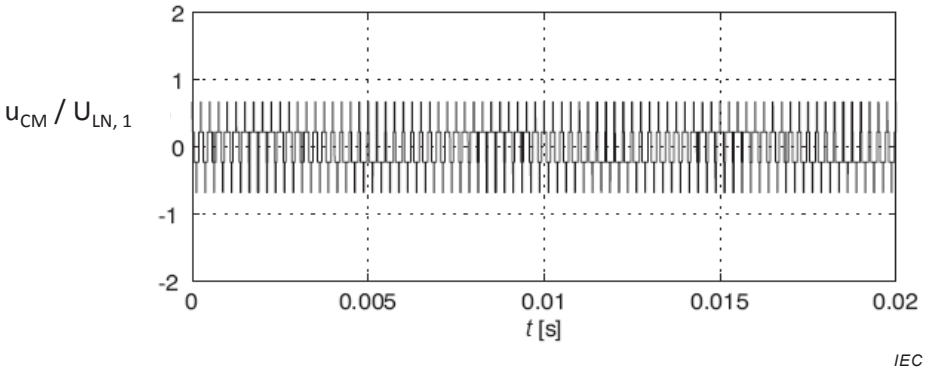
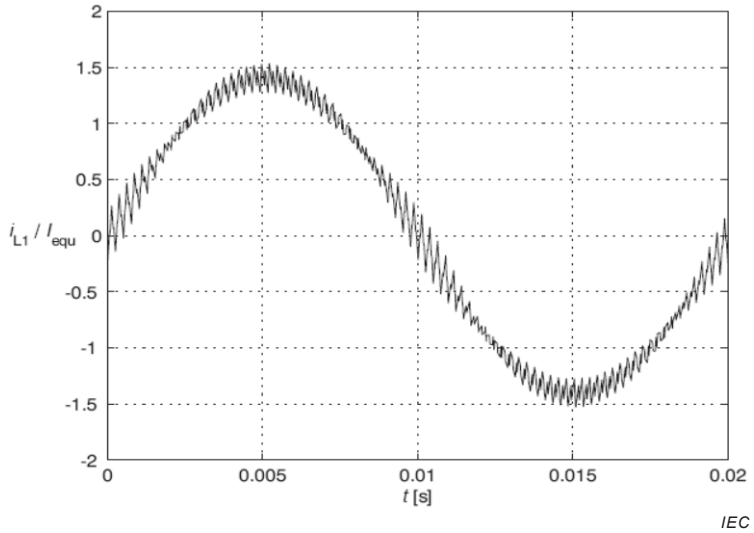


Figure 35 – Typical waveforms of the common mode voltage u_{CM} / $U_{LN,1}$ at pulse frequency of 4 kHz. Power supply frequency is 50Hz

Figure 36 shows a current i_{L1} at a pulse frequency of 4 kHz and with a relative impedance $u_{SCV,equ}$ of 6 % at rated load.

Increasing the pulse frequency or the reactances of X_{equ} reduces the current ripple. Normalized to the rated line current I_{equ}, the current ripple is nearly independent of supply power and power factor.



NOTE Power supply frequency is 50 Hz.

Figure 36 – Waveform of the current i_{L1} / I_{equ} at pulse frequency of 4 kHz, relative impedance of $u_{SCV,equ}$ = 6 %

6.3 Power control

Line currents or active and reactive power are controlled indirectly via the modulation index of the modulation circuit. All four quadrants of the current-voltage phase (i.e. all phase angles) are accessible (see 4.2.7).

Figure 37 shows as an example the block diagram of a control scheme of a two level PWM AIC with constant d.c.-link voltage.

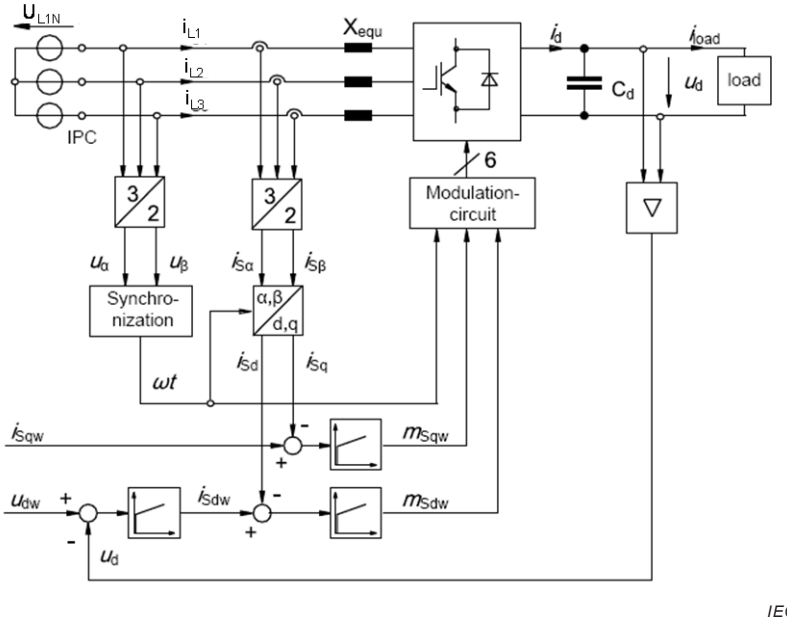


Figure 37 – Block diagram of a two level PWM AIC

Similar to vector control of rotating-field electrical machines the current components in d-q-coordinates are used, where the d-component represents the active current, the q-component the reactive current. The d.c.-link voltage control defines the reference value of the d-

component (active current) whereas the reference value of the q-component (reactive current) is arbitrary (usually zero, but can be set to any value within the current rating of the AIC).

The reference value of the d.c.-link voltage shall be higher than the peak to peak value of the phase-to-phase voltage for proper function and lower than the maximum d.c.-link voltage which is limited by the used electrical devices (semiconductor switches, capacitors).

6.4 Dynamic performance

The dynamic performance is mainly determined by the reactance X_{equ}. For fast current control a low reactance of X_{equ} is needed. Most applications are using a relative reactance of typically $u_{SCV,equ}$ = 2 % to 10 %.

A higher value of the d.c.-link voltage will improve the dynamic performance on one hand but on the other hand the switching losses and the cost of semiconductor valve devices and capacitors will rise accordingly. Therefore the reference voltage is set with additional safety margins to a value a few percent higher than the peak to peak value of the phase to phase voltage.

Two conflicting aspects to specify the d.c.-link capacitors (short term energy storage) are:

- lifetime of (electrolytic) capacitors, and
- dynamic behaviour of the d.c. load.

In applications where the d.c. load may change very quickly, the d.c.-link voltage can reach excessive values. Sufficient amount of capacitance is needed in order to reduce the voltage changes in the d.c.-link. When electrolytic capacitors are used, the capacitance is often high enough with typical dimensioning based on capacitor current rating and lifetime.

However, film capacitors have higher current ratings than equivalent electrolytic ones. Thus special attention has to be paid to d.c.-link voltage variation when film capacitors are used. Often feed forward of the d.c. load is needed to speed up and stabilize the d.c. voltage control.

Another advantage compared to thyristor controlled converters is the stable working in cases of high electrical power supply network impedances, if a current control is implemented.

6.5 Desired non-sinusoidal line currents

It is possible to use voltage source PWM AICs for compensation of specific harmonics.

If the pulse frequency is above 2 kHz these converters fulfil the requirements of the referenced International Standards in the low frequency range without additional filtering.

Harmonic components beneath the half of the pulse frequency of two level converters can be controlled to achieve very low values as shown in 4.2.3. Another advantage is that flicker due to changes in the AIC load may not be a problem, since the power factor of the line current is close to 1 or can even be set capacitive. The optimum power factor to suppress voltage changes is dependent on the electrical power supply network impedance which is normally inductive.

6.6 Undesired non-sinusoidal line currents

Figure 38 shows a simulated result of generated distortion of the current i_{L1} at a given reactance X_{equ}. Near to the pulse frequency of 4 kHz the highest distortion occur ("sidebands" of $f_p \pm g * f_L$ with $g = 2 * n - 1$).

NOTE f_p means the switching frequency of the semiconductors and f_L is the three phase output frequency

More spectral lines are near each multiple of the pulse frequency and decrease to higher frequencies. Those can only be reduced by a passive filter.

In addition harmonics of lower order caused by the supply voltage and controller deviations are measurable in real applications.

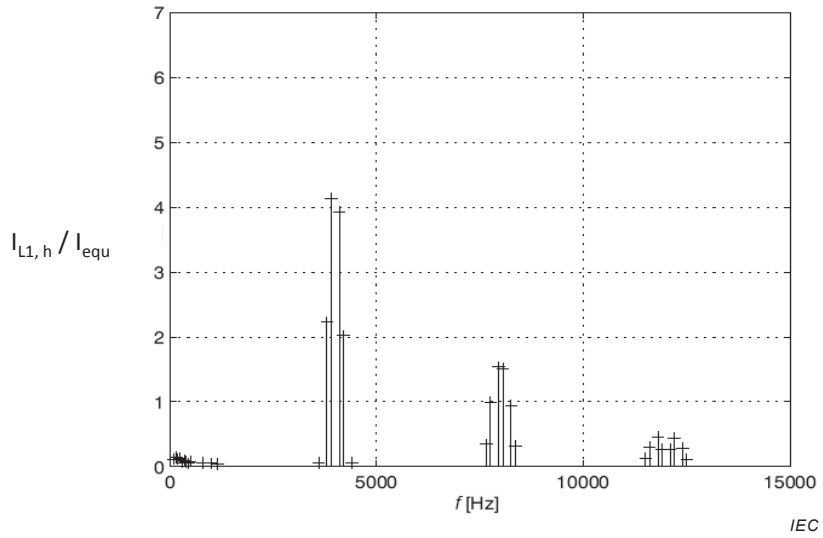


Figure 38 – Distortion of the current i_{L1} of reactance X_{equ}, pulse frequency: 4 kHz, relative reactance of $u_{SCV,equ}$ = 6 %

Figure 39 shows the supply voltages u_{L12} and u_{L1N}. The voltage distortion of both voltages with only a.c. side inductive impedance is about 6,6 %. See 4.2.3 for detail.

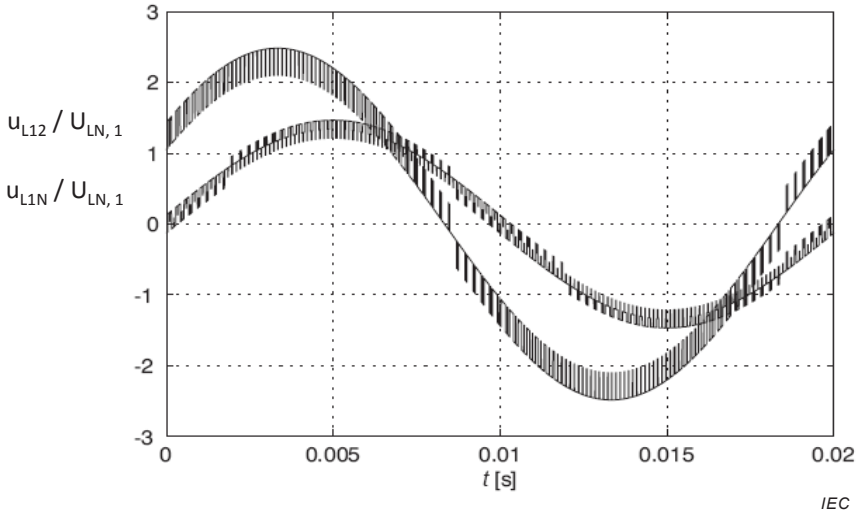


Figure 39 – Typical voltages $u_{L1N} / U_{LN,1}$ and $u_{L12} / U_{LN,1}$ at pulse frequency of 4 kHz, relative reactance $u_{SCV,equ}$ = 6 %, R_{SCe}= 100

6.7 Availability and system aspects

Two level PWM voltage source AICs are state of the art in the field of LV applications and are used for UPS, wind-power and solar energy applications and active filters. Electrical power drives systems generally use two level PWM voltage source AICs for regenerative energy supply.

The high frequency switching of the electronic valve devices of the AICs increases switching losses. With sinusoidal line currents and a power factor of approximately 1, the losses of an AIC using IGBT semiconductors are two to four times of the losses of thyristor controlled converters. On the other hand the RMS value of the line current is about 20 % lower compared to an uncontrolled rectifier. Thus losses in the power network are reduced considerably.

6.8 Operation in active filter mode

The control is similar to the block diagram in Figure 37. Additional harmonics are added to the reference values of the d- and q-components of the currents. Higher frequency distortion (see 4.2.3) is not affected.

7 Characteristics of a PWM active infeed converter of voltage source type and three level topology

7.1 General function, basic circuit topologies

A three level PWM converter is equivalent to a combination of two series connected two level systems with a common neutral point. This means that, with the same d.c. voltage level for each d.c. capacitor, a three level converter achieves an output voltage which is twice as high as that of a two level inverter system.

Mainly two basic topologies of three-level converters are used: neutral point clamped (NPC) (which is practically limited to three levels) and the flying capacitor (which can also be applied to multi-level topologies with more than three levels, see Clause 8).

In case of NPC technology, the neutral point is connected to the a.c. input terminals through diodes. In the active NPC-scheme transistors or GTO thyristors are connected in parallel with these diodes.

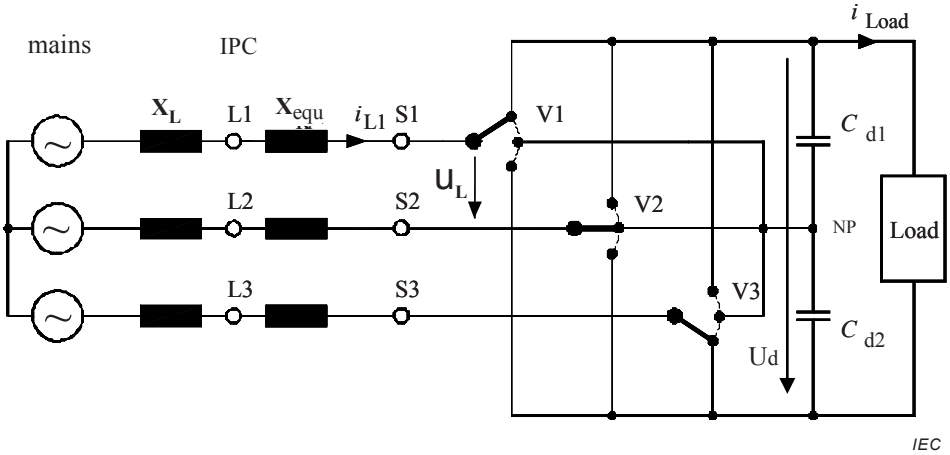


Figure 40 – Basic topology of a three level AIC. For a Power Drive System (PDS) the same topology may be used also on the load side

As the two level arm pairs of the three level phase leg are switched, they can provide three potentials referred to the potential of point "NP" of the d.c.-link, i.e.: 0 and +/- 0,5 U_d.

The suitably staggered switching of the arms gives phase-to-phase voltages of the three level inverter with five different voltage levels, i.e.: 0 and +/- 0,5 U_d, +/- U_d.

Referred to the potential of point "NP" in Figure 40 the resultant pulse frequency is two times the valves switching frequency (for example 150 Hz switching frequency of each valve device results in a 300 Hz switching frequency at the output). An example is shown in Figure 41.

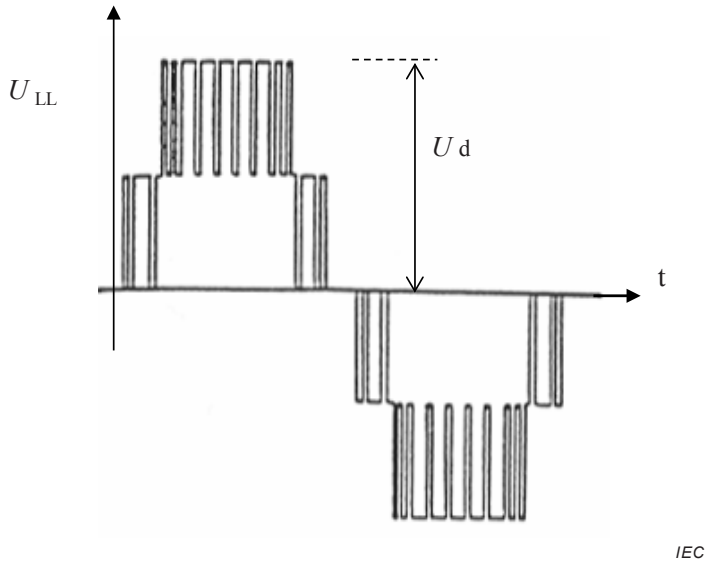


Figure 41 – Typical curve shape of the phase-to-phase voltage of a three level PWM converter

7.2 Power control

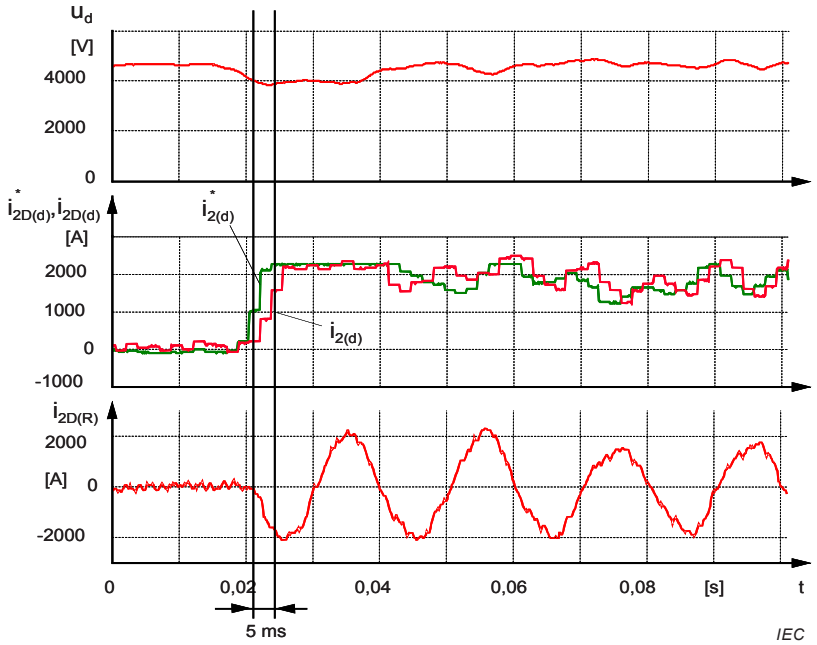
By using suitable semiconductors (IGBTs; GTOs; IGCTs) generally available on the market with a maximum peak forward blocking voltage of about 5 kV, the rated drive converter power ranges up to around 10 MVA with an output voltage of approximately 3,3 kV. With parallel connection it is possible to handle around 20 MVA and higher ratings with this technology.

Due to the increased switching losses of the semiconductor valve devices for high power and high voltages, the pulse frequency sometimes has to be reduced considerably compared with low power systems.

7.3 Dynamic performance

Digital control tasks of such PDS converters are normally handled by high performance microprocessor units in multi-tasking mode with sampling times shorter than 1 ms.

The controller features a highly dynamic control response with rise times in the order of a few milliseconds and permits flexible adaptation to the different requirements if suitably optimised pulse patterns are used. An example of a sudden load change of a huge 13 MW three level converter and its fast response is illustrated in Figure 42.



Top: d.c.-link voltage

Middle: reference value i^*_{2D} and actual value i_{2D} of the d.c-load current

Bottom: line current

Figure 42 – Example of a sudden load change of a 13 MW three level converter where the current control achieves a response time within 5 ms

7.4 Undesired non-sinusoidal line currents

The pulse frequency of a three-level converter determines the frequency band above which the undesirable distortion cannot be influenced.

In the case of a suitable PWM control, the phase voltage of a three-level converter never contains steps larger than 1/2 U_d. This reduces ripple currents resulting from these voltage steps compared to two-level converters.

As the voltage steps related to d.c.-link voltage are only 50 % of a comparable two-level AIC, the generated current distortion has a mean amplitude value of roughly 25 % up to 30 % of a two-level AIC with the same valve device switching frequency (see A.3.1).

7.5 Availability and system aspects

Three-level converters in neutral point clamped (NPC) and flying capacitors (FC) topologies are state of the art for high-power applications of any kind. Typical applications include process-oriented drives where additionally high dynamic behaviour is required (e.g. rolling mills) and the advantages of the power and harmonic control can be used. The efficiency of such high performance system reaches at least 96 %.

From the distortion point of view, the three level PWM AICs have the following characteristic: the lowest distorting frequency is the effective pulse frequency of the converter output voltage. The distortion level for this voltage, without additional filter, is approximately 10 %. The distortion of the integer multiples of the effective pulse frequency are generated additionally but with much smaller amplitudes.

The amplitude of the current distortion at the pulse frequency resulting from this voltage distortion depends on the impedances between the supply voltage and converter input and

the pulse frequency, is fairly independent from the load and is virtually negligible (3 %). If necessary the current distortion can be reduced by using additional filters.

8 Characteristics of a PWM Active Infeed Converter of Voltage Source Type and Multi Level Topology

8.1 General function, basic circuit topologies

For easier understanding, a multi-level converter can be treated as several two-level converters connected in series (see Figure 43). This means that, with the same semiconductor device, an n-level converter achieves an output voltage which is (n-1)-times as high as that of a two-level system.

Suitable control of the valve devices gives phase-to-phase voltages with many different voltage levels. With increasing number of levels the approximation of the desired voltage and current waveform (often sinusoidal) becomes better and better.

With several two level systems connected in series each of them is phase shifted and triggered in such a manner that at the output a terraced voltage curve shape arises which has a good approach to the sinusoidal waveform, even without filter. The correct voltage distribution between the respective valve devices is achieved by means of capacitors with floating potential which requires a switching frequency as high as possible and appropriate switching of the valve devices. The rating of the capacitors depends on the switching frequency (see A.3.2).

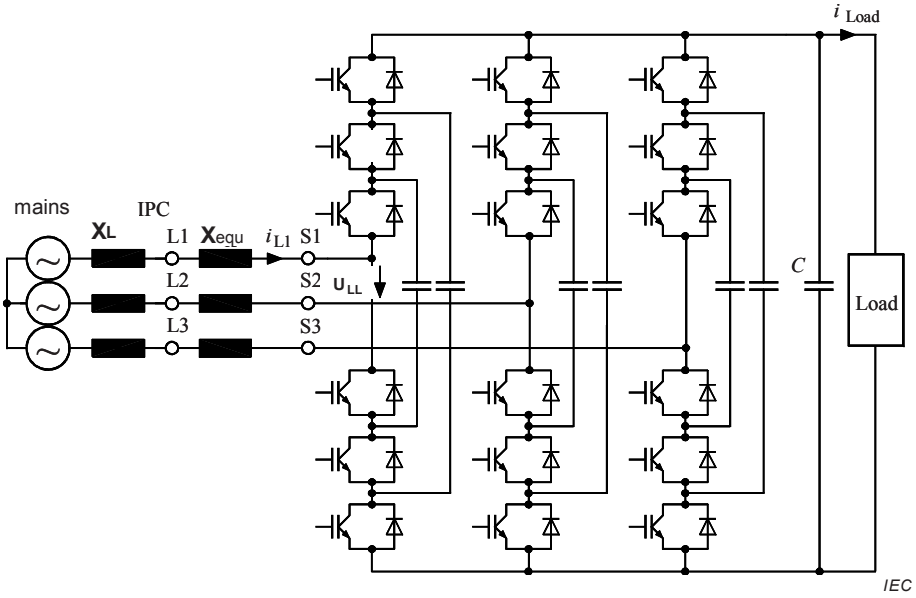


Figure 43 – Typical topology of a flying capacitor (FC) four level AIC using IGBTs

The respective two level systems of a multilevel converter are switched independently of each other, so that the power supply network side potential for a half wave can assume four potentials, if a four level converter is considered, i.e.: 0 and +/- 1/3 U_d; +/- 2/3 U_d; +/-U_d. (see Figure 44).

The suitably staggered control of the valve devices gives at a four level converter phase-to-phase voltages with seven different voltage levels for the entire inverter system (see A.3.2).

This FC technology is not limited to 4 levels. Six or more levels are possible but normally not applied because of economic reasons. The more the number of levels used the better is the

approach to the sinusoidal waveform and the lower is the dv/dt-stress for insulation systems of wound inductive components (e.g. transformers).

As the voltage steps of a four-level AIC related to d.c.-link voltage are only 30 % of a comparable two-level AIC and because the achievable input voltage is three times as much, the generated current distortion has a mean amplitude value of roughly 10 % of a two-level AIC with the same valve device switching frequency (see A.3.1).

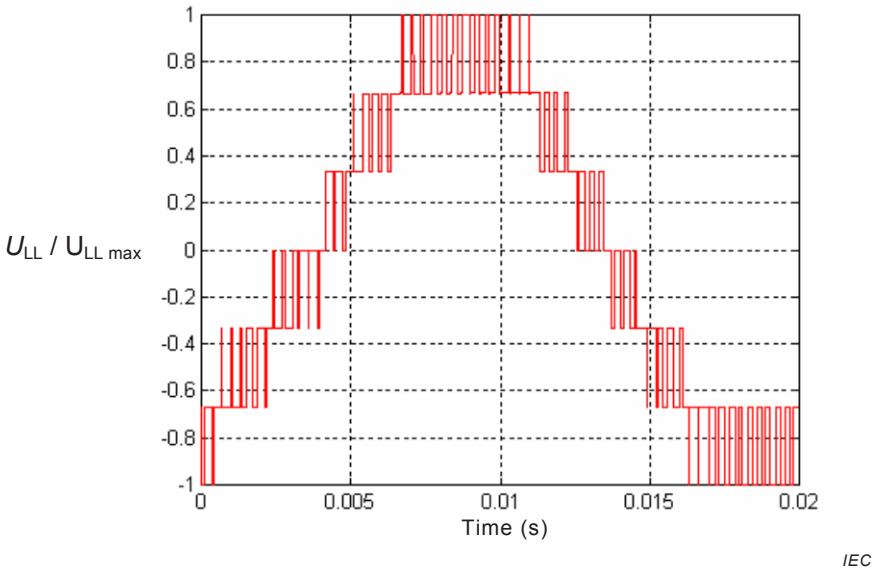


Figure 44 – Typical curve shape of the phase-to-phase voltage of a multi-(four)-level AIC

8.2 Power control

In comparison to two- and three-level converters only the following differences have to be taken into account when referring to Clauses 5 and 6.

- The visible resulting pulse frequency at the output increases with the number n of levels, while the switching frequency of the semiconductor valve devices remains constant. This leads to a better dynamic performance and an increased frequency range for desired (controllable) harmonics. Undesired (not controllable) distortion starts at higher frequencies.
- The voltage steps are reduced leading to smaller capacitive currents (reduced stress for any filters, connected cables and capacitors.
- Multilevel converters are normally used only if high power, high voltage and very low distortion is required.

By using suitable semiconductors (IGBTs) with a maximum blocking voltage of about 3 kV which are commonly available on the market, the rated output power ranges between 0,3 MVA and 3 MVA for air-cooled versions and 2 MVA up to 5 MVA for water-cooled versions, with output voltages of approximately 2,4 kV to 4,2 kV.

Due to the increased switching losses of the semiconductor valve devices for high power and high blocking voltages, the pulse frequency for high power AIC has to be reduced considerably compared with low power systems (two levels). Additionally it has to be considered that the effective visible switching frequency of the a.c. voltage of such a system is three times higher than the pulse frequency of each valve device (for example 1 kHz switching frequency of each valve device results in a 3 kHz switching frequency at the output).

8.3 Dynamic performance

Digital control tasks of such AICs are normally handled by high performance microprocessor units in multi-tasking mode with sampling times shorter than 1 ms.

The controller features short response times and permits flexible adaptation to the different requirements through the use of suitably optimised pulse patterns.

8.4 Power supply network distortion

From the point of view of distortion, the multilevel PWM AIC based on 4 levels have the following characteristics.

- The lowest distortion frequency which occurs is the effective pulse frequency of the converter output voltage. The distortion level for the voltage on the IPC, without additional filter, is approximately 5 % (an example is shown in Figure 45).
- Integer multiples of the pulse frequency occur additionally but with much smaller amplitudes. The amplitude of the current distortion for the pulse frequency resulting from this voltage distortion depends on the transformer impedance, the network impedance and the pulse frequency, is fairly independent from the load and virtually negligible (2 %). If necessary the distortion can be decreased by using additional filters.

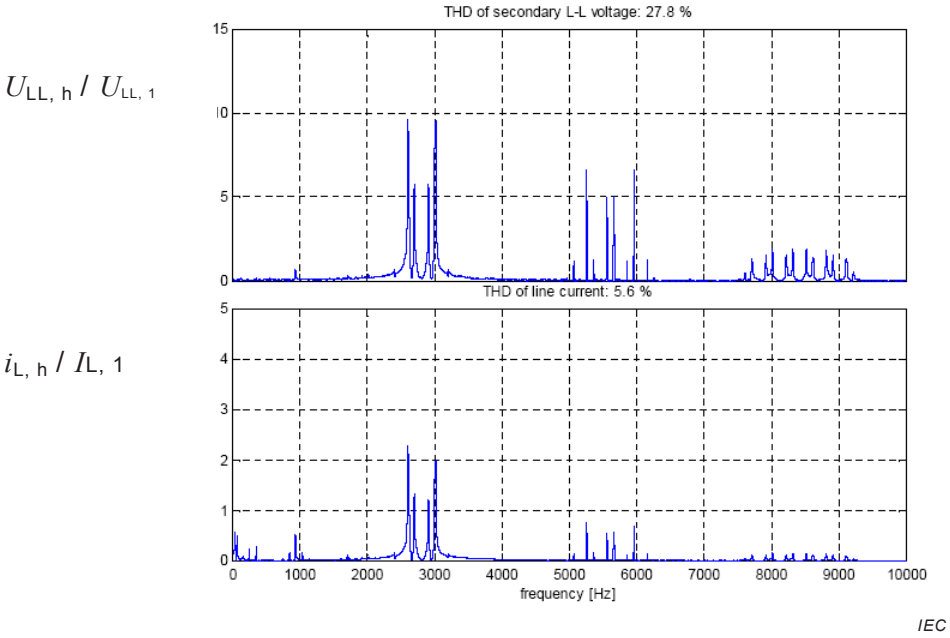


Figure 45 – Distorting frequencies and amplitudes in the line voltage (measured directly at the bridge terminals in Figure 25 and the line current of a multilevel (four) AIC (transformer with 10 % short-circuit voltage)

8.5 Availability and system aspects

This type of converter is used for high power applications in all branches of industry where the high dynamic of the AIC is required. Marine applications and network distribution systems (e.g. because of the excellent capability to perform active energy management (AEM) and active harmonic control) are typical examples for that.

The efficiency of such high performance system exceeds 96 %.

9 Characteristics of a F3E AIC of the Voltage Source Type

9.1 General function, basic circuit topologies

The topology of a F3E AIC consists of a fundamental frequency front end or so-called F3E-AIC connected to a load (see Figure 46).

The F3E AIC consists of a standard diode bridge with antiparallel connected IGBTs. If the current flows in the direction of the load (e.g. a PWM motor inverter) it goes through the diodes. If the current flow is in the direction of the power supply network it goes through the IGBTs.

The switching of the IGBTs is synchronous to the current flow in the respective antiparallel connected diodes and therefore very simple. Rectangular current pulses with duration of half the power supply network frequency period are achieved with low switching losses.

The topology of a F3E AIC consists of a fundamental frequency front end or so-called F3E-AIC connected to a load (see Figure 46).

The d.c.-link capacitor is basically replaced by an a.c. line side filter, designed to limit the voltage distortion caused by the PWM currents of the inverter stage as shown in Figure 46.

Compared to the standard PWM inverter topology with diode rectifier, braking chopper and electrolytic d.c.-link capacitors three major advantages, energy regeneration to power supply network, lower harmonics – nearly no inductors necessary, extended lifetime compared to a converter with electrolytic d.c.-link capacitors shall be noted. However the output voltage of the inverter might be slightly reduced and needs higher pulse frequencies and control effort for the connected PWM inverter and there may be some power losses in the F3E filter resistors.

From practical experience it has been shown that in many cases only small additional power supply network side inductor is necessary to protect other equipment, fed by the same supply system, against voltage distortion caused by the F3E AIC.

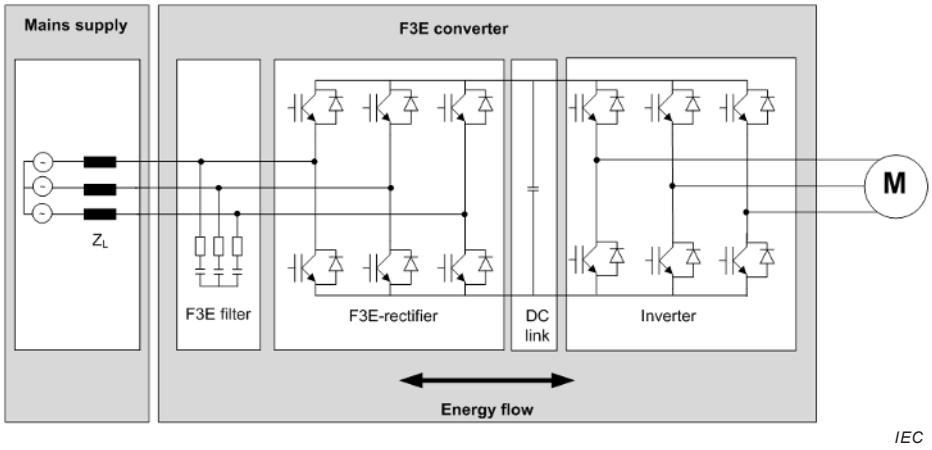


Figure 46 – Topology of a F3E AIC

Compared to a standard PWM converter with diode rectifier two major differences are obvious. In the case of power drive systems braking chopper and resistor are replaced by an F3E-AIC. The capacitors sourcing the PWM current of the inverter stage, move from d.c.-link to a.c. power supply network are of much smaller ratings and can therefore be changed from an electrolytic to a.c. metallised foil type capacitors.

9.2 Power control and line side filter

The line side filter is necessary to serve as a low-inductive source for the PWM currents of the output inverter stage and to limit the voltage distortion caused by these currents.

To avoid resonance problems the filter has to be damped by series resistors (see Figure 47). The effect of the filter can be demonstrated with a simple equivalent circuit representing the power supply network reactance Z_L, the filter capacitance C, the damping resistors R and the exciting a.c. current source i(t).

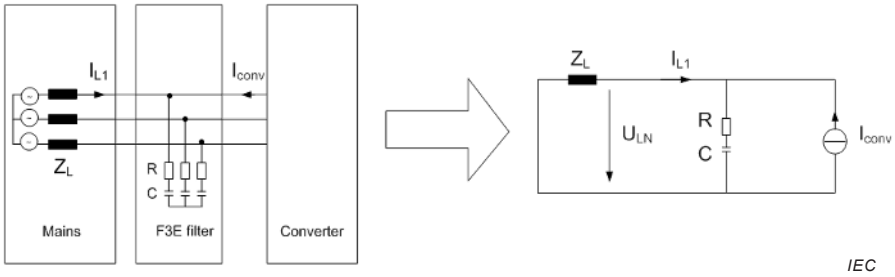


Figure 47 – Line side filter and equivalent circuit for the F3E-converter behaviour for the power supply network

The current transfer function G(f) depends upon the power supply network impedance. Here the power supply network impedance was supposed to be purely inductive. To normalise the reactance to the rated power of the converter the term R_{SCe} has been introduced in literature and standards (see definitions 3.24 to 3.26).

$$G(f) = i_{L1} / i_{conv} \quad (10)$$

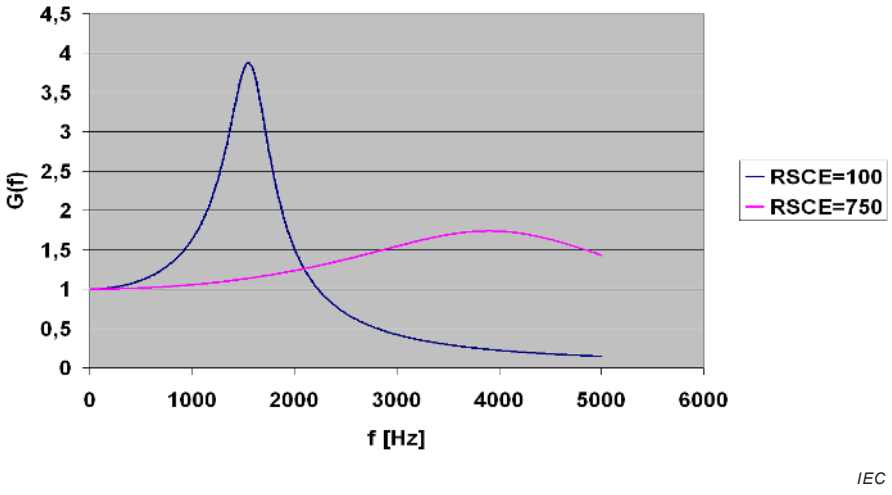


Figure 48 – Current transfer function together with R_{SCe} = 100 and R_{SCe} = 750 and a line side filter: G(f) = i_{L1}/ i_{conv}

The higher the value of R_{SCe}, the lower the value of the power supply network impedance. In Figure 48 the current transfer function G(f) for two different R_{SCe} values has been calculated.

At a switching frequency of for example 4 kHz the PWM current ripple will be attenuated by a factor of 5 in case of R_{Sce} =100, where in case of R_{Sce} = 750 it will be increased. This has to be considered and may affect other equipment.

Therefore the main focus should not be on the current, but on the voltage distortion caused by the current. To calculate this voltage distortion, one has to consider the current amplitude as well as the power supply network impedance.

$$U_{LN,h} = Z_L * I_{L,h} \quad (11)$$

Figure 49 shows how the power supply network voltage distortion changes with power supply network impedance, normalized to filter impedance.

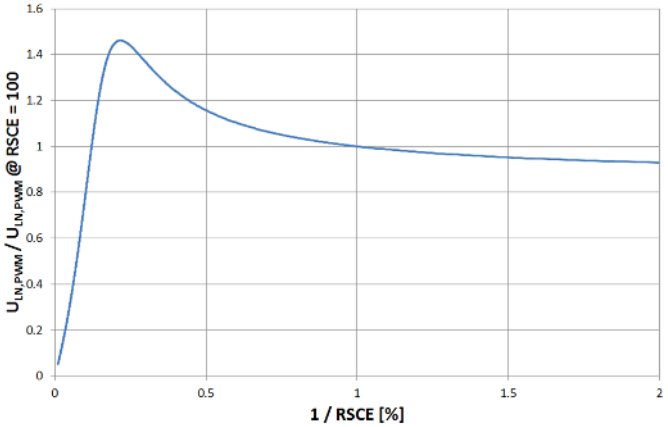


Figure 49 – PWM – voltage distortion over power supply network impedance for F3E-infeed including power supply network side filter

As expected from an ideal voltage source with no impedance, there is no voltage distortion – the result will be a clean, ideal sinusoidal waveform. No other equipment connected to this power supply network might be influenced.

In the resonance point the highest voltage distortion occurs. The filter should be designed so that this value is adapted to the PWM voltage distortion values of a general AIC.

Figure 50 shows the power spectrum of a 75 kW F3E-converter with the fundamental current being 116A (r.m.s. value) and a PWM-frequency of 4 kHz. The scaling is 2 kHz/div and 1,25 A/div.

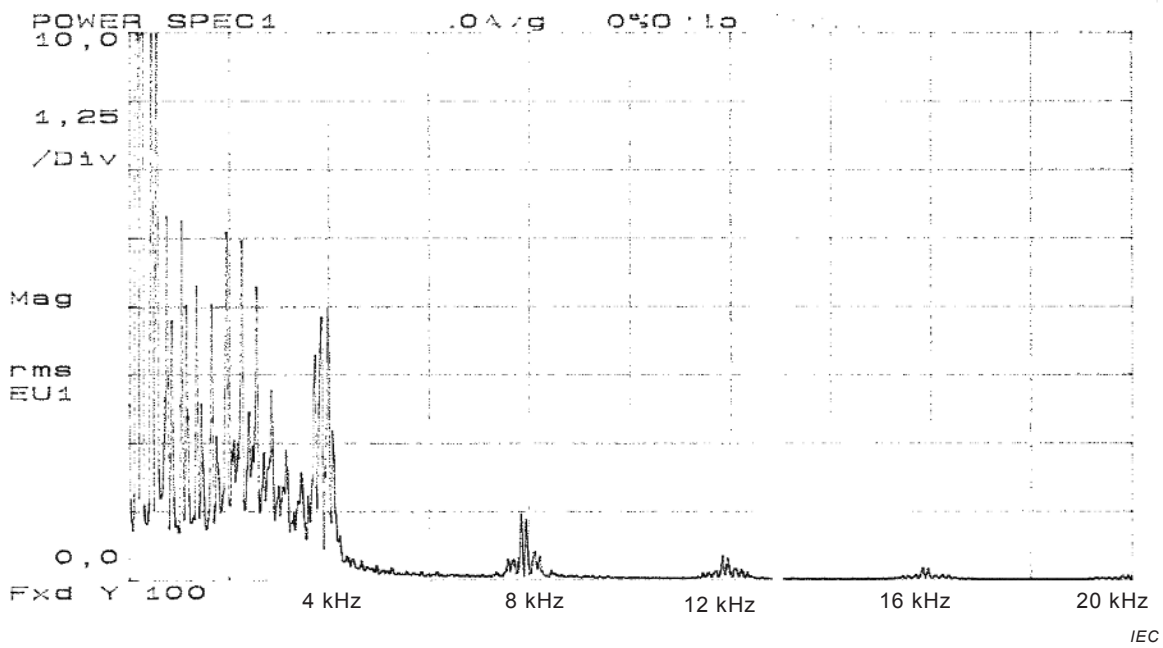


Figure 50 – Input current spectrum of a 75kW-F3E-converter

9.3 Dynamic performance

In case it is used as the infeed of a PDS, the dynamic behaviour of the PDS is not influenced at all by the F3E-AIC.

9.4 Harmonic current

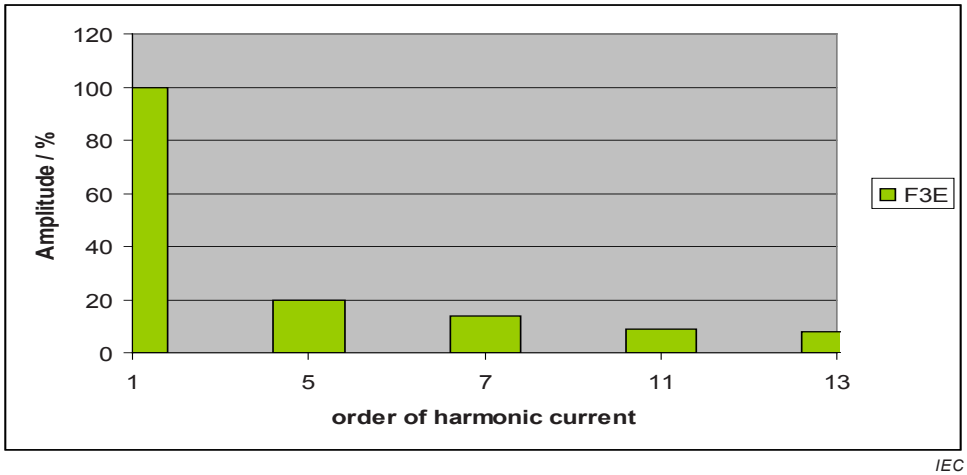


Figure 51 – Harmonic spectrum of the input current of an F3E-converter with R_{SCe} = 100

Figure 51 shows the typical harmonic spectrum of the input current under condition R_{SCe} = 100. With an F3E-Infeed the harmonic content represented by most significant harmonics influences can be reduced considerably (in case on the fifth harmonic down to less than 25 %).

10 Characteristics of an AIC of Voltage Source Type in Pulse Chopper Topology

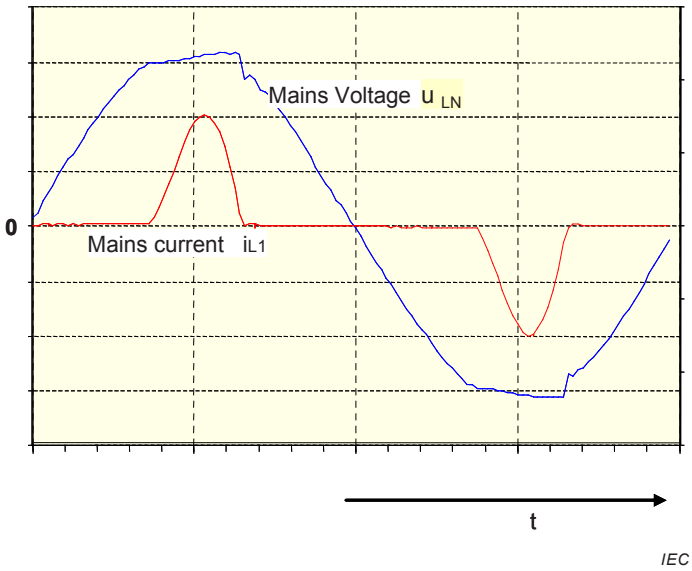
10.1 General

Many of the pulse choppers cannot control reactive power but they are operated at unity power factor and their current waveforms are sinusoidal. Therefore they are dealt as being an AIC.

10.2 General function, basic circuit topologies

Caused by a high population of single phase bridge fed electronic loads (TV-sets, power supplies of generic household and office equipment), with capacitive smoothing at the d.c. side, the voltage distortion of the power supply network is stressed towards mainly the 3rd and 5th harmonics.

This results from an arithmetic superposition phenomenon of all capacitive loading currents of all single phase equipment simultaneously (see Figure 52), which happens when the phase voltage reaches its periodical maximum.



NOTE The current waveforms of many units are similar and the effect on the power supply network is multiplied.

Figure 52 – An illustration of a distortion effect caused by a single phase converter with capacitive load

In order to improve this situation economically, mitigation methods are contemplated by the manufacturers of such products.

One commonly applied solution is based on the topology of so-called AIC Pulse Choppers. AIC Pulse choppers are PWM converters with a.c. power supply network input and d.c. or a.c. output. There are different variants of the pulse chopper according to the application. The AIC topology for a.c. to a.c. conversion is shown in Figure 53. These are normally used for power supplies and also known sometimes as "Power Factor Controllers".

The AIC pulse chopper controls the amplitude of the output voltage by means of pulse width modulation. Bidirectional and reverse blocking power semiconductors in the forward and freewheeling path are necessary. Because of the lack of these elements they are actually composed of a combination of power transistors and power diodes.

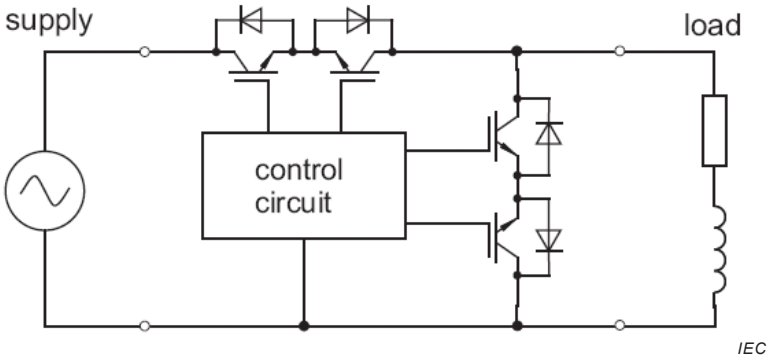


Figure 53 – a.c. to a.c. AIC pulse chopper, basic circuit

In operation the a.c. to a.c. converter circuit switches the sinusoidal a.c. power supply network voltage to the output a.c. side for a defined part of the PWM period in every pulse period.

Thus, for each PWM period the output voltage can be controlled between zero and the actual, sinusoidal time dependent power supply network voltage. As the load usually has an inductive component, the output or load current is moderately smoothed. The current shape depends on the PWM method. For steady state conditions, a constant modulation index can be assumed which leads to a sinusoidal voltage (sliding mean value) and sinusoidal current, both at mains frequency, with superimposed distortion at switching frequency.

Nevertheless, in dynamic operation the modulation index varies depending on the control. AIC pulse choppers generally operate with a switching frequency between 2 kHz and 10 kHz.

The use of an AIC pulse chopper instead of a thyristor phase angle controlled circuit is recommended for single phase applications if the power supply network harmonics are too large (the maximum of the third, fifth and seventh harmonic is already reached).

10.3 Desired non-sinusoidal line current

As the output voltage can be controlled with the PWM, it is possible to control specified harmonics desired for example, to compensate existing power supply network low order harmonics.

10.4 Undesired non-sinusoidal line current

AIC pulse choppers generate distortion on the power supply network side with a frequency of the pulse frequency, its sidebands and integer multiples. As a result some filtering elements might be included in the topology in order to mitigate the effect on the power supply network.

Not only the switching frequency is important; also the current and voltage slopes of the switching have to be taken into account.

The filter is often integrated in the AIC pulse chopper. The application and the design of the filter depends on the intended use in public or industrial power supply networks.

10.5 Reliability

A high reliability is expected, because the AIC pulse choppers are short-circuit-proof.

10.6 Performance

AIC pulse choppers are applicable for compensation of harmonics. Conventional power controllers have not until now been able to replace an auto transformer in boost-circuits. This is only possible with AIC pulse choppers with a controlled free-wheeling arm.

10.7 Availability and system aspects

The forward conduction losses arise in one active switch and the series diode and, during freewheeling, in the freewheeling diode (d.c. load) and additional active switch (for a.c. loads). So, compared to thyristor controlled rectifiers for d.c. loads, higher losses will occur. The losses are dependent on the load (impedance, transformer and boost).

11 Characteristics of a two level PWM AIC of current source type (CSC)

11.1 General

Current source type PWM AICs convert d.c. currents to three phase a.c. currents that are fed into the electrical power supply network or vice versa.

Full four quadrant operation of the electrical power supply network side quantities (voltage and current) is possible to fully control all types of apparent power, active and reactive.

11.2 General function, basic converter connections

A typical converter connection for a three phase current source PWM AIC is given by Figure 54.

The converter consists of three phase legs containing two switching devices i.e. power semiconductors. This current source AIC is connected to the electrical power supply network via a filter that most commonly consists of an inductor additional to the electrical power supply network impedance and of filter capacitors as required by this special converter topology.

At the d.c. side the converter is connected to a d.c. inductor for current smoothing and short time energy storage. At the d.c. terminals either an active or passive load can be connected.

Due to the special properties of this circuit, negative voltages can occur at the semiconductors which therefore have to be fully reverse blocking or otherwise diodes in series with the switching devices are to be added.

For medium to high power converters being applied in the industry reverse blocking Gate-Turn-Off Thyristors (GTOs) are commonly used.

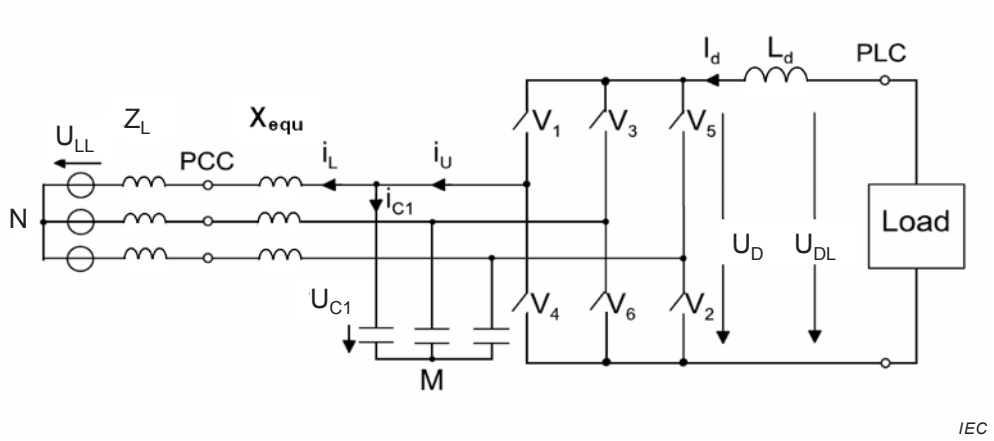


Figure 54 – Illustration of a converter topology for a current source AIC

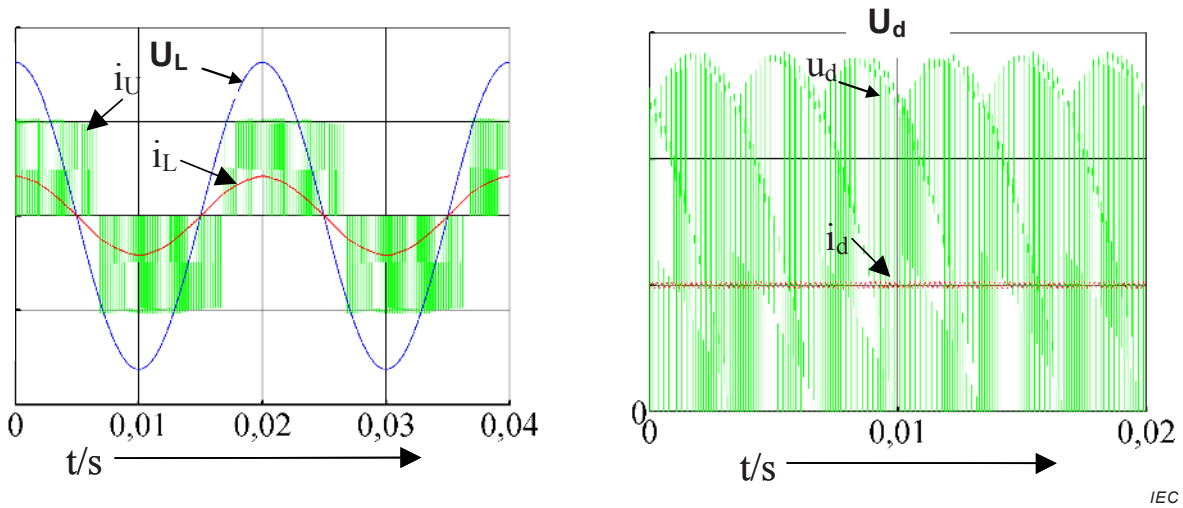
The current source converter is characterized by a step up behavior of the voltage towards the direction of the power supply network. While feeding power into the power supply network with a fixed voltage the mean value of the d.c. voltage U_d may assume values between zero and the amplitude value of U_{C1} of the power supply network filter capacitor.

The pulse width modulation of current source type AIC is very similar to that of the VSC, see references [25] to [28]. The a.c. side converter current consists of pulses of the d.c.-side current as can be seen in Figure 55 for a high frequency PWM converter.

They show a similar outline as the a.c. side line to line voltages of a VSC. The pulsed a.c. side converter current is smoothed by the LC filter yielding an almost sinusoidal electrical power supply network current waveform that is only superimposed by a small ripple.

The d.c. voltage U_d is composed of periodic pulses of all line to line capacitor voltages, being sectional switched to the d.c. side.

High power applications commonly use low switching frequencies of the semiconductors (typically from 300 Hz up to 1 000 Hz). Optimized pulse patterns are commonly calculated offline in order to eliminate specific harmonics.



a) Electrical power supply network voltage, electrical power supply network current, pulsed a.c. side converter current

b) Current and voltage on the d.c. side

Figure 55 – Typical waveforms of currents and voltages of a current source AIC with high switching frequency

11.3 Power control

The a.c. side control structure usually features a cascaded control structure with the inner control loop controlling the electrical power supply network current and the outer one controlling the power. The control of the current components can be realized similar to field oriented control for three phase a.c. machines.

As the a.c. side LC filter represents an oscillatory system it is recommended to implement damping functions (actively or with a subordinate capacitor control circuit [29] to [31]).

The control scheme (see Figure 56) is very similar to that of a VSC system. The superimposed d.c.-link current control replaces the d.c.-link voltage control, and the controlled modulation of the power supply network side converter currents is used instead of modulation of the voltages.

Conduction and switching losses in the power semiconductors devices are about the same as in VSCs and three to four times of the losses of a three phase diode bridge rectifier, [34].

For high power AICs an efficiency of 97,5 % to 98,5 % including the losses of the necessary passive elements can be achieved. If additional series diodes are required for a CSC with non-reverse blocking devices, the conduction losses and thus the overall losses may be higher than in the VSC.

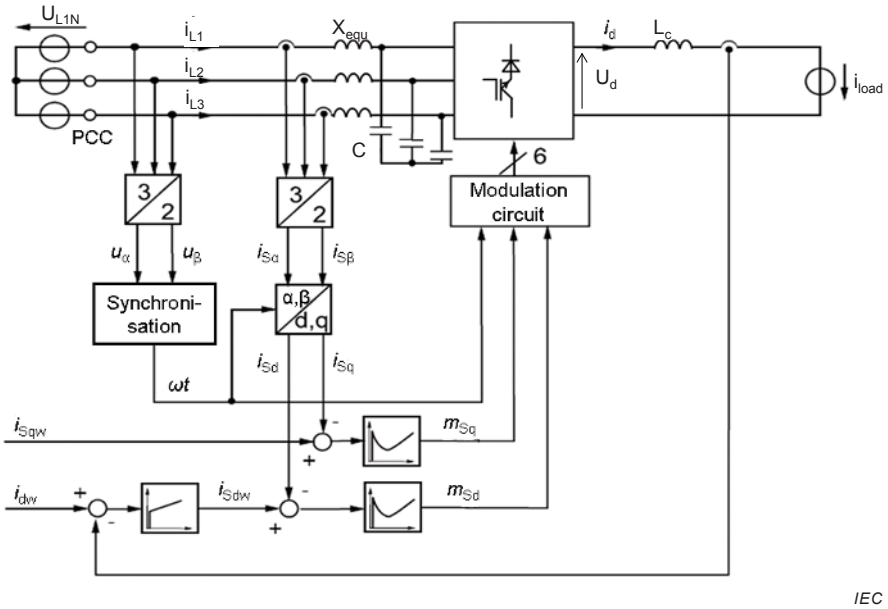


Figure 56 – Typical block diagram of a current source PWM AIC

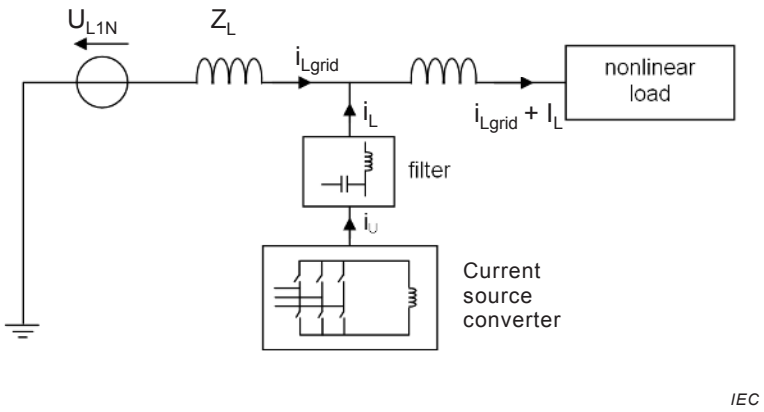


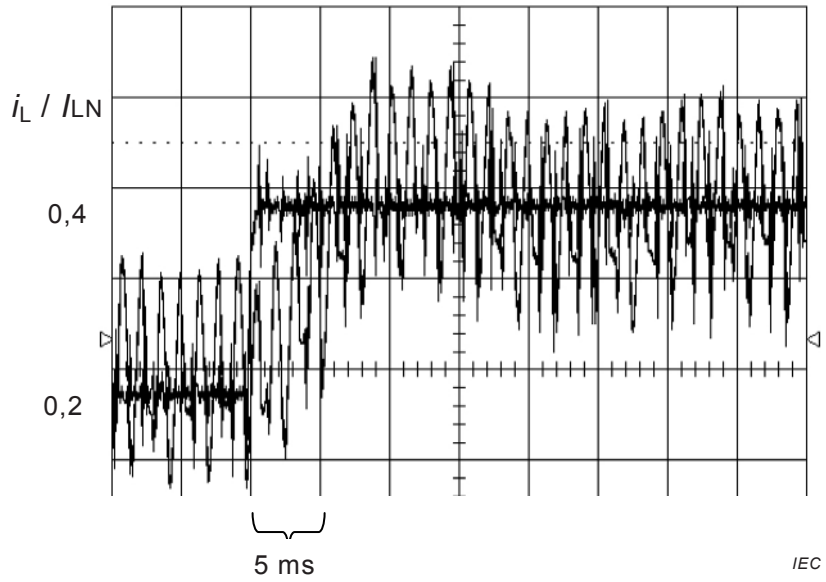
Figure 57 – Current source AIC used as an active filter to compensate the harmonic currents generated by a nonlinear load

In case of high pulse frequency, the current source converter possesses real active filter capability for a wider range of harmonics. Figure 57 shows a possible connection for a shunt active filter featuring a current source converter. The current reference corresponds to the harmonic content of the electrical power supply network current that should be compensated. The current i_L is controlled in such a way that the harmonics in current I_{Lgrid} are controlled down to zero.

11.4 Dynamic performance

The control performance is characterized by high dynamics.

Figure 58 shows the performance of a realized current source AIC for a step response of the current.



NOTE I_{LN} equals the rated current of the AIC.

Figure 58 – Step response (reference value and actual value) of current source AIC with low switching frequency [33]

11.5 Line current distortion

Current source AICs are used in the medium and high power range with GTOs and thus with low switching frequencies. If asynchronous PWM is used, only low distortion in the range of the pulse frequency is typically present. However, by using optimized synchronous pulse patterns for selective harmonic elimination [28], [32], this a.c. side low frequency distortion can be further decreased. In both cases, distortion near the resonance frequency of the filter have to be avoided.

Attention should be paid to the harmonics already existing in a distorted electrical power supply network which may cause resonances of the filter and may additionally distort the electrical power supply network current.

11.6 Operation in active filter mode

The current source PWM AIC can be controlled in a way to compensate selected low frequency harmonics present in the a.c. electric power supply network and/or to avoid selected low frequency harmonics.

This can be done by suitable pulse width modulation or by control of the harmonics. For example in the case of medium and high power GTO converters by means of synchronous PWM with optimized pulse patterns. This can be realized similarly to the VSC [28]. The maximum harmonic order that can be eliminated depends on the pulse frequency.

11.7 Availability and system aspects

The current source AIC is used in industrial applications for current source converter PDSs. As such it can be used as an alternative to line commutated thyristor converters. The application of such drives is in the range of medium to high power above 1 MW and at voltages above 1 kV.

Annex A
(informative)

A.1 Control methods for AICs in VSC (Voltage Source Converter) topology

A.1.1 General

Several control methods exist. Some are time-domain methods, partly instantaneous, based, e.g., on the original instantaneous p-q-theory or on the so-called FBD-theory. Others use filters or sliding integration over a period to generate quasi-stationary control signals out of the above-mentioned instantaneous quantities. Other control schemes apply frequency-domain techniques, either based on FFT algorithms, treating all harmonics simultaneously, or on the determination of selected frequencies.

A.1.2 Considerations of control methods

Amongst PWM-based schemes also a line flux oriented control scheme is known: the indirect stator-quantity control (ISR)-based scheme guides the converter flux on a basically circular track curve. A reference voltage vector is calculated for each period of pulse frequency. This reference voltage is then realised using a PWM scheme. Many of the control schemes are based on a.c. machine control schemes, because the structure of the line and the structure of an a.c. machine are quite similar.

Another control scheme is similar to the direct self-control method (DSC) or direct torque control (DTC) that is commonly known to control electrical machines.

The supply network including the filter is treated in these cases like a big electrical machine and its estimated torque and flux (often referenced as "virtual") are controlled by hysteresis control.

The torque reference is produced by the d.c.-link voltage control and the flux magnitude reference is calculated from the reactive power or reactive current reference.

It is also possible to estimate the active and reactive power of the AIC and control these directly with hysteresis control.

The advantage of synchronous pulse patterns results from the property of being synchronous to the line frequency. Stationary, all periods are identical. As a result, all harmonics are known and depend only on the pulse pattern. No interharmonics occur. Dynamic changes require carefully precalculated changes between the pulse patterns.

In case of PWM schemes the pulse pattern is generated automatically for steady-state and dynamic operating conditions. Reference values for fundamental and controllable harmonic components can easily be generated. The generated harmonics to be expected are known but can no longer be influenced. If the triangular reference of the PWM circuit is synchronous to the line frequency, no interharmonics are to be expected. Otherwise, interharmonics in the frequency region of generated harmonics are generated.

Line flux oriented pulse pattern generation schemes (DSR and DSC like) provide the advantage of quick dynamic reaction and optimum utilisation of switching, combined with reduced amplitudes of harmonics. However, harmonics leak from the sharp lines associated with fixed pulse patterns, leading to interharmonics. This effect can also be reached by modifying the base period of space vector modulation and PWM based pulse pattern generation schemes randomly. Then the pulse frequency is not constant, but varies slightly around its mean value. Such methods are known under the name of random PWM.

It is important to note that the total amount of distortion, measured as the r.m.s value of all components in a frequency band in the region of generated harmonics, is constant for all pulse pattern generation methods. It only depends on the mean value of the pulse frequency and on the actual d.c.-link voltage or current, respectively. The different methods for pulse pattern generation only shift the r.m.s value from one harmonic (or interharmonics) to another. In other words, the distribution of the undesirable signal components along the frequency axis is modified, not the total amount of undesirable signal components. Since, however, the line may contain resonances which vary from IPC to IPC and since other consumers may be more sensitive to one frequency component then to another, changing the distribution of the undesirable signal components along the frequency axis offers a method to solve EMC problems.

Special care should be taken concerning ripple control signals in the power supply network and time-transmission radio frequencies such as DCF77 (used for remote control clocks), because such signals may be interfered by some pulse patterns.

A.1.3 Short-circuit ride through functionality for decentralized power infeed with AIC

The increasing installation of distributed power generation systems affects the stability of electrical grids. Apart from pure energy feed-in, the distributed power systems are required to provide grid service functions that have been delivered so far by central large-scale power plants. Among these function is supplying reactive power for clearing temporary grid faults up to short-circuits. This is also true for asymmetric failures like single ground faults.

In such situations – in contrast to motor-side inverters of typical electrical machine applications – the AICs should keep stable controlled power generation and should not disconnect from line for a given fault-ride-trough-time.

The precise technical requirements are defined within the individual grid-codes of countries and network operators.

A.1.4 Fault ride through mode

A.1.4.1 General

The demand for riding-trough line faults with simultaneously generating a defined supporting power to the network sets new tasks for the control of the active infeed converters which exceed the regular operating conditions.

A.1.4.2 Special requirements for AICs in PWM mode

With voltage injecting converters using pulse-width-modulators a current impressing operation mode has to be realized. Thereby, the phase currents can be controlled, even when step changes of line voltage amplitudes or of the phase angle occur.

For regular operation conditions a digital current controller with PWM cycle time is adequate for controlling AIC line currents. In the case of step line changes which can also comprise varying line impedance the AIC currents may exceed maximal converter current within one controller cycle. Using an additional current injecting modulator the required current set point is realized with a minimal number of additional switching operations.

Figure A.1 shows the fundamental logical connection of both modulation principles with the resulting switching commands m_g for phase R.

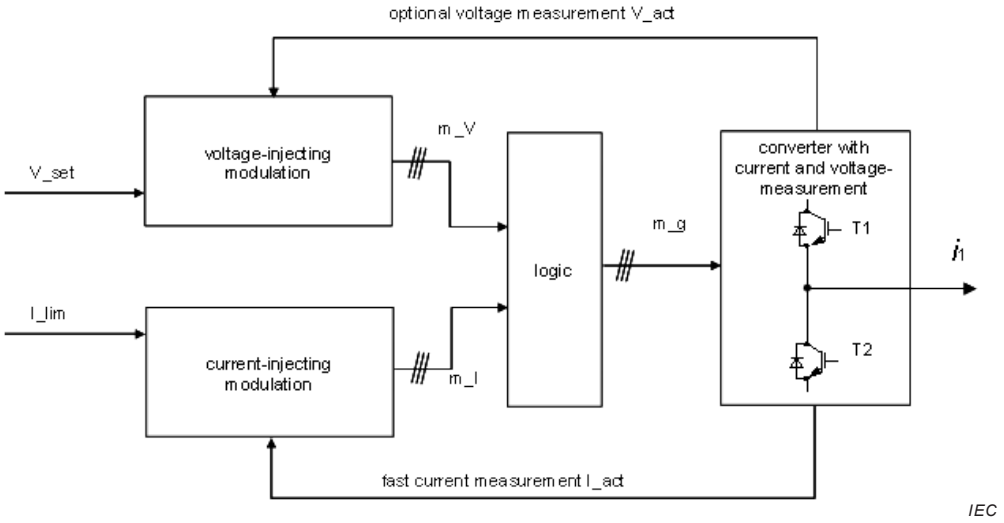


Figure A.1 – Principle sketch for combined voltage- and current-injecting modulation example for phase leg R

Table A.1, Table A.2 and Table A.3 show the resulting switching commands for the different operating conditions. Corresponding control rules are applied for all legs of the bridge topology.

Table A.1 – Condition state 1: positive current limit reached, transistor T1 is switch-off to reduce the current

Current range	Switching command I-injection m_I	Switching command V-injection m_U	Combined switching command (m_U and m_I
$i_1 \geq I_{\text{lim\_}lev}$	T_{1_I} = 0 T_{2_I} = 1	T_{1_U} from PWM T_{2_U} from PWM	T_1 = (T_{1_I} and T_{1_U}) = 0 T_2 = (T_{2_I} and T_{2_U}) = T_{2_U}

Table A.2 – Condition state 2: negative current limit reached, transistor T2 is switch-off to reduce the current

Current range	Switching command I-injection m_I	Switching command V-injection m_U	Combined switching command (m_U and m_I
$i_1 \leq I_{\text{lim\_}lev-}$	T_{1_I} = 1 T_{2_I} = 0	T_{1_U} from PWM T_{2_U} from PWM	T_1 = (T_{1_I} and T_{1_U}) = T_{1_U} T_2 = (T_{2_I} and T_{2_U}) = 0

Table A.3 – Condition state 0: current in phase R within tolerance range, pure voltage injection active (e.g. with PWM)

Current range	Switching command I-injection m_I	Switching command V-injection m_U	Combined switching command (m_U and m_I
$I_{\text{lim\_}lev2-} < i_1 \wedge$ $\wedge i_1 < I_{\text{lim\_}lev2}$	T_{1_I} = 1 T_{2_I} = 1	T_{1_U} from PWM T_{2_U} from PWM	T_1 = (T_{1_I} and T_{1_U}) = T_{1_U} T_2 = (T_{2_I} and T_{2_U}) = T_{2_U}

An example of the line currents at the AC input of the AIC during a voltage dip is shown in Figure A.2.

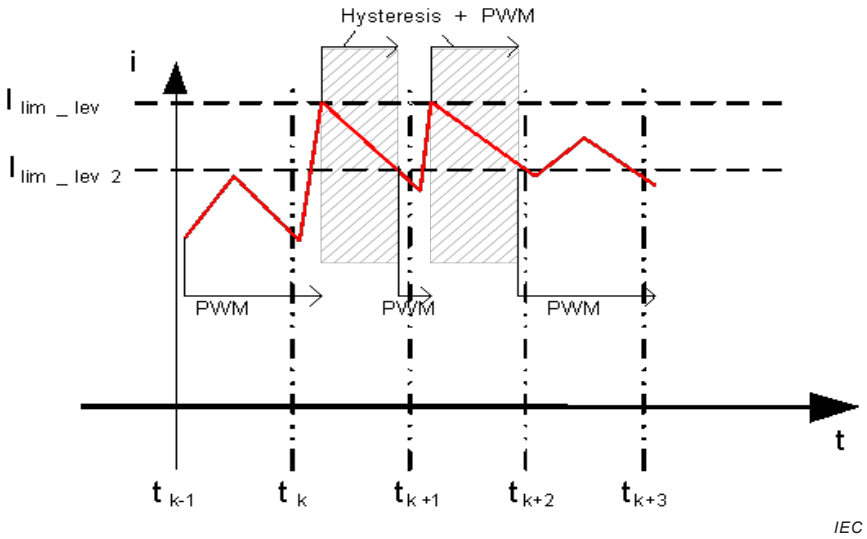


Figure A.2 – Example for controlled phase current during a voltage dip at the power supply network using hysteresis plus PWM control

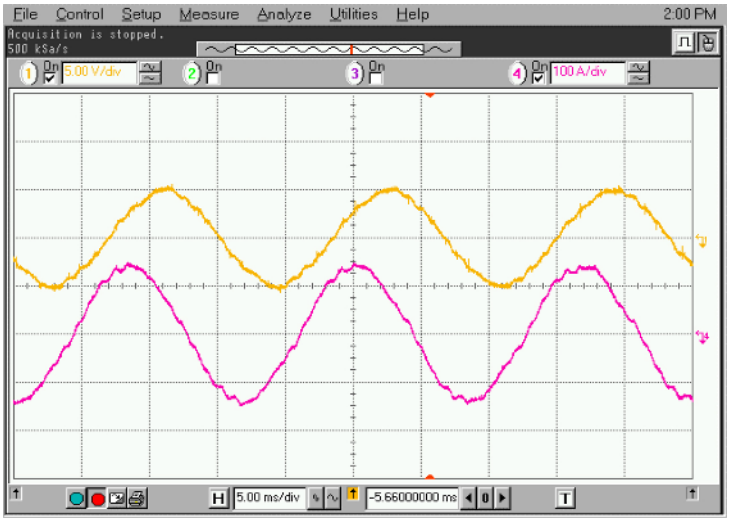
A.2 Examples of practical realized AIC applications

A.2.1 AIC of current source type (CSC)

Figure A.4 shows the power semiconductor current in a realized case. Here, synchronous PWM with selected harmonic elimination is applied. The number of pulses per period is 7; pulse frequency is equal to 350 Hz.

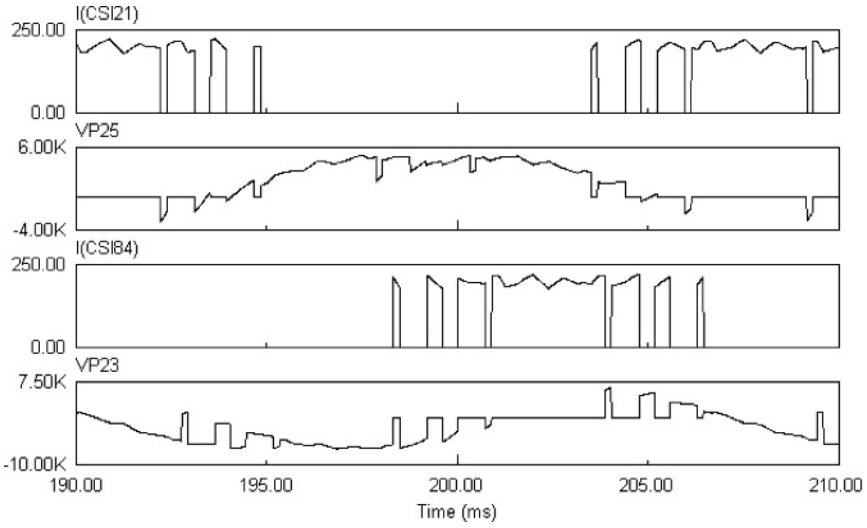
Because of the two stage a.c. side filter inherent to the system the pulse shaped converter currents are strongly filtered. Thus the current fed into the supply network is almost sinusoidal, see Figure A.3.

Realized nominal power 1 MW, supply voltage 4 160 V.



Top: electrical power supply network voltage 6 000 V/div;
Bottom: electrical power supply network current 100 A/div

Figure A.3 – Typical waveforms of electrical power supply network current and voltage for a current source AIC with low switching frequency [33]



Top to bottom: valve device current and valve device voltage of machine side converter, valve device current and valve device voltage of active feed in converter (measurement for SC_{MVA} = 38, normalized to full load current)

Figure A.4 – Currents and voltages in a (semiconductor) valve device of an AIC and a machine side converter both of the current source with low pulse frequency [33]

The electrical power supply network current shows sine shape with superimposed triangular pulsations and, owing to the filter greatly reduced harmonic content. Figure A.5 shows the total harmonic distortion (THD) for the active feed in converter current in a drive.

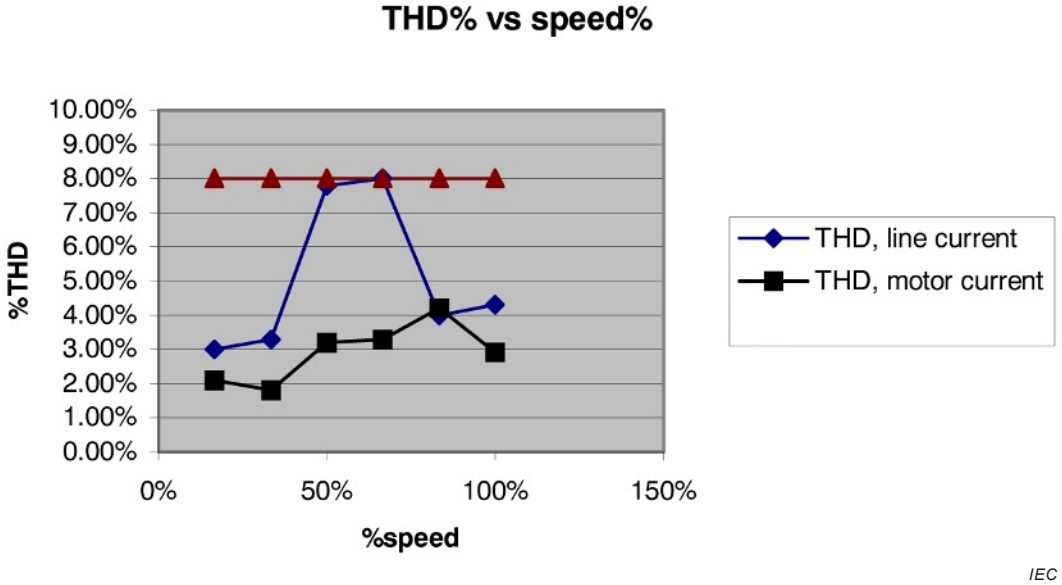


Figure A.5 – Total harmonic distortion of electrical power supply network and motor current [33] remains always below 8 % (triangles in straight line) in this application

A.2.2 Active infeed converter with commutation on the d.c. side (reactive power converter)

A.2.2.1 General function, basic topology

Self-commutated converters with forced commutation on the d.c. side can be realized as pure reactive power converters whereby their inductive or capacitive reactive power consumption can be arbitrarily varied.

For this purpose each arm of the bridge is equipped with switched valve devices with diodes connected in antiparallel (see Figure A.6) which enables the current to flow in both directions.

In contrary to converters with commutation on the a.c. side no current change from phase to phase of the infeed occur but the commutation takes place independently from the neighbour phase between the controlled and uncontrolled valve devices within each phase via the buffer capacitor $C_{B.}$

On the d.c. side only harmonic currents occur because the fundamental currents in the respective phases are totally deleted by mutual compensation. This kind of commutation presupposes that there is only a moderate reactance on the d.c. side while on the a.c. side a considerable reactance is required to limit the harmonic currents.

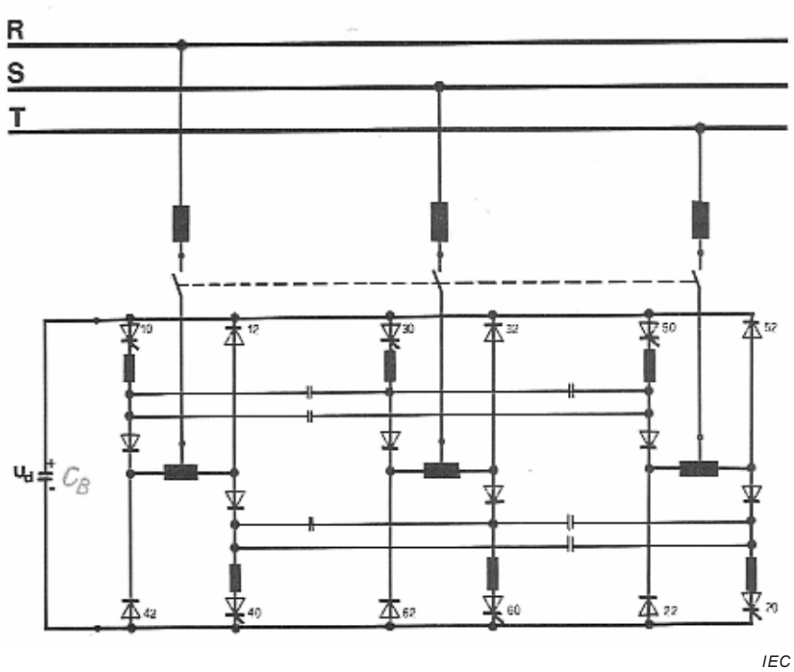


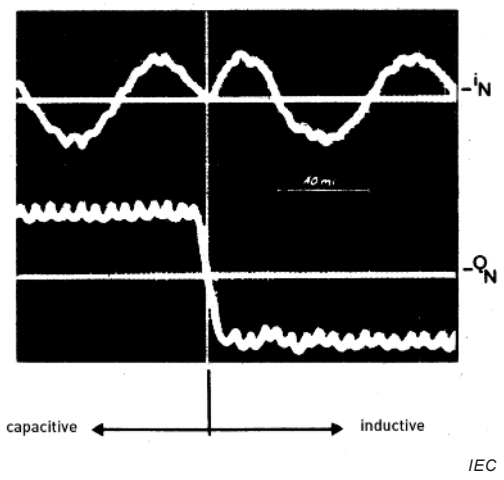
Figure A.6 – Basic topology of an AIC with commutation on the d.c. side (six pulse variant)

A.2.2.2 Power control

By small changes of the firing angle the flow of energy can be continuously controlled so that the fundamental power can lie in all four quadrants within a few milliseconds (see Figure A.7).

A.2.2.3 Dynamic performance

The outstanding dynamic performance of such kind of converter is shown in Figure A.7. The transition from the capacitive operating mode to the inductive one and inversely takes place rapidly with almost no time-delay when the reference value is changed accordingly.



left: capacitive mode; right: inductive mode

Figure A.7 – Dynamic performance of a reactive power converter

A.2.2.4 Distortion of the power supply network

Because of its capability to supply both, inductive and capacitive power in a very short time the Reactive Power Converter is eminently suited for energy management in the power supply network up to several Mvars. In view of the harmonics no intermittent current is flowing on the a.c. side with almost sinusoidal waveform in both operating ranges (inductive and capacitive). Higher frequency distortion does not occur at all (see Figure A.8).

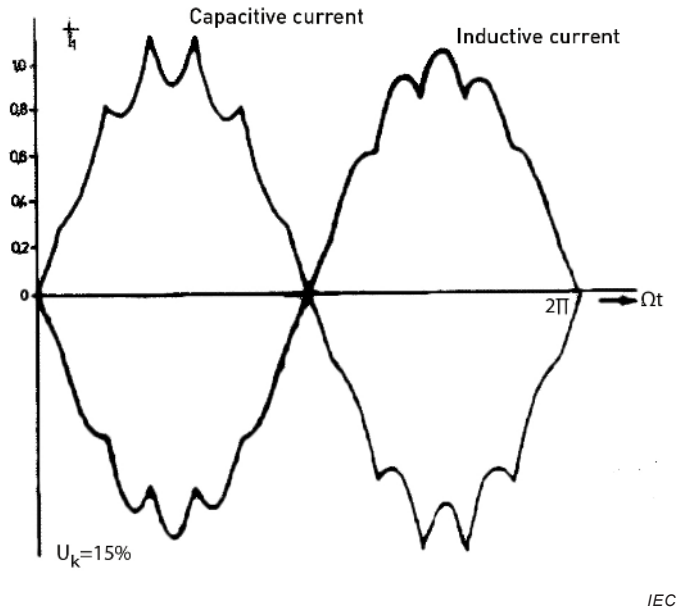


Figure A.8 – Line side current for a twelve pulse Reactive Power Converter in a capacitive and inductive operation mode ($u_{SCV,equ}$ = 15 %)

The rationale of how the a.c. current waveform originates by the rectangular waveform of the converter on the one hand and the sinusoidal waveform of the power supply on the other hand are shown in Figure A.9.

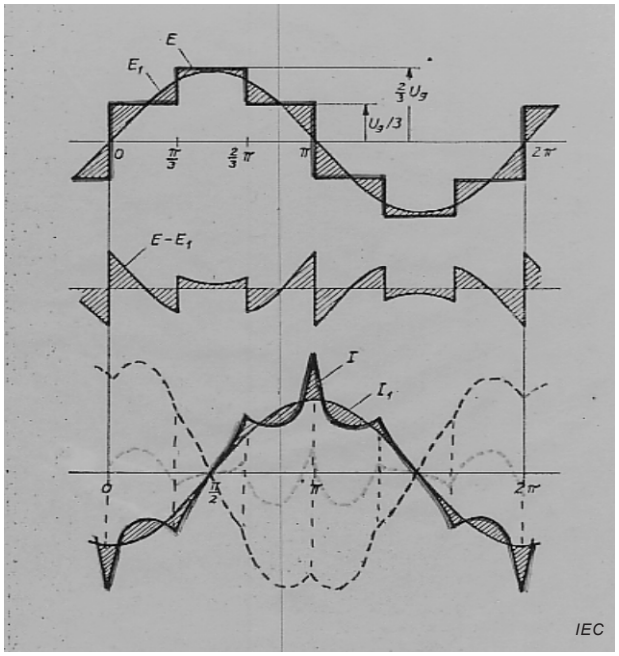


Figure A.9 – The origin of the current waveform of a RPC by the line voltage (sinusoidal) and the converter voltage (rectangular)

A.3 Details concerning two level and multi-level AICs in VSC Topology

A.3.1 Properties of active infeed converters (PWM) with different number of levels

Table A.4 gives a summary of main properties of two level and multilevel AICs in view of the output voltage waveform and the effects on the power supply network.

Table A.4 – Comparison of different PWM AICs of VSC topology

Property	Number of levels (L)					Remarks
	Generally	2	3	4	5	
Number of different potentials in the phase-to-phase voltage	(2L-1)	3 (0; +/- Ud)	5 (0; +/-(1/2)U_d; +/-U_d)	7 (0; +/-(1/3)U_d; +/-(2/3)U_d; +/-U_d)	9 (0; +/-(1/4)U_d; +/-(1/2)U_d; +/-(3/4)U_d; +/-U_d)	Referred to a d.c. line middle potential
Step size of the voltage waveform	1/(L-1)	1	1/2	1/3	1/4	Lower insulation stress
Max. achievable output voltage of the multi-level PWM converter compared to a 2-Level converter	(L-1)	1	2	3	4	Times referred to a d.c. line middle potential
Relative voltage distortion of the power supply network compared to the 2-Level converter.		1 1	1/2 1/4	1/3 1/9	1/4 1/16	– if Z_{mains} is kept constant – if R_{sce} is kept constant

A.3.2 Examples of typical waveforms of AICs

The following pictures show typical waveforms of the line to line voltage at the AIC input and the line current (SCV_{line} = $u_{SCV,equ}$ = 20 % at a switching frequency of 1 kHz).

Figure A.10, Figure A.11 and Figure A.12 are for qualitative illustration of three cases of PWM modulation schemes and different number of levels.

With higher levels, the approach to sinusoidal curve shape improves and the current ripple decreases.

In spite of showing different values for current and voltages the figures are comparable because they are nearly at the same power.

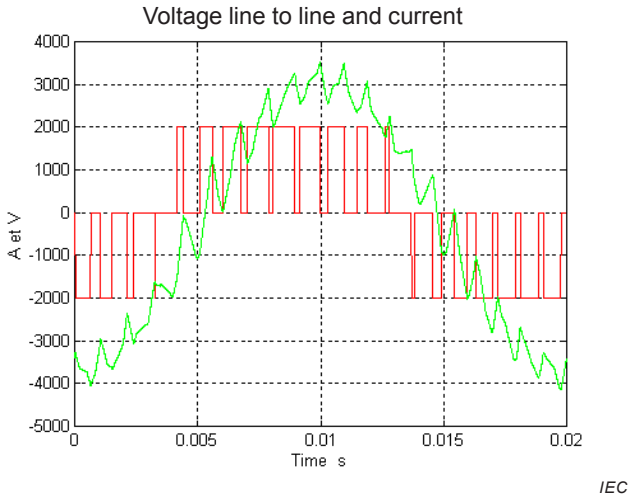


Figure A.10 – Two level topology with nominal voltage of maximum 1 200 V and timescale of 5 ms/div

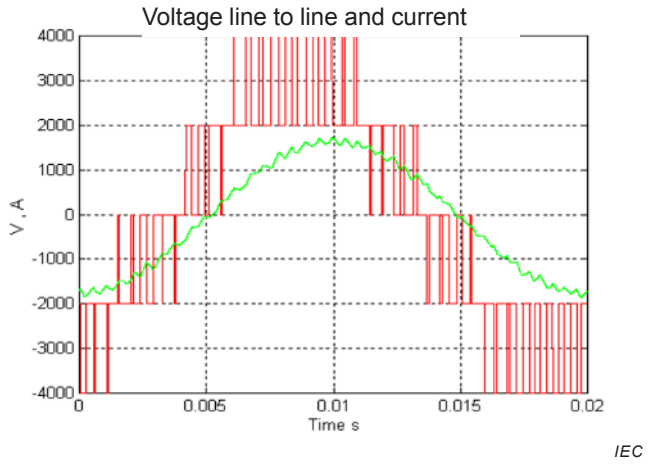


Figure A.11 – Three level topology with nominal voltage of maximum 2 400 V and timescale of 5 ms/div

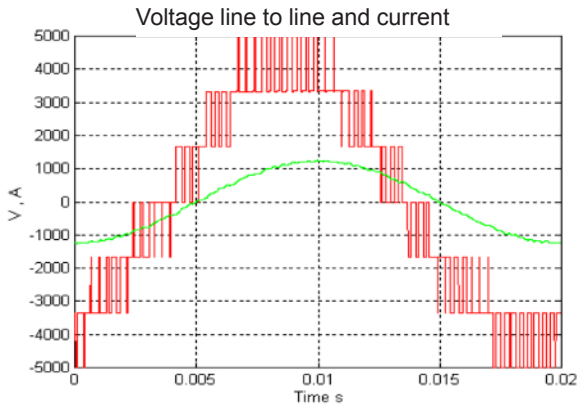


Figure A.12 – Four level topology with nominal voltage of maximum 3 300 V and timescale of 5 ms/div

A.3.3 Construction and realization

For lower output powers, the AICs might be incorporated in the housing of a power drive system or power supply network. Depending on the required power, the AICs might also be commonly designed and manufactured in a rack construction. They are designed as generic models which can be adapted by extension components to customer demands. The state of the art in realized output powers range from several kVA up to several MVA.

Cooling by air, water or air-water exchanger is possible.

The given data of a voltage source AIC in three level topology relate to a single construction in the 2006 market, i.e. without series or parallel connection and without the so-called tandem configuration.

Power range (limited through the semiconductor components):	7 MVA to 9 MVA
Maximum input voltage without transformer:	3,3 kV
Maximum output voltage:	3,3 kV
Usual rated current, r.m.s. value:	1 600 A

Cooling system, usually deionised water

The given data of a voltage source AIC in multi-level topology relate to a single construction unit, i.e. without series or parallel connection and without the so-called tandem configuration.

Power range (limited through the semiconductor components):	0,3 MVA to 5 MVA
Maximum input voltage without transformer:	4,2 kV
Maximum output voltage:	4,2 kV
Usual rated current, r.m.s value:	1 000 A

Cooling system generally air and above 3 MVA deionised water

A.4 Basic transfer rules between voltage and current distortion of an AIC

The voltage distortion depends on the voltage sharing given by the ratio of impedances Z_{equ} (expressed by $u_{\text{scv;equ}}$) to Z_{L}.

Provided this ratio is constant in the frequency range above 2 kHz

- the voltage distortion in the power supply network is almost independent of the pulse frequency, i.e. the amplitude of the voltage distortion does not change when the pulse frequency of the AIC is changed;
- just a small reduction of the distortion can be noticed at increasing frequency because of the non-proportional increase of the power supply impedance compared to the equipment impedance.

In comparison to the voltage distortion (Clause A.4) the characteristic of the current distortion of AIC is quite different. The impact of the most influencing parameters of the AIC as well as the supply system on the voltage and current distortion is illustrated in Figure A.13.

- The pulse frequency of the AIC plays a major role. The higher the frequency, the lower is the current distortion which is emitted to the power supply.
- At lower pulse frequencies the current emission may reach a comparatively high level although the voltage distortion in the network is acceptably low. This is especially the case if the power supply impedance is small compared to the equipment impedance and R_{sce} therefore is high.

Distortion	**Pulse Frequency**	**Rsce**	**kZred**
$U_{LL,\,h}/U_{LL,\,1}(U_{LN,\,h}/U_{LN,\,1})$	**small**	**big**	**big**
I_h /I_{L1} [%]	**big**	**small**	**small**

NOTE kz_{red} is the ratio of the power supply impedance according to 5.2.4 (95 % values) related to the frequency proportional extrapolated reference impedance according IEC 60725.

Figure A.13 – General influence of significant characteristics to the voltage distortion and current distortion

A.5 Examples of the influence of AICs to the voltage quality

AICs can be used to improve the quality of the power supply network voltage. The following case demonstrates a special application with low dynamic requirements of the controlled load; where even at weak power supply networks, exceptional filtering has been applied without any consideration to volume and cost of the filter (they may exceed the converter volume and cost).

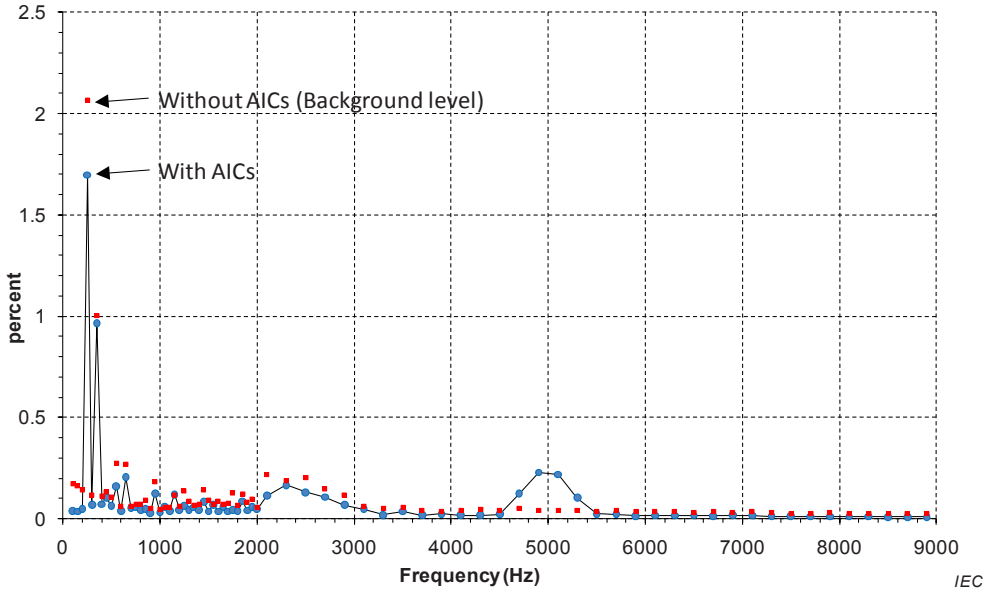
Four AICs with LCL filters and constant pulse frequency, each operating with an input current of 10 A, were connected at one point of coupling of a weak industrial network with a power supply network voltage of 400 V.

The short-circuit power of the 400 V supply was calculated to be 1,3 MVA and the rated current of each AIC was 93 A corresponding to 64 kVA power rating. Thus the R_{sce} for the four AICs together was about 5.

The damping of the LCL filter was realized by the AIC control in such a way that the impedance of the AIC was resistive up to about 1,5 kHz becoming inductive above that. However, no special harmonic cancelling algorithms were used.

The measured harmonic group voltage spectrum without and with AICs is shown in the Figure A.14. As can be seen, at least the tested AICs can significantly improve voltage quality in a wide frequency range. Without AICs the voltage THD calculated up to 2 kHz was 2,4 % and with the AICs 2,0 %. The only increase in the distortion was in the pulse frequency range, in this case 5 kHz, where the voltage distortion was increased above the background level.

NOTE 1 The change in the harmonic levels at 2 kHz is due to the IEC 61000-4-7+ specification where the grouping range is changed from 50 Hz to 200 Hz at that frequency.



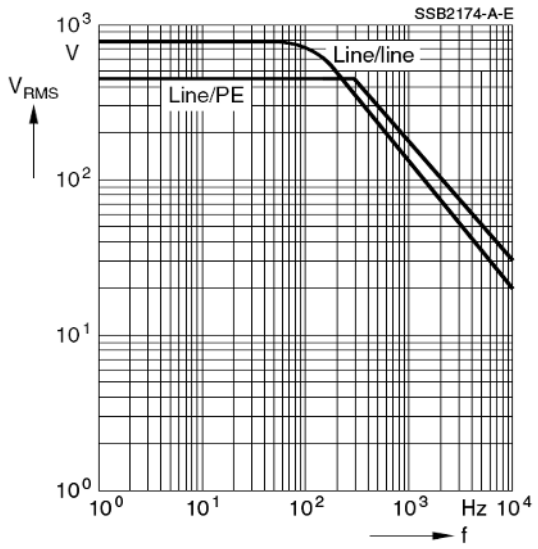
NOTE Harmonic groups shown were measured according to IEC 61000-4-7, R_{SCE} = 5, $u_{scv;equ}$ = 12 %.

Figure A.14 – Measured reduction of voltage distortion when four AICs are connected to the power supply network

A.6 Withstand capability of power capacitors towards distortion in the range of 2 kHz to 9 kHz

A.6.1 General

There is a need to know the withstand capability of capacitors in the frequency range considered. Catalogue data for standard AC-capacitors are usually focused on information about limiting conditions in context at the fundamental frequency.



Formula for calculating the additional heating of the dielectric caused by a singular frequency:

$$\Delta T_n = \frac{10 \times (V_{Mn})^2}{(V_{Gn})^2} [K]$$

V_{Mn} : Value measured at a frequency f_n
V_{Gn} : Limit value for a frequency f_n
ΔT_n : Calculated heating of the dielectric for a frequency f_n

IEC

Figure A.15 – Excerpts from a catalogue information of a power capacitor manufacturer; 760 V AC; (rated voltage: 690 V AC) for temperature calculation

Capacitors which are suited for power factor correction have to have a certain power reserve for additional harmonic load which normally is expressed in percentage of the rated reactive power (e.g.11,5 %) see Figure A.15.

This information can only be utilized for load characteristics with frequencies lower than approximately 1 kHz because the increase of losses due to harmonics is low compared to the fundamental losses in the low frequency range. The majority of losses in this case are determined by the dielectric losses which usually contribute more than 90 % of the total losses of the capacitor at the fundamental frequency.

The loss angle “tan delta” expressed in catalogues is usually representing this loss situation as well.

The losses change considerably when the capacitor is exposed to voltage distortion levels in the higher frequency range (2 kHz to 9 kHz). Here the losses of the capacitor increase rapidly with increasing frequency (see Figure A.16).

This increase is caused especially by the winding losses (P_{Rcs}) within the capacitor which do not play a major role in the lower frequency range.

The impact on the frequency to the dielectric losses (P_{Rcp}) is low compared to the winding losses because of the linear characteristic in comparison to the square root characteristic of the winding losses. Due to this fact R_{cp} can be assumed to be independent of the frequency as a first approximation. Also the inductive reactance of the capacitor can be left out of consideration because the internal resonance frequency of capacitors is generally >10 kHz.

There is also no need to consider chokes which are accommodated inside of the capacitor with the objective to avoid undesirable resonances in the low frequency range and which is tuned accordingly. Combinations of this kind present almost a pure inductance for 2 kHz to 9 kHz signals and therefore have no problem to cope with such signals at all.

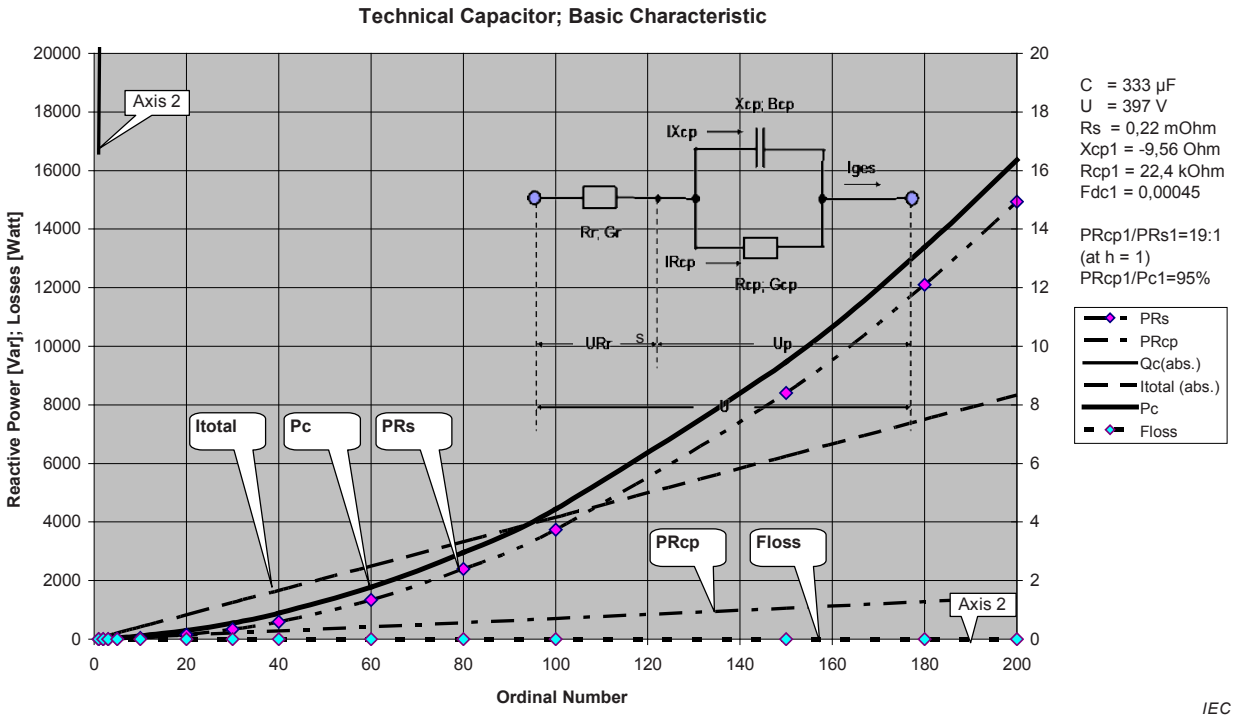


Figure A.16 – Reactive power and losses of a power capacitor supplied by a source with constant reference voltage and variable frequency (R_{cp} = f(h))

Additionally the following features have to be considered.

- The danger of an electrical defect due to distortion in this frequency range is primarily determined by over-current (not by over-voltage).
- Power capacitors are more prone to overload by distortion in this frequency range than small ones because the wiring losses are usually higher. Additionally fuses are sometimes used to protect the discrete capacitor elements within encased capacitors which often lead to additional wiring losses.

As conclusion for that one can generally say that considerations about the withstand capability of capacitors towards distortion in the frequency range between 2 and 9 kHz can be focused solely on power capacitors which represent the “worst case” victim in this respect.

A.6.2 Catalogue information about permissible harmonic load

Some capacitor manufacturers provide pertinent documentation about the capability of their capacitors to cope with additional harmonic load, also in this frequency range see Figure A.17.

Figure A.17 shows an example which allows the calculation of the dielectric temperature as result of this load.

A.6.3 Frequency boundaries for permissible distortion levels

A more general method is based on complex calculation and allows a general prediction for the capability of capacitors to withstand harmonic stress in the considered frequency range, derived from fundamental data.

The increase of losses leads to an increase of the apparent power and to an increase of temperature within the capacitor as well. Typical results for the loss situation at different distortion levels which might occur in the power supply voltage are shown in Figure A.17.

The results are independent from catalogue data and based on a loss ratio at the fundamental frequency of PR_{cp1}/P_{c1}=95 % which reflects the practical situation. The boundary, up to what frequency the assumed distortion level can be permitted without an inadmissible temperature rise of the capacitor can be derived from the point of intersection between the total losses which actually occur (at a singular frequency) and a loss limit which has been specified at $2 \times P_{c1}$ (total losses at the fundamental frequency) as an adequate permissible maximum value.

NOTE The expedience of this loss limit which leads to a reasonable temperature rise of 10 °K within the capacitor caused by distortion can be verified by comparison with capacitors where the information about this temperature rise is available and confirmed by capacitor manufacturers. For the loss angle of capacitors a tan delta of 0,000 45 or better is assumed.

Attention has to be paid to the fact that these results are still related to one distortion signal which based on a singular frequency (one frequency predominates). Such situation is indeed conceivable in practice too because the power supply network itself has the tendency to prefer a frequency which is exact or near by the frequency of its own network. In such cases the upper dashed curve shall not be exceeded.

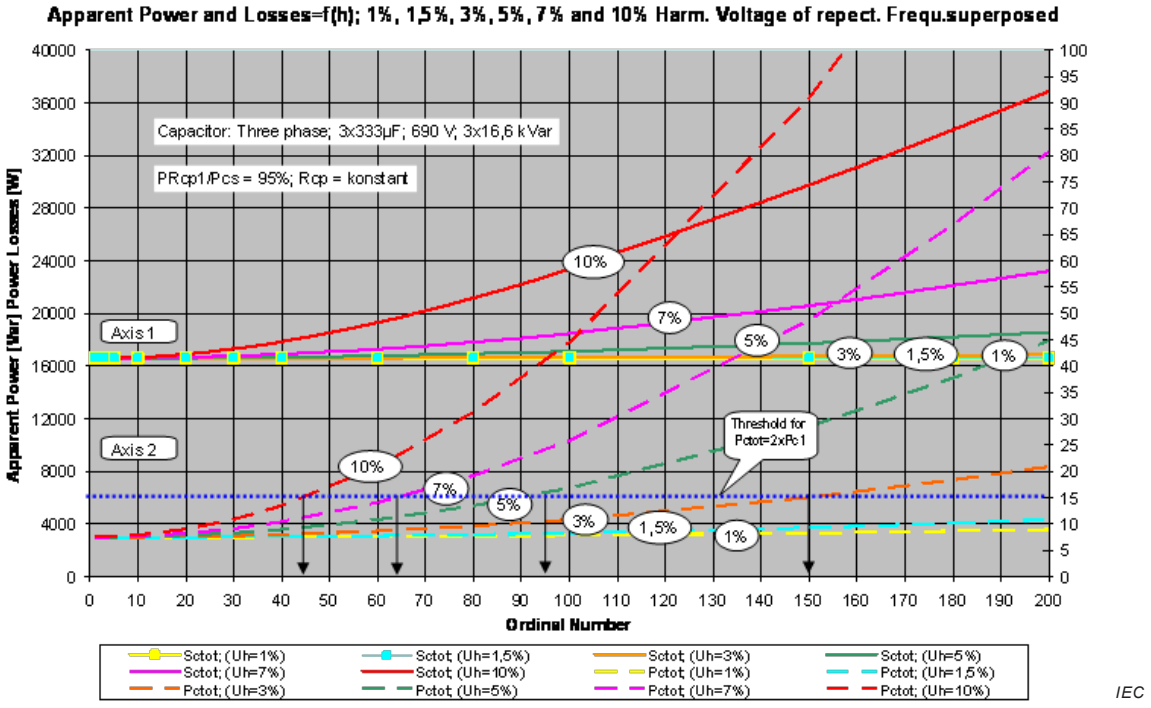


Figure A.17 – Apparent power and losses of a typical power capacitor at different voltage distortion levels and the critical frequency boundaries (at singular frequency) where the temperature rise reaches substantial values (vertical arrows)

A.6.4 Frequency spectrum of active infeed converters

If several AICs influence the distortion characteristic of the network, a frequency spectrum will occur (see Figure B.2).

Because each spectral line of the spectrum leads to another temperature rise within the capacitor one cannot decide whether the capacitor is overloaded or not, before this spectrum is known. For a control which based on synchronous pulse pattern distortions occur near the pulse frequency and integer multiples of it, as shown in 6.6 and Figure B.2.

For the stipulation of limits the 2-Level topology is the appropriate solution which has to be taken into consideration for that purpose. When the compatibility with this type of equipment is fulfilled, all other types based on PWM technology are also covered Table A.4.

To orientate the limits to this spectrum implies besides an advantage for practical use, because the ratio of the amplitude of a singular frequency which causes a certain temperature rise within the capacitor and the maximum of the highest spectral line of the frequency spectrum which effects the same temperature rise, is fairly constant and almost independent from the chosen pulse frequency.

This feature makes it possible to carry out the distortion measurement in the test laboratories instead on site (a suited artificial network provided).The ratio is even constant if the network impedance changes and the voltage distortion changes accordingly (see Figure A.18).

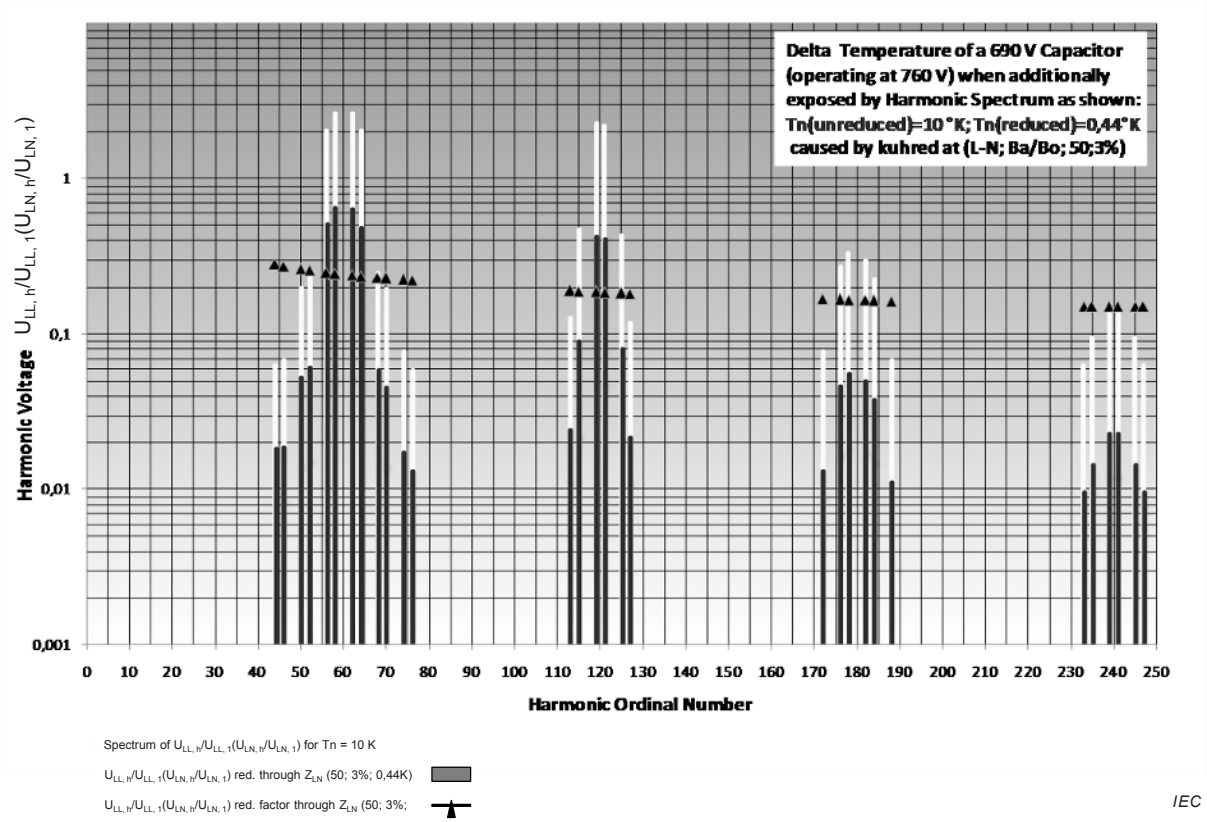


Figure A.18 – Voltage spectrum of an AIC and the impact of a line impedance reduction to the temperature of the capacitor (from 10 K to 0,44 K) and the composition of the spectrum

A.6.5 Conclusion

Capacitors being connected on networks where AICs are operating in parallel are sufficiently protected against overload, when the sum of the highest occurring spectral line of all AICs together do not exceed the voltage distortion which is shown in Figure B.1 as bottom curve and which ensures their withstand level in this respect.

The condition is also satisfied if each single AIC in combination with the network condition on site (R_{sce}) fulfils the boundaries which are expressed in Figure B.1 and Figure B.2 accordingly.

A.7 Impact of additional AIC filter measures in the range of 2 kHz to 9 kHz

A.7.1 General

As long as no other way is known to meet very strict requirements for permissible distortion than using huge passive filter circuits (necessarily tuned to higher frequencies, (i.e. usually >1kHz), the probability increases that problems occur in the lower frequency range. This is caused by resonances with the consequence of overload and voltage stress for all electric components being used in the network itself (generators, transformers, capacitors, cables, etc.) and for all components being connected thereto.

In the past a lot of examples have shown that overload or voltage stress problems on electric components were predominantly caused by resonances or cumulating effects instead of loads issued from the normal operating conditions of electric equipment which operate correctly or from voltage distortion levels which occur under normal operating conditions of the equipment without such effects.

Conventional equipment with non-linear load characteristic draw non-linear currents from the power supply network which contain low order harmonics (usually <1,5 kHz).The probability that overload and stress problems occur, increases rapidly when the non-linear current with a given frequency encounters a resonance in the network with the same frequency.

Since decades, the technicians pay attention to avoid such coincidences if imaginably possible. If filter circuits had to be installed in the past (for improving the power factor for example), it was strictly noted that the filtering procedures were started at the lowest frequency before filter circuits for higher frequencies were allowed to be switched on. The target was all the time to avoid resonances in the lower frequency range if possible. The less the natural damping effects of the network, the greater the need to follow this rule.

To follow it in the range of 2 kHz to 9 kHz is very difficult and mostly impossible. The application of filter measures in a great extent is inevitable if the requirement for the compliance of a low distortion level for a specific frequency is very strict. The current practice is therefore to install huge filter circuits with focus on a dedicated frequency in order to fulfil the requirements at the given target and to disregard undesired effects at this stage which might occur in the network later on by the mentioned coincidence with other equipment (in case of new installations or changing the network configuration for example).

A.7.2 Example of a PDS constellation (AIC and CSI)

A.7.2.1 General

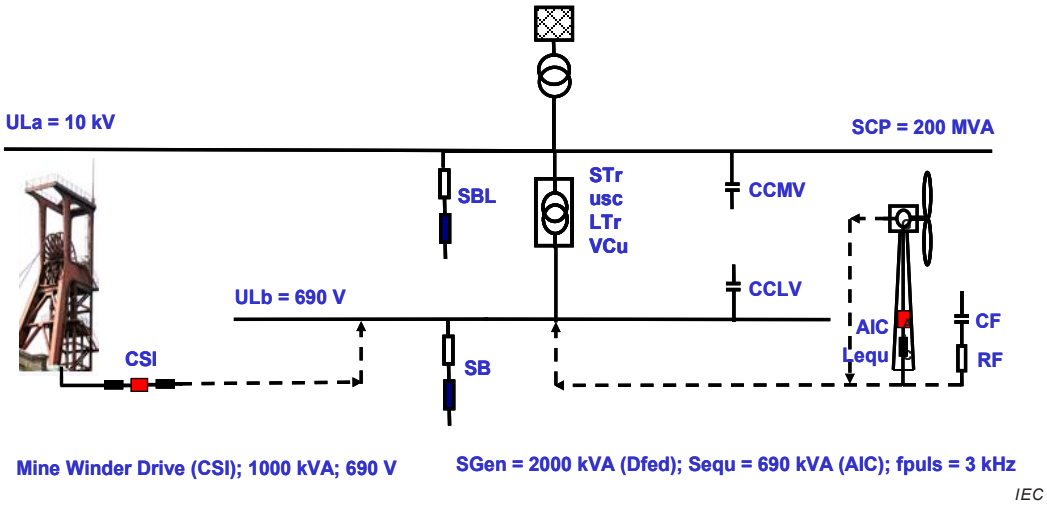


Figure A.19 – A wind turbine plant and a mine winder drive connected on the same power line

The AIC of the example is arranged in the rotor circuit of a double-fed asynchronous machine used for a wind generator. It is a two-level PWM voltage source inverter with a pulse frequency of 3 kHz, equipped with large filter circuits with the aim to reduce the voltage distortion near the pulse frequency to a voltage distortion level of 0,2 % in the MV network. The CSI is a d.c. drive for a main winder with impressed current characteristic generating typical harmonics at the ordinal number like the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{th}, 25^{th}, etc. Both converters are connected on the same power supply (Figure A.20).

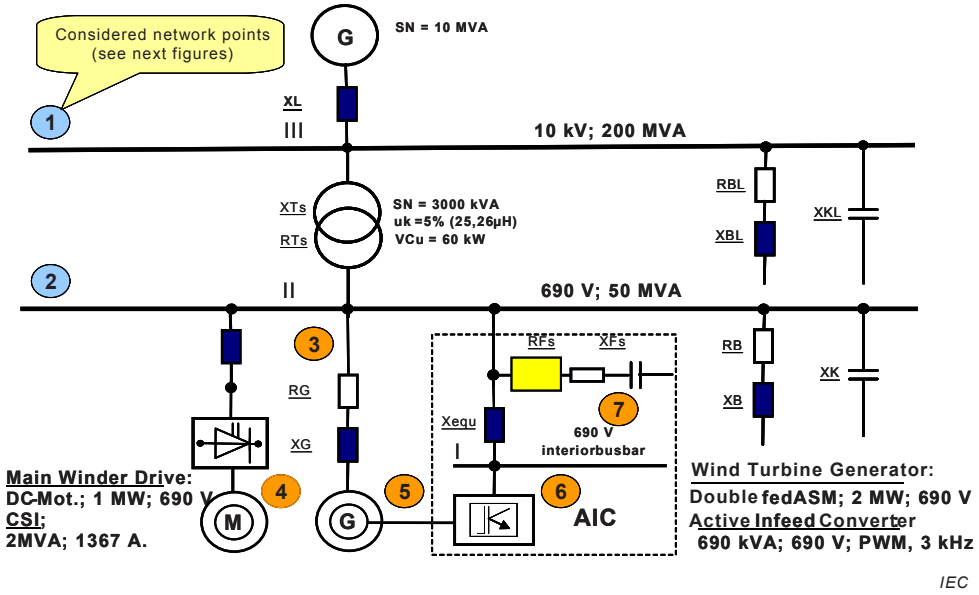


Figure A.20 – Power supply network configuration for the plant of Figure A.19 with allocated measurement points

A.7.2.2 Harmonic current behaviour without and with an AIC-filter

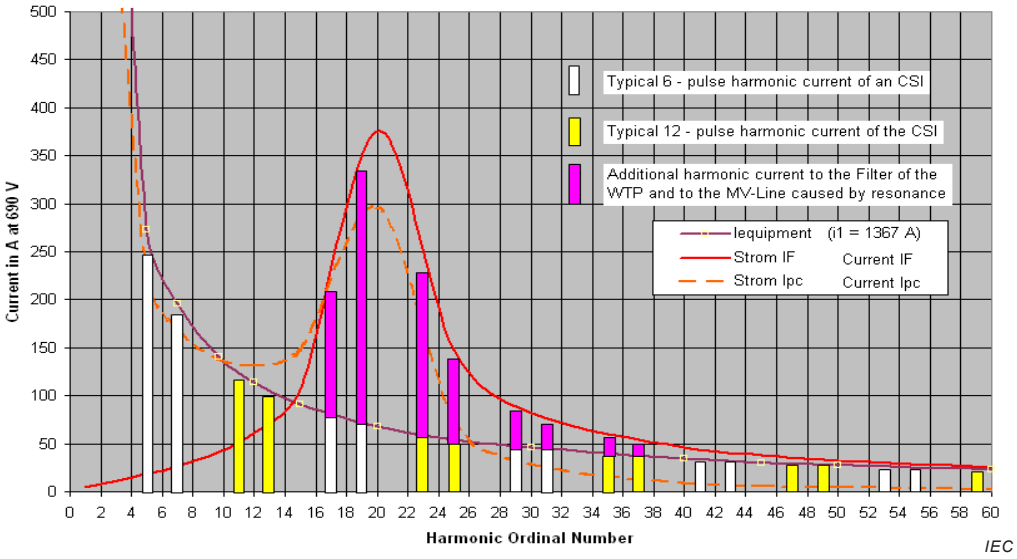


Figure A.21 – Regular current of the CSI (AIC-filter disabled) and amplification of the current in case of resonance caused by the AIC-filter circuit (when AIC filter is enabled)

A.7.2.3 Data for the voltage level on the power supply network with AIC filter enabled and disabled

The voltage distortion level for two specific frequencies is considered in Figure A.21. The frequency 3 kHz is in accordance with the pulse frequency of the AIC. The target in this case was to reduce the distortion level on the MV power supply line for this frequency from 1,3 % to 0,2 %. 1 kHz corresponds to the frequency where the resonance occurs if the filter circuit is switched on. The target of the intended effect at 3 kHz is achieved by the filter circuit, but the total harmonic situation has been changed for the worse. Table A.5 shows the voltage distortion dependency on filter circuits and the current distribution.

Table A.5 – Voltage distortion on both power lines (II and III) without and with filter circuit (the filter had been designed to achieve 0,2 % distortion level on the MV-power line)

Voltage distortion Uh/UL1 on the MV – busbar no. III			Filter circuit switched off	Filter circuit switched on	Remarks
①	3 kHz	Caused by CSI	–		
	3 kHz	Caused by AIC	1,3 %	0,2 %	Intended effect
	1 kHz	Caused by CSI	0,6 %	3,2 %	Unintended effect
	1 kHz	Caused by AIC	–		
Voltage distortion Uh/UL1 on the LV – busbar no.II			**Filter circuit switched off**	**Filter circuit switched on**	**Remarks**
②	3 kHz	Caused by CSI		–	
	3 kHz	Caused by AIC	5,5 %	0,5 %	Intended effect
	1 kHz	Caused by CSI	2,6 %	15,0 %	Unintended effect
	1 kHz	Caused by AIC		–	

A.7.2.4 Data for the current on the specific points with AIC filter enabled and disabled

For comparison purpose the fundamental and the r.m.s. current is also mentioned in the table. With the exception of the CSI for all components of the network the harmonic load increases considerably when the filter is switched on (note the square root addition of the fundamental and the harmonics in this context).

The only reason why the increase of the r.m.s. value for the transformer and the generator is comparatively low in comparison to the filter circuit is, because they have a big power reserve available due to the high fundamental current value.

The filter circuit however has just been designed for the purpose to absorb the 3 kHz harmonic current (64 A), superimposed to the fundamental current (125 A). (i.e. I_{RMS}=141 A in total). The r.m.s. overload for the filter capacitors amounts hence to 285 % referred to its rated load. It is obvious that the capacitors of the filter circuit are seriously endangered in this case. The effect can occur in other LV and MV power supply networks alike.

Table A.6 – Current distribution within the network described for specific frequencies and on allocated measurement points as pointed out in Figure A.20

Some accentuated currents of the main components			Filter circuit switched off	Filter circuit switched on	Remarks (Overload-Factor)
③	Transformer	I_1 [A]	1024	1027	
		I_{19} [A]	55	267	4,85
		I_{60} [A]	47	2	
		I_{RMS} [A]	1027	1061	1,03
④	LV-CSI	I_1 [A]	1367	1367	
		I_{19} [A]	72	72	
		I_{60} [A]	5	5	
		I_{RMS} [A]	1369	1369	
⑤	LV-Gen.	I_1 [A]	357	358	
		I_{19} [A]	16	76	4,75
		I_{60} [A]	14	1	
		I_{RMS} [A]	358	366	1,02
⑥	LV-AIC	I_1 [A]	58	58	
		I_{19} [A]	4	4	
		I_{60} [A]	56	64	lower impedance
		I_{RMS} [A]	81	86	1,06
⑦	LV-Filter	I_1 [A]	0	125	
		I_{19} [A]	0	376	Note: I_{19}/I_1
		I_{60} [A]	0	66	
		I_{RMS} [A]	0	402	2,85! (402/141)

A.7.3 Conclusion

The ambitious target to achieve a very low distortion level for the pulse frequency range of the AIC entails large filter circuits.

These circuits are predominantly composed of capacitors. The chokes are negligible (and sometimes not existent at all) in view of the high frequency and because they impair the desired effect to achieve low level distortion near the pulse frequency.

As a result, the natural frequency of the network is displaced to a quite lower frequency range where usually conventional equipment based on non-linear load with impressed current characteristic generate harmonic currents with the same frequency.

Due to this coincidence considerable accentuations of harmonic currents occur caused by resonance magnification at lower frequencies, which entail overload and stress problems in the entire network.

In order to avoid such effects it should be seriously contemplated to stipulate the highest possible values for the distortion limits in the frequency range considered.

A.8 Example of the power supply network impedance measurement

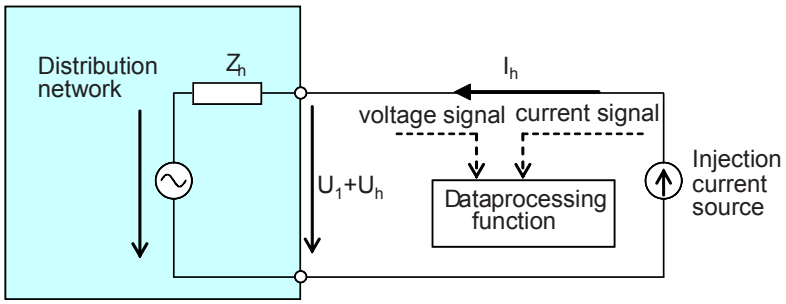
A.8.1 General

This annex introduces the technical trends to compliment 5.2.4 from the aspect of the power supply network impedance measurement.

A.8.2 Basic principle of measurement

A literature survey was performed to find technical background on the measurement of the power supply network impedance. The survey found especially five published papers [17] to [21] and an appropriate measuring device for the use on power supply networks. They describe basically the same principle; injection of harmonic current and analysis of the harmonic voltage component (see Figure A.22). In this annex, the measurement methods described in the reference papers are briefly introduced.

The voltage and current are measured with appropriate voltage and current sensors and introduced to data processing function. The function is generally made of A/D (Analogue to Digital) converters and numerical processors.



U_1: Fundamental voltage at zero impedance for h-th harmonics
U_1+U_h: Fundamental + h-th harmonic voltage
I_h: h-th harmonic current
Z_h: h-th harmonic impedance

IEC

Figure A.22 – Basic principle of impedance measurement

In the function, a Fourier transformation or equivalent analysis is performed to calculate the voltage component U_h and current component I_h at h^{th} harmonic frequency.

The power supply network impedance Z_h at the frequency is given by complex quantities with real and imaginary parts, which indicate the resistive component and inductive or capacitive component for the impedance, as $Z_h = U_h / I_h$.

By changing frequency, the impedance versus frequency characteristics can be obtained.

In the actual measurement, the cautions to already existing harmonics component in the power supply network, measurement errors of voltage and current etc. should be taken into consideration appropriately.

A.8.3 Harmonic component injection methods for measurement

Although the basic principle is the same, differences among the references from viewpoint of injection methods of current harmonics components may be found.

Method A: Current injection by disturbance. Injection of a current component with a wide frequency range, generated by a transient phenomenon, such as switching on and off a resistor or a capacitor to the power supply network. This might need shorter time for measurement because the method generates wide range of frequencies at a time.

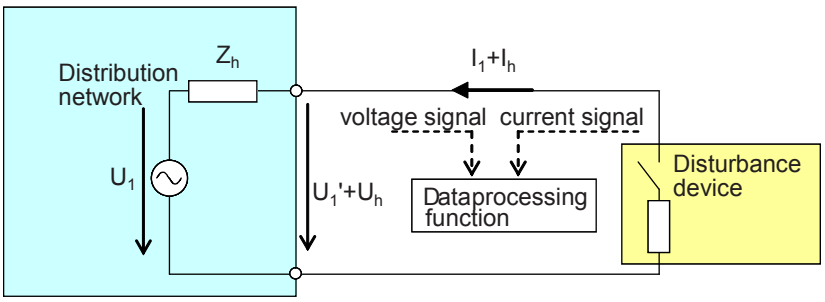
Method B: Sinusoidal single frequency injection. A method to inject a sinusoidal current component of a single frequency by an amplifier or equivalent device. This might require longer time for frequency scanning in case of measuring the impedance characteristics for a wide frequency range.

A.8.4 Harmonic current generation by disturbing device

A paper [17] discusses the measurement of the harmonic impedance of the distribution system. The paper introduces a disturbance device to generate and inject the harmonic current component into the power supply network as shown in Figure A.23.

As disturbing devices, the paper introduces capacitors or resistors provided with switches. The paper further introduces phase-controlled thyristor switches. The disturbance device conducts current components of wide frequency range including the fundamental frequency component.

In Figure A.23, only the fundamental component and the h^{th} harmonic components are shown for simple illustration.



$U_1'=U_1+Z_1 \cdot I_1$ U_1': Fundamental voltage across terminals
I_1: Fundamental current
Z_1: Impedance at fundamental frequency

IEC

Figure A.23 – Harmonic current generation by disturbing device

The paper also indicated the data processing system in the impedance measurement device with two A/D converters synchronized to measure the voltage and the current. Some notes are described for minimizing phase error between the voltage component and the current component.

A.8.5 References based on current injection by disturbance (Method A)

A.8.5.1 A measurement device based on resistor switching

A measurement device [18] is available on the market and used for measuring the power supply network impedance as shown in 5.2.4. In the measurement device, resistors are provided with semiconductor switches for three phases.

Figure A.24 shows the circuit for one phase. By switching on and off, the current flows through the resistor including harmonic components generated by the switching. At the same time, the voltage across the terminal is measured and analyzed. Although the detailed data process is not shown by the manufacturer, the measurement is performed based on the principle described in A.8.2.

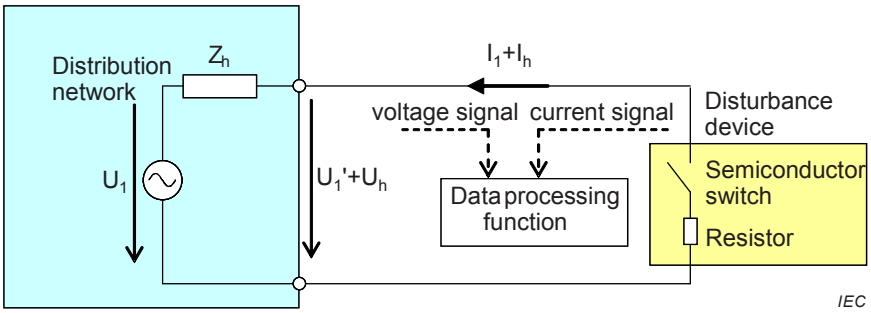


Figure A.24 – Measurement by switching a resistor

A.8.5.2 Harmonic current generation by capacitor switching

A paper [19] focused on the transient oscillation phenomena when the capacitor is switching into the power supply network as shown in Figure A.25. The paper analyzes the transient waveform theoretically, develops a method to calculate the resistance and inductance of the network impedance and finally performs measurement in an actual distribution network rated at 100 V in a building. The measurement is done for around 4 kHz to 10 kHz.

The paper discusses the measurement errors and proposes a method to improve the measurement accuracy by applying two capacitors with different capacitance. With the proposed method, sufficient results are obtained with economical measuring devices widely available in the market.

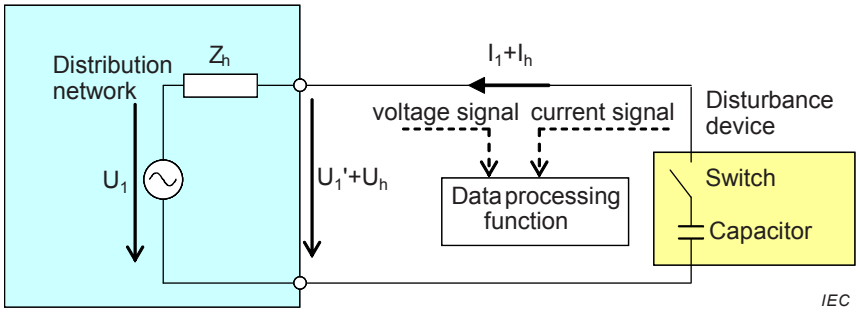


Figure A.25 – Measurement by a capacitor bank

A.8.5.3 Interharmonics signal injection

For distributed generation like an in-house generator, it is sometimes required to detect disconnection and islanding from the power supply network. A paper [20] introduces a method to detect islanding by measuring the 6,6 kV power supply network impedance seen from the in-house generator. If the impedance increases higher than normal range, then, the generator is considered to be islanded from the power supply network and disconnected from the power supply network.

The feature of the paper is to use interharmonics between 2nd harmonics and 3rd harmonics. The idea is from the fact that the interharmonics components are negligibly small on the power supply network. The high precision of measurement is expected with small signal injection of inter-harmonics component to the power supply network.

The proposed impedance measurement system consists of the interharmonics frequency generator, the amplifier, the insulation transformer, the voltage transducer, the current sensors and the impedance measurement function as shown in Figure A.26.

Because of the objective, the measurement system uses only a single frequency. The paper does not cover wide range of frequency. However, the structure of the impedance measurement system is very similar to that in 5.2.4.

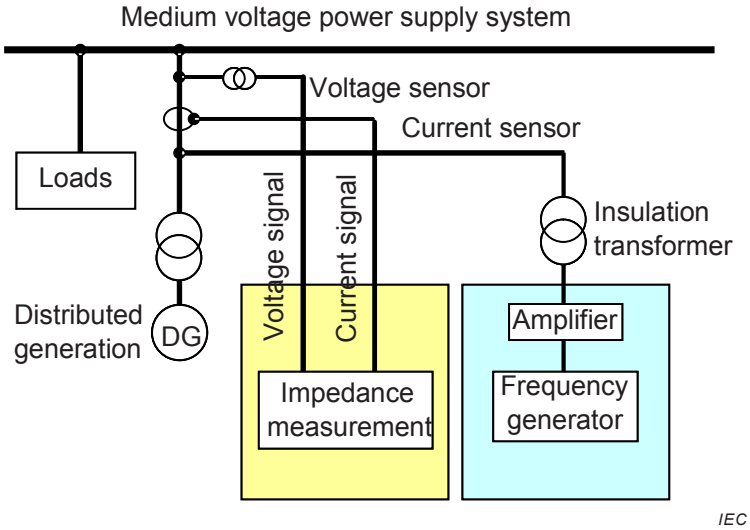


Figure A.26 – A 6,6 kV power supply network impedance measurement system for islanding detection by injecting interharmonics

A.8.6 References based on sinusoidal single frequency injection (Method B)

A.8.6.1 Measurement of line impedance with sinusoidal signal injection

A paper [21] proposes a line impedance measurement system and shows some results of measurements performed on lines in a U.S. university building in the frequency range from 50 Hz to 30 kHz.

The measurement system consists of two blocks similar to Figure A.26. The first block is for current injection of a frequency to the line. The second block is for measurement and analysis of current and voltage.

The first block consists of a sinusoidal signal frequency generator and an amplifier. The output of the amplifier is connected to the line through an isolation transformer. Between the transformer and the amplifier, a filter is connected to reject the fundamental frequency component and to protect the amplifier. The current amplitude injected to the line is set small to be two orders smaller than the line current rating so that the injection does not disrupt operation of other equipment on the line.

The second block consists of a current sensor, a voltage sensor and signal analyzers. The current signal and the voltage signal are introduced to the signal analyzers through tuned filters. The band widths of the filters are set narrow to eliminate effects from noise signals. The signal analyzers output the amplitudes and the phases of the current and the voltage. With these data, the line impedance are calculated and plotted for various frequencies with a personal computer connected to the analyzers.

A.8.6.2 Measurement of line impedance with a voltage source converter

Another paper [22] proposes a different measurement method with a voltage source converter and shows some results of measurements performed on lines in a German university building in the frequency range from 100 Hz to 10 kHz.

The measurement system consists of two blocks similar to Figure A.26. The first block is for current injection of a frequency to the line. The second block is for measurement and analysis of current and voltage.

The paper applies a three-phase PWM voltage source converter to generate and to inject the high frequency current components to the line. The converter output is controlled with the “tolerance band control” which generates current component of measurement frequency. Then, the converter is connected to the line with a transformer. The converter works as a high frequency component generator as well as the amplifier.

The second block consists of a current sensor, a voltage sensor and a FPGA based circuit. The current signal and the voltage signal are introduced to the FPGA through A/D converters with sufficiently high sampling speed. In the FPGA, DFT algorithm is implemented and the signals are analyzed. With the analyzed data, the line impedance are calculated and plotted for various frequencies with a personal computer connected to the analyzers.

Annex B
(informative)

B.1 Basic considerations for design recommendations of AICs in the range of 2 kHz to 9 kHz

B.1.1 Overview

Warning: The recommendations of maximum emission values for conducted emissions <150 kHz defined in this document are based on observations and experience gained made with state of the art AICs operating today in most power supply networks together with other equipment without creating intolerable interference.

B.1.2 General

Nevertheless it has to be highlighted that electromagnetic environment is subject to changes e.g. because of smart grid deployment and that emission limits that are currently under development by the IEC EMC Committees may be different to the maximum emission values recommended in this document.

The voltage distortion on the common power supply network is the main effect that may disturb those electric devices which are connected to the same supply system and which are operating in parallel.

Therefore it seems to be useful to define design guidelines for recommended maximum voltage distortion on the system regardless of the fact that the limitations of the permissible harmonic current for each single AIC unit is mainly considered for practical and measurement reasons.

The recommendations of emission values for conducted emissions < 150 kHz caused by AICs and the recommendations of boundary values for the withstand capability of significant products being exposed to emissions in the range of 2 kHz to 9 kHz are based on investigations, measurements and observations made on EMC-sensitive products and on state of the art AICs which operate today in most power supply networks without creating intolerable interference and should lead to an increased acceptance of using AICs.

Due to the special characteristics of the AIC in terms of its different behaviour on different networks (see 5.2.3.2), a current limitation seems to be inappropriate because the power supply network itself is part of its inherent current emission characteristic.

In this respect, some basic conclusions have been given in Clause A.4 in conjunction with the following main dedicated decisive conditions:

- power supply impedance (Z_{LN} see 5.2.4),
- equipment impedance ($u_{\mathrm{scv,equ}}$ see 3.13),
- short-circuit ratio (R_{SCe} see 3.28),
- cumulative effect for several AICs connected to the same point of coupling.

With regard to the power supply impedances, the latest measurement results derived from studies in Germany 2010 (see 5.2.4) have shown generally lower impedance values than currently stipulated in the measurement standard IEC 61000-4-7.

In cases when overhead lines are excluded, the given impedances for three phase systems from IEC 61000-4-7 are not appropriate.

B.1.3 Withstand capability of power capacitors connected to the power supply network and recommendation for the compatibility in the frequency range 2 kHz to 9 kHz

Based on long term experience, the power capacitors widely used in power supply networks e.g. for reactive power compensation, passive harmonic filters and starting of motors are especially defenceless against harmonic distortion in the supply voltage. Therefore this electrical component plays a major role in terms of proposing guidelines in the considered frequency range.

NOTE EMC capacitors are generally not negatively affected by frequencies in this range.

It should be distinguished between the sensitivity for a certain harmonic distortion which results from the basic characteristics of the equipment/component and the sensitivity which results from the used configuration or the construction of the equipment.

It is also not economically useful to only keep the disturbance level particularly low in order to avoid mechanical resonances in apparatus which may even partly generate noises at relatively low levels of harmonic voltage.

Such cases are better solved by increasing the immunity of the disturbed equipment if changing the pulse frequency of the AIC does not lead to the mitigation.

The result is summarized in Figure B.1 and B.1.4.

B.1.4 Basic conditions for setting the capacitor withstand capability curve

The results are given in Figure B.1.

a) Temperature rise of the capacitor should keep a maximum of 10 K due to harmonics in this frequency range.

b) Typical harmonic frequency spectrum of a two-level PWM-AIC is considered with no additional mitigation measures.

   NOTE Only the actual line inductance which is connected between the AIC and the power supply network has been considered.

c) Definition of the harmonic voltage distortion level is derived from the line to line voltage distortion according to 3.34.

d) Relation factor between a single dominant frequency and the highest occurring spectral line for a single phase (three phase) PWM-AIC equals F=2,5; (F=2,4).

NOTE See the small distance between the dashed limit curves in Figure B.3 and Figure B.4. Because of the small difference only the relation factor 2,5 has been used to stipulate the lower limiting line of Figure B.1. The difference causes some more effect and has been considered accordingly.

e) Coincidence factor (if several PWM-AICs are operating on the same power supply) as the superposition of the harmonic distortions in the line to line voltage equals 1,67 times the single distortion value.

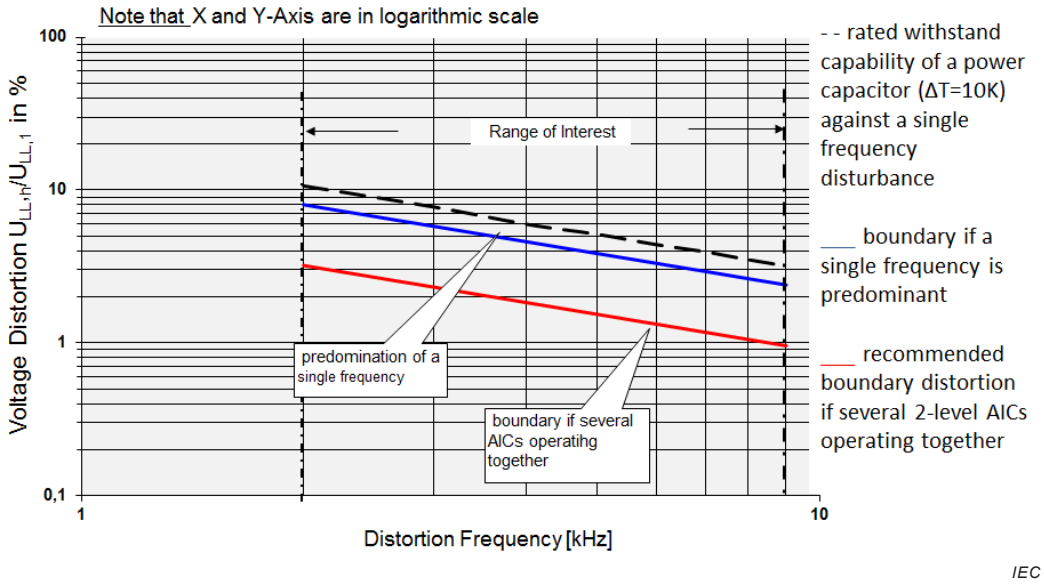


Figure B.1 – Withstand capability level towards harmonic voltages in the power supply network in view of permissible temperature rise within capacitors if the voltage distortion is determined either by one predominating frequency (upper line) or if the distortion is predominantly determined by a harmonic spectrum, caused by several parallel operated AICs (2-Level PWM) (lower line)

The dotted curve in Figure B.1 considers just one single dominating distorting frequency and is generally confirmed by power capacitor manufacturers as being permissible for those devices.

Regarding manufacturing tolerances of real capacitor types and possibly further safety margins, an appropriate distance of approximately 30 % between the dotted limit curve and the dashed curve for one dominating frequency were assumed. Such cases sometimes may exist e.g. for power supplies with distinctive resonances whereas the dotted line can also be regarded as a limit line. However in context with a typical AIC distortion, which is based on a harmonic spectrum, the dotted line should be used for comparison purposes only.

Figure B.1 represents the boundary which shall not be exceeded by the highest appearing spectral line of such a spectrum. The curve should also not be exceeded even if several AICs are operating simultaneously on the same power supply line.

It is typically correct and a good approximation that the distances between the solid limiting curve and the dashed (one dominating frequency) line are fairly constant and independent from the chosen pulse frequency of the AIC.

Therefore the solid curve in Figure B.1 also reflects the limit for the withstand level in the power supply network when AICs are predominating.

A typical harmonic frequency spectrum with acceptable temperature increase of a power capacitor not exceeding 10 K is shown in Figure B.2.

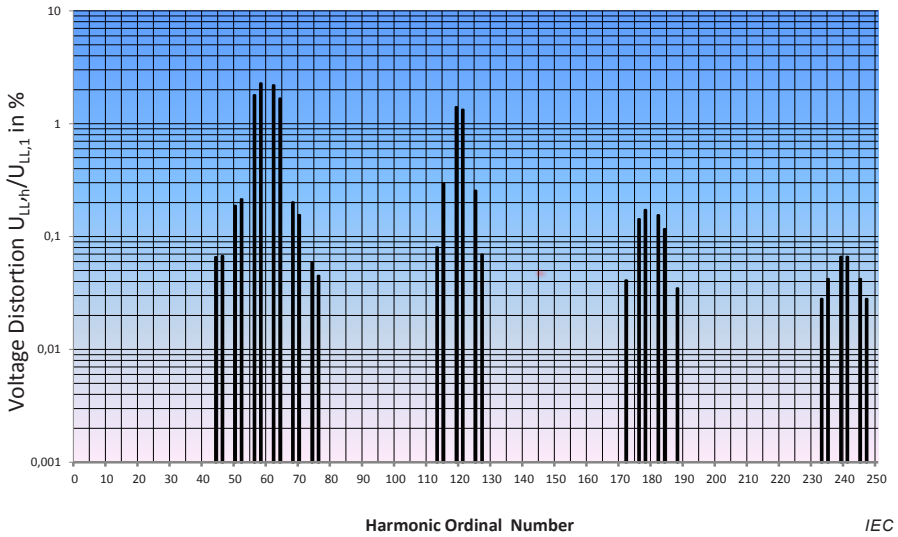


Figure B.2 – Harmonic voltage spectrum of one 2-Level PWM AIC with acceptable temperature increase of a power capacitor not exceeding 10 K

B.1.5 Matching of AIC converters (2-Level PWM) to different power supply network conditions without overloading the power capacitor burden

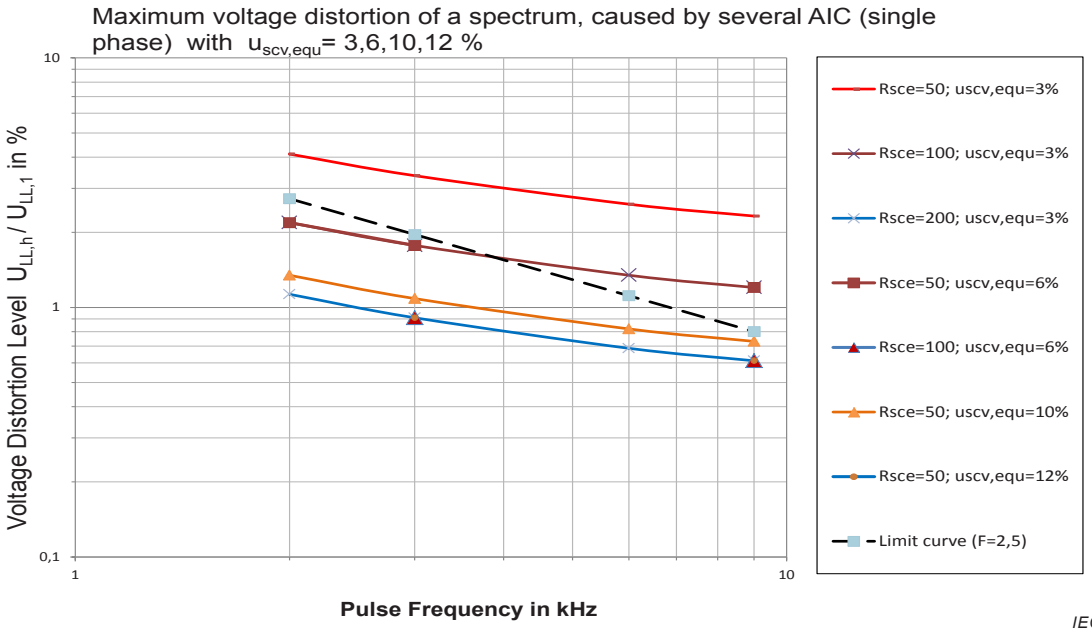
Figure B.3 (for single phase AIC) and Figure B.4 (for three phase AIC) show the voltage distortion created on the power supply network at different parameters (R_{SCe}; $u_{\mathrm{scv;equ}}$).

The lines in these figures summarize the distortion effects while the operation of several AICs simultaneously on the same power supply line (increasing factor = 5/3 = 1,67) and is shown on a double logarithmic scale.

Therefore it is possible to compare these curves directly with the power capacitor's limit curve in Figure B.1 that is derived from the capacitor’s temperature rise limits in the same frequency range which can be considered as withstand level in this respect.

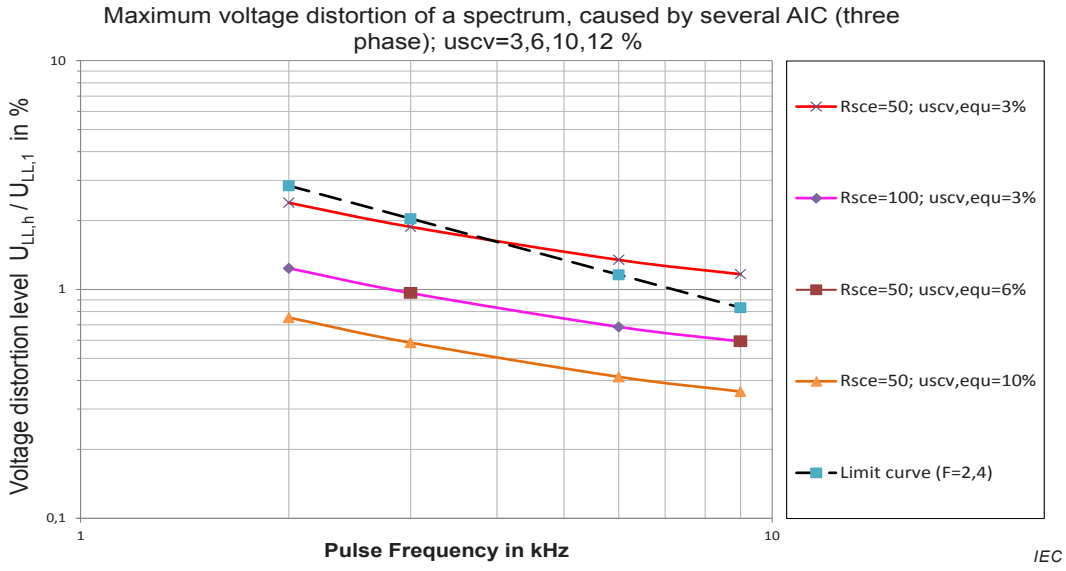
In comparison to the power capacitor limit curves some voltage distortion results are lower but others are higher or show an intersection at a certain frequency which means that the chosen AIC parameter set is insufficient to comply with the required power capacitor limits. In practice this mismatch may lead to reliability problems of the power capacitors and this should be avoided by choosing other AIC parameters or by using additional filter measures.

The higher the distortion curves and the lower the limit curve, the more additional filter measures are required under the same boundary conditions.



NOTE $u_{scv,equ}$ = 3 %, 6 %, 10 %, 12 % with intersection to the power capacitor temperature limiting curves at e.g. R_{SCe} = 50; $u_{scv,equ}$ = 6 %.

Figure B.3 – Maximum voltage distortion of a spectrum, caused by several AICs (single phase topologies)



NOTE $u_{scv,equ}$ = 3 %, 6 %, 10 %, 12 % with intersection to the power capacitor temperature limiting curves at e.g. R_{SCe} = 50; $u_{scv,equ}$ = 3 %.

Figure B.4 – Maximum voltage distortion of a spectrum, caused by several AICs (three phases topologies)

Although the voltage sharing between the inductance of the AIC and the line impedance is following quite different regularities which have been considered in the spread sheet results, the R_{SCe} in this context is furthermore the power ratio of the fundamental as defined generally.

In Figure B.5 and Figure B.6, three cases are addressed.

- Case A indicates, that there might be a mismatch for all switching frequencies of the AICs which may cause an over temperature of power capacitors and therefore higher values of R_{SCe} or $u_{scv,\ equ}$ or additional filters are required.
- Cases B indicate, that for switching frequencies below the displayed values, the AICs will match the requirements of the power capacitors with the indicated parameters R_{SCe} and $u_{scv,\ equ}$ and no additional filtering is required.
- Cases C indicate, that in this application the AICs may operate without any additional filtering while no over temperature of power capacitors will occur.

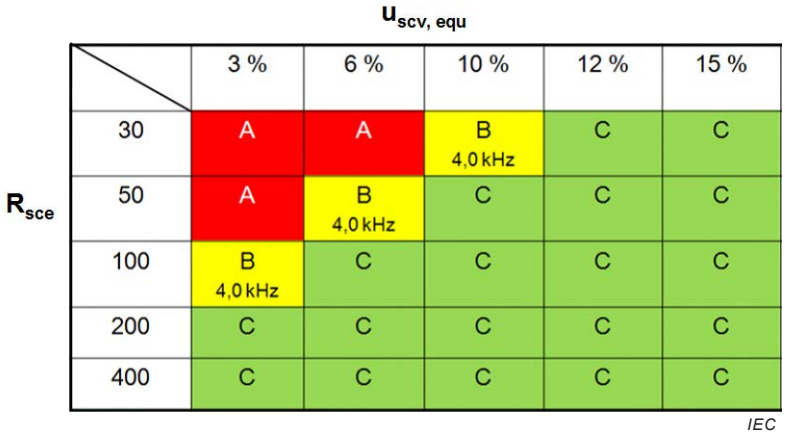


Figure B.5 – Spreadsheet of matching single phase AICs (2-level) to different power supply network conditions in order to apply the power capacitor limit curves

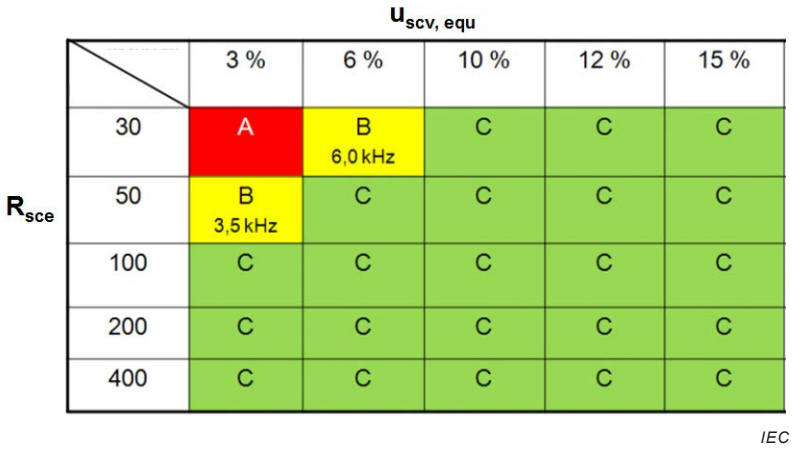


Figure B.6 – Spreadsheet of matching three phases AICs (2-level) to different power supply network conditions in order to apply the power capacitor limit curves

B.1.6 Considerations in regard to medium voltage power supply networks

For medium voltage power supply networks the following statements should be considered as far as harmonics are concerned.

– Usually less damping in the power supply network because of the reduced skin effect of the cabling and within the transformers and less ohmic consumers connected to this line.

– Less harmonic emissions because of generally using three or more level converters, see Table A.4.

– Dissipation factor and loss characteristic of the power capacitors are expected to be similar to those of the low voltage power capacitors.

– Due to these factors, a more cautious approach is required for medium voltage applications than for low voltage applications. This may lead to an increased amount of filtering.

B.1.7 AIC filtering considerations

The inclusion of large additional AIC filter measures (according to the fields “A” of Figure B.5 and Figure B.6) with the aim to decrease the AIC distortion levels would lead to serious problems in the power supply network at frequency ranges below the filter frequency, if the whole system topology may support this tendency. See also Figure B.7.

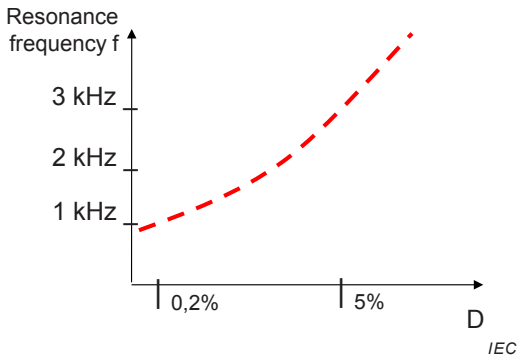


Figure B.7 – Illustration of the typical power supply network resonance frequency by increasing AIC filtering population, versus the voltage distortion level

The power supply network resonance frequency created by the increased filtering will generate low frequency currents circulating inside the passive filter. These currents are also susceptible to be trapped by compensating capacitor banks at both the low voltage as well as at the medium voltage network level. Damages on such equipment could be expected on a daily basis (see Clause A.7).

It is both an economic as well as a technical consideration, that under certain conditions a too strict limitation of the permissible emission levels in the power supply network may have negative effects on the supply system itself (deterioration of the resonance frequency) and the equipment connected thereto. If such cases are the goal, some "resonance hazard" effects may result in a worse and more dangerous operation of equipment (see example in Clause A.7).

The basic message of this illustrated example is, that too strict limitations of the permissible emission levels in the frequency range 2 kHz to 9 kHz (requiring extensive AIC filter measures) might be reconsidered in order not to shift the naturally given resonances of the power supply network towards much lower frequencies, but to allow smaller AIC filter measures which will work properly and not cause interference with other equipment.

The reduced dynamic performance of a PDS equipped with an AIC when increasing the inductive filter components needs also to be considered.

B.1.8 AIC appropriate technical and economical amount

The structure of a smart grid with decentralised energy generation and energy storage will get more and more complex therefore cohabitation regulations are needed i.e. in the frequency band 2 kHz to 9 kHz.

The unavoidable necessity to move forward in the usage of renewable energy will lead to the operation of distributed power source stations. These power sources, as well as other AICs in various other roles (AIF, power factor compensation and energy storage) will constitute the so called smart grid. These applications will increase as this high demand is sustained and supported by future power generation concepts.

The converter complexity, volume and cost increase while the passive filter volume and cost will decrease, as the AIC switching frequency increases, see Figure B.8.

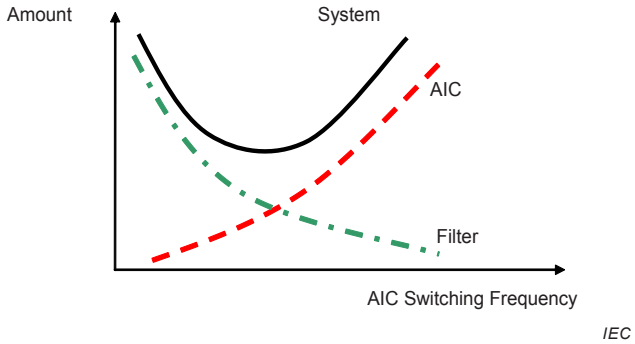


Figure B.8 – Sketch of the typical size/cost of an AIC application versus switching frequency of the AIC

The individual influences are illustrated in principle in Figure B.10 and have to be carefully examined. These typical illustrations as well as the intersection point at 4 % are in accordance to long time experiences with AICs and matches with the capacitor withstand capability in the frequency range 2 kHz to 4 kHz shown in Figure B.1.

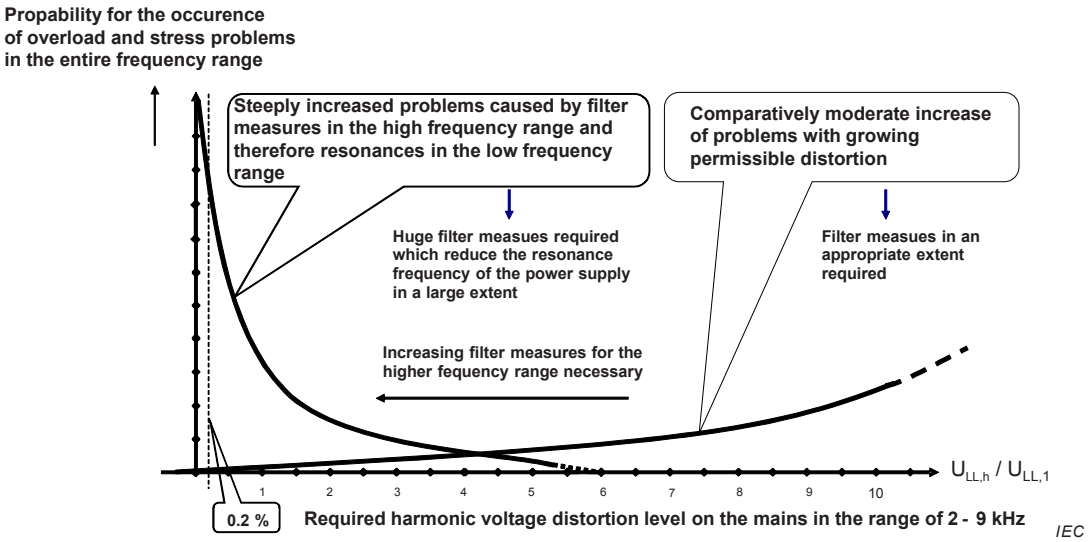


Figure B.9 – Illustration of the probability of overload and stress problems for the power supply network and the equipment connected thereto, depending on stipulated distortion levels fixed in miscellaneous assumptions

B.1.9 Frequency range from 2 kHz to 9 kHz

In Figure B.2, a harmonic voltage spectrum for an AIC has been shown. In order to propose AIC design recommendations for maximum emission values which are independent of the individual shape of the distortion curve as shown in Figure B.2, the sum of all harmonics in the frequency range from 2 kHz to 9 kHz is proposed to be limited, with the individual harmonic voltages being weighted according to their contribution on additional capacitor losses.

A spectral line of certain amplitude with higher frequency (e.g. 3 % at 8 kHz) contributes more to capacitor heating than the same amplitude at a lower frequency (e.g. 3 % at 4 kHz). Consequently, a weighted distortion factor D is proposed as shown in Formula B.1, which is

similar to the ”partial weighted harmonic distortion factor” PWHC as defined in IEC 61000-3-12.

$$D = \sqrt{\sum_{f=2kHz}^{9kHz} \left(0{,}9 \cdot \left(\frac{f}{2kHz} + 0{,}5\right) \cdot \frac{U_{LN,h}}{U_{LN,1}}\right)^2} \quad \text{(B.1)}$$

Voltages $U_{\mathrm{LN,\ h}}$ in equation (B.1) shall be measured from line to the star point of the power supply network. $U_{\mathrm{LN,\ 1}}$ is the fundamental of that supply voltage. The measurement method is according to IEC 61000-4-7:2002, Annex B.

Depending on the environment in which the AIC of a dedicated category is intended to be used, the design of the AIC is recommended not to exceed the distortion factor D like shown below.

The values for the distortion factor D have been derived from AIC category C1 from applying Formula B.1 to Figure B.2 which also matches Figure B.1.

For AIC category C3 the values for the distortion factor D have been derived from an extrapolation of the category C3 values above 150 kHz from IEC 61800-3 and IEC 62040-2.

The AIC design recommendations given in Table B.1 for category C2 are reasonably in between.

Table B.1 – AIC design recommendation for a maximum distortion factor in the frequency range from 2 to 9 kHz

D <	Category of recommended AIC
6 %	C1
8 %	C2
25 %	C3 below 100 A
60 %	C3 above 100 A

B.2 Design recommendations for conducted emission of low voltage AICs in the reasonable context of higher frequencies between 9 kHz and 150 kHz

B.2.1 General

When a product is connected to a network to get the necessary energy for the accomplishment of its purpose, a side effect can be stated in terms of re-injection of harmonics to the network. As soon as the product uses voltage switching technology, disturbance voltage will exist below and above 150 kHz.

The disturbance voltage with a frequency higher than 150 kHz shall comply with the product standard, therefore these harmonics are measured by the manufacturer.

In the frequency range from 2 kHz to 150 kHz, up to now, no conducted emission limit has been defined in the CISPR 11 or in IEC product standards dealing with power electronic systems and equipment. Manufacturers have no obligations to check them and these emissions are most of the time not known.

Earlier in this document, IEC TS 62578 proposes maximum values for conducted emissions. It seems logical to compare such proposal to the reality of products already on the market.

In order to get a statement about the conducted emission generated by the products already presents on the market, a data collection has been organized.

The questionnaire has been sent through the manufacturers' associations (CEMEP, JEMA, NEMA and GAMBICA) so that the manufacturers' measurements could be gathered in an anonymous way with the help of these organisations.

The request was to get 2 measurements in terms of magnitude and frequency: one measurement between 9 kHz and 50 and a second one in the frequency band from 50 kHz up to 150 kHz.

The means and method necessary for such measurements are described in the CISPR 16.

B.2.2 Data collection results

The information gathered during the collection period has been split into three different sets. The first one is about products rated above 75 kVA, the second one is about the products rated below 75 kVA, both able to operate in the industrial environment and the third one is about C1 and C2 products able to operate in the residential environment without or with a specific attention during the installation.

For C3 products rated above 75 kVA, the feedbacks from the data collection brought a few measurements in the frequency band between 9 kHz and 50 kHz (Figure B.10). The magnitudes measured are consistent with the maximum magnitude proposed in IEC TS 62578 for this category (dark line in Figure B.10).

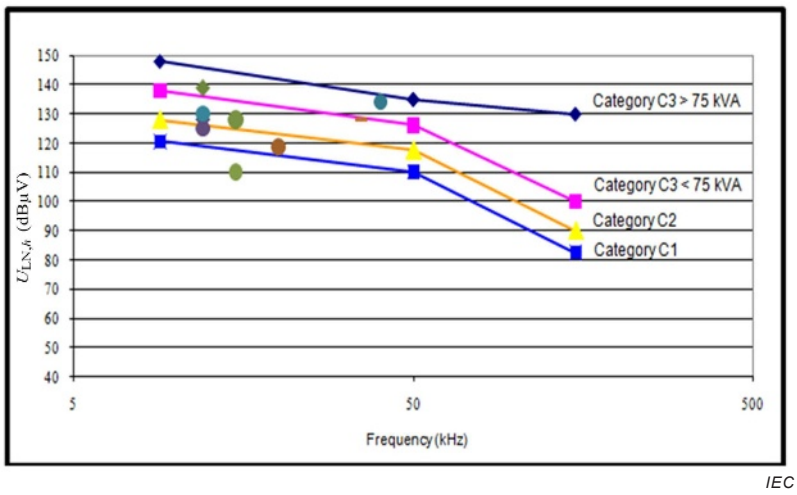


Figure B.10 – Results of the data collection versus the maximum values proposed in the IEC TS 62578 for products rated above 75 kVA

For C3 products rated below 75 kVA, the feedbacks from the data collection brought few measurements but here again the same statement of consistency can be made between the magnitudes measured and the maximum magnitude proposed in IEC TS 62578 (pink line in Figure B.11).

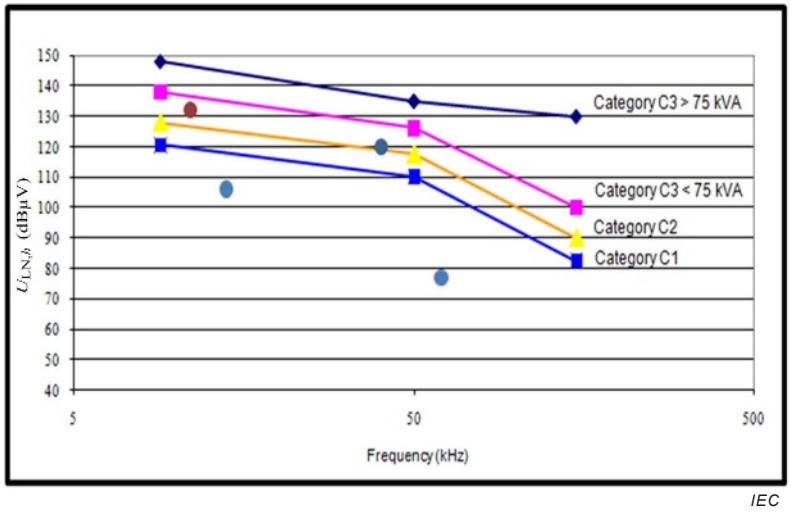


Figure B.11 – Results of the data collection versus the maximum values proposed in the IEC TS 62578 for products rated below 75 kVA

For C1 and C2 products that can be installed in a residential environment, the feedbacks from the data collection brought more measurements. Compared to the maximum magnitude proposed in IEC TS 62578 (blue or yellow lines in Figure B.12), some products have been measured with higher magnitudes than suggested by this revision of IEC TS 62578.

As no specific information was given with the measurements about the market and application for which the product was developed, no information is available to understand why some measurements are with lower magnitudes than others.

The fact that can be stated is, that some products are measured with magnitudes above the maximum values suggested by this revision of IEC TS 62578.

In case the suggested values would be lowered, much more products would be impacted; in fact a large majority of them would be impacted as a lot of measurements are close to the Category 1 line shown in Figure B.12.

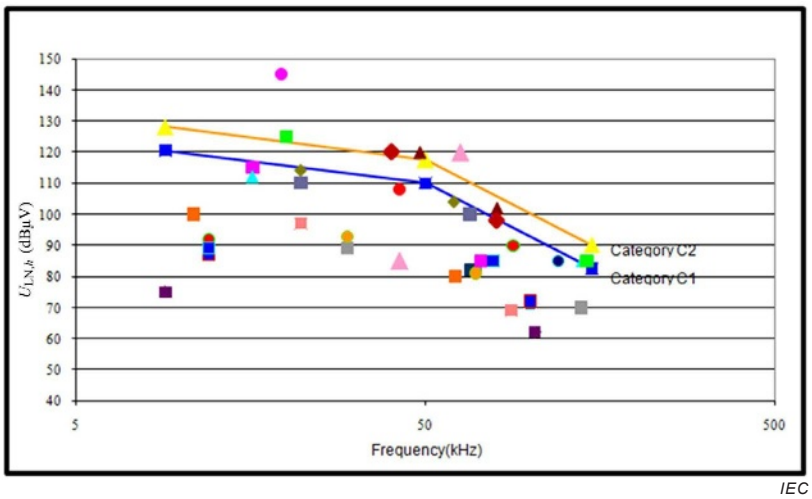


Figure B.12 – Results of the data collection versus the maximum values proposed in the IEC TS 62578 for products rated above 75 kVA

As a general conclusion, the proposal from the IEC TS 62578 would already be a stringent one for manufacturers if such proposal was retained for standardisation purpose.

B.2.3 Conclusions

In the frequency range from 9 kHz to 150 kHz, an impedance network is already defined in CISPR 16. It is consequently recommended to use the same impedance network for the measurements on an AIC inverter. In the frequency range from 2 kHz to 9 kHz, the line impedance is in accordance to 5.2.6 with the parameter values given in Table 2.

For the definition of the classes C1, C2, C3 (AIC categories) see IEC 61800-3 or IEC 62040-2.

The design recommendations for maximum quasi-peak values in this frequency range are shown in Figure B.13 and Table B.2 as follows:

For AIC Category C2, the design recommendation for the maximum emission value at 9 kHz is 128 dBμV according to Figure B.1. Starting at this value, the recommended maximum values up to 50 kHz may decrease depending on the eventual immunity level set in IEC 61000-4-10 and may change further with frequency above 50 kHz in order to be compatible with other technologies.

For AIC Category C3 below 100 A, the design recommendation for the maximum emission value at 150 kHz is chosen according to CISPR 11. For frequencies below 150 kHz, the margin to the C2 values is kept constant at 10 dB.

For AIC Category C3 above 100 A, the design recommendation for the maximum emission value at 150 kHz is chosen according to CISPR 11. At 9 kHz, the margin to C3 below 100 A is chosen to 10 dB. The values for frequencies in between follow a straight line in logarithmic scale.

For AIC Category C1, the design recommendation for the maximum emission value at 50 kHz is chosen according to CISPR 11. For other frequencies, the margin to C2 values is kept constant at 7,5 dB.

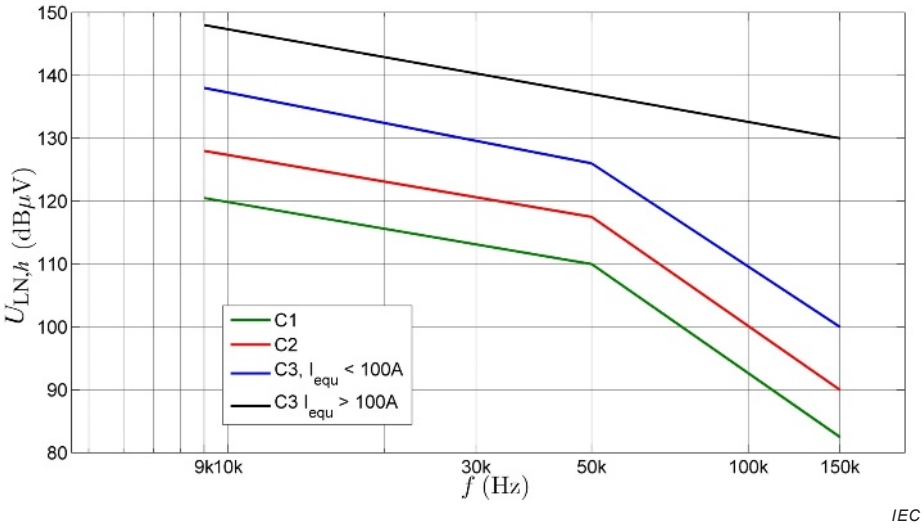


Figure B.13 – Recommended maximum emission values for AIC of different categories in the range from 9 kHz up to 150 kHz

Table B.2 – Recommended maximum emission values for AIC of different categories in the range from 9 kHz up to 150 kHz

	C1 **Quasi peak** dB(μV)	**C2** **Quasi peak** dB(μV)	**C3** **I_{equ} < 100 A** **Quasi peak** dB(μV)	**C3** **I_{equ} > 100 A** **Quasi peak** dB(μV)
9 kHz	120,5	128	138	148
50 kHz	110	117,5	127,5	137,5
150 kHz	82,5	90	100	130

NOTE These values may be superseded by other generally agreed emission limits for this type of equipment published by SC77A or CISPR.

Bibliography

[1] DEPENBROCK, M.: Pulse Width Control of a 3-Phase Inverter with non-sinusoidal phase Voltages, IEEE/IAS International semiconductor power converter conference, 1977, Orlando, Florida, USA, S. 399 – 403.

[2] GREEN, A.; BOYS, J.; GATES, G.: 3-phase voltage sourced reversible rectifier, IEEE Proceedings, Vol. 135, Pt. B, No. 6, November 1988.

[3] WU, R.; DEWAN, S.; SLEMON, G.: A PWM a.c.-To-d.c. Converter with Fixed Switching Frequency, IEEE 1988.

[4] BOOST, M.; ZIOGAS, P.: State-of-the-Art Carrier PWM Techniques: A Critical Evaluation, IEEE Transactions on Industry Applications, Vol. 24, No. 2, 3/4 1988.

[5] DIXON, J.W.; OOI, B.T.: Dynamically stabilized indirect current controlled SPWM boost type 3-phase rectifier, IEEE Trans. Ind. Electronics, Vol. IE-34, 1988.

[6] SUGIMOTO, H.; MORIMOTO, S.; Yano, M.: A high performance control method of a voltage-type PWM converter, PESC '88 Record (April 1988).

[7] OHNISHI, T.: Three-Phase Voltage-Fed Type PWM Power Converter via Power Factor Control, Electrical Engineering in Japan, Vol. 111, No. 7, 1991.

[8] WU, R.; DEWAN, S.; SLEMON, R.: Analysis of a PWM a.c. to d.c. Voltage Source Converter under Predicted Current Control with a Fixed Switching Frequency, IEEE Transactions on Industry Applications, Vol. 27, No. 4, 7/8 1991.

[9] WEINHOLD, M.: Optimal Control and Appropriate Pulse Width Modulation for a Three-Phase Voltage d.c.-link PWM Converter, EPE Journal, Vol. 1, No. 2, October 1991, S. 139 – 148.

[10] MORÁN, L.; ZIOGAS, P.; JOOS, G.: Design Aspects of Synchronous PWM Rectifier-Inverter Systems under unbalanced Input Voltage Conditions, IEEE Transactions on Industry Applications, Vol. 28, No. 6, 11/12 1992.

[11] IWAJI, Y.; FUKUDA, S.: A Parameter Design Method of PWM Voltage Source Rectifier, Electrical Engineering in Japan, Vol. 112-D, No. 7, July 1993.

[12] HOLTZ, J.: Pulsewidth Modulation for Electronic Power Conversion, Proceedings of the IEEE, Vol. 82, No. 8, August 1994.

[13] OLLILA, J.: A PWM-rectifier without current measurement, EPE Journal, Vol. 4, No. 2, Juni 1994

[14] Borcherding, H., Balzer, E.:Netzrückwirkungen von Netzpulsstromrichtern im Einzel- und Parallelbetrieb in industriellen und öffentlichen Netzen, Hochschule Ostwestfalen Lippe, 2012

[15] Balzer, E., Borcherding, H., Garbe, H.: Messung der Netzimpedanz im Frequenzbereich bis 20 kHz und Analyse der Oberschwingungen. EMV, International Congress on Electromagnetic Compatibility, pages 511–518, Stuttgart, September 2010

[16] HEUCK, K., DETTMANN, K. SCHULZ, D.: Electric power supply, 7th Edition, Vieweg Verlag, Hamburg, 2007

[17] Leszek S. Czamecki and Zbigniew Staroszczyk, "On-Line Measurement of Equivalent Parameters for Harmonic Frequencies of a Power Distribution System and Load", IEEE Trans. on INSTRUMENTATION AND MEASUREMENT, Vol. 45, No. 2, April 1996

[18] Brochure of HAAG, "EWS 120 Netzimpedanz – Messgerät"

[19] Toru Miki et.al. "Estimation of Backward Impedance on Low-Voltage Distribution System using Measured Resonant Current", Trans. on PE of IEEJ , Vol.128, No.3, 2008

[20] S. Nishimura et.al., "Advanced Islanding Phenomenon Detection Method for Dispersed Power Sources and a New Product ", Technical report of Nissin Electric, Vol. 46, No. 2, May 2001

[21] M. B. Harris et.al., "INSTRUMENTATION FOR MEASUREMENT OF LINE IMPEDANCE", IEEE Applied Power Electronics Conference and Exposition, 1994. APEC '94. Conference Proceedings, Vol.2, pp.887-893

[22] Knop, Andre; Fuchs, Friedrich W.: High Frequency Grid Impedance Analysis with Three-Phase Converter and FPGA-Based Controller; IEEE Compatibility and Power Electronics (CPE), 2009 7th International Conference-Workshop, pp. 286 – 291, Badajoz, Spain.

[23] GOEPFRICH,K.; REBBEREH,C.; SACK,L.: Fundamental frequency front end converter (F3E) – a d.c.-link drive converter without an electrolytic capacitor, PCIM Europe 2003, International exhibition and conference for power electronics, intelligent motion, power quality, Nuremberg, DE, May 20 – 22, 2003

[24] BURGHOLTE A.; SCHIRMANN U.; WESNER C.: limits of harmonics and accuracy of the measurement

[25] KOLAR, J. W., ERTL, H., ZACH, F., "Quasi-dual modulation of three-phase PWM converters", IEEE Trans. on Industry Appl., 1993, vol. 29, no. 2, pp. 313-318

[26] KOLAR, J. W., ERTL, H., ZACH, F. C., "Analysis of the duality of three phase PWM converters with d.c. voltage link and d.c. current link", Conf. Rec. IAS Ann. Mtg., San Diego CA, Oct. 2-5, 1989, vol. 1, pp. 724-737

[27] ZMOOD, D. N., HOLMES, D. G., "A generalised approach to the modulation of current source inverters", Power Electr. Spec. Conf., 1998, vol. 1, pp. 739-745

[28] ESPINOZA, J. R., JOOS, G., GUZMAN, J. I., MORAN, L. A., BURGOS, R. P., "Selective harmonic elimination and current/voltage control in current/voltage-source topologies: a unified approach", IEEE Trans. on Industrial Electr., Feb. 2001, vol. 48, no. 1, pp. 71-81

[29] SCHROEDER, D., Elektrische Antriebe – Regelung von Antriebssytemen, Springer, Berlin, 2001

[30] SATO, Y., KATAOKA, T., "A current-type PWM rectifier with active damping function", IEEE Trans. on Industry Appl., May-June 1996, vol. 32, no. 3, pp. 533-541

[31] MA, J. D., WU, B., RIZZO, S., "Active damping control of PWM CSI high power induction motor drives", Power Electr. Spec. Conf., 2000, vol. 1, pp. 61-66

[32] KARSHENAS, H. R., KOJORI, H. A., DEWAN, S. B., "Generalized techniques of selective harmonic elimination and current control in current source inverters/converters", IEEE Trans. on Power Electr., Sept. 1995, vol. 10, no. 5, pp. 566-573

[33] ZAGARI, N., PANDE, M, WISEMAN, J, RIZZO, S., "A Medium Voltage a.c. Drive with Active Front End and Improved Performance", European Conference on Power Electronics 2001, proceedings on CD

[34] SUH, Y., STEINKE, J., STEIMER, P., "Efficiency Comparison of Voltage Source and Current Source Drive System for Medium Voltage Applications", European Conference on Power Electronics 2005, proceedings on CD

[35] IEC 61000-4-19, *Electromagnetic compatibility (EMC) – Part 4-19: Testing and measurement techniques – Test for immunity to conducted, differential mode disturbances and signalling in the frequency range 2 kHz to 150 kHz at a.c. power ports*

[36] CLC/TR 50627, *Study Report on Electromagnetic Interference between Electrical Equipment/Systems in the Frequency Range Below 150 kHz Ed. 2*[2]

[37] IEC 62040-2, *Uninterruptible power systems (UPS) – Part 2: Electromagnetic compatibility (EMC) requirements*

2 To be published.

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