#### PD IEC/TS 62564-1:2016



### **BSI Standards Publication**

# Process management for avionics — Aerospace qualified electronic components (AQEC)

Part 1: Integrated circuits and discrete semiconductors



#### **National foreword**

This Published Document is the UK implementation of IEC/TS 62564-1:2016. It supersedes DD IEC/TS 62564-1:2011 which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee GEL/107, Process management for avionics.

A list of organizations represented on this committee can be obtained on request to its secretary.

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## TECHNICAL SPECIFICATION

Process management for avionics – Aerospace qualified electronic components (AQEC) –

Part 1: Integrated circuits and discrete semiconductors

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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#### INTERNATIONAL ELECTROTECHNICAL COMMISSION

PROCESS MANAGEMENT FOR AVIONICS –
AEROSPACE QUALIFIED ELECTRONIC COMPONENTS (AQEC) –

#### Part 1: Integrated circuits and discrete semiconductors

#### **FOREWORD**

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Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC TS 62564-1, which is a technical specification, has been prepared by IEC technical committee 107: Process management for avionics.

This third edition cancels and replaces the second edition, published in 2011. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) IEC TS 62239 changed to IEC TS 62239-1, and IEC PAS 62686-1 changed to IEC TS 62686-1;
- b) JESD48 changed to J-STD-048 and added to the Bibliography;
- c) AEC-Q100 revision G changed to AEC-Q100:2014 in 4.5 (which is now revision H);
- d) revision of AEC-Q101 removed in Bibliography;
- e) J-STD-609 for "Marking and labelling" added to the Bibliography;
- f) information added regarding components' life expectancy in 4.2.5.

GEIA-STD-0002-001 (June 2006), Aerospace Qualified Electronic Component (AQEC) Requirements, Volume 1 – Integrated Circuits and Semiconductors, has served as a basis for the elaboration of this technical specification.

The text of this technical specification is based on the following documents:

| Enquiry draft | Report on voting |
|---------------|------------------|
| 107/276/DTS   | 107/283/RVC      |

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62564 series, under the general title *Process management for avionics – Aerospace qualified electronic components (AQEC)*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- · replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

#### INTRODUCTION

Aerospace qualified electronic components (AQEC) plans are developed by manufacturers in order to document compliance with AQEC requirements. For AQEC designated components, the intention is to

- a) provide AQEC users access to information from the AQEC manufacturers that is necessary for using commercial-off-the-shelf (COTS) products;
- b) better enable AQEC users to assess whether these parts are capable of operating reliably in their applications;
- c) minimize deviations from the AQEC manufacturers' COTS products;
- d) have minimal impact on the AQEC manufacturers' standard operating or business procedures;
- e) promote communication between the AQEC manufacturers and users.

## PROCESS MANAGEMENT FOR AVIONICS – AEROSPACE QUALIFIED ELECTRONIC COMPONENTS (AQEC) –

#### Part 1: Integrated circuits and discrete semiconductors

#### 1 Scope

This part of IEC 62564, which is a Technical Specification, defines the minimum requirements for integrated circuits and semiconductors which are designated as an "aerospace qualified electronic component (AQEC)". It applies to integrated circuits and semiconductors exhibiting the following attributes:

- a) a minimum set of requirements, or information provided by the part manufacturer, which will allow a standard COTS component to be designated AQEC by the manufacturer;
- b) as a minimum, each COTS component (designated AQEC) will have been designed, fabricated, assembled, and tested in accordance with the component manufacturer's requirements for standard data book components;
- c) qualification of, and quality systems for, the COTS components to be designated as AQEC should include the manufacturer's standards, operating procedures, and technical specifications. This information should be available when requested;
- d) components manufactured before the manufacturer has addressed AQEC requirements, but utilizing the same processes, are also considered AQEC compliant;
- e) additional desired attributes of a device designated AQEC (that will support AQEC users) are found in Annex B of this technical specification.

NOTE Parts qualified to military specifications (except those identified as being for "logistic support" purposes only) are considered AQEC; the remainder of this technical specification only addresses non-military specification parts.

Parts qualified to AEC-Q100, grade 0 through to grade 3 are considered AQEC. For those applications where a 0 °C to +70 °C temperature range is appropriate, grade 4 is also considered to be AQEC. The users should document that the grade category used is compatible with the application in accordance with their IEC TS 62239-1 electronic components management plan (ECMP).

#### 2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC TS 62239-1, Process management for avionics – Management plan – Part 1: Preparation and maintenance of an electronic components management plan

IEC 62396-1, Process management for avionics – Atmospheric radiation effects – Part 1: Accommodation of atmospheric radiation effects via single event effects within avionics electronic equipment

IEC TS 62668-1, Process management for avionics — Counterfeit prevention — Part 1: Avoiding the use of counterfeit, fraudulent and recycled electronic components

ISO 9001, Quality management systems – Requirements

J-STD-048, Notification Standard for Product Discontinuance

#### 3 Terms, definitions and abbreviations

For the purposes of this document, the following terms, definitions and abbreviations apply.

#### 3.1 Terms and definitions

#### 3.1.1

#### **AQEC** specification

document prepared by or for the manufacturer to describe an AQEC product

Note 1 to entry: It includes a data sheet and may include other documents, such as material descriptions, environmental test procedures, quality monitoring processes, etc. It may be a stand-alone document or a clearly denoted item within a larger documentation system. There may be additional data associated with specific applications which may be requested separately.

#### 3.1.2

#### **AQEC** plan

instrument prepared by the plan owner (see 3.1.10) that clearly, concisely, and unambiguously documents the processes used by the plan owner to satisfy the requirements of this technical specification

Note 1 to entry: The plan contains auditable content.

#### 3.1.3

#### assessment

evaluation of a plan owner's AQEC plan to determine if it is compliant with this technical specification

Note 1 to entry: It may be conducted by IECQ, the customer, the customer's designee, or by a third party designated by the customer community.

#### 3.1.4

#### microcircuit

#### integrated circuit

microcircuit (device with a high circuit-element density) in which all or some of the circuit elements are inseparably associated and electrically interconnected (on one or more substrates, in a unique indivisible package) so that the microcircuit is considered to be indivisible for the purpose of construction and commerce

#### 3.1.5

#### semiconductor

#### discrete semiconductor device

semiconductor device that is specified to perform an elementary function and that is not divisible into separate components functional in themselves (for example diodes, transistors, optocouplers, LEDs and related products)

#### 3.1.6

#### component

#### part

microcircuit, integrated circuit, semiconductor or discrete semiconductor for the purpose of this specification

#### 3.1.7

#### customer

#### user

#### designer

original equipment manufacturer (OEM) that procures integrated circuits and/or semiconductor devices compliant with this technical specification and uses them to design, produce, and maintain systems

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#### 3.1.8

#### customer community

body of customers that may act together to address issues related to this technical specification

#### 3.1.9

#### data sheet

document prepared by the manufacturer that describes the electrical, mechanical, and environmental characteristics of the component

#### 3.1.10

#### manufacturer

#### plan owner

producer of integrated circuits, microcircuits, or other semiconductor devices that may be designated AQEC

Note 1 to entry: A manufacturer may produce the components directly or may oversee subcontracted manufacturing according to their own processes. The manufacturer is also the plan owner.

#### 3.1.11

#### supplier

distributor of components

Note 1 to entry: A plan for controlling AQEC inventory is in place in order to supply AQECs. A manufacturer can be a supplier in the case where no distributor is involved.

#### 3.1.12

#### third party

party designated to act on the behalf of the customer community

#### 3.1.13

#### termination

element of a component that connects it electrically and mechanically to the next level of assembly

Note 1 to entry: A termination includes base materials and coatings (including underplates).

#### 3.1.14

#### form

shape, size, arrangement of parts, visible aspect, mode in which a part exists or manifests itself, or the material an item is constructed from

#### 3.1.15

#### fit

qualified and competent

#### 3.1.16

#### function

work to a specification that an item is designed for without degrading reliability

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#### 3.2 Abbreviations

AQEC Aerospace qualified electronic component

Bi-CMOS Bipolar CMOS

BPSG Borophosphosilicate glass
COTS Commercial off the shelf

CMOS Complementary metal oxide semiconductor

DDR Double data rate

DRAM Dynamic random access memory

DSCC Defence supply centre Columbus (see http://www.dscc.dla.mil/)

DSIAC Defense systems information analysis center ECMP Electronic component management plan

FFF Form, fit and function

FIT Failures in time

FPGA Field programmable gate array

GIDEP Government industry data exchange program

HAST Highly accelerated stress test

HCI Hot carrier injection

HTOL High temperature operating life

LED Light emitting diode

LTB Last time buy

MCU Multiple cell upset

MRAM Magnetoresistive random access memory

NAND Negation AND

NBTI Negative bias temperature Instability

NOR Negation OR

PBTI Positive bias temperature instability

PCN Product change notification

SDRAM Synchronous dynamic random access memory

SEE Single event effect
SEU Single event upset
SER Soft error rate
SEL Single event latch

SEFI Single event functional interrupt
SRAM Static random access memory

SOS Silicon on sapphire

TDDB Time dependant dielectric breakdown

THB Temperature humidity bias

VID Vendor item drawing (controlled and released by DSCC)

#### 4 Technical requirements

#### 4.1 AQEC plan

The processes used to ensure compliance with the following requirements shall be documented by the AQEC manufacturer and included in their AQEC plan. These requirements

identify the additional processes, documentation and procedures required to supply a manufacturer's COTS part as an AQEC. The plan includes, but is not limited to, identifying data sheet parameters and/or conditions that are different for the AQEC versus the COTS part. These differences shall be identified and the data made available upon request.

#### 4.2 AQEC documentation

#### 4.2.1 General

For an avionics customer, the information supplied by the AQEC manufacturer will be normally utilised and retained in accordance with the customer electronic component management plan (see IEC TS 62239-1).

#### 4.2.2 AQEC data sheet

The AQEC manufacturer shall provide and maintain under revision control a data sheet that includes operating characteristics, as well as physical characteristics. Any known environmental limitations applicable to the application being addressed (see 4.3.1.2) shall be identified. This documentation shall specify the form, fit and function for a given part number. This baseline shall not be changed without proper notification (see 4.7). Use of a unique published or posted AQEC data sheet is encouraged. As a minimum, the AQEC manufacturer shall document, individually or by family,

- a) the functional operating temperature range;
- b) the defined performance (mechanical and electrical) at the operating temperature range;
- c) the maximum storage temperature;
- d) the maximum operating junction temperature or operating case temperature;
- e) the defined lead material, underplate, and termination finish;
- f) a package outline drawing;
- g) the designation of applicable COTS data sheet (or AQEC unique data sheet, as applicable) and reference to additional data, if applicable.

NOTE For further guidance, see Annex B.

#### 4.2.3 Material content

For each AQEC covered by this technical specification, the manufacturer shall make available, upon request, information that describes the material content of the part. Annex A describes typical material content for an AQEC. Materials that are considered proprietary by the AQEC manufacturer and are not designated hazardous, may be excluded from public disclosure.

#### 4.2.4 AQEC visibility

Each data sheet shall either state that the parts meet AQEC requirements (preferred) or optionally, the component manufacturer may list on its website all the part numbers that are AQEC or include an AQEC reference in a description of another compliant class of parts.

#### 4.2.5 AQEC life expectancy

The AQEC manufacturer shall identify the limiting wear-out failure mechanisms for a given AQEC in a given application environment (see 4.3.1.2) for highly complex silicon based technology components of feature size 90 nm and below including SRAMs, DRAMs (SDRAMSs, DDR series), flash memories (NOR logic gate, NAND logic gate, MRAMS, microprocessors, FPGAs). The AQEC manufacturer shall use acceleration models and failure rate estimating and reporting methods vetted through peer reviewed publications or described in industry standards and publications. This information shall be available on a website, data sheet, alternative database, or provided on an as requested basis.

NOTE 1 Examples of die related reliability wear-out failure mechanisms include electromigration, gate oxide breakdown (TDDB), positive (PBTI) and negative bias temperature instability (NBTI), hot carrier injection (HCI), etc.

NOTE 2 Examples of package reliability wear-out include mechanisms such as delamination, wire bond intermetallic formation, etc.

NOTE 3 Industry standards and publications which can assist include: JESD94, JEP122, JP001, JESD47, JESD91, DSIAC (formerly RIAC) publication ("Physics of failure based handbook of microelectronics systems").

The AQEC manufacturer should have reliability models for the lifetime limiting wear-out failure modes that can predict the failure rate of that AQEC for a given end of lifetime frame and use environment.

#### 4.2.6 Device technology

Different technologies (e.g. bipolar and bi-CMOS; bulk CMOS and CMOS/SOS) shall not be furnished under the same part number.

#### 4.2.7 SEE data

Avionics equipment is subjected to ionising radiation that increases with altitude. At an altitude of 40 000 feet (12,2 km) the radiation flux is approximately 300 times the atmospheric radiation flux at sea level. The principal causes of atmospheric radiation single event effects (SEE) on devices with geometric feature sizes below a micron are high energy neutrons and thermal neutrons (see IEC 62396-1).

The following information is required, where available, for designers to assess the impact of component SEE when using small geometric feature size devices, typically below 1 micron.

- a) High energy neutron (>10 MeV) measured single event upset (SEU) cross section or the terrestrially measured soft error rate (SER).
- b) High energy neutron (>10 MeV) or terrestrially measured multiple cell upset (MCU) cross section.
- c) For memory devices, the way in which the bits in an individual word are stored within the device, i.e. contiguously or non-contiguously.
- d) The cross sections of any hard SEE, for example single event latch (SEL), single event functional interrupt (SEFI) or stuck bits.
- e) Thermal neutron sensitivity and the thermal neutron SEE cross sections. Where the manufacturer uses Borophosphosilicate glass (BPSG) as a passivation and it contains boron 10 or natural boron (20 % boron 10), this is to be declared.

#### 4.2.8 Termination finish

Only one type of termination finish may be furnished on an individual part number supplied as part of the AQEC program. As a minimum, a change to a different single lead finish or ball alloy requires a PCN that includes the date and lot code of implementation. A new assigned part number is preferred.

#### 4.2.9 Third party part numbers

Where applicable, the data sheet shall state the third party part number (e.g. DSCC VID) for the AQEC manufacturer's part number (preferred). Optionally, the AQEC manufacturer may list this data on their website or provide a link to the third party information.

#### 4.3 AQEC performance

#### 4.3.1 Performance

#### 4.3.1.1 General

The manufacturer shall have documented processes to identify and verify the performance of the given AQEC or component family in all environmental conditions identified in the manufacturer's published data sheet.

#### 4.3.1.2 Additional performance information

The environmental conditions encountered in commercial and military aircraft are sometimes outside the conditions typically addressed by the semiconductor industry. At the same time, the functional requirements of the applications mandate that increasingly high functional performance components be compatible with the application.

NOTE Experience has shown that the part manufacturer often has sufficient information to determine if a specific part being considered for an application has sufficient margin to operate successfully in a proposed application with defined environment and reliability criteria.

To minimize the disruption to the manufacturer by continual requests for information, the AQEC program has defined specific multiple operating environments to group AQEC applications into. If a specific application does not comply with one of these categories, additional manufacturer information is recommended.

#### **Environment 1:**

Temperature range: -40 °C to +85 °C case/ambient;

Failure rate versus time at temperature: 23 °C and 85 °C;

Atmospheric neutron SEE upset rate: upset rate and basis of information, see 4.2.7;

Wear-out life expectancy: 23 °C and 85 °C, conditions for which wear-out expectancy is calculated.

#### **Environment 2:**

Temperature range: -40 °C to +100 °C case/ambient;

Failure rate versus time at temperature: 23 °C and 100 °C;

Atmospheric neutron SEE upset rate: upset rate and basis of information, see 4.2.7;

Wear-out life expectancy: 23 °C and 100 °C, conditions for which wear-out expectancy is calculated.

#### **Environment 3:**

Temperature range: -55 °C to +125 °C case/ambient;

Failure rate versus time at temperature: 23 °C and 125 °C;

Atmospheric neutron SEE upset rate: upset rate and basis of information, see 4.2.7;

Wear-out life expectancy: 23 °C and 105 °C, conditions for which wear-out expectancy is calculated.

#### **Environment 4:**

Temperature range: -40 °C to +125 °C case/ambient;

Failure rate versus time at temperature: 23 °C and 125 °C;

Atmospheric neutron SEE upset rate: upset rate and basis of information, see 4.2.7;

Wear-out life expectancy: 23 °C and 125 °C, conditions for which wear-out expectancy is calculated.

#### 4.3.2 Functional parameters

The manufacturer shall have documented processes for identifying the functional parameters of the given AQEC within the published data sheet or the limits of 4.3.1.2, whichever is more severe.

#### 4.3.3 Known limitations

The manufacturer shall have documented processes to identify and publish any known limitations of the AQEC within the published data sheet or the limits of 4.3.1.2 whichever is more severe.

#### 4.4 Quality system certification

As a minimum, the AQEC manufacturer (and its applicable subcontractors) shall be certified in accordance with ISO 9001. Additional certifications to AS/EN/JISQ 9100, and/or ISO TS 16949 and/or IEC TS 62686-1 and/or STACK S/0001 are strongly encouraged, but not required.

#### 4.5 Component qualification and re-qualification

The manufacturer's documented processes shall assure that the AQEC parts are qualified to meet the requirements of the data sheet for the environment specified (per 4.3.1.2). Examples of acceptable qualification processes include: AEC-Q100, AEC-Q101, JESD47, IEC TS 62686-1 or STACK S/0001.

Initial product qualification tests shall include temperature cycling, moisture (HAST or THB), and life test. Preconditioning is required for surface mount devices to simulate their assembly. Similar parts (e.g. AEC-Q100:2014, Appendix 1, or AEC-Q101) from the same family may be tested in lieu of the actual part.

The stresses applied during re-qualification of changes should be chosen in accordance with recognized process change tables such as those in AEC-Q100:2014, Table 3, AEC-Q101 or JESD47. The results of those re-qualification stress tests shall meet or exceed the original qualification requirements for those stresses.

The AQEC manufacturer shall make available the initial qualification and any appropriate requalification data upon request.

NOTE JEDEC has released alternate part qualification procedures (i.e. JESD94) to allow the manufacturer to more closely match the qualification process for an individual part specifically to a commercial customer's actual application. It is the responsibility of the customer for an AQEC to determine that the qualification process is appropriate for the AQEC application, see 4.11.

#### 4.6 AQEC quality assurance and reliability monitoring

The AQEC manufacturer shall have documented controls in place to assure the stability of the specified AQEC device characteristics. The AQEC manufacturer shall also have processes in place to ensure that the reliability of the product continues to meet or exceed the initial reliability performance on an on-going basis.

This may be accomplished through periodic (e.g. quarterly) reliability stress testing of packaged units that includes temperature cycling, HAST, and HTOL (such as in IEC TS 62686-1 and STACK S/0001). This may also be accomplished through in-line measurements collected in real time such as statistical process control charts, probe yield monitoring, statistical bin limits, burn-in limits, etc. If in-line data is used, the AQEC manufacturer shall have demonstrated and documented the relevance of that in-line data to product reliability.

Data collected to ensure the ongoing reliability of the AQEC shall be made available.

#### 4.7 Product change notification (PCN)

The manufacturer's AQEC plan shall document the PCN process. Guidance for PCN requirements in support of the AQEC plan may be found in JESD46 (to the revision in effect at the time of the product change) and Annex A of JESD46:2011. AQEC manufacturers shall include reference to external failure and change control databases (e.g. GIDEP) in the PCN process where possible.

AQEC manufacturers shall include the relevant part number(s) on AQEC PCNs.

AQEC manufacturers shall include the relevant part number(s) on AQEC LTBs.

#### 4.8 Last time buy (LTB) notification

Last time buy notification shall be provided under a PCN system with the terms of J-STD-048 as a minimum with a goal of at least 12 months from PCN notice date to LTB date. AQEC manufacturers shall use relevant external obsolescence reporting databases (e.g. GIDEP) in the PCN process.

AQEC manufacturers shall include the relevant part number(s) on AQEC LTBs.

#### 4.9 Obsolescence management

The production life goal for an AQEC is a minimum of 5 years, with 10+ years preferred. For AQEC with expected production lives less than 5 years, the AQEC manufacturer shall provide an estimate of the actual expected production life. As soon as new information is available, the AQEC manufacturer should suggest alternative components, preferably FFF alternatives.

#### 4.10 Counterfeit prevention

The component manufacturer shall destroy or effectively render unusable all non-conforming products (see IEC TS 62668-1).

#### 4.11 User or customer guide

It is recommended that an avionics user of an AQEC component select, apply and qualify the component for the intended application, monitor the on-going quality throughout production, check compatibility with the manufacturing process, control the configuration management and associated data and control the component dependability (e.g. obsolescence, reliability, risk management, etc.) in accordance with their electronic component management plan (ECMP, see IEC TS 62239-1). IEC TS 62239-1 third party certification is recommended and may be mandated.

#### Annex A

(informative)

#### AQEC material content and construction table

Material content may vary depending upon product technology (e.g. wire bond versus flip chip), see Table A.1.

Table A.1 – AQEC material content and construction

| Item name   | Manufacturer response |
|---|-----------------------|
| AQEC manufacturer's part:     Number/date code:   |                       |
| 2. Die fab facility and process ID:   |                       |
| Assembly facility and process ID:   |                       |
| 4. Die:  a. Die family:  b. Die mask set revision and name:   |                       |
| <ul> <li>5. Die technology description:</li> <li>a. Die process technology:</li> <li>b. Die geometric feature size of the technology<sup>a</sup>:</li> <li>c. Is boron 10 or natural boron one of the materials used within the die <sup>b</sup>?</li> </ul>              |                       |
| 6. Die dimensions:  a. Die width:  b. Die length:  c. Die thickness:  |                       |
| Die metallization (top level only):     a. Die metallization material(s):   |                       |
| 8. Die passivation:  a. Die passivation material(s)  (list all):  |                       |
| 9. Die attach: a. Die attach material ID: b. Die attach method:   |                       |
| 10. Mould compound:  a. Mold compound supplier and ID:  b. Mould compound type:  c. MSL level (if known):   |                       |
| 11. Wire bond:  a. Wire bond material:  b. Wire bond diameter (mils):   |                       |
| 12. Wire bond (e.g. wedge, ball):  a. Type of wire bond at die:  b. Type of wire bond at leadframe:   |                       |
| 13. Leadframe/header:  a. Paddle/flag material:  b. Termination material:  c. Underplate material and thickness:  d. Final termination finish and thickness:  e. Is final finish annealed within 24 h?  f. Details or the location of any reports on tin whisker testing: |                       |

| Item name   | Manufacturer<br>response |  |  |  |
|---|--------------------------|--|--|--|
| 14. Unpackaged die (if not packaged):   |                          |  |  |  |
| a. Cap metal composition:   |                          |  |  |  |
| b. Size of cap metal:   |                          |  |  |  |
| c. Bump composition:  |                          |  |  |  |
| d. Ball size:   |                          |  |  |  |
| i. Part assembly application notes:   |                          |  |  |  |
| a. Soldering recommendations:   |                          |  |  |  |
| b. Cleaning recommendations:  |                          |  |  |  |
| c. X-ray inspection recommendations:  |                          |  |  |  |
| d. Remarks:   |                          |  |  |  |
| a Geometric feature size is generally defined as the gate channel length for the transistors. |                          |  |  |  |

b Boron 10 and natural boron can cause thermal neutron single event effects.

## Annex B (informative)

#### Additional desired data

The purpose of Annex B is to promote improved communication between the AQEC manufacturer and user, especially regarding the environmental conditions guaranteed for the data sheet parameters/limits. In no way is the contents of this annex required to satisfy acceptance to this document and it is not subject to assessment. The need for additional data is generally based on that dialog as it relates to the customer's application with respect to performance, environmental conditions, production life, service life, etc., as well as the aforementioned environmental conditions as they affect parameters and limits.

EXAMPLE A typical ambient temperature for a component operating in the equipment bay of a commercial or military aircraft might range from  $-40\,^{\circ}\text{C}$  to  $+75\,^{\circ}\text{C}$ .

This implies that the component requires an ambient temperature range from +80 °C to +105 °C (upper limit) to -40 °C (lower limit). After considering the current business climate, technical capability of the components, availability of existing test data and other relevant information and any other mitigating factors, the AQEC manufacturer can choose a temperature (upper limit) of any place between the +80 °C to +105 °C, specify that temperature and test to the extended limit in order to guarantee meeting that temperature.

- 1) Functional parameters are typically specified on the AQEC manufacturer's data sheet (see 3.1.9). Most parameters will be unchanged from the standard COTS component to the AQEC device; however, there may be changes due to expected harsher operating conditions. Changes in such parameters as frequency, power, temperature, etc., should be highlighted to the AQEC user for use by their systems designer(s). The possibility is that compensatory variances could be made to improve system performance or reliability, for example as described in JEP149.
- 2) The AQEC manufacturer should provide any data regarding parametric limits versus application environmental conditions that would be of particular interest to users who need to make trade-offs among characteristics (such as temperature, power, frequency, and timing), while still operating the AQEC within the manufacturer's recommended operating conditions.
- 3) Roadmap information would likewise assist the system designer in anticipating future device parametric shifts and/or obsolescence and make provisions for them within the design or in the planning ahead for revisions to the design. Appropriate roadmap data includes but is not limited to
  - parameter trends;
  - design life;
  - production life;
  - wear-out lifetime and conditions:
  - radiation sensitivity, particularly atmospheric neutron SEE sensitivity;
  - product lifecycle status;
  - packaging trends;
  - die revisions.
- 4) Access to the AQEC manufacturer's die and package related testing will be desirable in order to characterize parts for some applications.
- 5) An AQEC manufacturer's data that characterizes reliability for life cycle environmental and operational stresses, such as sequential environmental tests and reliability versus time at temperature, will be desired to characterize reliability for some applications.
- 6) Minimum steady state life failure in time (FIT) numbers given here. IEC TS 62686-1 and the STACK S/0001 requirements could be used as minimum requirements.
- 7) Lead finish changes indicated by an easily identified new part number (different from the original by a mark other than just a new date code) are preferred; refer to IPC/JEDEC J-STD-609, JEITA ETR-7021 and JEDEC JIG101.

#### Bibliography

IEC TS 62686-1, Process management for avionics – Electronic components for aerospace, defence and high performance (ADHP) applications – Part 1: General requirements for high reliability integrated circuits and discrete semiconductors

ISO TS 16949, Quality management systems – Particular requirements for the application of ISO 9001:2008 for automotive production and relevant service part organizations

AEC-Q100:2014, Failure Mechanisms Based Stress Qualification For Integrated Circuits

AEC-Q101, Failure Mechanism Based Stress Test Qualification For Discrete Semiconductors

AS/EN/JISQ 9100, Quality management systems – Requirements for Aviation, Space and Defense Organizations

DSIAC (formerly RIAC), Physics of Failure Based Handbook of Microelectronics Systems (webpage:

https://books.google.fr/books?hl=fr&lr=&id=k38AluHcSvQC&oi=fnd&pg=PR5&dq=riac+physics +of+failure&ots=Q8JWzNO7gj&sig=dfx9ODET16b\_u0tqkgpRGA4Vt-M#v=onepage&q=riac%20physics%20of%20failure&f=false)

IPC-1066, Marking, Symbols and Labels for Identification of Lead-Free and Other Reportable Materials in Lead-Free Assemblies, Components and Devices

IPC/JEDEC J-STD-609, Marking and Labelling of Components, PCBs and PCBAs to Identity Lead (Pb), Lead-Free (Pb-Free) and Other Attributes

JEDEC JIG101, Material composition declaration for electronic products.

JEITA ETR-7021, Guidance for the Lead-Free Marking of Materials, Components and Mounted Boards used in Electronic and Electric Equipment

JESD46:2011, Customer notification of product/process changes by semiconductor suppliers

JESD47, Stress-test-driven qualification of integrated circuits

JESD91, Method for developing acceleration models for electronic component failure mechanisms

JESD94, Application specific qualification using knowledge based test methodology

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JEP122, Failure mechanisms and models for semiconductor devices

JEP149, Application thermal derating methodologies

JP001, Foundry process Qualification Guidelines (Wafer Fabrication Manufacturing Sites)

STACK S/0001, General Requirements For Integrated Circuits And Discrete Semiconductors



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