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## **BSI Standards Publication**

Electrical interface specifications for self ballasted lamps and controlgear in phase-cut dimmed lighting systems



#### **National foreword**

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The UK participation in its preparation was entrusted to Technical Committee CPL/34, Lamps and Related Equipment.

A list of organizations represented on this committee can be obtained on request to its secretary.

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# TECHNICAL REPORT

Electrical interface specifications for self ballasted lamps and controlgear in phase-cut dimmed lighting systems

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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#### CONTENTS

		RD	
IN	ITRODU	JCTION	6
1	Scop	e	7
2	Norm	native references	7
3	Term	s, definitions and abbreviated terms	7
	3.1	Terms and definitions	7
	3.2	Abbreviated terms	9
4	Gene	eral description	10
5	Gene	eral requirements	10
	5.1	Voltage rating	10
	5.2	Frequency rating	11
	5.3	Marking of controlgear	11
6	Desc	ription of the lighting system and its components	11
	6.1	Wiring method	11
	6.2	Wiring diagram	11
7	Elect	rical specification	12
	7.1	General	12
	7.2	Electrical characteristics during the on state of a phase-cut dimming system	12
	7.2.1		
	7.2.2		
	7.2.3	3 3 3	
_	7.3	Electrical characteristics during the off state of a phase-cut dimming system	
8		procedures	
	8.1	General	
	8.2	Tests for leading edge dimmable devices	
	8.2.1		
	8.2.2	5 1	25
	8.2.3	Test related to the transition from the non-conducting to the conducting phase and to the conducting phase	25
	8.3	Tests for trailing edge dimmable devices	
	8.3.1		
	8.3.2		
	8.3.3		
	8.3.4		
	8.4	Tests for characteristics during electronic off state	
Αr	nnex A	(informative) Voltage shapes to be used with the tests in IEC TR 63037	28
	A.1	General	28
	A.2	Waveform description	28
	A.3	Waveform description	
Ar	nnex B	(informative) Equivalent phase-cut dimmer circuit	29
Bi	bliograp	phy	30
Fi	aure 1 -	- Example of wiring diagram	11
	•	- Timing leading edge dimming method	
	_		_

Figure 3 – Timing trailing edge dimming method	18
Figure 4 – Test setup for testing the conducting phase	24
Figure 5 – Test setup for the transition from the conducting to the non-conducting phase	26
Figure 6 – Test setup for the non-conducting phase	27
Figure A.1 – Waveform of AC voltage source	28
Figure A.2 – Waveform of AC voltage source	28
Figure B.1 – Scheme of the EC_D	
Table 1 – Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz	14
Table 2 – Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz	14
Table 3 – Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz	14
Table 4 – Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz	15
Table 5 – Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz	15
Table 6 – Slew rate for voltage decrease across the phase-cut dimmer	16
Table 7 – Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz	16
Table 8 – Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz	16
Table 9 - Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz	17
Table 10 - Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz	17
Table 11 - Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz	17
Table 12 - Nominal mains voltage from 100 V to 277 V; frequency 50 Hz or 60 Hz	19
Table 13 – Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz	20
Table 14 – Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz	21
Table 15 - Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz	21
Table 16 - Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz	22
Table 17 - Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz	22
Table 18 – Currents and voltages for controlgear during the electronic off state	23
Table 19 – Parameters for testing nurnoses	24

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## ELECTRICAL INTERFACE SPECIFICATIONS FOR SELF BALLASTED LAMPS AND CONTROLGEAR IN PHASE-CUT DIMMED LIGHTING SYSTEMS

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IEC TR 63037, which is a Technical Report, has been prepared by IEC technical committee 34: Lamps and related equipment.

The text of this Technical Report is based on the following documents:

Enquiry draft	Report on voting
34/305/DTR	34/325/RVC

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

#### INTRODUCTION

This document describes the technical requirements for self-ballasted lamps and controlgear to work with phase-cut dimmers. For a complete picture of the technical requirements the user should also refer to the companion document that contains technical requirements and testing methods for phase-cut dimmers (IEC TR 63036).

## ELECTRICAL INTERFACE SPECIFICATIONS FOR SELF BALLASTED LAMPS AND CONTROLGEAR IN PHASE-CUT DIMMED LIGHTING SYSTEMS

#### 1 Scope

This document specifies the electrical interface between phase-cut dimming equipment and lighting equipment, such as LED integrated lamps and light sources with external controlgear, with the intention of helping designers of both types of equipment to develop products that will work together properly.

This document describes both the dimming phase and the off phase. In addition to the specification of the interface, test procedures are given for testing the proper operation.

It may be expected that controlgear fulfilling the requirements of this document are also suited to be used with electronic switches that use a circuitry comparable with that of a phase-cut dimmer, but do not contain means for the adjustability of the phase-cut angle.

Safety requirements are not covered by this document, but by respective product standards

#### 2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-845, International Electrotechnical Vocabulary. Lighting (available at http://www.electropedia.org)

IEC 62504, General lighting – Light emitting diode (LED) products and related equipment - Terms and definitions

#### 3 Terms, definitions and abbreviated terms

#### 3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62504 and IEC 60050-845 as well as the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

#### 3.1.1

#### phase-cut dimmed lighting system

combination of a phase-cut dimmer and one or more controlgear and light sources

#### 3.1.2

#### off state

state of a phase-cut dimming system when no light is emitted

#### 3.1.3

#### on state

state of a phase-cut dimming system when light is emitted

#### 3.1.4

#### phase-cut dimmer

electronic switch which is connected in series with a load and changes the supply voltage waveform applied to the load from the pure mains voltage waveform to a leading edge (forward phase) or a trailing edge (reverse phase) AC voltage waveform or is capable of switching between both waveforms

Note 1 to entry: The output voltage waveform of a phase-cut dimmer is applied to one or more loads. The conduction angle of the voltage waveform is adjustable.

Note 2 to entry: Within this document, where the term "dimmer" is used the term "phase-cut dimmer" is meant.

#### 3.1.5

#### two-wire phase-cut dimmer

phase-cut dimmer which is connected in series with the load and has no connection to neutral

#### 3.1.6

#### three-wire phase-cut dimmer

phase-cut dimmer which is connected in series with the load and has in addition a connection to neutral

#### 3.1.7

#### controlgear

device between the phase-cut dimmer and one or more lamps which may serve to transform the AC mains power, limit the current of the lamp(s) to the required value, provide starting voltage and preheating current, prevent cold starting, correct power factor or reduce radio interference

Note 1 to entry: Lamps may have integrated controlgear such as an integrated LED lamp. Any references to controlgear will include any such integrated lamps.

#### 3.1.8

#### load side

connection from the output of the phase-cut dimmer to the supply input of one or more controlgear

#### 3.1.9

#### conducting period

time period during which the phase-cut dimmer supplies power to a controlgear

#### 3.1.10

#### non-conducting period

time period during which the phase-cut dimmer does not supply power to a controlgear

#### 3.1.11

#### half-wave

positive or negative 180 degrees of an AC sine wave starting and ending at the zero crossing point

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#### 3.1.12

#### phase angle

position within a half-wave expressed in degree, being in the range of 0° to 180°, referred to the beginning of the half-wave

#### 3.2 Abbreviated terms

To describe the electrical characteristics of the phase-cut interface, the following abbreviations are used:

- $\alpha_{\rm X}$  Angle where the test voltage starts rising with the given slew rate SR as shown in Figure A.1
- $\beta_{x}$  Angle where the test voltage starts falling with the given slew rate SR as shown in Figure A.2
- C<sub>f</sub> Filter capacitor to reduce high frequency disturbances
- EC\_CG Equivalent circuit that represents a controlgear for phase-cut dimmer testing purposes
- EC\_D Equivalent circuit that represents a phase-cut dimmer for controlgear testing purposes
- $I_{\text{CG}}$  Current through the input terminals of the controlgear
- $I_{\text{CG pk}}$  Repetitive peak current of the controlgear in leading edge mode
- $I_{\text{CG\_SL}}$  Current-carrying capability of the controlgear with  $V_{\text{CG}} \leq V_{\text{SW}}$  in leading edge mode
- $I_{\text{CG\_STH}}$  Current-carrying capability of the controlgear with  $V_{\text{CG}} \leq V_{\text{SW}}$  in trailing edge mode
- $I_{\text{CG\_STL}}$  Current-carrying capability of the controlgear with  $V_{\text{CG}} > V_{\text{SW}}$  in trailing edge mode
- $I_{\mathsf{D}}$  Current through the load side terminal of the phase-cut dimmer
- $I_{\rm D\_nc}$  Maximum current through the phase-cut dimmer during the non-conducting period, limited by the phase-cut dimmer
- $I_{\mathsf{EC}\ \mathsf{CG}}$  Value of test current of EC\_CG in the test circuit in Figure A.1
- $I_{PO}$  Minimum current carrying capability of the controlgear during the electronic off state
- $I_{\rm trans}$  Current sourced by the phase-cut dimmer during the transition from the conducting to the non-conducting state in trailing edge mode.
- Required minimum number of controlgear connected with one phase-cut dimmer (named in phase-cut dimmer installation sheet)
- $P_{\text{CG}}$  Rated input power of the controlgear (as marked)
- $P_{\max}$  Maximum permissible nominal load of phase-cut dimmer (according to installation sheet)
- $P_{\min}$  Minimum nominal load required by phase-cut dimmer (according to installation sheet)
- $R_{R}$  Resistance value of resistive load R of the test circuit of Figure 5 (according to 8.3.3), dependent on maximum permissible load of phase-cut dimmer  $P_{max}$
- SR The absolute value of the slew rate of the decrease of the voltage across the input terminals of a controlgear in trailing edge dimming mode when the phase-cut dimmer switches off at time  $t_{\rm s1}$  (see Figure 3).
- SR<sub>L</sub> The absolute value of the slew rate of the increase of the voltage across the input terminals of a controlgear in leading edge dimming mode when the phase-cut dimmer under test switches on (according to Clause 8)
- $SR_{\mathsf{T}}$  The absolute value of the slew rate of the decrease of the voltage across the input terminals of a controlgear in trailing edge dimming mode when the phase-cut dimmer under test switches off (according to Clause 8)
- $t_{\text{HW}}$  Time related to previous zero crossing of the mains to the subsequent zero crossing of the mains (duration of a half-wave)

$t_{S}$	Time related to previous zero crossing of the mains when the leading edge phase- cut dimmer reduces its impedance towards zero by activating its power switch
t <sub>s1</sub>	Time related to previous zero crossing of the mains when the trailing edge phase- cut dimmer increases its impedance towards infinite by deactivating its power switch
$t_{s2}$	Time related to previous zero crossing of the mains when the voltage $V_{\rm CG}$ falls below $V_{\rm SW}$ in trailing edge method
$t_{s3}$	Time related to previous zero crossing of the mains when the transition from the conducting period to the non-conducting period is finished
$t_{\sf SW}$	Time related to previous zero crossing of the mains when voltage $V_{\mathrm{CG}}$ crosses $V_{\mathrm{SW}}$
$t_{t}$	Transition time for trailing edge mode; equals $t_{\rm S2}$ – $t_{\rm S1}$ .
$V_{CG}$	Voltage across the input terminals of the controlgear
$V_{D}$	Voltage between the line side (L) and load side terminal of the phase-cut dimmer
$V_{M}$	Mains voltage (rated nominal value)
$V_{ME}$	Phase cut voltage for testing purposes; sinusoidal part of the waveform ( $\alpha_1$ to $t_{HW}$ , 0 to $\beta$ ) equivalent to mains voltage.
$V_{PO}$	Lower limit for voltage across the input terminals of the controlgear to provide a current carrying capability $I_{\sf PO}$ during the electronic off state
$V_{\sf SW}$	Voltage across the input terminals of the controlgear at the time that leads to disabling ( $V_{\rm M}(t) > V_{\rm SW}$ ) or enabling ( $V_{\rm M}(t) < V_{\rm SW}$ ) a current path having a current carrying capability of $I_{\rm CG\_SL}$ or $I_{\rm CG\_STH}$
$V_{\sf test}$	Value of test voltage of test circuit Figure 6 (according to 8.4)
xx(t)	Instantaneous values of current or voltage xx
$Z_{\sf CG}$	Impedance across the input terminals of the controlgear
$Z_{D}$	Impedance between the line side (L) and the load side terminals of the phase-cut $\operatorname{dimmer}$
$Z_{D\_max}$	Maximum impedance between the line side (L) and load side terminal of the phase-cut dimmer, defined by the technical properties of the phase-cut dimmer

#### 4 General description

 $Z_{\mathsf{D}_{\mathsf{min}}}$ 

A phase-cut dimmer either cuts the mains voltage immediately after the zero crossing of the mains (leading edge) or towards the next projected zero crossing of the mains (trailing edge). The functionality of both methods can be implemented in one device (universal dimmers).

phase-cut dimmer, defined by the power properties of the phase-cut dimmer

Minimum impedance between the line side (L) and the load side terminal of the

This document describes requirements for controlgear during the on state of a phase-cut dimming system. Specifications are provided dependent on the dimming method for the conducting period, the non-conducting period of the phase-cut dimmer and the transitions between the conducting and non-conducting period.

In addition, this document describes requirements for controlgear during the off state of a phase-cut dimming system. Specifications are provided independently from the dimming method.

#### 5 General requirements

#### 5.1 Voltage rating

This document applies to one or more of the following mains voltages:

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100 V, 120 V, 200 V, 230 V, 277 V, according to IEC 60038.

#### 5.2 Frequency rating

This document applies to one or more of the following mains frequencies:

50 Hz or 60 Hz, according to IEC 60038.

#### 5.3 Marking of controlgear

The following information should be provided by the manufacturer on the product or in the accompanying instruction sheets.

Controlgear should be marked with the following indication:



#### 6 Description of the lighting system and its components

#### 6.1 Wiring method

The wiring of the devices is in accordance with the installation rules given in IEC 60364 (all parts) and also with the national wiring rules applicable in the country where the devices are installed.

#### 6.2 Wiring diagram

The wiring of the lighting system uses the traditional method of connecting the phase-cut dimmer to the mains and to the controlgear. Figure 1 is an example of a lighting system with one phase-cut dimmer and one or two controlgears.

Regarding the connections of the phase-cut dimmer shown in Figure 1, the drawn lines represent a two wire installation and the dashed line represents the direct connection of the phase-cut dimmer to the mains which is used in three-wire installations.

The direct connection of the phase-cut dimmer to neutral (dashed line in Figure 1) will have consequences on the power supply requirement and synchronization to the phase-cut dimmer.

This document defines requirements that enable compatibility between phase-cut dimmer and controlgear in two-wire installations. However, all predications are also valid for three-wire phase-cut dimmers to ensure proper operation of controlgear.

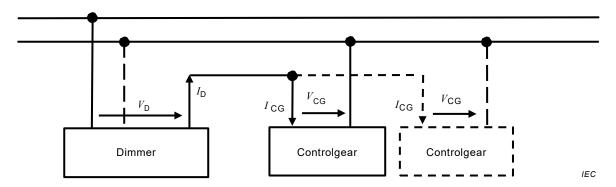


Figure 1 - Example of wiring diagram

#### 7 Electrical specification

#### 7.1 General

All information given in this document is related to a half-wave of the mains. Due to the polarity change between subsequent half-waves, all values have to be regarded as absolute values.

The phase-cut dimming system is either in on state or in off state.

In on state, light sources controlled by controlgear being part of the phase-cut dimming system emit light. In off state, light sources controlled by controlgear being part of the phase-cut dimming system do not emit light.

The off state may be realized as mechanical off state by opening the current loop of the phase-cut dimming system with mechanical means, for example a switch. For this case, no requirements need to be fixed.

Alternatively, the off state may be realized as electronic off state. In this case, the phase-cut dimmer increases its impedance (i.e. stops producing phase-cut) while continuing its operation, for example to keep its control interface activated. In this case, the connected controlgear are not energized sufficiently to operate a light source, but should provide a current path that allows the phase-cut dimmer to draw current continuously from the mains.

NOTE Applications that provide a connection to neutral allow using a three-wire device, enabling the usage of lamps that do not provide a current carrying capability according to 7.2 and 7.4.

During the on state and the electronic off state, it should be ensured that the phase-cut dimmer is supplied sufficiently with power and that the synchronization of phase-cut dimmer and controlgear with the mains is ensured.

#### 7.2 Electrical characteristics during the on state of a phase-cut dimming system

#### 7.2.1 General

For the on state of a phase-cut dimming system, specifications are dependent on the dimming method, leading edge or trailing edge.

Each half-wave is divided into two periods, the conducting period and the non-conducting period of the phase-cut dimmer.

During the conducting period of the phase-cut dimmer, the mains voltage is applied to the controlgear. During the non-conducting period, the voltage between terminals of the phase-cut dimmer is almost equal to the mains voltage  $(V_D \approx V_M)$ .

#### 7.2.2 Electrical characteristics for leading edge dimming method

#### 7.2.2.1 **General**

Starting from the mains zero crossing, the phase-cut dimmer remains in non-conducting state until its timing element activates the power switch at  $t_{\rm s}$ . Afterwards, the phase-cut dimmer is supplying power to the load for the entire remaining part of the mains half-wave (see Figure 2).

To achieve synchronization with the mains and to control the phase-cut angle correctly, leading edge phase-cut dimmers need to draw a current also during the non-conducting state.

Thus, the controlgear has to be able to conduct a current  $I_{\text{CG\_SL}}$ , which allows synchronization of the phase-cut dimmer with the mains and ensures the supply of power to the phase-cut dimmer even in a two-wire installation.

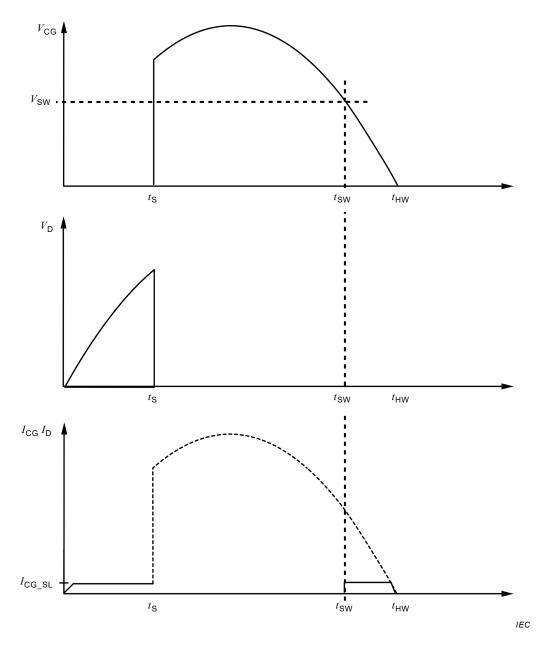


Figure 2 - Timing leading edge dimming method

#### 7.2.2.2 Electrical characteristics during the non-conducting period

During the non-conducting period, the controlgear should comply with the electrical characteristics listed in Tables 1 to 5.

The non-conducting period starts at the zero crossing of the mains and ends at time  $t_s$  when the timing element of the phase-cut dimmer activates the power switch.

During this period, the controlgear should provide a current path with a minimum current-carrying capability of  $I_{\text{CG\_SL}}$  as listed in Tables 1 to 5. At small input voltages of the controlgear when  $I_{\text{CG\_SL}}$  cannot be reached due to the characteristics of its input circuitry (e.g. inrush current limiting elements), only its impedance  $Z_{\text{CG}}$  is defined as listed in Tables 1 to 5.

The controlgear may deactivate its current-carrying capability during the non-conducting period after it has not detected an input voltage waveform showing an unsteady waveform (leading edge characteristic) for 100 ms.

NOTE This is for reducing power losses in case a controlgear is used without a phase-cut dimmer.

Table 1 - Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
	0 V $\leq V_{\text{CG}} \leq$ 3 V: $Z_{\text{CG}}$ not defined
	$3 \text{ V} < V_{CG} \le 6 \text{ V}: Z_{CG} \le 1 200 \Omega$
	$6 \text{ V} < V_{\text{CG}} < V_{\text{SW}} = 22 \text{ V}$ :
0 to t <sub>S</sub>	0 V $\leq$ $V_{\rm CG} \leq$ 3 V: $Z_{\rm CG}$ not defined 3 V $<$ $V_{\rm CG} \leq$ 6 V: $Z_{\rm CG} \leq$ 1 200 $\Omega$ 6 V $<$ $V_{\rm CG} <$ $V_{\rm SW} =$ 22 V: $P_{\rm CG} <$ 12 W: $I_{\rm CG}(t) = I_{\rm CG\_SL} \geq$ 13,8 mA/W $\cdot$ $P_{\rm CG}$
	$P_{\text{CG}} \ge 12 \text{ W}$ : $I_{\text{CG}}(t) = I_{\text{CG\_SL}} \ge 165,6 \text{ mA}$

Table 2 - Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
	$0 \text{ V} \leq V_{\text{CG}} \leq 3 \text{ V}$ : $Z_{\text{CG}}$ not defined
	$3 \text{ V} < V_{CG} \le 6 \text{ V}: Z_{CG} \le 1 \text{ 200 } \Omega$
0 to t <sub>S</sub>	$\begin{array}{l} 0 \; \text{V} \leq V_{\text{CG}} \leq 3 \; \text{V:} \; Z_{\text{CG}} \; \text{not defined} \\ 3 \; \text{V} < V_{\text{CG}} \leq 6 \; \text{V:} \; Z_{\text{CG}} \leq 1 \; 200 \; \Omega \\ 6 \; \text{V} < V_{\text{CG}} < V_{\text{SW}} = 26 \; \text{V:} \\ P_{\text{CG}} \geq 12 \; \text{W:} \\ I_{\text{CG}}(t) = I_{\text{CG\_SL}} \geq 138 \; \text{mA} \end{array}$
	$P_{CG} \ge 12 \text{ W}$ :
	$I_{\text{CG}}(t) = I_{\text{CG\_SL}} \ge 138 \text{ mA}$

Table 3 - Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
	0 V $\leq V_{CG} \leq$ 3 V: $Z_{CG}$ not defined
	$3 \text{ V} < V_{\text{CG}} \le 6 \text{ V}: Z_{\text{CG}} \le 1 \text{ 200 } \Omega$
	6 V < V <sub>CG</sub> < V <sub>SW</sub> = 43 V:
0 to t <sub>s</sub>	$\begin{array}{l} 0 \; \text{V} \leq V_{\text{CG}} \leq 3 \; \text{V} \colon Z_{\text{CG}} \; \text{not defined} \\ 3 \; \text{V} < V_{\text{CG}} \leq 6 \; \text{V} \colon Z_{\text{CG}} \leq 1 \; 200 \; \Omega \\ 6 \; \text{V} < V_{\text{CG}} < V_{\text{SW}} = 43 \; \text{V} \colon \\ P_{\text{CG}} < 12 \; \text{W} \colon \\ I_{\text{CG}} \left(t\right) = I_{\text{CG\_SL}} \geq 6,9 \; \text{mA/W} \cdot P_{\text{CG}} \end{array}$
	$I_{\text{CG}}(t) = I_{\text{CG\_SL}} \ge 6.9 \text{ mA/W} \cdot P_{\text{CG}}$ $P_{\text{CG}} \ge 12 \text{ W}:$
	$I_{\text{CG}} \ge 12 \text{ W}$ : $I_{\text{CG}}(t) = I_{\text{CG\_SL}} \ge 82.8 \text{ mA}$

Table 4 - Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
	0 V $\leq V_{CG} \leq$ 3 V: $Z_{CG}$ not defined
	3 V < $V_{\text{CG}} \leq$ 6 V: $Z_{\text{CG}} \leq$ 1 200 $\Omega$
	6 V < V <sub>CG</sub> < V <sub>SW</sub> = 40 V:
0 to <i>t</i> <sub>S</sub>	$\begin{array}{l} 0 \; \text{V} \leq V_{\text{CG}} \leq 3 \; \text{V} \colon Z_{\text{CG}} \; \text{not defined} \\ 3 \; \text{V} < V_{\text{CG}} \leq 6 \; \text{V} \colon Z_{\text{CG}} \leq 1 \; 200 \; \Omega \\ 6 \; \text{V} < V_{\text{CG}} < V_{\text{SW}} = 40 \; \text{V} \colon \\ P_{\text{CG}} < 12 \; \text{W} \colon \\ I_{\text{CG}}(t) = I_{\text{CG\_SL}} \geq 6 \; \text{mA/W} \cdot P_{\text{CG}} \end{array}$
	$P_{\text{CG}} \ge 12 \text{ W}$ : $I_{\text{CG}}(t) = I_{\text{CG\_SL}} \ge 72 \text{ mA}$

Table 5 - Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
	$0 \text{ V} \leq V_{\text{CG}} \leq 3 \text{ V}: Z_{\text{CG}} \text{ not defined}$
	$3 \text{ V} < V_{CG} \le 6 \text{ V}: Z_{CG} \le 1 \text{ 200 } Ω$
	6 V < V <sub>CG</sub> < V <sub>SW</sub> = 60 V:
) to <i>t</i> <sub>S</sub>	$\begin{array}{l} 0 \; \text{V} \leq V_{\text{CG}} \leq 3 \; \text{V} \colon Z_{\text{CG}} \; \text{not defined} \\ 3 \; \text{V} < V_{\text{CG}} \leq 6 \; \text{V} \colon Z_{\text{CG}} \leq 1 \; 200 \; \Omega \\ 6 \; \text{V} < V_{\text{CG}} < V_{\text{SW}} = 60 \; \text{V} \colon \\ P_{\text{CG}} < 12 \; \text{W} \colon \\ I_{\text{CG}}(t) = I_{\text{CG\_SL}} \geq 5 \; \text{mA/W} \cdot P_{\text{CG}} \\ P_{\text{CG}} \geq 12 \; \text{W} \colon \\ I_{\text{CG}}(t) = I_{\text{CG\_SL}} \geq 60 \; \text{mA} \end{array}$
	$P_{\text{CG}} \ge 12 \text{ W}$ : $I_{\text{CG}}(t) = I_{\text{CG\_SL}} \ge 60 \text{ mA}$

### 7.2.2.3 Electrical characteristics during the transition from the non-conducting to the conducting period

The transition from the non-conducting to the conducting state of the phase-cut dimmer starts at time  $t_{\rm S}$ .

Starting from time  $t_{\rm S}$ , the impedance  $Z_{\rm D}$  of the phase-cut dimmer decreases until its minimum  $Z_{\rm D\_min}$  is reached. The voltage  $V_{\rm CG}$  applied to the controlgear increases towards the instantaneous value  $V_{\rm M}(t)$  of the mains minus the voltage drop across the phase-cut dimmer.

The absolute value of the slew rate of the voltage change of  $V_{\mathsf{D}}$  during the transition period does not exceed the values as listed in Table 6 when the phase-cut dimmer is connected to the marked maximum resistive load.

The slew rate should be calculated based on the measurement of the voltage slope of  $V_{\rm D}$  by measuring the time (dt) between  $V_{\rm D}$ = 0,8 ·  $V_{\rm D}(t_{\rm S})$  and  $V_{\rm D}$  = 0,1 ·  $V_{\rm D}(t_{\rm S})$  and by calculating the differential voltage d  $V_{\rm D}$  = 0,8 ·  $V_{\rm D}(t_{\rm S})$  - 0,1 ·  $V_{\rm D}(t_{\rm S})$ .

When the voltage  $V_{\rm CG}$  exceeds  $V_{\rm SW}$ , the controlgear may deactivate its current carrying capability, thus possibly no current can flow through the controlgear.

NOTE Values for slew rate represent a compromise between EMC, repetitive peak current in the controlgear and switching losses in the phase-cut dimmer power semiconductors.

Table 6 - Slew rate for voltage decrease across the phase-cut dimmer

<i>V</i> <sub>M</sub> [V]	100	120	200	230	277
$dV_D/dt$ [V/ $\mu$ s]	≤ 6,5	≤ 300	≤ 6,5	≤ 6,5	≤ 300

#### 7.2.2.4 Electrical characteristics during the conducting period

During the conducting period, the controlgear should comply with the electrical characteristics listed in Tables 7 to 11.

During this period, full power is applied continuously to the controlgear from the phase-cut dimmer to allow power to be supplied to the controlgear. The values of peak current in Table 7 to 11 apply at the maximum slew rate values given in Table 6.

Due to the low impedance of the phase-cut dimmer during the conducting period, the input voltage of the controlgear is almost equal to the mains voltage.

At time  $t_{SW}$ , the input voltage  $V_{CG}$  of the controlgear falls below  $V_{SW}$ .

From time  $t_{\rm SW}$  to the end of the period, the controlgear should provide a current path with a minimum current-carrying capability of  $I_{\rm CG-SL}$ .

Table 7 - Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
, to .	$Z_{\rm CG}$ not defined
$t_{\rm s}$ to $t_{\rm SW}$	$I_{\text{CG}_{pk}}(P_{\text{CG}}) < 0.111 \text{ A/W}$
	$\begin{array}{l} 0 \; \text{V} \leq V_{\text{CG}} \leq 3 \; \text{V} \colon Z_{\text{CG}} \; \text{not defined} \\ 3 \; \text{V} < V_{\text{CG}} \leq 6 \; \text{V} \colon Z_{\text{CG}} \leq 1 \; 200 \; \Omega \\ 6 \; \text{V} < V_{\text{CG}} < V_{\text{SW}} = 22 \; \text{V} \colon \\ I_{\text{CG}}(t) = I_{\text{CG\_SL}} \geq (0,7 \cdot P_{\text{CG}})/V_{\text{M}} \; \text{or} \\ I_{\text{CG}}(t) = I_{\text{CG\_SL}}(t) \geq (0,7 \cdot V_{\text{CG}}(t))/(V_{\text{M}}^{\; 2}/P_{\text{CG}}) \end{array}$
	$3 \text{ V} < V_{CG} \le 6 \text{ V}: Z_{CG} \le 1 \text{ 200 } \Omega$
$t_{SW}$ to $t_{HW}$	6 V < V <sub>CG</sub> < V <sub>SW</sub> = 22 V:
	$I_{\text{CG}}(t) = I_{\text{CG\_SL}} \ge (0.7 \cdot P_{\text{CG}})/V_{\text{M}} \text{ or}$
	$I_{\text{CG}}(t) = I_{\text{CG SL}}(t) \ge (0.7 \cdot V_{\text{CG}}(t))/(V_{\text{M}}^2/P_{\text{CG}})$

Table 8 - Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t to t	$Z_{\mathrm{CG}}$ not defined
$t_{\rm s}$ to $t_{\rm SW}$	$Z_{\rm CG}$ not defined $I_{\rm CG\_pk} \ (P_{\rm CG}) < {\rm to \ be \ defined}$
	$\begin{array}{l} 0 \; V \leq V_{\mathrm{CG}} \leq 3 \; V \colon Z_{\mathrm{CG}} \; \mathrm{not} \; \mathrm{defined} \\ \\ 3 \; V < V_{\mathrm{CG}} \leq 6 \; V \colon Z_{\mathrm{CG}} \leq 1 \; 200 \; \Omega \\ \\ 6 \; V < V_{\mathrm{CG}} < V_{\mathrm{SW}} = 26 \; V \colon \\ \\ I_{\mathrm{CG}}(t) = I_{\mathrm{CG\_SL}} \geq (0,7 \cdot P_{\mathrm{CG}})/V_{\mathrm{M}} \; \mathrm{or} \\ \\ I_{\mathrm{CG}}(t) = I_{\mathrm{CG\_SL}}(t) \geq (0,7 \cdot V_{\mathrm{CG}}(t))/(V_{\mathrm{M}}^2/P_{\mathrm{CG}}) \end{array}$
	$3 \text{ V} < V_{\text{CG}} \le 6 \text{ V}: Z_{\text{CG}} \le 1 \text{ 200 } Ω$
$t_{SW}$ to $t_{HW}$	$6 \text{ V} < V_{\text{CG}} < V_{\text{SW}} = 26 \text{ V}$ :
	$I_{\text{CG}}(t) = I_{\text{CG\_SL}} \ge (0.7 \cdot P_{\text{CG}})/V_{\text{M}} \text{ or}$
	$I_{CG}(t) = I_{CG\_SL}(t) \ge (0.7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$

Table 9 - Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits			
, to .	$Z_{\rm CG}$ not defined			
$t_{\rm s}$ to $t_{\rm SW}$	$I_{\text{CG\_pk}}(P_{\text{CG}}) < 0.077 \text{ 25 A/W}$			
	$0 \text{ V} \leq V_{\text{CG}} \leq 3 \text{ V}$ : $Z_{\text{CG}}$ not defined			
	$3 \text{ V} < V_{CG} \le 6 \text{ V}: Z_{CG} \le 1 \text{ 200 } \Omega$			
$t_{SW}$ to $t_{HW}$	6 V < V <sub>CG</sub> < V <sub>SW</sub> = 43 V:			
	$3 \ \lor \ \lor \ _{CG} \le 6 \ \lor \ _{Z_{CG}} \le 1200 \ \Omega$ $6 \ \lor \ \lor \ _{C_{G}} < V_{SW} = 43 \ \lor :$ $I_{CG}(t) = I_{CG\_SL} \ge (0,7 \cdot P_{CG})/V_{M} \text{ or}$ $I_{CG}(t) = I_{CG\_SL}(t) \ge (0,7 \cdot V_{CG}(t))/(V_{M}^{2}/P_{CG})$			
	$I_{\text{CG}}(t) = I_{\text{CG\_SL}}(t) \ge (0.7 \cdot V_{\text{CG}}(t)) / (V_{\text{M}}^2 / P_{\text{CG}})$			

Table 10 - Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits			
, to .	$Z_{\rm CG}$ not defined			
$t_{\rm s}$ to $t_{\rm SW}$	$I_{\text{CG\_pk}}(P_{\text{CG}}) < 0.077 \text{ 25 A/W}$			
	0 V $\leq V_{CG} \leq$ 3 V: $Z_{CG}$ not defined			
	$3 \text{ V} < V_{CG} \le 6 \text{ V}: Z_{CG} \le 1 200 \Omega$			
$t_{SW}$ to $t_{HW}$	6 V < V <sub>CG</sub> < V <sub>SW</sub> = 50 V:			
	$I_{\text{CG}}(t) = I_{\text{CG\_SL}} \ge (0.7 \cdot P_{\text{CG}})/V_{\text{M}} \text{ or}$			
	$I_{CG}(t) = I_{CG\_SL}(t) \ge (0.7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$			

Table 11 - Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits			
t to t	$Z_{\rm CG}$ not defined			
$t_{\rm s}$ to $t_{\rm SW}$	$I_{\text{CG\_pk}}\left(P_{\text{CG}}\right) < \text{to be defined}$			
	$0 \text{ V} \leq V_{CG} \leq 3 \text{ V}: Z_{CG} \text{ not defined}$			
	$3 \text{ V} < V_{\text{CG}} \le 6 \text{ V}: Z_{\text{CG}} \le 1 \text{ 200 } \Omega$ $6 \text{ V} < V_{\text{CG}} < V_{\text{SW}} = 60 \text{ V}:$			
$t_{SW}$ to $t_{HW}$	$6 \text{ V} < V_{\text{CG}} < V_{\text{SW}} = 60 \text{ V}$ :			
	$I_{\text{CG}}(t) = I_{\text{CG\_SL}} \ge (0.7 \cdot P_{\text{CG}})/V_{\text{M}} \text{ or }$ $I_{\text{CG}}(t) = I_{\text{CG\_SL}}(t) \ge (0.7 \cdot V_{\text{CG}}(t))/(V_{\text{M}}^2/P_{\text{CG}})$			
	$I_{CG}(t) = I_{CG\_SL}(t) \ge (0.7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$			

#### 7.2.3 Electrical characteristics for trailing edge dimming method

#### 7.2.3.1 **General**

Starting from the mains zero crossing, the phase-cut dimmer operates in conducting state until its timing element deactivates the power switch at time  $t_{\rm s1}$ . Afterwards, the phase-cut dimmer is not significantly supplying power to the load for the entire remaining part of the mains half-wave (see Figure 3).

To achieve synchronization with the mains and to control the phase-cut angle correctly, trailing edge phase-cut dimmers need to draw a current also during the non-conducting state.

Thus, the controlgear has to be able to conduct a current  $I_{\text{CG\_STH}}$ , which allows synchronization of the phase-cut dimmer with the mains and ensures the supply of power to the phase-cut dimmer even in a two-wire installation.

Since the negative voltage slope that is triggered by the switch-off of the power switch of the phase-cut dimmer is not only determined by the current  $I_{\text{CG\_STL}}$  that is conducted by the controlgear, but also by the effective capacitance of the wiring and the capacitance being effective in parallel to the phase-cut dimmer, the sum of these capacitances has to be considered.

This document and all listed values are based on systems having a maximum capacitance of the wiring of 10 nF being effective in parallel to the controlgear.

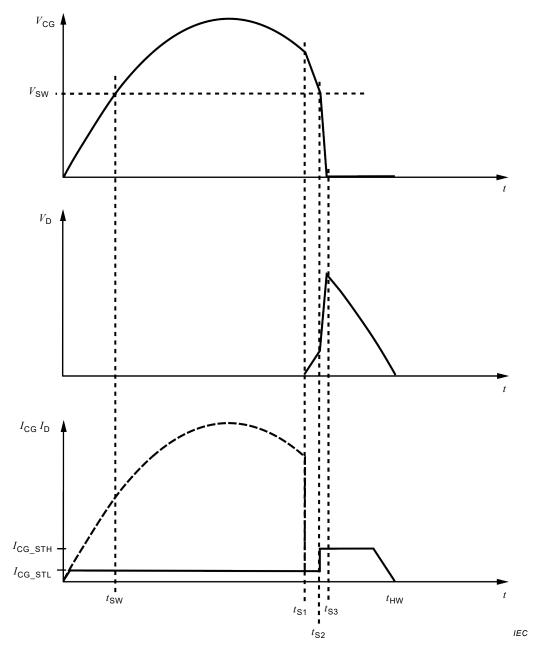


Figure 3 - Timing trailing edge dimming method

#### 7.2.3.2 Electrical characteristics during the conducting period

The conducting period starts at the zero crossing of the mains and ends at time  $t_{\rm S1}$  when the timing element of the phase-cut dimmer deactivates its power switch and the impedance of the phase-cut dimmer  $Z_{\rm D}$  increases towards  $Z_{\rm D-max}$ .

During the conducting period, the controlgear should comply with the electrical characteristics listed in Table 12.

During this period, the phase-cut dimmer continuously applies full power to the controlgear. Therefore, the impedance  $Z_{\rm D}$  of the phase-cut dimmer remains continuously at its minimum value  $Z_{\rm D}$  min, independently from the current  $I_{\rm D}$  =  $I_{\rm CG}$ .

The impedance  $Z_{\rm D}$  of the phase-cut dimmer is  $Z_{\rm D\_min}$  when the voltage  $V_{\rm D}(t)$  across the phase-cut dimmer is less than 0,1  $\cdot$   $V_{\rm M}(t)$  during the entire conduction period.

Due to the low impedance of the phase-cut dimmer during the conducting period, the input voltage of the controlgear is almost equal to the instantaneous value of the mains voltage.

From the zero crossing of the mains to time  $t_{\rm s1}$ , the controlgear should provide a current path with a minimum current-carrying capability of  $I_{\rm CG-STL}$  as listed in Table 12.

Since the current  $I_{\text{CG\_STL}}$  is based on nominal data of a controlgear, a factor of 0,7 is inserted to account for the fact that the current drawn by the controlgear will have some distortion or displacement and may not be a perfect sine-wave or rectangular shape. Therefore the factor 0,7 introduces some margin for this. Additionally, according to this document the controlgear may not operate with its nominal wattage even at the maximum conduction angle.

Table 12 - Nominal mains voltage from 100 V to 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits			
	0 V $\leq V_{CG} \leq$ 3 V: $Z_{CG}$ not defined			
	0 V $\leq$ $V_{\rm CG} \leq$ 3 V: $Z_{\rm CG}$ not defined 3 V $<$ $V_{\rm CG} \leq$ 6 V: $Z_{\rm CG} \leq$ 1 200 $\Omega$			
0 to t <sub>s1</sub>	$V_{\text{CG}} > 6 \text{ V}$ : $I_{\text{CG}}(t) = I_{\text{CG\_STL}} \ge (0.7 \cdot P_{\text{CG}})/V_{\text{M}} \text{ or}$ $I_{\text{CG}}(t) = I_{\text{CG\_STL}}(t) \ge (0.7 \cdot V_{\text{CG}}(t))/(V_{\text{M}}^2/P_{\text{CG}})$			
	$I_{\text{CG}}(t) = I_{\text{CG\_STL}} \ge (0.7 \cdot P_{\text{CG}})/V_{\text{M}} \text{ or}$			
	$I_{\text{CG}}(t) = I_{\text{CG\_STL}}(t) \ge (0.7 \cdot V_{\text{CG}}(t))/(V_{\text{M}}^2/P_{\text{CG}})$			

### 7.2.3.3 Electrical characteristics during the transition from the conducting to the non-conducting period

The transition from the conducting to the non-conducting state of the phase-cut dimmer starts at time  $t_{s1}$  and ends at time  $t_{s3}$ .

At the time  $t_{\rm S1}$ , the impedance  $Z_{\rm D}$  of the phase-cut dimmer starts to increase towards  $Z_{\rm D\_max}$ . From time  $t_{\rm S1}$  to  $t_{\rm S2}$ , the phase-cut dimmer limits the current  $I_{\rm D}$ .

The minimum value for  $t_t = t_{s2} - t_{s1}$  should be as listed in Tables 13 to 17.

Since the controlgear provides a minimum current-carrying capability of  $I_{\text{CG\_STL}}$  (see Tables 13 to 17), the voltage across the input terminals of the controlgear decreases towards zero and falls below the voltage  $V_{\text{SW}}$  at  $t_{\text{S2}}$  (see Figure 3).

NOTE 1 This requirement is to ensure that parasitic capacities of the installation, the active capacity  $C_f$  between the terminals of the phase-cut dimmer (see Figure 3) and a capacitor that might be assembled inside the

controlgear and which is connected directly with the mains terminals of the controlgear is discharged in a reasonable time to allow the phase-cut dimmer to supply itself sufficiently.

NOTE 2 The ratio between the values for the period  $t_{\rm S2}$  to  $t_{\rm HW}$  as given in Tables 13 to 17 for the different mains voltages is proportional to the ratio of the relevant mains voltages. The values for  $I_{\rm CG\_STH}$  scale inversely with the mains voltage. The value for  $I_{\rm D\_nc}$  is always 10 % lower than the relevant  $I_{\rm CG\_STH}$ .

The slew rate SR should be calculated based on the measurement of the voltage slope of  $V_{\text{CG}}$  by measuring the time (dt) between  $V_{\text{CG}}$  = 0,8 ·  $V_{\text{CG}}(t_{\text{S1}})$  and  $V_{\text{CG}}$  =  $V_{\text{SW}}$  and by calculating the differential voltage d $V_{\text{CG}}$  = 0,8 ·  $V_{\text{CG}}(t_{\text{S1}})$  –  $V_{\text{SW}}$ .

When the voltage  $V_{\rm CG}$  falls below  $V_{\rm SW}$  (time  $t_{\rm S2}$ ), the controlgear should provide a minimum current-carrying capability of  $I_{\rm CG}$  STH as listed in Tables 13 to 17.

NOTE 3 The values for  $V_{\rm SW}$  and  $I_{\rm CG\ STH}$  are selected to achieve a good compromise between the ability for the phase-cut dimmer to supply itself on one side and the appearing power loss in the controlgear on the other side.

NOTE 4  $t_{\rm s2}$  is defined by the time at which  $V_{\rm CG}$  falls below  $V_{\rm SW}$ .  $V_{\rm CG}$  and  $I_{\rm D}$  can be measured simultaneously with a 4-channel oscilloscope, and the value of  $I_{\rm D}$  between  $t_{\rm s1}$  and  $t_{\rm s2}$  can be determined. The break in slope of  $V_{\rm D}$  at  $t_{\rm s2}$  (if such a break in slope exists) is not a criteria to define  $t_{\rm s2}$ .

Table 13 - Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability			
$t_{s1}$ to $t_{s2}$	$\begin{aligned} t &= t_{\text{s1}}: \\ I_{\text{CG}}(t) &= I_{\text{CG\_STL}} \ge (0.7 \cdot P_{\text{CG}}) / V_{\text{M}} \text{ or } \\ I_{\text{CG}}(t) &= I_{\text{CG\_STL}}(t) \ge (0.7 \cdot V_{\text{CG}}(t)) / (V_{\text{M}}^2 / P_{\text{CG}}) \end{aligned}$			
$t_{s2} - t_{s1} \ge t_{t}$ $t_{t} = (1/SR) \cdot V_{M}(t_{s1})$	$t_{s1} < t \le t_{s2}$ : $SR =  dV_{CG}/dt  \ge 0.09 \text{ V/}\mu\text{s} (50 \text{ Hz})$ $SR =  dV_{CG}/dt  \ge 0.108 \text{ V/}\mu\text{s} (60 \text{ Hz})$			
	when the CG is supplied by a current source driving (2,8 mA $\cdot$ $P_{\rm CG}$ )/W from $t_{\rm s1}$ to $t_{\rm s2}$ .			
	$0 \text{ V} \leq V_{\text{CG}} \leq 3 \text{ V}: Z_{\text{CG}} \text{ not defined}$			
$t_{s2}$ to $t_{HW}$	3 V < $V_{\rm CG} \le$ 6 V: $Z_{\rm CG} \le$ 1 200 $\Omega$ 6 V < $V_{\rm CG} < V_{\rm SW} =$ 22 V: $P_{\rm CG} <$ 12 W: $I_{\rm CG} (t) = I_{\rm CG\_STH} \ge$ 13,8 mA/W · $P_{\rm CG}$ $P_{\rm CG} \ge$ 12 W: $I_{\rm CG} (t) = I_{\rm CG\_STH} \ge$ 165,6 mA			

Table 14 - Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability			
$t_{s1}$ to $t_{s2}$	$\begin{array}{l} t = t_{\text{s1}}: \\ I_{\text{CG}}(t) = I_{\text{CG\_STL}} \ge (0.7 \cdot P_{\text{CG}}) / V_{\text{M}} \text{ or } \\ I_{\text{CG}}(t) = I_{\text{CG\_STL}}(t) \ge (0.7 \cdot V_{\text{CG}}(t)) / (V_{\text{M}}^2 / P_{\text{CG}}) \end{array}$			
$t_{s2} - t_{s1} \ge t_{t}$	$t_{s1} < t \le t_{s2}$ : $SR =  dV_{CG}/dt  \ge 0.0105 \text{ V/}\mu\text{s} (50 \text{ Hz})$			
$t_{t} = (1/SR) \cdot V_{M}(t_{s1})$	$SR =  dV_{CG}/dt  \ge 0.126 \text{ V/}\mu\text{s} (60 \text{ Hz})$			
t / Misi/	when the CG is supplied by a current source driving (2,8 mA $\cdot$ $P_{\rm CG})$ /W from $t_{\rm s1}$ to $t_{\rm s2}.$			
	$0 \text{ V} \leq V_{CG} \leq 3 \text{ V}: Z_{CG} \text{ not defined}$			
	$3 \text{ V} < V_{CG} \le 6 \text{ V}: Z_{CG} \le 1 200 \Omega$			
	$6 \text{ V} < V_{\text{CG}} < V_{\text{SW}} = 26 \text{ V}$ :			
$t_{\rm s2}$ to $t_{\rm HW}$	$P_{\text{CG}} < 12 \text{ W}:$ $I_{\text{CG}}(t) = I_{\text{CG\_STH}} \ge 11,5 \text{mA/W} \cdot P_{\text{CG}}$			
	$P_{\text{CG}} \ge 12 \text{ W}$ : $I_{\text{CG}}(t) = I_{\text{CG\_STH}} \ge 138 \text{ mA}$			

Table 15 - Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability				
$t_{s1}$ to $t_{s2}$ $t_{s2} - t_{s1} \ge t_{t}$	$\begin{split} t &= t_{\text{s1}}; \\ I_{\text{CG}}(t) &= I_{\text{CG\_STL}} \ge (0,7 \cdot P_{\text{CG}}) / V_{\text{M}} \text{ or } \\ I_{\text{CG}}(t) &= I_{\text{CG\_STL}}(t) \ge (0,7 \cdot V_{\text{CG}}(t)) / (V_{\text{M}}^2 / P_{\text{CG}}) \\ t_{\text{s1}} &< t \le t_{\text{s2}}; \\ SR &=  \text{d}V_{\text{CG}} / \text{d}t  \ge 0,175 \text{ V/}\mu\text{s } (50 \text{ Hz}) \\ SR &=  \text{d}V_{\text{CG}} / \text{d}t  \ge 0,210 \text{ V/}\mu\text{s } (60 \text{ Hz}) \end{split}$				
$t_{t} = (1/SR) \cdot V_{M}(t_{s1})$	when the CG is supplied by a current source driving (2,8 mA $\cdot$ $P_{\rm CG}$ )/W from $t_{\rm s1}$ to $t_{\rm s2}$ .				
$t_{\rm s2}$ to $t_{\rm HW}$	$\begin{array}{l} 0 \; \text{V} \leq V_{\text{CG}} \leq 3 \; \text{V: } Z_{\text{CG}} \; \text{not defined} \\ 3 \; \text{V} < V_{\text{CG}} \leq 6 \; \text{V: } Z_{\text{CG}} \leq 1 \; 200 \; \Omega \\ 6 \; \text{V} < V_{\text{CG}} < V_{\text{SW}} = 43 \; \text{V:} \\ P_{\text{CG}} < 12 \; \text{W:} \\ I_{\text{CG}} \; (t) = I_{\text{CG\_STH}} \geq 6.9 \; \text{mA/W} \; \cdot P_{\text{CG}} \\ P_{\text{CG}} \geq 12 \; \text{W:} \\ I_{\text{CG}} \; (t) = I_{\text{CG\_STH}} \geq \; 82.8 \; \text{mA} \end{array}$				

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability				
$t_{s1}$ to $t_{s2}$	$ \begin{aligned} t &= t_{\text{S1}}: \\ I_{\text{CG}}(t) &= I_{\text{CG\_STL}} \ge (0,7 \cdot P_{\text{CG}})/V_{\text{M}} \text{ or } \\ I_{\text{CG}}(t) &= I_{\text{CG\_STL}}(t) \ge (0,7 \cdot V_{\text{CG}}(t))/(V_{\text{M}}^2/P_{\text{CG}}) \end{aligned} $				
$t_{s2} - t_{s1} \ge t_{t}$	$t_{s1} < t \le t_{s2}:$ $SR =  dV_{CG}/dt  \ge 0.2 \text{ V/}\mu\text{s (50 Hz)}$				
$t_{t} = (1/SR) \cdot V_{M}(t_{s1})$	$SR =  dV_{CG}/dt  \ge 0.24 \text{ V/}\mu\text{s} (60 \text{ Hz})$				
	when the CG is supplied by a current source driving (2,8 mA $\cdot$ $P_{\rm CG}$ )/W from $t_{\rm s1}$ to $t_{\rm s2}$ .				
	$0 \text{ V} \leq V_{CG} \leq 3 \text{ V}: Z_{CG} \text{ not defined}$				
	$3 \text{ V} < V_{CG} \le 6 \text{ V}: Z_{CG} \le 1 200 \Omega$				
	6 V < V <sub>CG</sub> < V <sub>SW</sub> = 40 V:				
$t_{\rm s2}$ to $t_{\rm HW}$	$P_{\text{CG}} < 12 \text{ W}:$ $I_{\text{CG}}(t) = I_{\text{CG\_STH}} \ge 6 \text{ mA/W} \cdot P_{\text{CG}}$				
	$P_{\text{CG}} \ge 12 \text{ W}$ : $I_{\text{CG}}(t) = I_{\text{CG\_STH}} \ge 72 \text{ mA}$				

Table 16 - Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz

Table 17 - Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability				
$t_{s1}$ to $t_{s2}$ $t_{s2} - t_{s1} \ge t_{t}$ $t_{t} = (1/SR) \cdot V_{M}(t_{s1})$	$\begin{split} t &= t_{\text{s1}} : \\ I_{\text{CG}}(t) &= I_{\text{CG\_STL}} \ge (0,7 \cdot P_{\text{CG}}) / V_{\text{M}} \text{ or } \\ I_{\text{CG}}(t) &= I_{\text{CG\_STL}}(t) \ge (0,7 \cdot V_{\text{CG}}(t)) / (V_{\text{M}}^2 / P_{\text{CG}}) \\ t_{\text{s1}} &< t \le t_{\text{s2}} : \\ SR &=  \text{d}V_{\text{CG}} / \text{d}t  \ge 0,245 \text{ V/} \mu \text{s (50 Hz)} \\ SR &=  \text{d}V_{\text{CG}} / \text{d}t  \ge 0,295 \text{ V/} \mu \text{s (60 Hz)} \end{split}$				
	when the CG is supplied by a current source driving (2,8 mA $\cdot$ $P_{\rm CG})$ /W from $t_{\rm s1}$ to $t_{\rm s2}.$				
$t_{\rm s2}$ to $t_{\rm HW}$	$\begin{array}{l} 0 \; \text{V} \leq V_{\text{CG}} \leq 3 \; \text{V} \colon Z_{\text{CG}} \; \text{not defined} \\ 3 \; \text{V} < V_{\text{CG}} \leq 6 \; \text{V} \colon Z_{\text{CG}} \leq 1 \; 200 \; \Omega \\ 6 \; \text{V} < V_{\text{CG}} < V_{\text{SW}} = 60 \; \text{V} \colon \\ P_{\text{CG}} < 12 \; \text{W} \colon \\ I_{\text{CG}} \; (t) = I_{\text{CG\_STH}} \geq 5 \; \text{mA/W} \cdot P_{\text{CG}} \\ P_{\text{CG}} \geq 12 \; \text{W} \colon \\ I_{\text{CG}} \; (t) = I_{\text{CG\_STH}} \geq \; 60 \; \text{mA} \end{array}$				

#### 7.2.3.4 Electrical characteristics during the non-conducting period

During the non-conducting period, the controlgear should comply with the electrical characteristics listed in Tables 13 to 17.

The non-conducting period ends at the next zero crossing of the mains at time  $t_{\rm HW}$ .

During this period, the controlgear should provide a minimum current-carrying capability of  $I_{\text{CG\_STH}}$  as listed in Tables 13 to 17. At small input voltages of the controlgear when  $I_{\text{CG\_STH}}$  cannot be reached due to the characteristics of its input circuitry (e.g. inrush current limiting elements), only its impedance  $Z_{\text{CG}}$  is defined as listed in Tables 13 to 17.

During this period, the phase-cut dimmer limits the current  $I_{\rm D}$  to  $n \cdot I_{\rm D\_nc}$  as listed in IEC TR 63036, whereby  $I_{\rm D}$  nc is related to  $P_{\rm min}$  of the phase-cut dimmer.

The controlgear may deactivate its current-carrying capability during the non-conducting period after it has not detected an input voltage waveform showing trailing edge characteristics for 100 ms.

NOTE This is for reducing power losses in case a controlgear is used without a phase-cut dimmer.

#### 7.3 Electrical characteristics during the off state of a phase-cut dimming system

The off state of a phase-cut dimming system is when no lamp connected with a controlgear is emitting light.

To set a controlgear in the off state, the phase-cut dimmer increases its impedance  $Z_D$  until the controlgear is not sufficiently supplied with power to operate the lamp.

A phase-cut dimmer that needs no supply during the off state of all connected controlgear may open the current loop of the system, for example by means of a mechanical switch.

A phase-cut dimmer that needs a power supply also during the off state of all connected controlgear requires that the connected controlgear provide a current carrying capability, although no lamp is operated (electronic off state) in order to provide power to the electronic circuits within the dimmer to enable returning to the on-state when demanded.

If none of the connected controlgear is able to provide the current carrying capability due to insufficient power, the impedance  $Z_{\rm CG}$  of the controlgear will increase.

The phase-cut dimmer may reduce its impedance  $Z_{\rm D}$  to supply power to the connected controlgear in order to reestablish a current carrying capability that carries the needed supply current  $I_{\rm D_nc}$ .

By reducing  $Z_{\rm D}$ , the voltage  $V_{\rm D}$  will decrease and the voltage  $V_{\rm CG}$  will increase, thus all connected controlgear are energized and the requested current carrying capability is generated in the system to carry the required supply current  $I_{\rm D}$  of the phase-cut dimmer.

The controlgear should provide a minimum current carrying capability of  $I_{PO}$  when the voltage  $V_{CG}$  is in the range of  $V_{PO}$  to  $V_{SW}$  (see Table 18). For voltages  $V_{CG}$  smaller than  $V_{PO}$  and higher than  $V_{SW}$ , the current carrying capability of the controlgear is not defined.

The controlgear should not operate the lamp when the voltage  $V_{\rm CG}$  is below  $V_{\rm SW}$ , so no light should be emitted.

The phase-cut dimmer limits the current to a level that ensures that the voltage  $V_{\rm CG}$  that is applied to the controlgear does not exceed  $V_{\rm SW}$ .

Table 18 – Currents and voltages for controlgear during the electronic off state

V <sub>M</sub> [V]	100	120	200	230	277
V <sub>PO</sub> [V]	15	15	30	30	30
I <sub>PO</sub> [mA]	20	20	10	10	10
I <sub>PO _rms</sub> [mA]	8	8	4	4	4

Values for voltages and currents are instantaneous values except  $I_{\mbox{\footnotesize{PO}}}$   $_{\mbox{\footnotesize{rms}}}.$ 

#### 8 Test procedures

#### 8.1 General

To simplify the description of the test setups and the test procedures, testing conditions for controlgear related to specific moments in time are defined in degree phase angle related to the mains zero crossings. Thus, a definition of different values for the moments in time such as  $t_{\rm S1}$ ,  $t_{\rm S2}$  or  $t_{\rm HW}$  is not necessary for different mains frequencies.

<i>V</i> <sub>M</sub> [V]	100	120	200	230	277	
$R_{R}$	$V_M^2 / P_max$	$V_M^2 / P_max$	$V_M^2 / P_max$	$V_M^2 / P_max$	$V_M^2 / P_max$	
V <sub>test</sub> [V]	0 to 23	0 to 23	0 to 45	0 to 45	0 to 45	
V <sub>1</sub> [V]	8	8	8	8	8	
SR <sub>L</sub> [V/μs]	Refers to Table 2	Refers to Table 2				
$\alpha_{L}$	90°	90°				
$\beta_{L}$	120°	120°				
SR <sub>T</sub> [V/ms]	200	200	200	200	200	
$\alpha_{T}$	120°					

Table 19 - Parameters for testing purposes

#### 8.2 Tests for leading edge dimmable devices

#### 8.2.1 General

Tests concerning the electrical characteristics should ensure compliance of devices with this document in terms of electrical behavior of controlgear during different periods of mains waveform according to 7.2.2.

A test circuit as shown in Figure 4 should be used to test the controlgear.

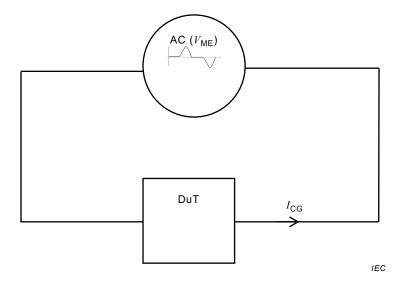


Figure 4 - Test setup for testing the conducting phase

#### 8.2.2 Test related to the non-conducting phase

Pre-condition

Controlgear applied to an AC test voltage source ( $V_{\rm ME}$ ) providing the relevant mains voltage according to Clause A.2 with the values of  $V_{\rm 1},~\alpha_{\rm L}$  and  $SR_{\rm L}$  given in Table 19.

Test:

Measure the current  $I_{\rm CG}$  of the controlgear.

Measure  $I_{\rm CG}$  from 0° until  $V_{\rm CG} > V_{\rm SW}$ 

Expected results:

6 V  $\leq$   $V_{\rm CG} \leq$   $V_{\rm SW}$ :  $I_{\rm CG} \geq$   $I_{\rm CG-SL}$  as listed in Tables 1 to 5

NOTE The controlgear may deactivate its current-carrying capability during the non-conducting phase after it has not detected an input voltage waveform showing an unsteady waveform (leading edge characteristic) for one minute.

## 8.2.3 Test related to the transition from the non-conducting to the conducting phase and to the conducting phase

Pre-condition:

Controlgear applied to an AC test voltage source (VME) providing the relevant mains voltage according to Clause A.2 with the values of  $V_1$ ,  $\alpha_1$  and  $SR_1$  given in Table 19.

Test:

Measure the current  $I_{\rm CG}$  of the controlgear

Measure  $I_{\text{CG}}$  from  $t_{\text{s}}$  ( $\alpha_{\text{L}}$ ) to  $t_{\text{SW}}$  and

Measure  $I_{\rm CG}$  from  $t_{\rm SW}$  to  $t_{\rm HW}$ 

Expected results:

from  $t_s$  to  $t_{SW}$ :

 $I_{\text{CG}} \leq I_{\text{CG_pk}} \left( P_{\text{CG}} \right)$ 

from  $t_{\rm SW}$  to  $t_{\rm HW}$ :

3 V <  $V_{\rm CG}$   $\leq$  6 V:  $I_{\rm CG}$   $\geq$   $V_{\rm CG}/Z_{\rm CG}$  with  $Z_{\rm CG}$  as listed in Tables 7 to 11

6 V <  $V_{\rm CG}$  <  $V_{\rm SW}$ :  $I_{\rm CG}$  =  $I_{\rm CG~SL}$  as listed in Tables 7 to 11

#### 8.3 Tests for trailing edge dimmable devices

#### 8.3.1 General

Tests concerning the electrical characteristics should ensure compliance of devices with this document in terms of electrical behavior of controlgear during different periods of mains waveform according to 7.2.3.

#### 8.3.2 Test related to the conducting phase

For an applicable test circuit, see Figure 4.

#### Pre-condition:

Controlgear applied to an AC test voltage source ( $V_{\rm ME}$ ) providing the relevant mains voltage according to Clause A.3 with the values of  $V_1, \alpha_{\rm T}$  and  $SR_{\rm T}$  given in Table 19

Time related to last zero crossing: 0 to  $V(t) < V_{SW}$ 

Test: Measure  $I_{\rm CG}$  in dependence of instantaneous value of applied voltage

Expected results:

3 V  $\leq V_{\text{CG}} \leq$  6V:  $I_{\text{CG}} \geq V_{\text{CG}}/Z_{\text{CG}}$  with  $Z_{\text{CG}}$  as listed in Table 12

 $V_{\text{CG}} \ge 6 \text{ V}$ :  $I_{\text{CG}} = I_{\text{CG\_SL}} \ge (0.7 \cdot P_{\text{CG}})/V_{\text{M}} \text{ or } I_{\text{CG}} = I_{\text{CG\_STL}}(t) \ge (0.7 \cdot V_{\text{CG}}(t))/(V_{\text{M}}^2/P_{\text{CG}})$ 

## 8.3.3 Test related to the transition from the conducting phase to the non-conducting phase

For an applicable test circuit, see Figure 5.

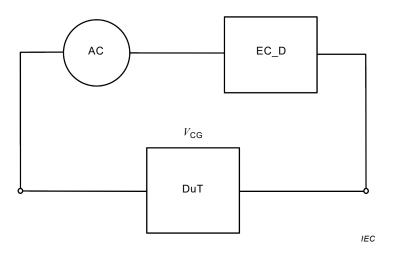


Figure 5 – Test setup for the transition from the conducting to the non-conducting phase

#### Pre-condition:

Controlgear connected to the EC\_D according to Annex B as shown in Figure 5, system powered with relevant mains voltage. Adjust the current  $I_D$  according to Annex B as given in Tables 13 to 17

Time related to last zero crossing:  $t_{s1}$  to  $t_{s2}$ 

Test

Measure  $|dV_{CG}/dt|$  with a conduction angle of the EC\_D of 90°, repeat this measurement with conducting angles of the EC\_D of 60° and 120°

Expected result:

When the conduction angle of EC\_D is terminated ( $t_{s1}$ ), the voltage across the input terminals of the controlgear decreases with  $|dV_{CG}/dt| \ge SR$ , as listed in Tables 13 to 17.

The slew rate SR should be calculated based on the measurement of the voltage slope of  $V_{\rm CG}$  by measuring the time (dt) between  $V_{\rm CG}$ = 0,8 ·  $V_{\rm CG}(t_{\rm S1})$  and  $V_{\rm CG}$  =  $V_{\rm SW}$  and by calculating the differential voltage d $V_{\rm CG}$  = 0,8 ·  $V_{\rm CG}(t_{\rm S1})$  –  $V_{\rm SW}$ .

#### 8.3.4 Test related to the non-conducting phase

For an applicable test circuit, see Figure 6.

#### Pre-condition:

Controlgear applied to an AC test voltage source ( $V_{\rm ME}$ ) providing the relevant mains voltage according to Clause A.2 with the values of  $V_{\rm 1}$ ,  $\alpha_{\rm L}$  and  $SR_{\rm L}$  given in Table 19.

Time related to last zero crossing:  $t_{\rm s2}$  to  $t_{\rm HW}$ 

Test: Measure  $I_{\rm CG}$  in dependence of instantaneous value of applied voltage

Expected results:

 $6V \leq V_{CG} \leq V_{SW}$ :  $I_{CG} \geq I_{CG STH}$ 

 $3V \le V_{\rm CG} < 6V$ :  $I_{\rm CG} \ge V_{\rm CG}/Z_{\rm CG}$  with  $Z_{\rm CG}$  as listed in Tables 13 to 17

#### 8.4 Tests for characteristics during electronic off state

Tests concerning the electrical characteristics should ensure compliance of devices with this document in terms of electrical behavior of controlgear during the electronic off state of a phase-cut dimming system according to 7.3.

A test circuit as shown in Figure 6 should be used to test the controlgear.

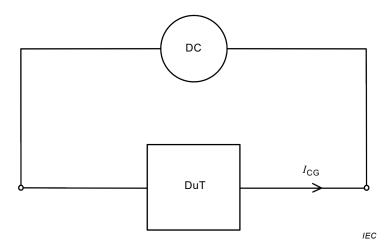


Figure 6 - Test setup for the non-conducting phase

Pre-condition:

Controlgear connected to a controllable DC voltage source

Test:

Vary the voltage of the DC source within the range for  $V_{\rm test}$  as given in Table 19 for the relevant mains voltage.

Measure  $I_{\mathrm{CG}}$  and record at which voltages in the range of  $V_{\mathrm{test}}$  the current carrying capability is activated

Expected results

Controlgear provides a current carrying capability  $I_{PO}$  at  $V_{PO} \le V_{PO} < V_{SW}$  as listed in Tables 1 to 5, 7 to 11, 13 to 17

Controlgear does not operate the lamp at  $V_{\rm CG} \leq V_{\rm SW}$ , no light is emitted

## Annex A (informative)

#### Voltage shapes to be used with the tests in IEC TR 63037

#### A.1 General

A test AC voltage source ( $V_{\text{ME}}$ ) with the waveform as shown in Figure A.1 or Figure A.2 should be used as indicated in the defined tests. The detailed settings for time and voltage should be set with an accuracy of  $\leq$  1 %. The internal resistance of this voltage source should not exceed 1  $\Omega$ .

#### A.2 Waveform description

 $0^{\circ}$  to  $\alpha^{\circ}$ : constant voltage with the value  $V_1$ 

 $\alpha^{\circ}$  to  $\alpha_1^{\circ}$ : constant slew rate (SR)

 $\alpha_1^{\circ}$  to 180°: sinusoidal voltage according to  $V_{\rm M}$ 

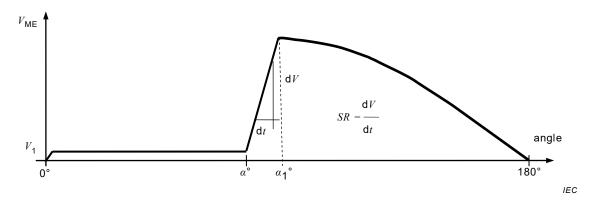


Figure A.1 - Waveform of AC voltage source

#### A.3 Waveform description

 $0^{\circ}$  to  $\beta^{\circ}$ : sinusoidal voltage according to  $V_{\mathsf{M}}$ 

 $\beta^{\circ}$  to  $\beta_{1}^{\circ}$ : constant slew rate (SR)

 $\beta_1^{\circ}$  to 180°: constant voltage with the value  $V_1$ 

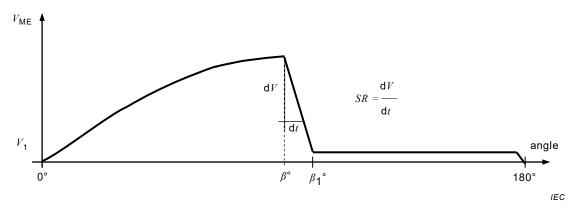


Figure A.2 - Waveform of AC voltage source

## Annex B (informative)

#### Equivalent phase-cut dimmer circuit

Figure B.1 shows the equivalent circuit EC\_D for a phase-cut dimmer:

Components and values are only exemplary beside capacitance C2 which is mandatory, representing the maximum wiring capacitance.

V2 is a pulse generator that provides a control signal for the transistors T1 and T2 leading to conduction states of these two transistors in order that the correct phase angle is adjusted.

Adjust the current  $I_{\rm D}$  = ( $I_{\rm trans} \cdot P_{\rm min}$ )/W according to Tables 13 to 17 by varying R20.

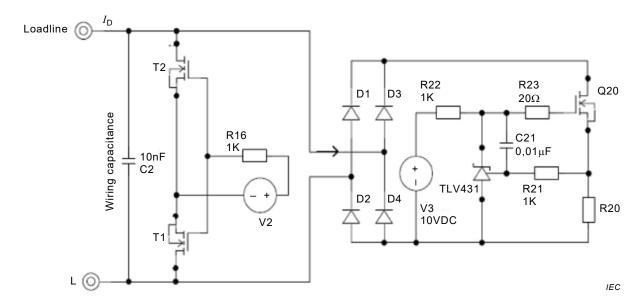


Figure B.1 - Scheme of the EC\_D

#### Bibliography

IEC 60038, IEC standard voltages

IEC 60364 (all parts), Low-voltage electrical installations

IEC TR 63036, Electrical interface specification for phase-cut dimmer in phase-cut dimmed lighting systems



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