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BSI Standards Publication

Device embedded substrate

Part 2-2: Guidelines — Electrical testing

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National foreword

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A list of organizations represented on this committee can be obtained on request to its secretary.

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RAPPORT TECHNIQUE

colour inside

Device embedded substrate –
Part 2-2: Guidelines – Electrical testing

Substrat avec appareil(s) intégré(s) –
Partie 2-2: Directives – Essai électrique

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ELECTROTECHNICAL
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CONTENTS

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DEVICE EMBEDDED SUBSTRATE –

Part 2-2: Guidelines – Electrical testing

FOREWORD

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IEC TR 62878-2-2, which is a Technical Report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this Technical Report is based on the following documents:

Enquiry draft	Report on voting
91/1220/DTR	91/1245/RVC

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

The French version of this Technical Report has not been voted upon.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62878 series, published under the general title *Device embedded substrate*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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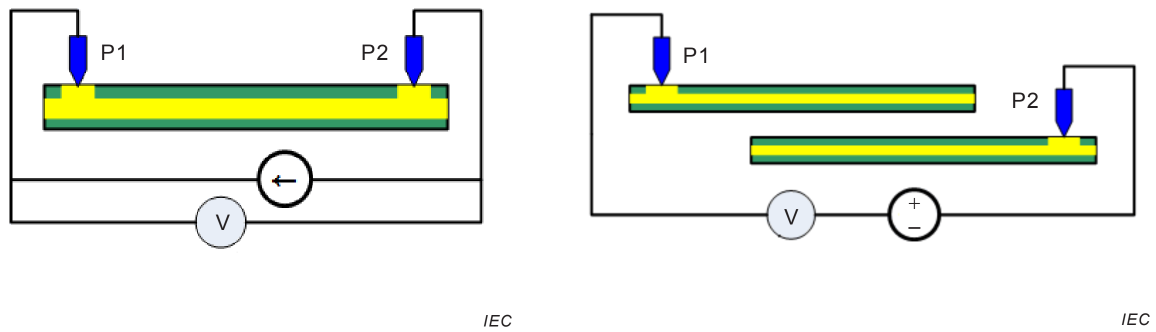
INTRODUCTION

Current electrical package designs are becoming more complex, more functionally integrated, more reliable and more miniaturized than ever. Hence, electrical tests should be classified into levels in order to ensure the performance and quality of device embedded substrates since the substrate contains active/passive devices within it. While the interconnection open/short test is enough for general substrates, functional tests should be done when active/passive devices are embedded inside the substrate. However, the main problem is that we need to understand which devices are embedded and how they are connected functionally to each other. This is the main reason that there should be standardized test methods for device embedded substrate. Figure 1 shows the existing substrate test method: the interconnection open/short test.



a) **Open test** b) **Short test**

Figure 1 – Interconnection open/short test

DEVICE EMBEDDED SUBSTRATE –

Part 2-2: Guidelines – Electrical testing

1 Scope

This part of IEC 62878, which is a Technical Report, describes the necessary information on electrical testing for device embedded substrate. This includes the interconnection open- and short-circuit tests as well as the device functional test. It also provides guidelines by demonstrating the electrical test for device embedded substrate.

This part of IEC 62878 is applicable to device embedded substrates fabricated by use of organic base material, which include for example active or passive devices, discrete components formed in the fabrication process of electronic wiring board, and sheet formed components.

The IEC 62878 series does not apply to the re-distribution layer (RDL) nor to the electronic modules defined as an M-type business model in IEC 62421.

2 Electrical tests

2.1 Test level 1A for device embedded substrate

Test level 1A for device embedded substrate is to check the continuity and isolation of interconnections which are not connected to any embedded components. This is shown in Figure 2. Test point 1 and test point 2 are on different networks. After measuring the resistance between net 1 and net 2, it can be found that net 1 and net 2 are short if the measured resistances are below a certain resistance. Test point 3 and test point 4 are on the same net, which is net 3. They are open if the measured resistance between the two test points is over a certain resistance. It means that they are not electrically connected.

Multi-testers which can measure voltage and current are commercially available. The source meter can measure the resistance directly since it has its own power supply. In terms of reliability, a high-current or low-level voltage test can be done to check the micro-open which causes the latent defects in the printed-circuit board and to check the micro-short which causes noise in the RF system.

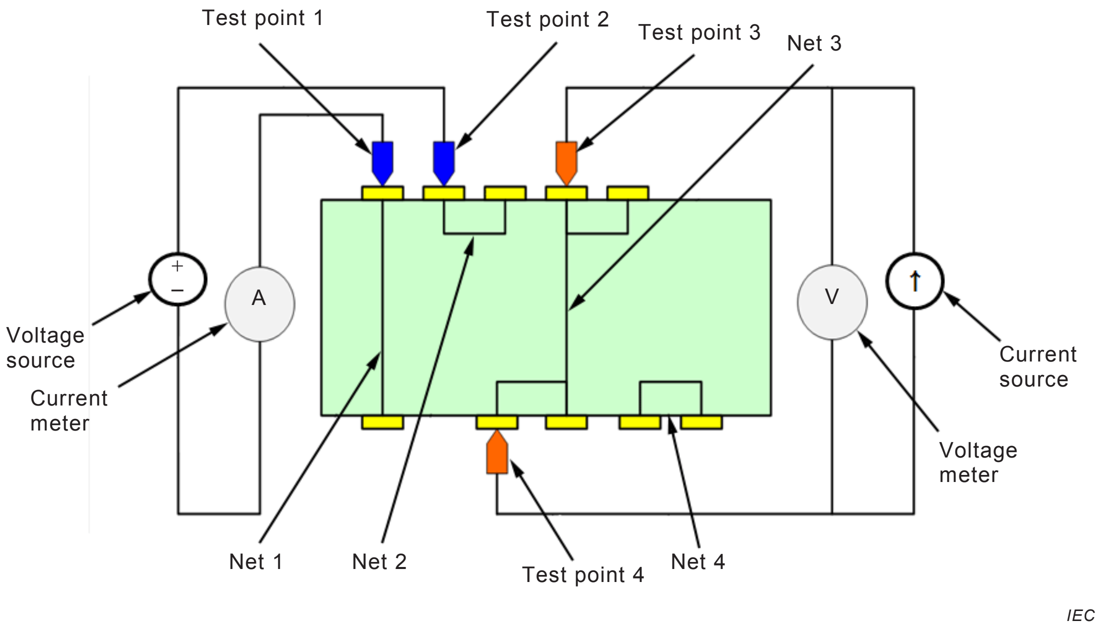


Figure 2 – Test level 1A

2.2 Test level 1B for component embedded substrate

Test level 1B is for testing electrical interconnection between wiring nets and component nets. This is shown in Figure 3. The test method of this level is the same as that of test level 1A because test level 1B is to check the isolation interconnection. Electrical interconnections are short if the measured resistance between wiring nets and component nets is below a certain resistance. It means that they are electrically connected.

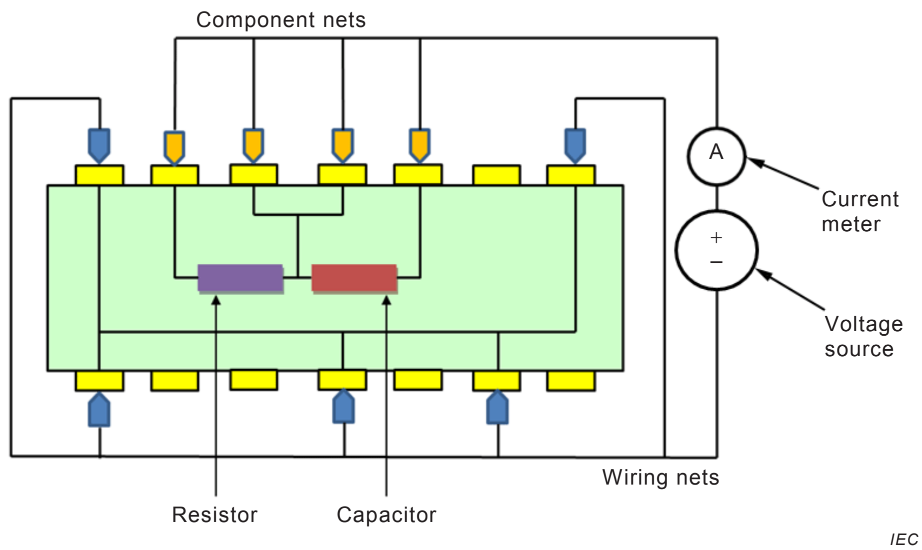
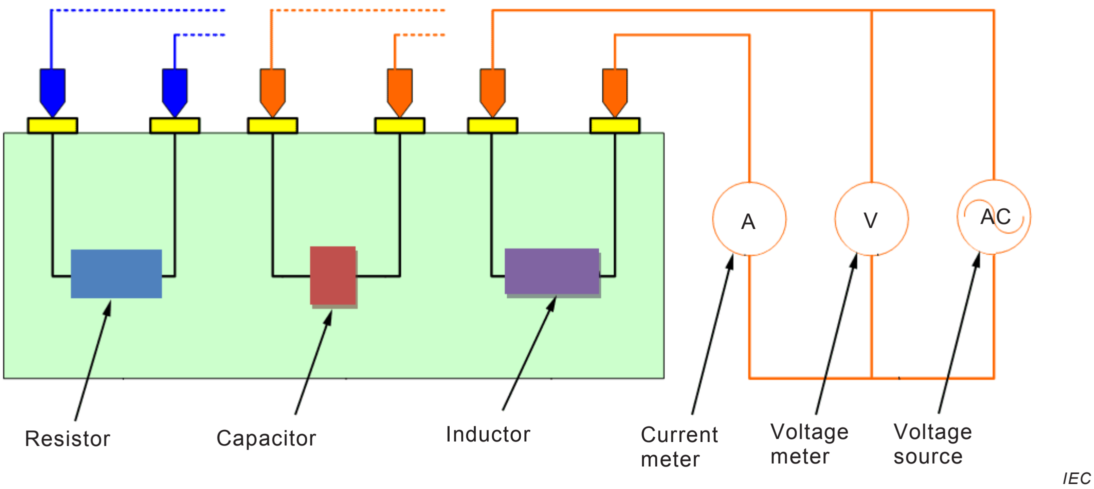


Figure 3 – Test level 1B

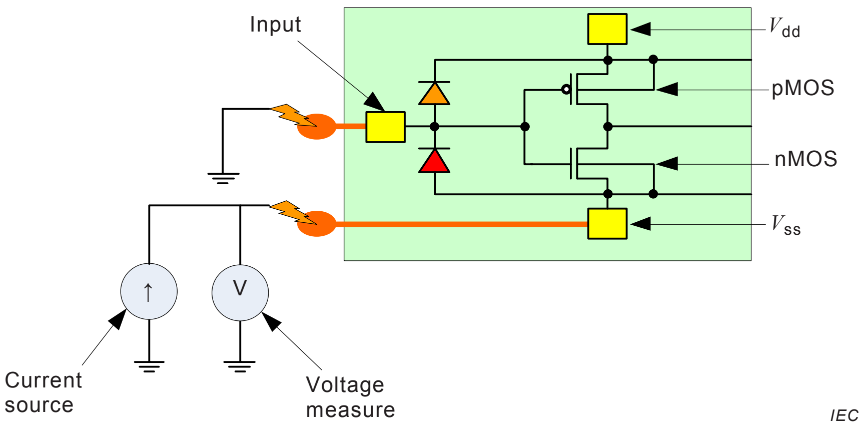
2.3 Test level 2A for component embedded substrate

Test level 2A is for testing a single component embedded substrate. Figure 4 a) shows the passive component scheme. Through this test, the electrical performance of the passive component and the continuity of the net can be measured. However, only the electrical performance test is suitable because the performance of the passive component will be affected if there is a problem with the continuity. In order to measure the performance of the passive component, the test method and the test signal need to be changed along with the type of passive component. In the case of resistors, resistance can be measured by detecting the current/voltage ratio using constant voltage and constant current as in test levels 1A and 1B. However, in the case of capacitors and inductors, capacitance and inductance need to use an AC source to get the values. LCR meters and impedance analyzers are commercially available to measure resistance, capacitance, inductance and impedance. The equipment should be selected based on the frequency range to be measured.

Figure 4 b) shows the active component circuit diagram, the method and the design of the electrostatic discharge (ESD) protection diode. Test level 2A is achieved by applying positive/negative bias to the circuit.



a) Passive component scheme



b) Active component circuit diagram and the method

Key

V_{dd}	drain voltage
V_{ss}	source voltage
pMOS	p-channel metal oxide semiconductor
nMOS	n-channel metal oxide semiconductor

Figure 4 – Test level 2A

2.4 Test level 2B for passive device embedded substrate

Test level 2B is for a simple passive structure which consists of a few passive components. These components are connected either in parallel or in series (Figure 5). This test will measure the electrical performance of the structure and the continuity of the transmission lines. For this case, only the electrical performance test is suitable because the performance of the passive components will be affected if there is a problem with the continuity, as for test level 2A. To be able to test passive components, test level 2B uses an AC source like test level 2A. However, it cannot measure the performance of individual passive components because the measured impedance will be the combination of impedances of all passive components. Moreover, tolerance values are introduced when the passive components are measured.

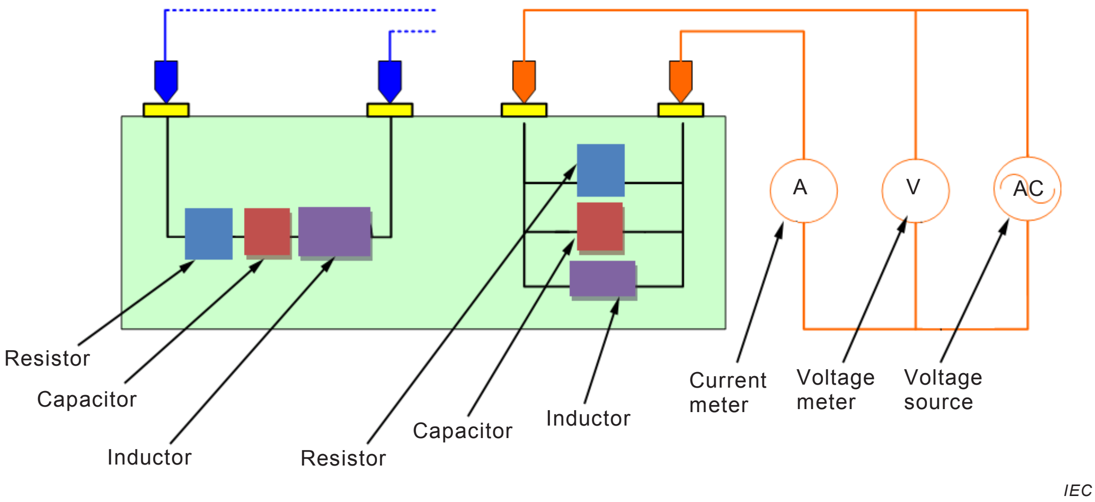
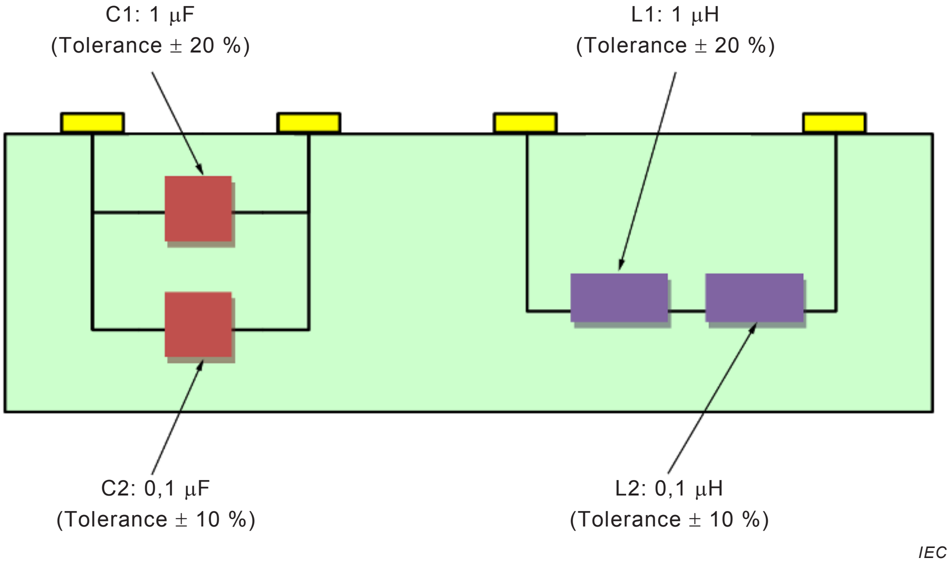
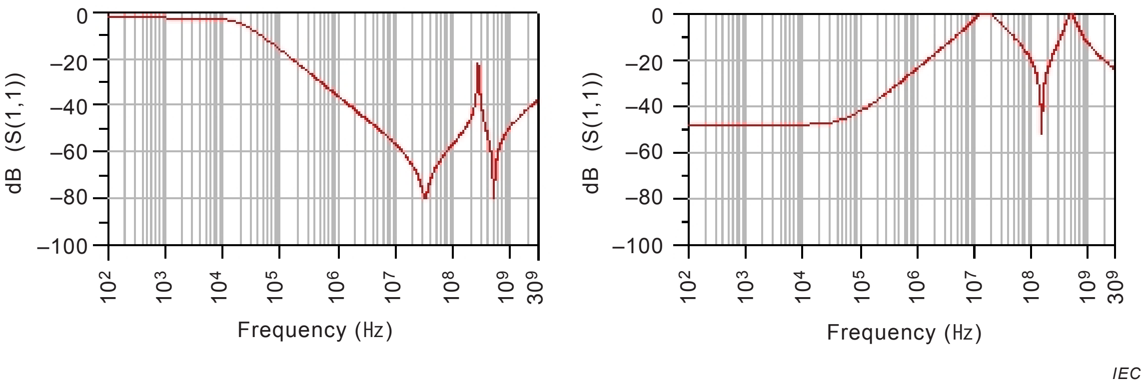


Figure 5 – Test level 2B

For example, as shown in Figure 6 a), if the capacitance of C1 is 1 μF with a tolerance of ± 20 %, the capacitance of C2 is 0,1 μF with a tolerance of ± 10 % and they are good components, then the total capacitance will be 0,89 μF ≤ (C1 + C2) ≤ 1,31 μF because of their tolerances. Thus, the passive component is good if the measured capacitance is between 0,89 μF and 1,31 μF. However, if C1 is good and C2 (< 0,09 μF) is bad, or C1 is good and C2 (> 0,11 μF) is bad, then the results are 0,8 μF ≤ (C1 + C2) ≤ 1,29 μF and (C1 + C2) > 0,91 μF, respectively. In these cases, we cannot judge if the passive components are good or bad because the results of both experiments are good even though one component is bad. However, if the frequency dependence of impedance is measured as in Figure 6 b), then the performances of each individual capacitor can be seen. Hence we can decide if C1 and/or C2 are good or bad depending on the frequency difference of resonance frequency. The inductance case between L1 and L2 of Figure 6 a) is similar to the capacitance case of Figure 6 a).



a) Parallel and series structures of passive devices with tolerances



b) Graph for frequency dependence of impedance from the structure in a)

Figure 6 – Device embedded substrate with two or more passive devices

Therefore, it is necessary to judge whether each series or parallel passive component is good or bad at more than two specific frequency points by measuring total impedance and phase difference as test level 2B. The frequency points will be selected from simulation results or calculation. For more detailed analysis, continuous changes of impedance or phase difference need to be measured along with the frequency.

There is commercially available measurement equipment such as impedance analyzer and network analyzer. If the equipment has a wider measurable frequency range, the measurement result from the equipment will be more accurate. When a very high frequency measurement is required, the equipment setting such as probe tips and transmission lines to the equipment should be changed for a very high frequency measurement. One tip for easier measurement at high frequency is to design external test pads well so as not to use a high-cost probe card for high frequency measurement but to use RF probe tips which are commercially available.

2.5 Test level 3 for device embedded substrate

Figure 7 shows the functional test method of device embedded substrate which acts like a signal filter. The passive components in the substrate are connected to each other either in parallel or in series. In case of such a structure, the test result will not be the performance of individual passive components, but the performance of the filter. Typical open/short tests are not required since the performance of the filter will be affected when the continuity of nets has a problem.

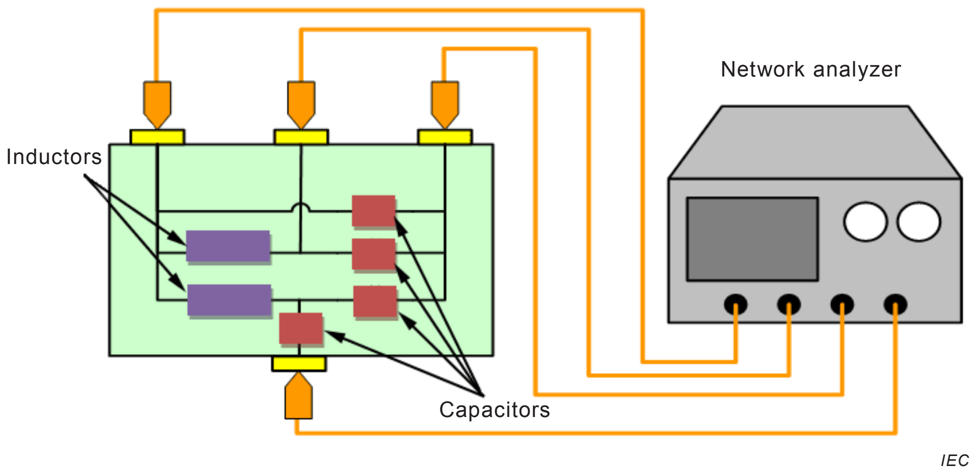
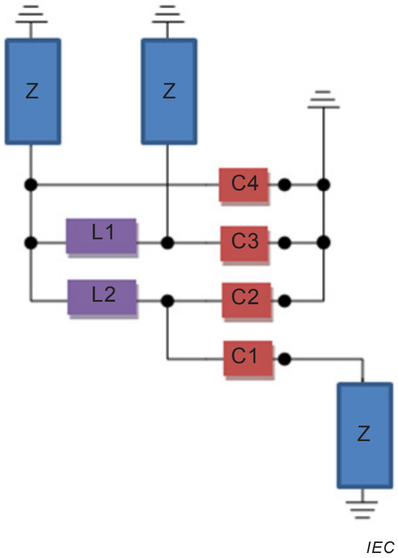
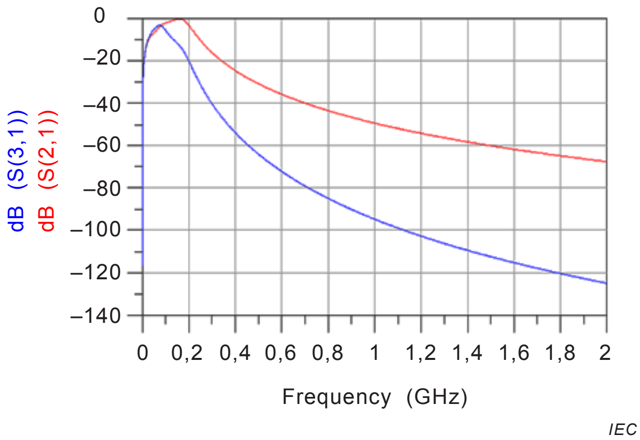


Figure 7 – Test level 3 for functional test

Test level 3 is to test the functional performance of passive device embedded substrate when the embedded passive devices function as a filter or filter banks. The scattering parameter (S-parameter) is measured to test the embedded substrate with the network analyzer, time domain reflectometry (TDR) and time domain transmission (TDT) within the specific frequency range. Each of the ports of the filter in Figure 8 will be connected to each measuring port of the network analyzer to get input and output signal distributions. The S-parameter can be measured by dividing the input voltage into the output voltage. For example, the embedded filter which consists of embedded passive components can be modelled and simulated. The circuit model of the filter is shown in Figure 8 a) and the response is shown in Figure 8 b). The simulation result becomes a basis for deciding if the filter is either good or bad. Since the filter is measured as one device, the individual passive components cannot be measured or tested. Therefore, we do not know which passive component is bad if there is a problem with the filter. Comparing the measured data to the simulation data, the specifications to pay attention to are insertion loss, bandwidth skirt properties, ripple level, rejection loss, noise level, etc.



a) Circuit model



b) Simulation result

Key

Z	50 Ω	C2	22 pF
L1	47 nH	C3	22 pF
L2	100 nH	C4	47 pF
C1	47 pF		

NOTE In case of testing device embedded substrate, all of the functional testing such as digital testing, analogue testing, mixed signal testing, RF testing, memory testing, and image sensor testing may be needed. For this test, the performance board, substrate handler for a double side probing, and automatic test equipment are prepared.

Figure 8 – Circuit model and simulation result

3 Electrical test procedure for device embedded substrate

A test design review is important to decide how to test device embedded substrate and how to define test specifications. In order to decide test specifications, active device information is especially required. This is the main reason that the test method of device embedded substrate has not been standardized. For the standardization test for device embedded substrate, the test specification of the embedded active device may be required for evaluating the embedded active device.

In order to set up the test for device embedded substrate, information such as the design and the structure of device embedded substrate and embedded passive component specifications is required. Also, information on test pattern and performance measurement should be gathered to test embedded devices before the actual test. It will affect the final yield on device embedded substrate and will be the important indicator when test specifications are defined. Figure 9 and Figure 10 show the test design review and the preparation flow for the test setup.

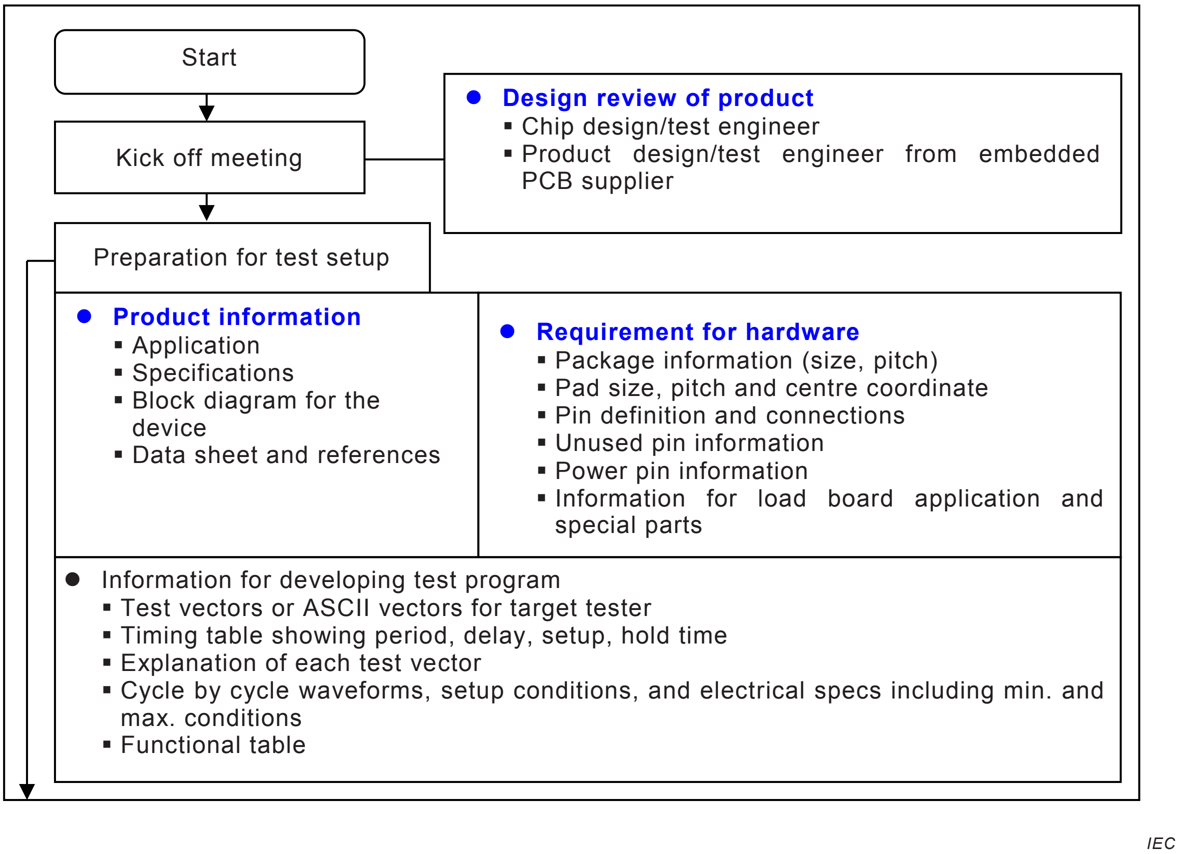


Figure 9 – Preparation for the test setup

The first thing to do, after finishing the test design review and the preparation for the test setup, is to make a test plan. The plan includes a test circuit and test interface such as test socket and test board. After that, a test interface will be made with the selected test circuit. Meanwhile, the test program will be written so that the whole pilot test can be done by using the test program after making the test interface.

Using the test result, the original test design will be verified. If there is a problem with the test design, the test should be redesigned. Or, the program needs to be debugged if the test program causes any problems. If the test passes, the specifications of device embedded substrate need to be registered after the final test and the design review. Afterwards, the manufacturing test on device embedded substrate can be applied with the registered specifications.

NOTE A total plan is developed for the final test design and any debugging that needs to take place. It would be relatively difficult to get to the final functional test of an electronic assembly and find that a portion of the circuit is inoperable without access to those features in order to determine whether it is an internal function that is not working, a circuit conductor that has broken, or a component on the outer layers that needs to be replaced.

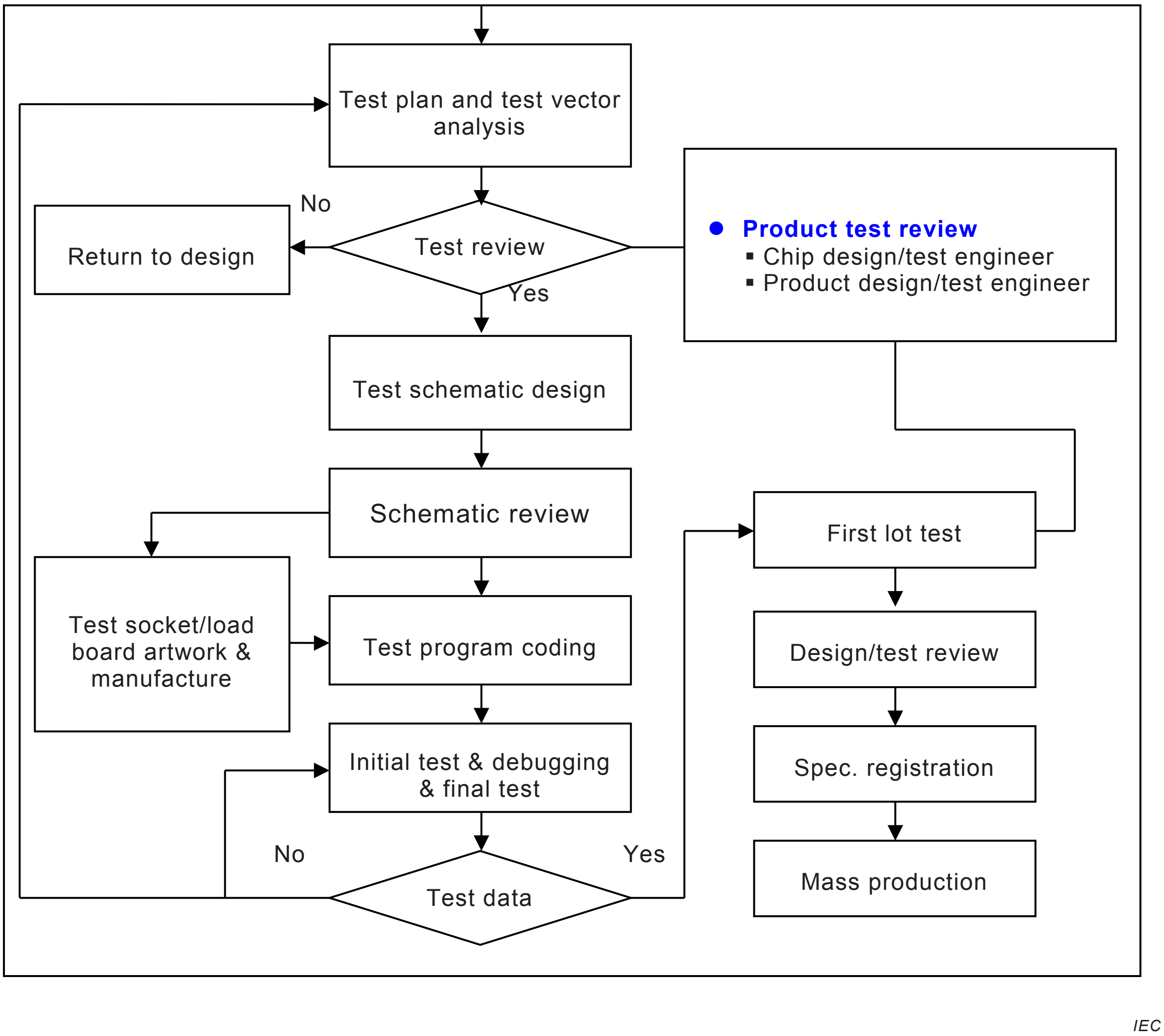


Figure 10 – Test procedure flow

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