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EMC IC modelling

Part 2-1: Theory of black box modelling
for conducted emission

National foreword

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Part 2-1: Theory of black box modelling for conducted emission

Modèles de circuits intégrés CEM –
Partie 2-1: Théorie du modèle de la boîte noire pour les émissions conduites

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CONTENTS

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EMC IC MODELLING –

Part 2-1: Theory of black box modelling for conducted emission

FOREWORD

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IEC 62433-2-1, which is a technical report, has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
47A/826A/DTR	47A/834/RVC

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of IEC 62433 series, under the general title *EMC IC modelling*, can be found on the IEC website.

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EMC IC MODELLING –

Part 2-1: Theory of black box modelling for conducted emission

1 Scope

This part of IEC 62433-2-1 covers black box modelling which has the potential to make the modelling of conducted emission very simple, very fast, and can provide complete protection of proprietary information of IC vendors.

This technical report is intended to provide the theoretical background on black box modelling for IC conducted emission.

2 Integrated circuit and modelling board

Figure 1 shows an integrated circuit (IC) and a modelling board. The IC is equipped with power/ ground pins, output pins and input pins. Usually an IC requires different power supply connections, namely, to supply digital cores, I/Os, and analogue circuits. Each one of these power supplies may have plural pins.

An IC cannot be activated by itself. To activate the IC properly, the IC has to be provided with power supplies, a set of input signals or an input signal vector, and appropriate loads for output pins.

To achieve these requirements, the modelling board is used. The modelling board provides minimum requirements for the activation. It supplies power, and input signals to the IC, and it gives typical loads for the output pins. In addition, power/ ground pins of the same category are connected to each other in the modelling board resulting in one terminal for each category of the power/ ground supply at the interface of the modelling board.

The board is also used for parameter extractions for modelling the IC. The IC modelling includes the board. The relationship between the IC modelling and the modelling board is just like the relationship between measured data and measurement board that affects measurement data. Therefore the modelling board should be as simple and general as possible.

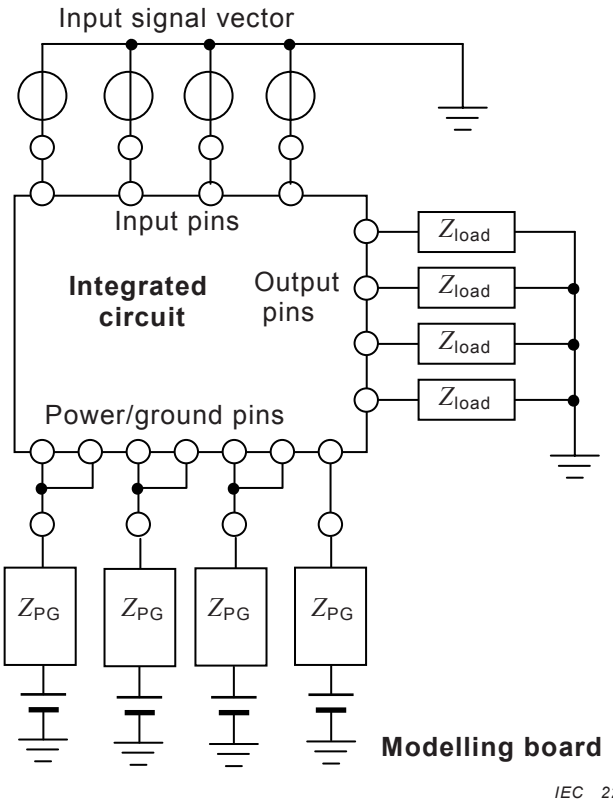

Figure 1a) – Entire structure

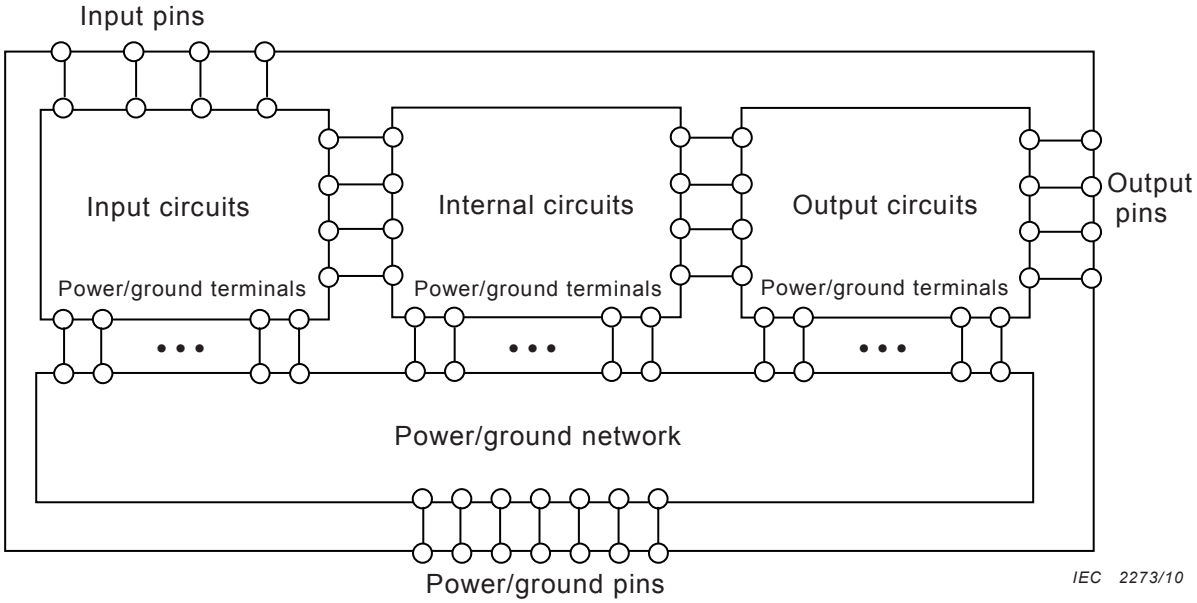

Figure 1b) – Structure of the IC part

Figure 1 – Integrated circuit and its modelling board

3 Assumptions

3.1 ICEM-CE

ICEM-CE is a macro model that approximates conducted emission behaviour of an IC using two types of components, internal activity (IA) and passive distribution network (PDN) as shown in Figure 2. These two types of components are connected through internal terminals (ITs).

The IAs represent noise sources that originate in switching of active devices within the IC. The PDN represents noise propagation characteristics from the internal terminals to the external terminals (ETs).

The black box modelling is based on this ICEM-CE model structure.

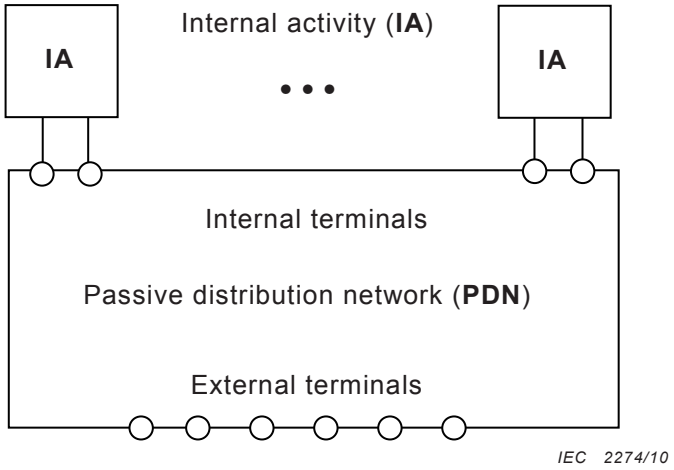

Figure 2 – Basic ICEM-CE model structure for an IC

Figure 3 shows how to make an ICEM-CE model for the example of an IC and its modelling board shown in Figure 1. Figure 3a) shows the assignment of IA and PDN. The IA part includes input vector generators and output loads on the modelling board. The PDN part consists of the IC PDN part and Board PDN part. The IC PDN part consists of the power/ ground network of the die and the package of the IC. Figure 3b) shows the ICEM-CE structure of the IC and its modeling board with IAs and PDNs.

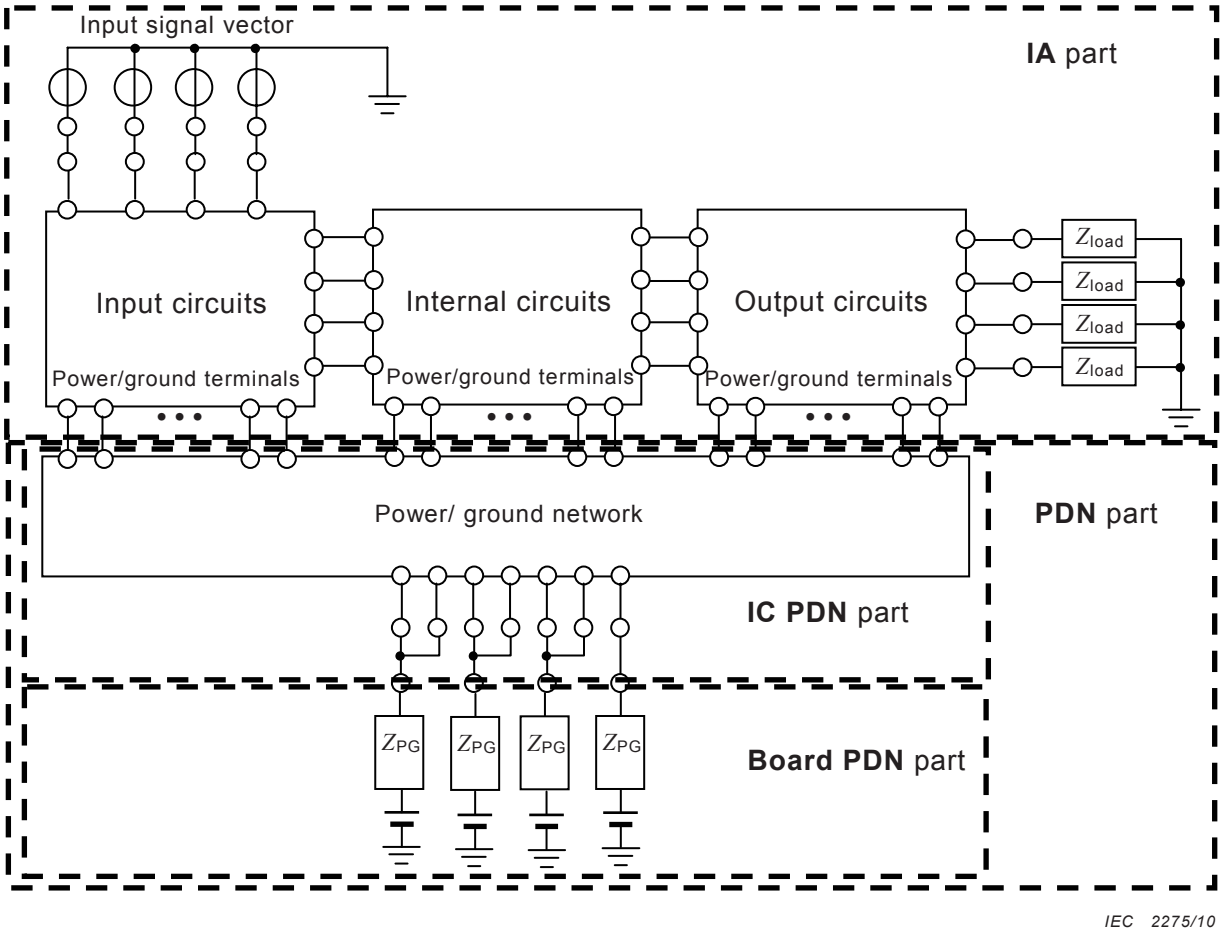

Figure 3a) – IA and PDN assignment

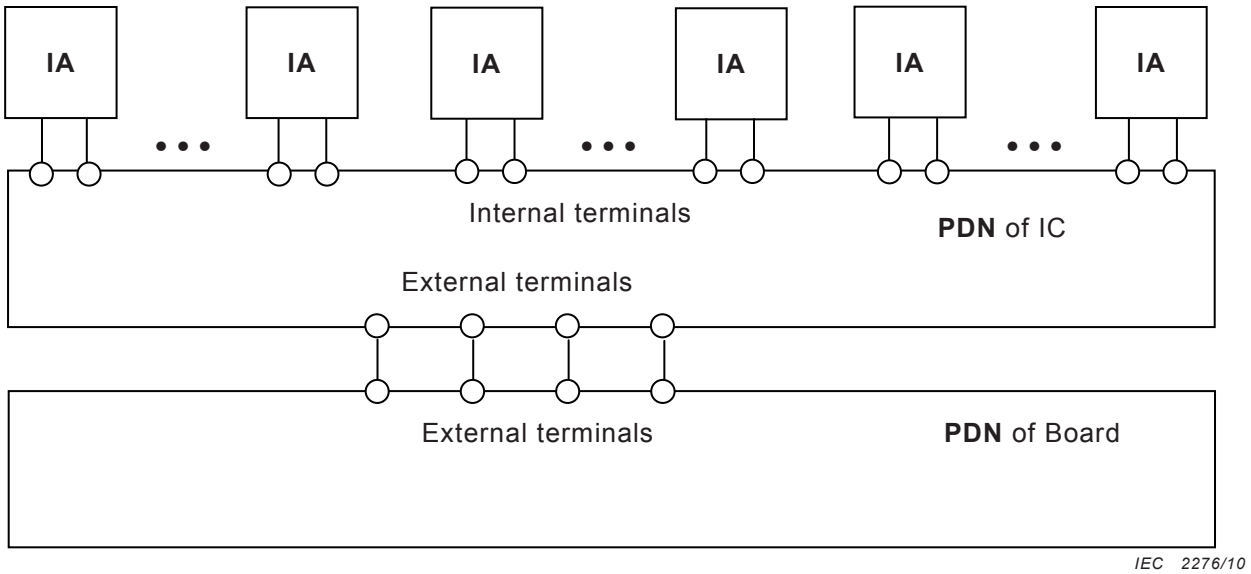

Figure 3b) – ICEM-CE representation

Figure 3 – Representation of the integrated circuit and its modelling board by ICEM-CE

3.2 Black box model

In black box modelling, the PDN is described using a numerical matrix. To represent the PDN using a matrix, the PDN is assumed to be a linear circuit. Although the PDN is usually non-linear, this assumption is generally valid because noise voltages are small enough.

The elements of the matrix depend on noise frequency. Therefore, the PDN and the IAs should be described in frequency domain, and the PDN and IAs should be given for each frequency concerned.

The PDN can be represented either by an impedance matrix or an admittance matrix. This technical report uses an admittance matrix because admittance is more convenient than impedance to combine other models to the black box model.

4 Modelling

4.1 Terminals and objectives

As shown in Figure 1 and Figure 3, an input signal vector is applied to the IC through input terminals. The signal vector activates the IC and it causes IAs inside the IC. Therefore, the voltages and currents of the input terminals are conditions for the modelling. Noise voltages and currents at the input terminals are not the objectives of the modelling.

For the output pins of the IC, the modelling board provides typical loads. These loads generate IAs at the output circuits of the IC and consequently, from the IAs noise voltages and noise currents appear at the power/ ground terminals. This effect is included into the black box modelling. Output terminals themselves are also a source of conducted emissions, but the black box modelling given in this technical report cannot handle these emissions, because the characteristics of output circuits are non-linear. To simulate conducted emissions through output terminals, other black box modelling such as IMIC or IBIS has to be combined with this black box modelling.

Users cannot manipulate the internal terminals shown in Figure 2 that connect the IAs to the PDN. Therefore, the noise voltages and noise currents of internal terminals are also not the objectives of the black box modelling. But for the first step of this study, these terminals have to be used for the modelling, because these terminals provide the noise sources to the PDN. They are necessary particularly when a model is built from design data.

As the result, the objectives of the black box modelling are to provide models that can be used for numerical calculation of conducted emissions through power and ground terminals of an IC, which is applicable for an application board.

The ICEM-CE model structure for the black box modelling is shown in Figure 4. The IAs are expressed by current sources, and the PDN is given as an admittance matrix.

The noise voltages of the power/ ground terminals are defined with reference to a reference ground terminal (ET0) that is directly connected to the reference plane of the modelling board. The other power/ ground terminals of the PDN are named as ETx. The value of n is the number of power/ ground terminals minus one. The number of IAs is m. Therefore there are $2 \cdot m$ internal terminals, and these terminals are named as ITx as shown in Figure 4.

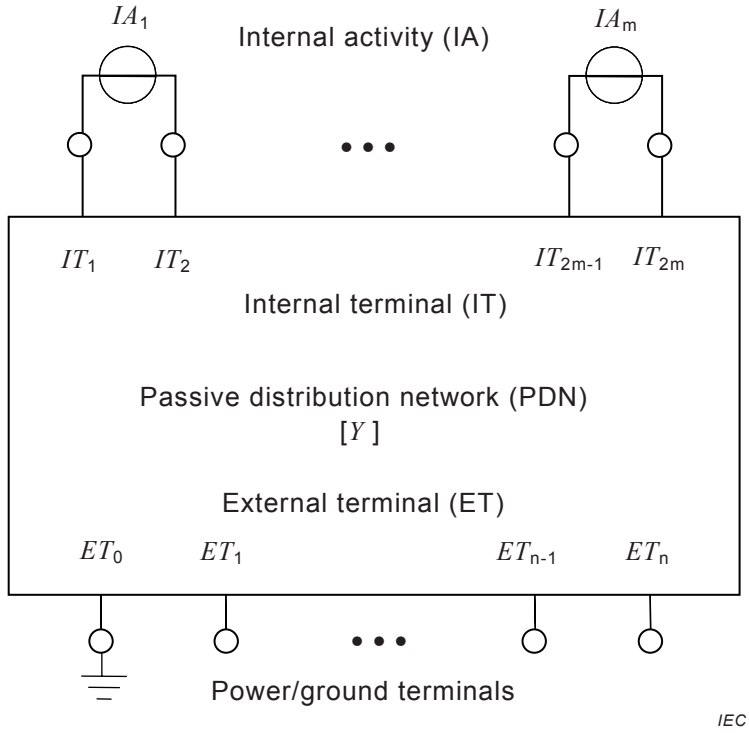

Figure 4 – Structure of the ICEM-CE for IC black box modelling

4.2 Admittance matrix

The PDN in Figure 4 is assumed to be a linear circuit. Therefore, the PDN can be expressed using an admittance matrix based on the nodal analysis method. The equation that expresses the IC, shown as Figure 4, is given below.

$$\left[\begin{array}{ccc|ccc} Y_{ET1\ ET1} & \cdot & Y_{ET1\ ETn} & Y_{ET1\ IT1} & \cdot & Y_{ET1\ IT2m} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ Y_{ETn\ ET1} & \cdot & Y_{ETn\ ETn} & Y_{ETn\ IT1} & \cdot & Y_{ETn\ IT2m} \\ \hline Y_{IT1\ ET1} & \cdot & Y_{IT1\ ETn} & Y_{IT1\ IT1} & \cdot & Y_{IT1\ IT2m} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ Y_{IT2m\ ET1} & \cdot & Y_{IT2m\ ETn} & Y_{IT2m\ IT1} & \cdot & Y_{IT2m\ IT2m} \end{array}\right] \times \left[\begin{array}{c} V_{ET1} \\ \cdot \\ V_{ETn} \\ \hline V_{IT1} \\ \cdot \\ \cdot \\ \cdot \\ V_{IT2m} \end{array}\right] = \left[\begin{array}{c} I_{ET1} \\ \cdot \\ I_{ETn} \\ \hline I_{IT1} \\ I_{IT2} \\ \cdot \\ \cdot \\ I_{IT2m-1} \\ I_{IT2m} \end{array}\right] \quad (1)$$

Here, V_{ETx} and I_{ETx} are the noise voltage and the noise current of ETx, respectively. V_{ITx} and I_{ITx} represent the noise voltage and the noise current of ITx, respectively.

NOTE Equation 1 describes the PDN without using variables of voltages and currents for internal nodes, which connect passive elements making up the PDN. Annex A gives the proof of the equation.

The admittance matrix is regular and its dimension is (n+2m, n+2m). For simplicity, Equation (1) is represented using sub-matrices and vectors as follows. In this equation, IAs substitute the currents of the internal terminals.

$$\left[\begin{array}{cc} [Y_{ET\,ET}] & [Y_{ET\,IT}] \\ [Y_{IT\,ET}] & [Y_{IT\,IT}] \end{array}\right] \times \left[\begin{array}{c} [V_{ET}] \\ [V_{IT}] \end{array}\right] = \left[\begin{array}{c} [I_{ET}] \\ [I_{IT}] \end{array}\right] \quad (2)$$

where,

$[Y_{ET\,ET}]$ is the regular admittance sub-matrix that represents interactions between ETs;

$[Y_{ET\,IT}]$ is the admittance sub-matrix that represents interactions between ETs and ITs;

$[Y_{IT\,ET}]$ is the admittance sub-matrix that represents interactions between ITs and ETs;

$[Y_{IT\,IT}]$ is the regular admittance sub-matrix that represents interactions between ITs;

$[V_{ET}]$ is the voltage vector that represents noise voltages of ETs;

$[V_{IT}]$ is the voltage vector that represents noise voltages of ITs;

$[I_{ET}]$ is the current vector that represents noise currents of ETs; and

$[I_{IT}]$ is the current vector that represents noise currents of ITs.

$[I_{IT}]$ is given as follows.

$$[I_{IT}] = [IA] \equiv \begin{bmatrix} IA_1 \\ -IA_1 \\ \cdot \\ \cdot \\ IA_m \\ -IA_m \end{bmatrix} \tag{3}$$

4.3 Matrix compaction

$[V_{IT}]$ is eliminated out from Equation (2), as follows.

Equation (2) can be expanded into following two equations, combining Equation (3).

$$[Y_{ET\,ET}] \times [V_{ET}] + [Y_{ET\,IT}] \times [V_{IT}] = [I_{ET}] \tag{4}$$

$$[Y_{IT\,ET}] \times [V_{ET}] + [Y_{IT\,IT}] \times [V_{IT}] = [IA] \tag{5}$$

From Equation (5), $[V_{IT}]$ is obtained as follows.

$$[V_{IT}] = [Y_{IT\,IT}]^{-1} \times ([IA] - [Y_{IT\,ET}] \times [V_{ET}]) \tag{6}$$

By substituting Equation (6) by Equation (4), $[V_{IT}]$ can be eliminated out from Equation (4).

$$\left([Y_{ET\,ET}] - [Y_{ET\,IT}] \times [Y_{IT\,IT}]^{-1} \times [Y_{IT\,ET}]\right) \times [V_{ET}] = [I_{ET}] - [Y_{ET\,IT}] \times [Y_{IT\,IT}]^{-1} \times [IA] \tag{7}$$

The coefficient of $[V_{ET}]$ in the left-hand side is an admittance matrix whose dimension is (n, n). And the second term of the right-hand side is a current vector with n-dimension. The dimension of $[IA']$ is n, and the dimension of $[Y'_{ET\,ET}]$ is (n, n). Therefore, $[IA']$ and $[Y'_{ET\,ET}]$ can be defined as follows.

$$[IA'] \equiv -[Y_{ET\,IT}] \times [Y_{IT\,IT}]^{-1} \times [IA] \tag{8}$$

$$[Y'_{ET\,ET}] \equiv [Y_{ET\,ET}] - [Y_{ET\,IT}] \times [Y_{IT\,IT}]^{-1} \times [Y_{IT\,ET}] \tag{9}$$

Then, Equation (7) becomes very simple.

$$[Y'_{ET\,ET}]\times[V_{ET}]=[I_{ET}]+[IA'] \tag{10}$$

4.4 Black box model structure

In Equations (8) and (9), $[IA']$ and $[Y'_{ET\,ET}]$ are constant. Therefore $[IA']$ and $[Y'_{ET\,ET}]$ are named as "equivalent internal activities (equivalent IAs)" and "equivalent passive distribution network (equivalent PDN)", respectively.

Equation (10) means that the black box model structure consists of an equivalent PDN and equivalent IAs as illustrated in the dotted area of Figure 5.

Compared with Figure 4, the IAs at the internal terminals are modified and transferred to the parallel positions to the external terminals. And the PDN is modified and simplified.

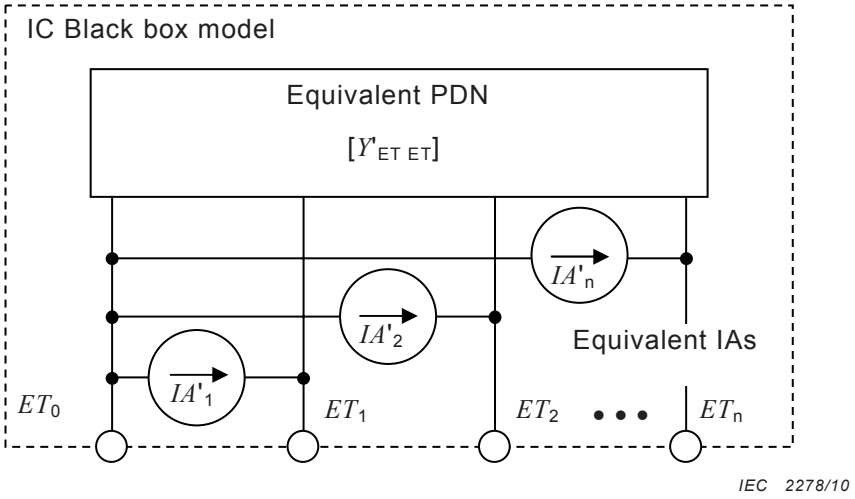

Figure 5 – IC Black box model structure

The IC black box model structure, as shown in Figure 5, is modelled using the expression having the (n+1) external terminals including the reference, where the number of the independent terminal voltage is n. Equation (10) is the Y matrix expression that determines the n external terminal voltages except for the reference as independent variables, and it is the n port circuit which has the reference terminal as the common negative terminal and the other terminals as the positive terminals. A n port circuit of black box model is expressed with circuit elements as shown in Figure 6. It consists of the parallel connection of passive elements having the admittance of the diagonal elements of the Y matrix, voltage controlled current sources having the current of the product of the non-diagonal element value and the other port voltage, and the independent current source having the current calculated from Equation (8).

The Y matrix expression of Equation (10) can be converted into an expression using Z or S matrices easily using conversion formulas.

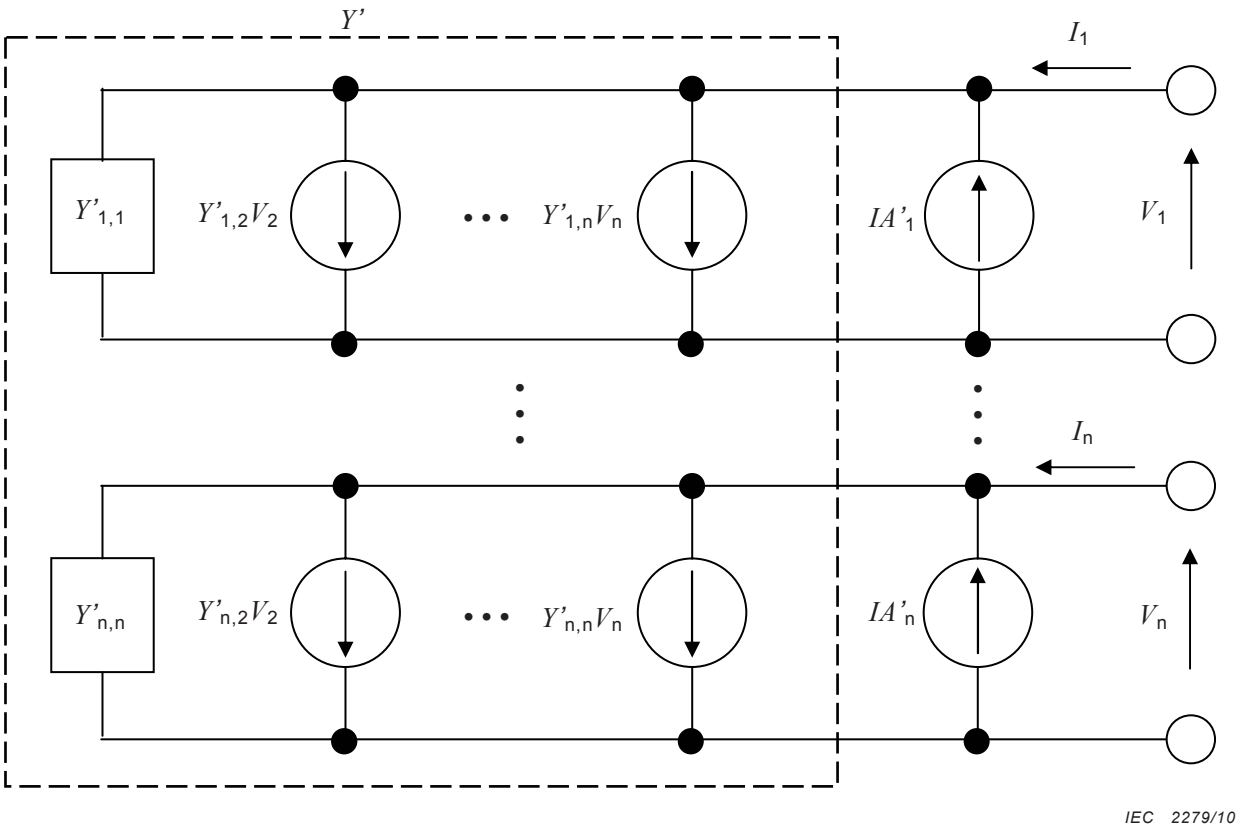

Figure 6 – IC black box model description with circuit elements

5 Parameter extractions

5.1 General

The black box model for conducted emission consists of two components, the equivalent IAs and the equivalent PDN. To build a black box model from measurements, elements of these two components should be obtained. This clause describes the methods used to obtain these components from measurements.

The equivalent IAs depend on the operational mode and power supply condition of the IC. Therefore, the typical power supply condition and the repetitive specific input signal vector that corresponds to the operational mode should be applied to the power/ ground terminals and the input terminals of the modelling board during the measurements of equivalent IAs, respectively.

The equivalent PDN is assumed as a linear function, but it actually depends on voltages. Therefore, the typical power supply is given to the power/ground terminals of the modelling board during the measurements. Relatively small signals should be used for the measurements to assure the assumption is valid.

5.2 Equivalent internal activities

From Equation (10), the equivalent noise current sources can be,

$$[IA'] = -[I_{ET}], \text{ when } [V_{ET}] = [0] \quad (11)$$

This means that the equivalent IAs can be obtained by measuring the $[I_{ET}]$ under the condition that all the external terminals are RF shorted to the reference terminal. The configuration of the measurement setup is shown in Figure 7.

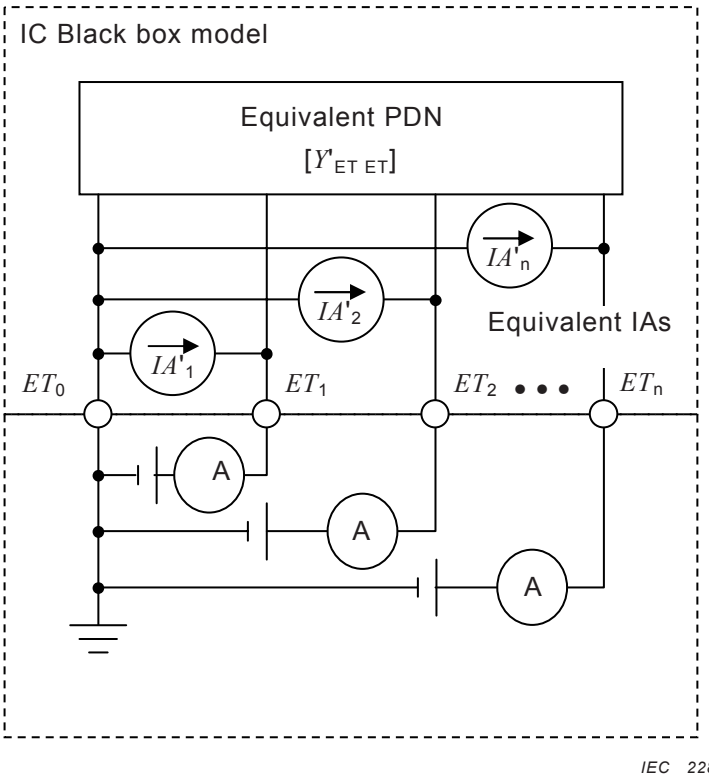

Figure 7 – Setup for extraction of equivalent IAs

Each value of $[I_{ET}]$ is a complex number; therefore, the amplitude and phase for each current element should be measured.

One way is to measure the amplitude and phase in frequency domain directly for each external terminal for each frequency concerned. In this method, the phases should be determined with reference to the cycle of the input signal vector. The definition is given in Figure 8.

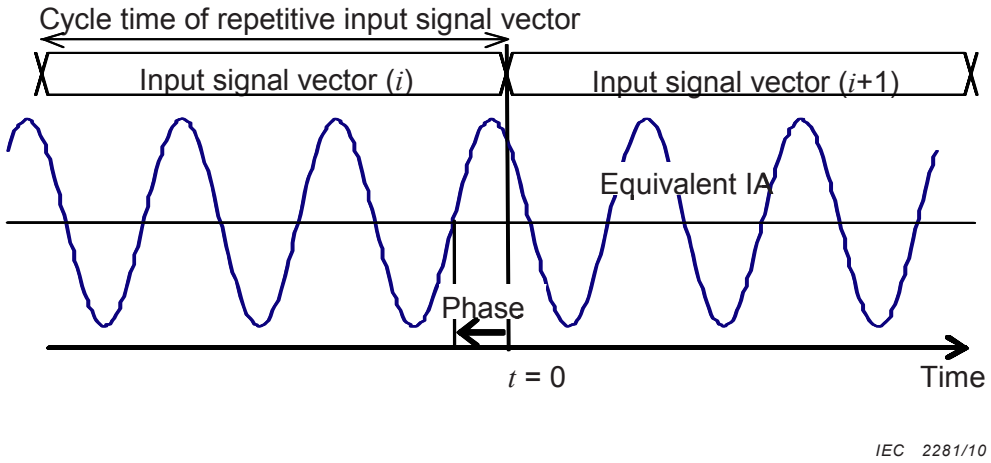

Figure 8 – Definition of phase

The other way is to measure the waveforms of the external terminals in the time domain. The time is also determined with reference to the start of the cycle of the input signal vector. After that, the waveforms should be converted into frequency domain using the Fourier transformation.

5.3 Equivalent passive distribution network

Now all elements of the equivalent IAs are already known. Therefore each element of the admittance matrix of equivalent PDN can be derived from Equation (10) as shown in Equation (12).

$$Y'_{ij} = \frac{I_i + IA'_i}{V_j}, \text{ at all } V_{i \neq j} = 0 \qquad (12)$$

Here, I_i is the measured current while V_j is the given signal voltage for the measurement. The configuration of the measurement setup for Y'_{ij} is shown in Figure 9. In this measurement, the phase of V_j and I_i should be given with reference to the cycle of the input vector, because the input signal vector determines the phase of IA.

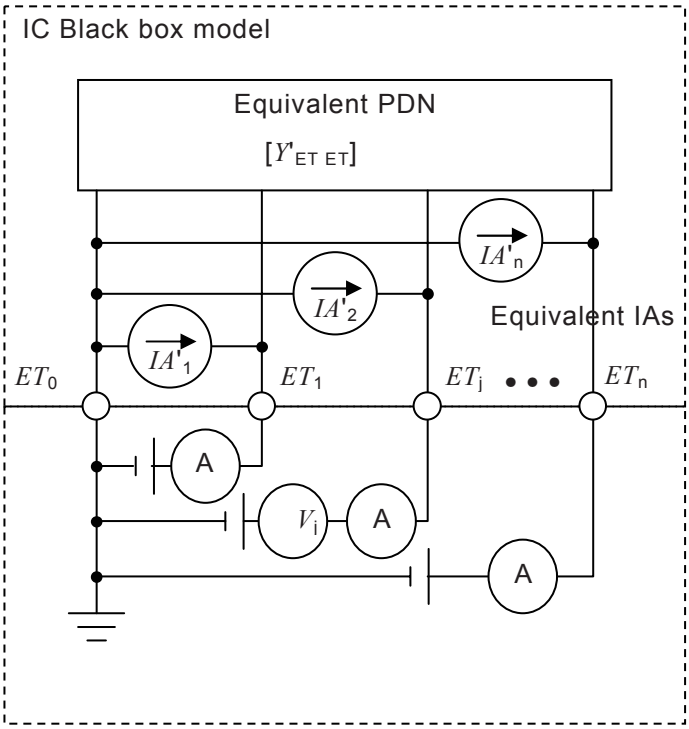

Figure 9 – Setup for extraction of equivalent PDN

5.4 Parameter extraction method using finite impedance termination

The parameter extraction method explained above is the one by using RF short termination for each external port. In reality a complete RF short is difficult for some cases, in particular for measurements of the real devices. Thus a parameter extraction method using finite impedance termination is described herein.

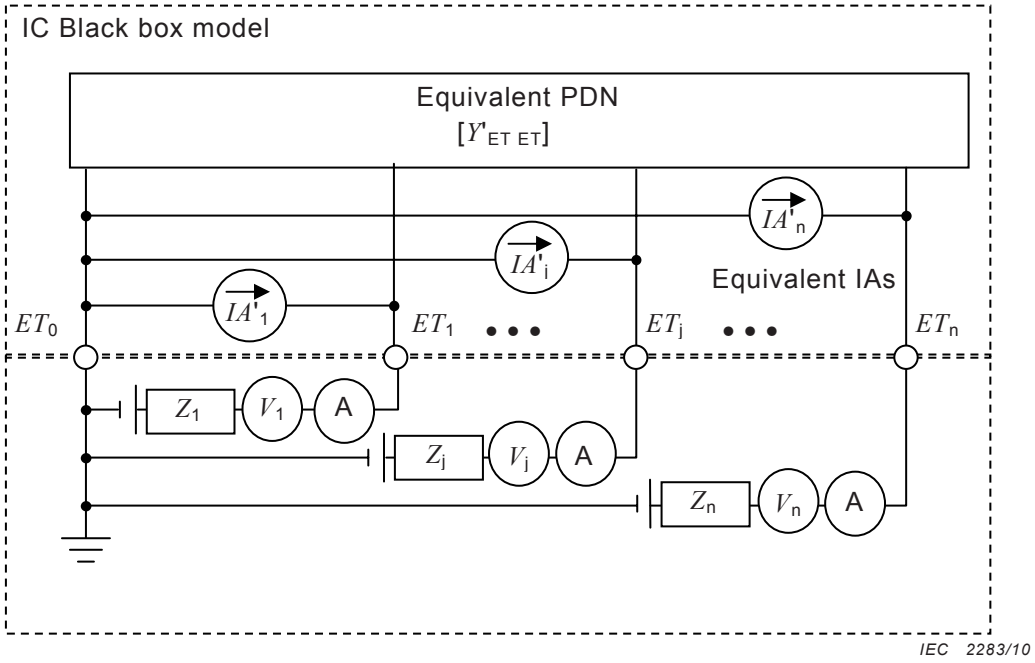

Figure 10 – Setup for extraction of equivalent IAs and PDN

Figure 10 shows the setup structure of limited impedance termination. Each terminal is terminated with a series of a DC power supply, an AC voltage source, a current meter, and a finite impedance element. The circuit of Figure 10 can be expressed using n independent equations. The number of elements of Y' is n^2 and that of the IA' is n. Then the number of unknowns is n(n+1). Then n(n+1) equations are necessary to get all element values of Y' and IA'. As the circuit of Figure 10 has n independent equations for each excitation, it needs (n+1) independent sets of external AC voltage sources to determine the all unknown values.

For Figure 10, its terminal condition is expressed as below.

$$[V_{ET}] = [Z_{PSPS}] \times [I_{ET}] + [V] \tag{13}$$

$$[I_{ET}] = [Z_{PSPS}]^{-1} \times [[V_{ET}] - [V]] = [Y_{PSPS}] \times [[V_{ET}] - [V]] \tag{14}$$

The combination of Equations (10) and (13), or Equations (10) and (14), give the following equations.

$$[Y'_{ETET}] \times [[Z_{PSPS}] \times [I_{ET}] + [V]] = [I_{ET}] + [IA'] \tag{15}$$

$$[Y'_{ETET}] \times [V_{ET}] = [[Y_{PSPS}] \times [[V_{ET}] - [V]]] + [IA'] \tag{16}$$

By using Equation (15), the combination according to (n+1) of input $[V]$ and its response $[I_{ET}]$ leads $[Y'_{ETET}]$ and $[IA']$. And by using Equation (16), the combination according to (n+1) of input $[V]$ and its response $[V_{ET}]$ leads $[Y'_{ETET}]$ and $[IA']$.

To do this for example, we can input one AC voltage source at one external terminal while setting all other AC sources to zero, and repeat this for each external terminal. There will also be one case where all AC sources are zero. When we solve the equations from real measurement data, we can add the other drive patterns (the drive from plural ports) because with measurement error, it is useful to use the least-squares method to optimize the parameters.

5.5 Black box model including the reference terminal

The reference terminal is not included in $[IA']$ and $[Y']$ described above. When we implement ICs on a board, expanding $[IA']$ and $[Y']$ so that they include the reference terminal is convenient because generally the reference terminal is necessary when an IC is placed on a board like the other terminals. As shown in detail in Annex A, IA' element of the reference terminal is calculated from the summation of IA' elements with the reference terminal set as zero. The Y' element of the reference terminal is calculated from the summation of Y' elements where the reference terminal along a row or a column is zero.

6 Implementation

6.1 General

This clause describes the methodology for implementation of the black box models into an application board, taking as an example an application board with two black box models. An example is given in Annex B.

6.2 Configuration of the application board

The configuration of the application board is shown in Figure 11. The board contains two ICs, IC-A and IC-B, and these are connected to the application board using the terminal group A and the terminal group B, respectively.

The board is also equipped with the terminal group C. The application board receives power supplies and ground from the outside environment using these terminals.

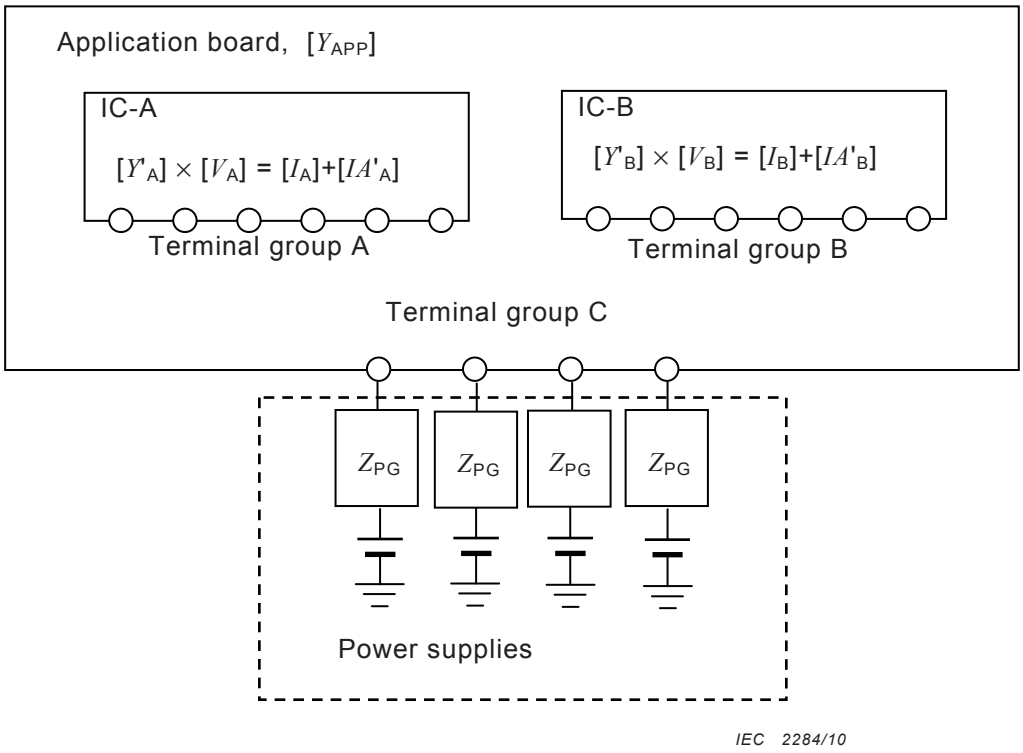

Figure 11 – Configuration of the application board

The components for simulation of the application board consist of IC-A black box model, IC-B black box model, PDN model of the power/ ground network of the application board, and models of the power supplies. The connection of the components for simulation is shown in Figure 12.

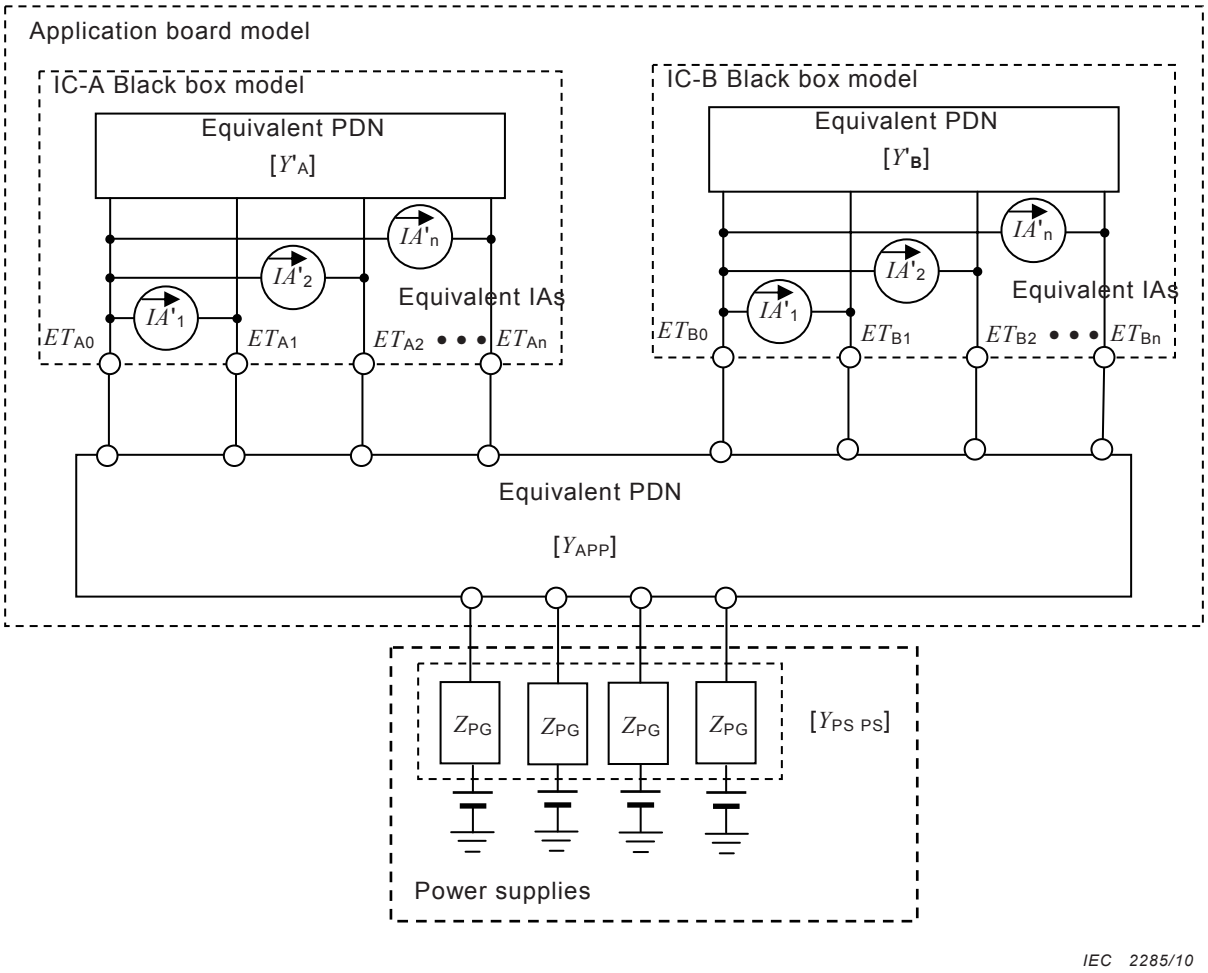

Figure 12 – Setup for simulation of the application board

Let's suppose that the black box models for IC-A and IC-B, and the admittance matrix of the application board are already known as follows. Each IC model used here is the black box model including its reference terminal.

$$[Y'_{\mathrm{A}}]\times[V_{\mathrm{A}}]=[I_{\mathrm{A}}]+[IA'_{\mathrm{A}}] \tag{17}$$

$$[Y'_{\mathrm{B}}]\times[V_{\mathrm{B}}]=[I_{\mathrm{B}}]+[IA'_{\mathrm{B}}] \tag{18}$$

Here, $[V_{\mathrm{A}}]$, $[V_{\mathrm{B}}]$ and $[V_{\mathrm{C}}]$ are the noise voltage vectors of terminal group A, B and C, respectively. $-[I_{\mathrm{A}}]$, $-[I_{\mathrm{B}}]$ and $[I_{\mathrm{C}}]$ are the noise current vectors of terminal group A, B and C, respectively.

And the admittance matrix of the application board is given as follows.

$$[Y_{\mathrm{APP}}]=\begin{bmatrix}[Y_{\mathrm{AA}}] & [Y_{\mathrm{AB}}] & [Y_{\mathrm{AC}}]\\ [Y_{\mathrm{BA}}] & [Y_{\mathrm{BB}}] & [Y_{\mathrm{BC}}]\\ [Y_{\mathrm{CA}}] & [Y_{\mathrm{CB}}] & [Y_{\mathrm{CC}}]\end{bmatrix} \tag{19}$$

In Equation (19), the sub-matrix $[Y_{\mathrm{AB}}]$ represents the interactions between terminal A and terminal B, the sub-matrix $[Y_{\mathrm{AC}}]$ represents interactions between terminal A and terminal C, etc.

6.3 Implementation of black box models

The whole application board can be expressed by Equation (20) as shown below.

$$\begin{bmatrix} [Y_{AA}] & [Y_{AB}] & [Y_{AC}] \\ [Y_{BA}] & [Y_{BB}] & [Y_{BC}] \\ [Y_{CA}] & [Y_{CB}] & [Y_{CC}] \end{bmatrix} \times \begin{bmatrix} [V_A] \\ [V_B] \\ [V_C] \end{bmatrix} = \begin{bmatrix} -[I_A] \\ -[I_B] \\ [I_C] \end{bmatrix} \tag{20}$$

The currents of terminal group A and B have negative signs, since the noise currents to the IC models and the noise currents to the application board are opposite.

$[I_A]$ and $[I_B]$ in Equation (20) can be eliminated out by substituting these using Equation (17) and (18). As the result, the following equation that represents the whole system is obtained.

$$\begin{bmatrix} [Y_{AA}]+[Y'_A] & [Y_{AB}] & [Y_{AC}] \\ [Y_{BA}] & [Y_{BB}]+[Y'_B] & [Y_{BC}] \\ [Y_{CA}] & [Y_{CB}] & [Y_{CC}] \end{bmatrix} \times \begin{bmatrix} [V_A] \\ [V_B] \\ [V_C] \end{bmatrix} = \begin{bmatrix} [IA'_A] \\ [IA'_B] \\ [I_C] \end{bmatrix} \tag{21}$$

6.4 Solutions to noise voltages and noise currents

Initially, one supposes that as a general boundary condition of the system, an admittance matrix of power supplies $[Y_{PSPS}]$ is given. The relationship between $[V_C]$ and $[I_C]$ is given by the following equation.

$$[Y_{PSPS}] \times [V_C] = -[I_C] \tag{22}$$

Equation (21) becomes Equation (23) by substituting $[I_C]$ using Equation (22).

$$\begin{bmatrix} [Y_{AA}]+[Y'_A] & [Y_{AB}] & [Y_{AC}] \\ [Y_{BA}] & [Y_{BB}]+[Y'_B] & [Y_{BC}] \\ [Y_{CA}] & [Y_{CB}] & [Y_{CC}]+[Y_{PSPS}] \end{bmatrix} \times \begin{bmatrix} [V_A] \\ [V_B] \\ [V_C] \end{bmatrix} = \begin{bmatrix} [IA'_A] \\ [IA'_B] \\ [0] \end{bmatrix} \tag{23}$$

Then, the general solutions of $[V_A]$, $[V_B]$ and $[V_C]$ can be derived as follows.

$$\begin{bmatrix} [V_A] \\ [V_B] \\ [V_C] \end{bmatrix} = \begin{bmatrix} [Y_{AA}]+[Y'_A] & [Y_{AB}] & [Y_{AC}] \\ [Y_{BA}] & [Y_{BB}]+[Y'_B] & [Y_{BC}] \\ [Y_{CA}] & [Y_{CB}] & [Y_{CC}]+[Y_{PSPS}] \end{bmatrix}^{-1} \times \begin{bmatrix} [IA'_A] \\ [IA'_B] \\ [0] \end{bmatrix} \tag{24}$$

And the general solutions of $[I_A]$, $[I_B]$ and $[I_C]$ are obtained from Equation (20) using voltage vectors given in Equation (24).

$$\begin{bmatrix} -[I_A] \\ -[I_B] \\ [I_C] \end{bmatrix} = \begin{bmatrix} [Y_{AA}] & [Y_{AB}] & [Y_{AC}] \\ [Y_{BA}] & [Y_{BB}] & [Y_{BC}] \\ [Y_{CA}] & [Y_{CB}] & [Y_{CC}] \end{bmatrix} \times \begin{bmatrix} [V_A] \\ [V_B] \\ [V_C] \end{bmatrix}$$

$$= \begin{bmatrix} [Y_{AA}] & [Y_{AB}] & [Y_{AC}] \\ [Y_{BA}] & [Y_{BB}] & [Y_{BC}] \\ [Y_{CA}] & [Y_{CB}] & [Y_{CC}] \end{bmatrix} \times \begin{bmatrix} [Y_{AA}]+[Y'_A] & [Y_{AB}] & [Y_{AC}] \\ [Y_{BA}] & [Y_{BB}]+[Y'_B] & [Y_{BC}] \\ [Y_{CA}] & [Y_{CB}] & [Y_{CC}]+[Y_{PSPS}] \end{bmatrix}^{-1} \times \begin{bmatrix} [IA'_A] \\ [IA'_B] \\ [0] \end{bmatrix} \tag{25}$$

Second, one considers a specific boundary condition that the impedances of the power supplies are low enough compared to other components. This condition is specific but it is a normal assumption for many applications. In this case, $[V_C]$ can be assumed as $[0]$.

The particular solutions of the noise voltage vectors for this condition are obtained from Equation (21).

$$\begin{bmatrix} [Y_{AA}]+[Y'_A] & [Y_{AB}] & [Y_{AC}] \\ [Y_{BA}] & [Y_{BB}]+[Y'_B] & [Y_{BC}] \\ [Y_{CA}] & [Y_{CB}] & [Y_{CC}] \end{bmatrix} \times \begin{bmatrix} [V_A] \\ [V_B] \\ [0] \end{bmatrix} = \begin{bmatrix} [IA'_A] \\ [IA'_B] \\ [I_C] \end{bmatrix} \tag{26}$$

$$\begin{bmatrix} [V_A] \\ [V_B] \end{bmatrix} = \begin{bmatrix} [Y_{AA}]+[Y'_A] & [Y_{AB}] \\ [Y_{BA}] & [Y_{BB}]+[Y'_B] \end{bmatrix}^{-1} \times \begin{bmatrix} [IA'_A] \\ [IA'_B] \end{bmatrix} \tag{27}$$

By setting $[V_C]$ as $[0]$ in Equation (20), the noise current vectors are derived as follows.

$$\begin{bmatrix} -[I_A] \\ -[I_B] \\ [I_C] \end{bmatrix} = \begin{bmatrix} [Y_{AA}] & [Y_{AB}] & [Y_{AC}] \\ [Y_{BA}] & [Y_{BB}] & [Y_{BC}] \\ [Y_{CA}] & [Y_{CB}] & [Y_{CC}] \end{bmatrix} \times \begin{bmatrix} [V_A] \\ [V_B] \\ [0] \end{bmatrix} \tag{28}$$

$$\begin{bmatrix} -[I_A] \\ -[I_B] \\ [I_C] \end{bmatrix} = \begin{bmatrix} [Y_{AA}] & [Y_{AB}] \\ [Y_{BA}] & [Y_{BB}] \\ [Y_{CA}] & [Y_{CB}] \end{bmatrix} \times \begin{bmatrix} [V_A] \\ [V_B] \end{bmatrix} \tag{29}$$

As described in this clause, using the black box model, the noise voltages and the noise currents of an application board can be obtained by simple matrix calculations.

Annex A
(informative)

Nodal equation

A.1 Purpose

This annex is intended to review the fundamentals of the nodal equation. The annex gives proof of Equation (1) that represents characteristics of a PDN using only its external nodes; i.e. external terminals and internal terminals.

A.2 Review

Consider a passive distribution network with (n + 1) nodes. The 0 node is the reference node. For each node, the following equation is derived from Kirchhoff's first law.

$$I_{\mathrm{i}} = \sum_{\mathrm{j}\neq\mathrm{i}} y_{\mathrm{i\,j}} \times (V_{\mathrm{i}} - V_{\mathrm{j}}) \tag{A.1}$$

$$I_{\mathrm{i}} = \sum_{\mathrm{j}\neq\mathrm{i}} y_{\mathrm{i\,j}} \times V_{\mathrm{i}} - \sum_{\mathrm{j}\neq\mathrm{i}} y_{\mathrm{i\,j}} \times V_{\mathrm{j}} \tag{A.2}$$

Here, V_{i} and I_{i} are the voltage and the current flowing into the node i, respectively. $y_{\mathrm{i\,j}}$ is the admittance of the element that is located between node i and node j.

Using an admittance matrix, Equation (A.2) can be rewritten as a nodal equation as follows.

$$\begin{bmatrix}
\sum_{\mathrm{j}\neq0} y_{0,\mathrm{j}} & -y_{0,1} & \cdot & -y_{0,\mathrm{i}-1} & -y_{0,\mathrm{i}} & -y_{0,\mathrm{i}+1} & \cdot & -y_{0,\mathrm{n}-1} & -y_{0,\mathrm{n}} \\
-y_{1,0} & \sum_{\mathrm{j}\neq1} y_{1,\mathrm{j}} & \cdot & -y_{1,\mathrm{i}-1} & -y_{1,\mathrm{i}} & -y_{1,\mathrm{i}+1} & \cdot & -y_{1,\mathrm{n}-1} & -y_{1,\mathrm{n}} \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
-y_{\mathrm{i}-1,0} & -y_{\mathrm{i}-1,1} & \cdot & \sum_{\mathrm{j}\neq\mathrm{i}-1} y_{\mathrm{i}-1,\mathrm{j}} & -y_{\mathrm{i}-1,\mathrm{i}} & -y_{\mathrm{i}-1,\mathrm{i}+1} & \cdot & -y_{\mathrm{i}-1,\mathrm{n}-1} & -y_{\mathrm{i}-1,\mathrm{n}} \\
-y_{\mathrm{i},0} & -y_{\mathrm{i},1} & \cdot & -y_{\mathrm{i},\mathrm{i}-1} & \sum_{\mathrm{j}\neq\mathrm{i}} y_{\mathrm{i},\mathrm{j}} & -y_{\mathrm{i},\mathrm{i}+1} & \cdot & -y_{\mathrm{i},\mathrm{n}-1} & -y_{\mathrm{i},\mathrm{n}} \\
-y_{\mathrm{i}+1,0} & -y_{\mathrm{i}+1,1} & \cdot & -y_{\mathrm{i}+1,\mathrm{i}-1} & -y_{\mathrm{i}+1,\mathrm{i}} & \sum_{\mathrm{j}\neq\mathrm{i}+1} y_{\mathrm{i}+1,\mathrm{j}} & \cdot & -y_{\mathrm{i}+1,\mathrm{n}-1} & -y_{\mathrm{i}+1,\mathrm{n}} \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
-y_{\mathrm{n}-1,0} & -y_{\mathrm{n}-1,1} & \cdot & -y_{\mathrm{n}-1,\mathrm{i}-1} & -y_{\mathrm{n}-1,\mathrm{i}} & -y_{\mathrm{n}-1,\mathrm{i}+1} & \cdot & \sum_{\mathrm{j}\neq\mathrm{n}-1} y_{\mathrm{n}-1,\mathrm{j}} & -y_{\mathrm{n}-1,\mathrm{n}} \\
-y_{\mathrm{n},0} & -y_{\mathrm{n},1} & \cdot & -y_{\mathrm{n},\mathrm{i}-1} & -y_{\mathrm{n},\mathrm{i}} & -y_{\mathrm{n},\mathrm{i}+1} & \cdot & -y_{\mathrm{n},\mathrm{n}-1} & \sum_{\mathrm{j}\neq\mathrm{n}} y_{\mathrm{n},\mathrm{j}}
\end{bmatrix}
\cdot
\begin{bmatrix} V_0 \\ V_1 \\ \cdot \\ V_{\mathrm{i}-1} \\ V_{\mathrm{i}} \\ V_{\mathrm{i}+1} \\ \cdot \\ V_{\mathrm{n}-1} \\ V_{\mathrm{n}} \end{bmatrix}
=
\begin{bmatrix} I_0 \\ I_1 \\ \cdot \\ I_{\mathrm{i}-1} \\ I_{\mathrm{i}} \\ I_{\mathrm{i}+1} \\ \cdot \\ I_{\mathrm{n}-1} \\ I_{\mathrm{n}} \end{bmatrix} \tag{A.3}$$

The value of each diagonal element is the summation of admittances of passive elements that are connected to the corresponding node. The matrix is symmetrical because $y_{\mathrm{i\,j}} = y_{\mathrm{j\,i}}$.

In Equation (A.3) the summation of all elements in each column or each row becomes zero. Namely this matrix is singular. Therefore we usually use the partial matrix and the partial

vector except the reference node. With these relations, we can generate a matrix including the reference node from the partial matrix excluding the reference node.

A.3 Proof of Equation (1)

Consider the PDN that consists of n-nodes. And m-nodes are external nodes and n minus m nodes are internal nodes. Then, Equation (A.3) can be written as follows.

$$\left[\begin{array}{ccc|ccc} Y_{11} & \cdot & Y_{1m} & Y_{1m+1} & \cdot & Y_{1n} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ Y_{m1} & \cdot & Y_{mm} & Y_{mm+1} & \cdot & Y_{mn} \\ \hline Y_{m+11} & \cdot & .Y_{m+1m} & Y_{m+1m+1} & \cdot & Y_{m+1n} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ Y_{n1} & \cdot & Y_{nm} & Y_{nm+1} & \cdot & Y_{1nn} \end{array}\right] \cdot \left[\begin{array}{c} V_1 \\ \cdot \\ V_m \\ \hline V_{m+1} \\ \cdot \\ V_n \end{array}\right] = \left[\begin{array}{c} I_1 \\ \cdot \\ I_m \\ \hline I_{m+1} \\ \cdot \\ I_n \end{array}\right] \tag{A.4}$$

$$\begin{bmatrix} [Y_{EE}] & [Y_{EI}] \\ [Y_{IE}] & [Y_{II}] \end{bmatrix} \times \begin{bmatrix} [V_E] \\ [V_I] \end{bmatrix} = \begin{bmatrix} [I_E] \\ [I_I] \end{bmatrix} \tag{A.5}$$

where,

$[Y_{EE}]$ is the regular admittance matrix that represents interactions between external nodes;

$[Y_{EI}]$ is the matrix that represents admittances between external and internal nodes;

$[Y_{IE}]$ is the matrix that represents admittances between internal and external nodes;

$[Y_{II}]$ is the regular matrix that represents admittances between internal nodes;

$[V_E]$ is the vector that represents voltages of external nodes;

$[V_I]$ is the vector that represents voltages of internal nodes;

$[I_E]$ is the vector that represents currents of external nodes; and

$[I_I]$ is the vector that represents currents of internal nodes.

Equation (A.5) can be expanded into following two equations.

$$[Y_{EE}] \times [V_E] + [Y_{EI}] \times [V_I] = [I_E] \tag{A.6}$$

$$[Y_{IE}] \times [V_E] + [Y_{II}] \times [V_I] = [I_I] \tag{A.7}$$

Note that $[I_I]$ is $[0]$, because the outside environment cannot access internal nodes. From Equation (A.7), $[V_I]$ is obtained as follows.

$$[V_I] = [Y_{II}]^{-1} \times [Y_{IE}] \times [V_E] \tag{A.8}$$

By substituting Equation (A.8) into Equation (A.6), $[V_I]$ can be eliminated.

$$\left([Y_{EE}] + [Y_{IE}] \times [Y_{II}]^{-1} \times [Y_{IE}]\right) \times [V_E] = [I_E] \tag{A.9}$$

The coefficient of $[V_E]$ is an admittance matrix that is represented only by external nodes.

Annex B
(informative)

Example of black box modelling

B.1 Objective

This annex gives an example of black box modelling and its application taking an example of ICEM-CE model.

A diagram of the ICEM-CE model that includes the IC, PCB, and power source models is given in Figure A.1. The IC model has two IAs, an IA for core activity and an IA for I/O activity. And the IC model has one external terminal (node (1)), and two internal terminals (node (2), (3)).The IC is operated under a 10 MHz clock, and the operational mode needs four machine cycles. Therefore, the cycle time of the operation is 400 ns. The Waveforms of the IAs over the operational cycle time are given in Figure B.1b).

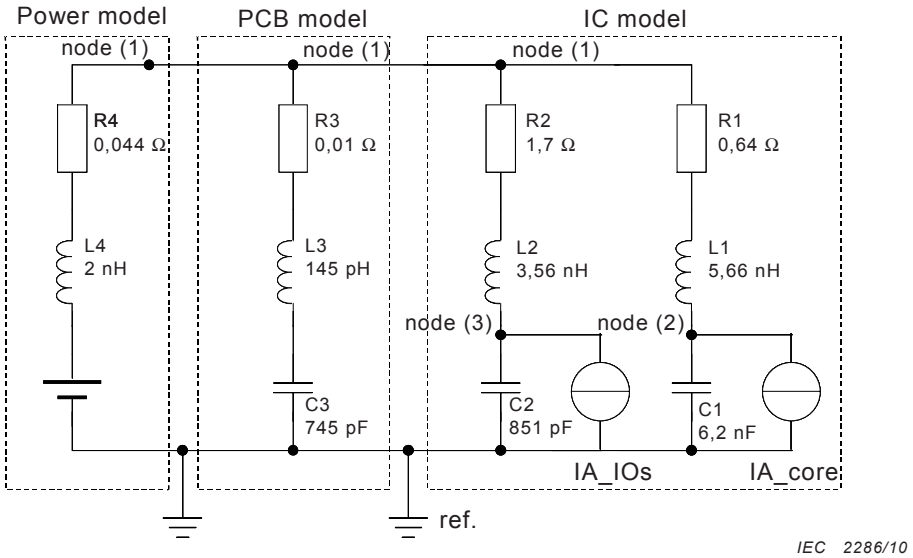

Figure B.1a) – Circuit diagram

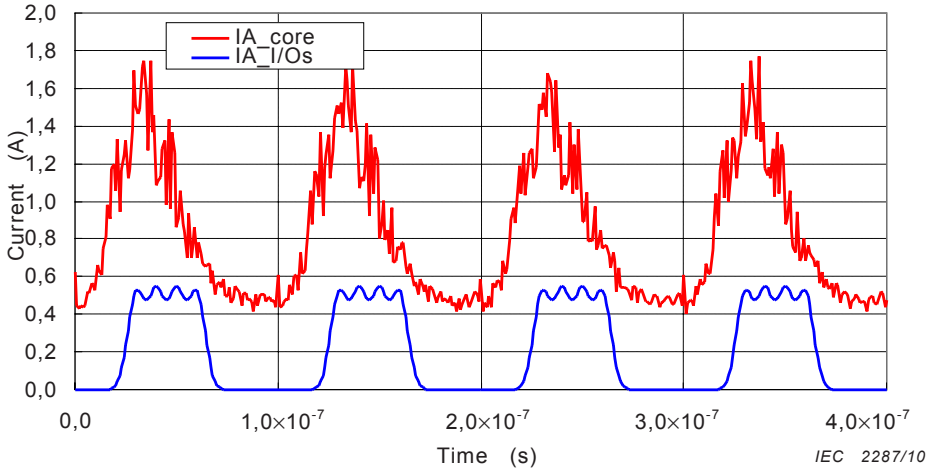

Figure B.1b) – Waveforms of internal activities

Figure B.1 – The ICEM-CE model

B.2 Black box modelling

B.2.1 Equivalent PDN

Equation (2) for the IC model becomes as Equation (B.1).

$$\left[\begin{array}{c|cc} (R_1+j\omega L_1)^{-1}+(R_2+j\omega L_2)^{-1} & -(R_1+j\omega L_1)^{-1} & -(R_2+j\omega L_2)^{-1} \\ \hline -(R_1+j\omega L_1)^{-1} & (R_1+j\omega L_1)^{-1}+j\omega C_1 & 0 \\ -(R_2+j\omega L_2)^{-1} & 0 & (R_2+j\omega L_2)^{-1}+j\omega C_2 \end{array}\right] \times \left[\begin{array}{c} V_1 \\ \hline V_2 \\ V_3 \end{array}\right] = \left[\begin{array}{c} I_1 \\ \hline IA_{\text{core}} \\ IA_{\text{I/Os}} \end{array}\right] \quad \text{(B.1)}$$

The admittance matrix of Equation (B.1) can be compacted using Equation (2). As a result, the admittance matrix, voltage vector and current vector become simple complex numbers as shown below.

$$Y'_{\text{ET ET}} \times V_1 = I_1 + IA' \quad \text{(B.2)}$$

$$Y'_{\text{ET ET}} \equiv [Y_{\text{ET ET}}] - [Y_{\text{ET IT}}] \times [Y_{\text{IT IT}}]^{-1} \times [Y_{\text{IT ET}}] \quad \text{(B.3)}$$

B.2.2 Equivalent IA

According to Equation (8), the equivalent IA can be obtained using the following equation. IA_{core} and $IA_{\text{I/Os}}$ can be derived from waveforms using Fourier transformation.

$$IA' = -[Y_{\text{ET IT}}] \times [Y_{\text{IT IT}}]^{-1} \times \left[\begin{array}{c} IA_{\text{core}} \\ IA_{\text{I/Os}} \end{array}\right] \quad \text{(B.4)}$$

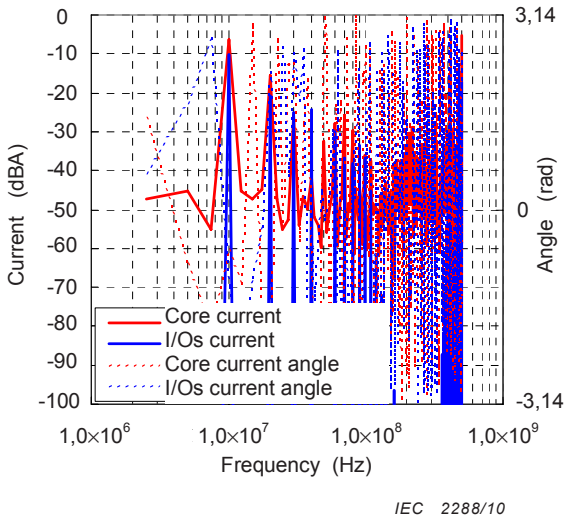

Figure B.2a) – IA_core and IA_I/Os

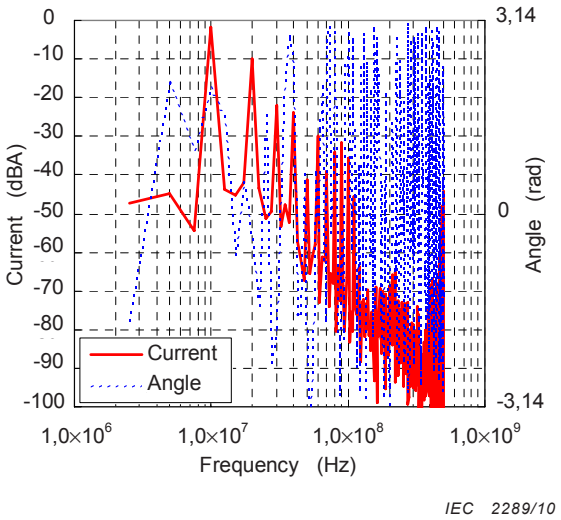

Figure B.2b) – Equivalent IA

Figure B.2 – Spectrum of equivalent IA

B.3 Noise voltage and noise current

The PCB and power source models are given in Equation (B.5) and (B.6), respectively. Figure B.3 shows the calculated admittance of the IC, PCB and power source.

$$Y_{\mathrm{PCB}} = \left(0{,}01 + j\omega \times 145E-12 + \frac{1}{j\omega \times 745E-12}\right)^{-1} \tag{B.5}$$

$$Y_{\mathrm{Power}} = \left(0{,}044 + j\omega \times 2E-9\right)^{-1} \tag{B.6}$$

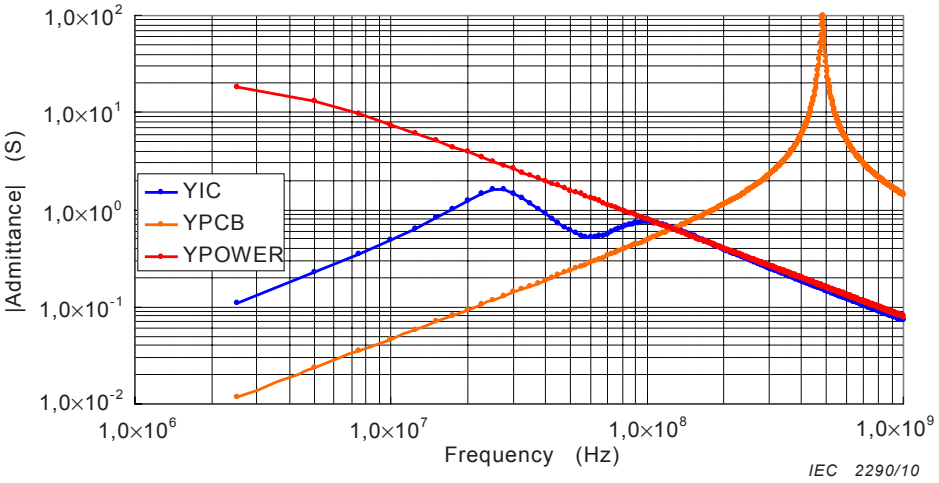

Figure B.3 – Calculated admittances

The noise voltage and noise current of node (1) can be calculated using the following equations. Figure B.4 shows the results.

$$V_1 = \left(Y'_{\mathrm{ETET}} + Y_{\mathrm{PCB}} + Y_{\mathrm{Power}}\right)^{-1} \times IA' \tag{B.7}$$

$$I_{PCB} + I_{Power} = (Y_{PCB} + Y_{Power}) \times V_1 \quad \text{(B.8)}$$

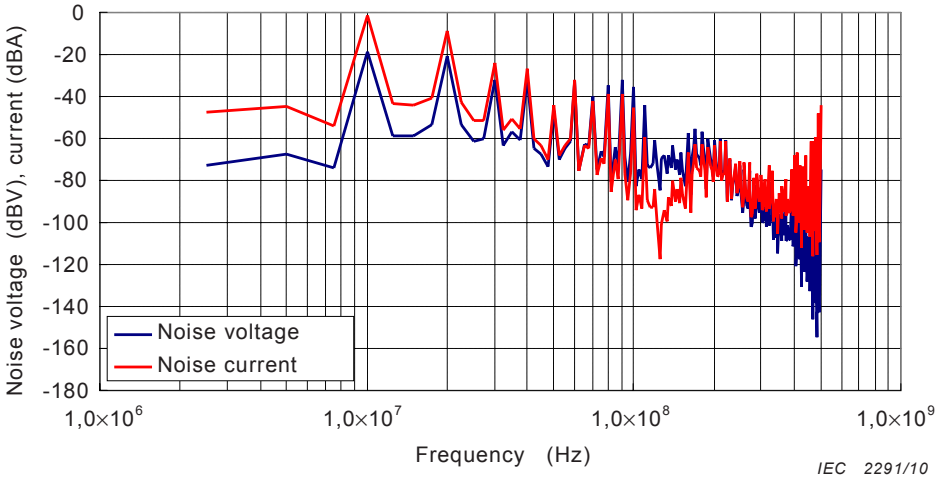

Figure B.4 – Noise voltage and noise current

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1 *To be published.*

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