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High-voltage switchgear and controlgear —

Part 305: Capacitive current switching capability of air-insulated disconnectors for rated voltages above 52 kV

National foreword

This Published Document is the UK implementation of IEC/TR 62271-305:2009.

The UK participation in its preparation was entrusted by Technical Committee PEL/17, Switchgear, controlgear, and HV-LV co-ordination, to Subcommittee PEL/17/1, High-voltage switchgear and controlgear.

A list of organizations represented on this committee can be obtained on request to its secretary.

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HIGH-VOLTAGE SWITCHGEAR AND CONTROLGEAR –

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IEC 62271-305, which is a technical report, has been prepared by subcommittee 17A: High-voltage switchgear and controlgear, of IEC technical committee 17: Switchgear and controlgear.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
17A/872/DTR	17A/885/RVC

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of the IEC 62271 series, published under the general title *High-voltage switchgear and controlgear,* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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HIGH-VOLTAGE SWITCHGEAR AND CONTROLGEAR –

Part 305: Capacitive current switching capability of air-insulated disconnectors for rated voltages above 52 kV

1 Scope

This technical report applies to high-voltage air-insulated disconnectors for rated voltages above 52 kV. The report describes the capacitive current switching duty and provides guidance on laboratory testing to demonstrate the switching capability. Air-insulated disconnectors equipped with auxiliary interrupting devices are included under this scope.

NOTE For manually operated disconnectors, the in-service safety of the operator should be considered and it should be recognized that the results of the switching tests described herein (performed using motor-operated disconnectors) are not necessarily representative of the performance of such disconnectors in actual service. Due diligence should be exercised if the switching tests indicate that prolonged arc durations are probable.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62271-1: *High-voltage switchgear and controlgear – Part 1: Common specifications*

IEC 62271-102:2001 *High-voltage switchgear and controlgear – Part 102: Alternating current disconnectors and earthing switches*

3 Terms and definitions

For purposes of this part of IEC 62271 the terms and definitions in IEC 62271-1 and IEC 62271-102 apply.

4 Background and purpose

Disconnectors do not have current interrupting ratings but, by virtue of having one or more moving contacts during opening operations, they have a certain current switching capability. For capacitive currents and air-insulated disconnectors, this capability has in the past been taken as 0,5 A or less and no testing was defined. For gas-insulated disconnectors, the required capacitive current switching capability and test requirements are specified in Annex F of IEC 62271-102.

User requirements for capacitive current switching using air-insulated disconnectors frequently exceed the above-stated 0,5 A. The purpose, therefore, of this report is to provide an analysis of the switching duty (refer to Annex A) and to define testing procedures.

5 Switching tests

5.1 Arrangement of the disconnector for tests

The disconnector under test should be completely mounted on its own support or on an equivalent support. For safety reasons and to obtain consistent results, only motor operation should be used. Motor operation should be at the minimum supply voltage.

Before commencing switching tests, resistance measurement of the main circuit and no-load operations should be made and details of the operating characteristics of the disconnector such as contact separation (arc initiation), closing time and opening time, should be recorded. Only singe-phase tests on one pole of a three-pole disconnector need be performed provided that the pole is not in a more favourable condition than the complete three-pole disconnector with respect to

- closing time;
- opening time;
- influence of adjacent phases.

NOTE Single-phase tests are adequate to demonstrate the switching performance of a disconnector provided that the arcing time and arc reach are such that there is no possibility of involvement of an adjacent phase. If excessive arc reach is encountered during single-phase testing, then three-phase testing should be performed. A reach of the tip of the arc towards an adjacent phase equal to or greater than half the metal-to-metal spacing between phases is to be considered as excessive.

5.2 Earthing of the test circuit and disconnector

The frame of the disconnector should be earthed and the current to earth should be measured.

5.3 Test frequency

Disconnectors may be tested using either 50 Hz or 60 Hz since both frequencies are considered to be equivalent.

5.4 Test voltage

The test voltage should be the phase-to-earth voltage based on the rated voltage of the disconnector. In the event of three-phase testing, the test voltage should be the rated voltage of the disconnector applied on a three-phase basis.

NOTE Due to laboratory limitations, testing on one break of double break disconnectors at half the test voltage is permissible. An even voltage distribution across the two breaks can be assumed.

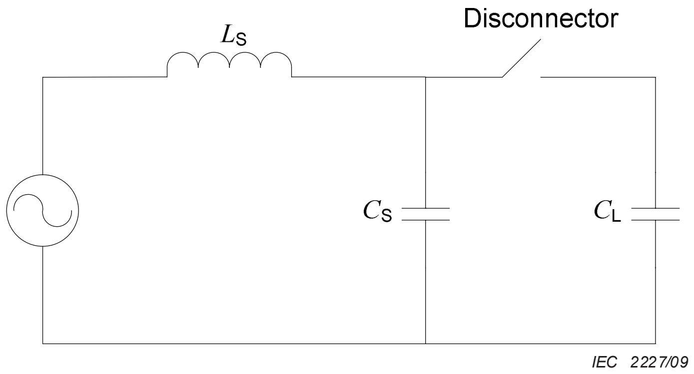
5.5 Test current

The test current, or currents if more than one current level is to be tested, should be as agreed between the manufacturer and the user.

NOTE Typical capacitive charging current values for station equipment and lines are shown in Annex B.

5.6 Test circuit

The test circuit in principle should be as shown in Figure 1.



Key

L_S	Short-circuit inductance
C_S	Supply side capacitance
C_L	Load side capacitance

Figure 1 – Test circuit in principle for capacitive current switching

L_S should be based on the rated short-time withstand current at the rated voltage of the disconnector under test. However this will require a circuit with a strong source, which is impractical in many cases. An alternative circuit is described in Annex C.

For each test current, the test should be performed at C_S/C_L = 0,1.

The permissible tolerances for the test quantities are as shown in Table 1.

Table 1 – Test tolerances

Test quantity	Tolerance
Test voltage	±5 %
Test current	±10 %
C_S/C_L	±20 %

5.7 Tests

5.7.1 Test duties and measurements

Twenty CO operations should be made for each test current with no trapped charge on the load capacitance prior to closing. Twenty such operations are considered to be statistically acceptable. The recovery voltage shall be maintained for ten seconds (10 s) after the disconnector reaches its fully open position.

The following measurements should be made during the test:

a) power frequency source voltage and load side dc and transient overvoltages;

b) current;

c) arc duration;

d) video recordings of arc propagation (the intent is to record the extreme vertical and horizontal reach of the arc as viewed along the longitudinal line of the disconnector).

NOTE If the tests are performed outdoors, atmospheric conditions should be recorded to include wind direction and velocity, humidity, air pressure and ambient temperature. No corrections for such elements are required.

5.7.2 Behaviour of disconnector during tests

The disconnector shall meet the following requirements during the tests:

a) the disconnector shall interrupt the current before the moving blade or blades reach their fully open position;

b) no earth faults, or phase-to-phase faults in the event of three-phase testing, shall occur.

5.7.3 Condition of disconnector after tests

The disconnector shall meet the following requirements after the tests:

a) a visual inspection is considered sufficient to verify that the mechanical parts and insulators are in essentially the same condition as before the tests;

b) the condition of the main contacts, in particular with regard to wear, contact area, pressure and freedom of movement, shall be such that they are capable of carrying the rated normal current of the disconnector;

c) the resistance of the main circuit after the test shall not exceed that before the test by more than +10 %;

d) the operating times before and after the tests shall be essentially the same.

5.8 Test reports

The results of all tests should be recorded in test reports. Sufficient information should be included so that the essential parts of the disconnector tested can be identified.

The test report should at least contain the following information:

a) typical oscillographic or similar records of the tests performed;

b) test circuit;

c) test currents;

d) test voltages including overvoltages;

e) arc durations;

f) arc extreme reach in vertical and horizontal directions;

g) number of CO operations;

h) record of the condition of the of the main and arcing contacts after test;

i) resistance of the main circuit before and after the test sequence;

j) operating times before and after the tests.

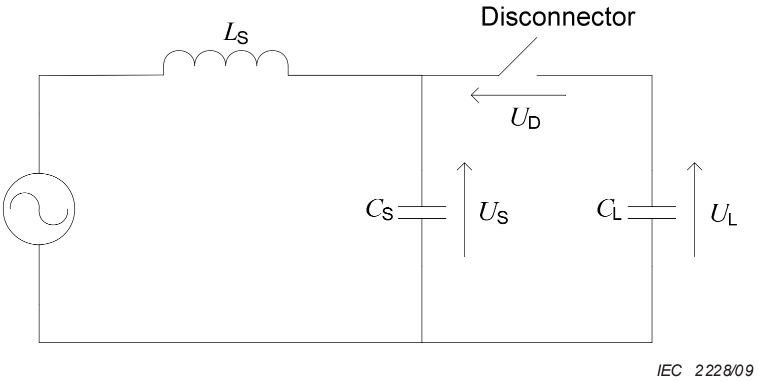
k) Atmospheric conditions: ambient temperature, air pressure, humidity and, if outdoors, wind velocity and direction.

General information concerning the supporting structure of the disconnector should be included. The type of operating device employed during the tests should be recorded.

Annex A
(informative)

Analysis

Capacitive current switching is a circuit and arc interactive event with varying severities of restriking and arc duration. The severity of restriking both in terms of frequency, current and overvoltage magnitudes, is dependent on the relative values of the source side (C_S) and load side (C_L) capacitances as shown in the basic capacitive current switching circuit Figure A.1.

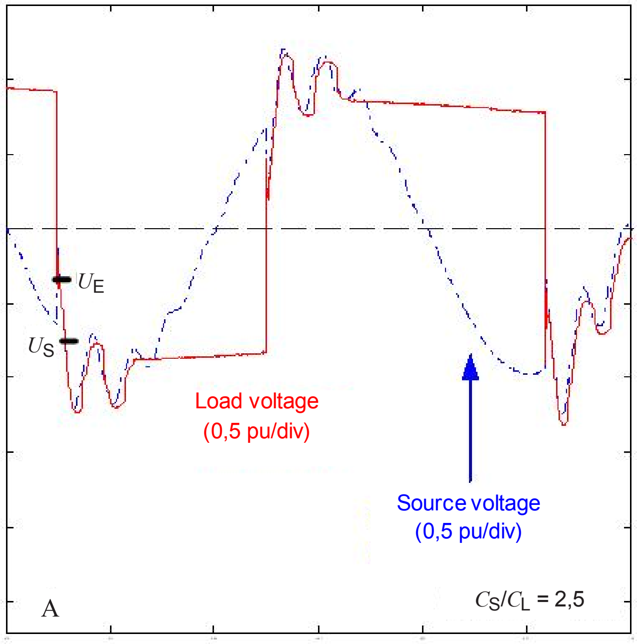


Key

L_S	Short-circuit inductance
C_S	Supply side capacitance
C_L	Load side capacitance
U_S	Source side voltage
U_L	Load side voltage
U_D	Voltage across disconnector

Figure A.1 – Basic capacitive current switching circuit

Typical test oscillograms are shown in Figure A.2 and this behaviour is explained in the following.



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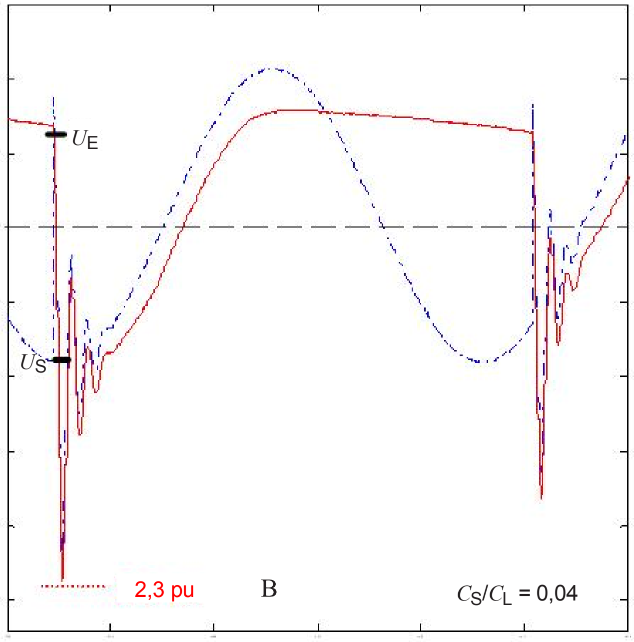


IEC 2230/09

Key

C_S	Source side capacitance	U_E	Equalization voltage
C_L	Load side capacitance	U_S	Supply side voltage

Figure A.2 – Test oscillograms for current of 2 A and C_S/C_L ratios of 2,5 (Trace A) and 0,04 (Trace B)

When a restrike occurs, the voltage on C_S and C_L will first equalize at U_E (equalization voltage). Taking the voltages on the source and load side capacitances as U_S and U_L, the corresponding charges are:

$$Q_\mathrm{S} = U_\mathrm{S} C_\mathrm{S}$$

$$Q_\mathrm{L} = -U_\mathrm{L} C_\mathrm{L}$$

and $$Q_\mathrm{total} = U_\mathrm{S} C_\mathrm{S} + (-U_\mathrm{L} C_\mathrm{L})$$

After restriking and charge redistribution, U_E is given by:

$$U_\mathrm{E} = \frac{Q_\mathrm{total}}{C_\mathrm{S} + C_\mathrm{L}}$$

or $$U_\mathrm{E} = \frac{U_\mathrm{S} C_\mathrm{S} - U_\mathrm{L} C_\mathrm{L}}{C_\mathrm{S} + C_\mathrm{L}} \tag{A.1}$$

Prior to restriking the voltage across the disconnector, U_D is:

$$U_\mathrm{D} = U_\mathrm{S} + U_\mathrm{L}$$

and substituting in Equation (A.1) for U_L

$$U_\mathrm{E} = \frac{U_\mathrm{S} C_\mathrm{S} - C_\mathrm{L}(U_\mathrm{D} - U_\mathrm{S})}{C_\mathrm{S} + C_\mathrm{L}}$$

or $$U_\mathrm{E} = U_\mathrm{S} - \frac{U_\mathrm{D}}{1 + C_\mathrm{S} / C_\mathrm{L}} \tag{A.2}$$

The peak overvoltage value to ground U_OV is given by:

$$U_\mathrm{OV} = U_\mathrm{S} + \beta(U_\mathrm{S} - U_\mathrm{E}) \tag{A.3}$$

where β is the damping factor of value less than 1.

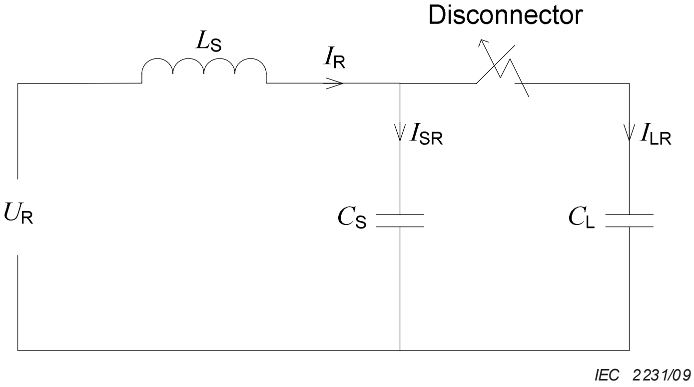
Substituting from Equation (A.2):

$$U_\mathrm{OV} = U_\mathrm{S} + \beta\left(\frac{U_\mathrm{D}}{1 + C_\mathrm{S} / C_\mathrm{L}}\right) \tag{A.4}$$

The dependency on the ratio $C_\mathrm{S}/C_\mathrm{L}$ is evident and can be summarized as follows:

- $C_\mathrm{S}/C_\mathrm{L} > 1$, the difference between U_S and U_E will be low, giving lower values of U_OV and shorter arcing times due to lower injected energy into the arc (Figure A.2, Trace A);
- $C_\mathrm{S}/C_\mathrm{L} < 1$, the difference between U_S and U_E will be high, giving higher values of U_OV and longer arcing times due to higher injected energy into the arc (Figure A.2, Trace B).

The restriking current I_LR through the arc to C_L is calculated using the circuit in Figure A.3.



Key

U_R	Supply side voltage	I_{LR}	Restriking current
L_S	Short-circuit inductance	C_S	Supply side capacitance
I_R	Supply current	C_L	Load side capacitance
I_{SR}	Current through the supply side capacitance		

Figure A.3 – Circuit for restriking current calculation

I_R is given by:

$$I_R = \frac{U_R}{\sqrt{\dfrac{L_S}{C_S + C_L}}}$$

where $U_R = U_S - U_E$

$$I_{LR} = \frac{I_R}{\omega(C_S + C_L)} \times \omega C_L$$

$$= U_R \sqrt{\frac{C_S + C_L}{L_S}} \times \frac{C_L}{C_S + C_L}$$

$$= U_R \sqrt{\frac{C_L}{L_S}\left(\frac{1}{1 + C_S/C_L}\right)} \qquad \text{(A.5)}$$

I_{LR} is thus dependent on C_L, L_S and the ratio C_S/C_L. Equations (A.4) and (A.5) show that these parameters should be properly represented in type test circuits in order for the testing to be valid.

For switching tests, C_S/C_L = 0,1 is taken as being representative for the vast majority of applications. The value of L_S is selected on the basis of the disconnector being applied on a system with a fault level equal to the rated short-time current of the disconnector.

In addition to the influence of the ratio C_S/C_L and L_S, the arc may also exhibit thermal properties, which will tend to increase the arc duration. Based on field and laboratory test observations, arc duration dependency can be summarized as follows:

- For currents of 1 A or less, thermal effects are not significant and the arc duration is dependent mainly on achieving the minimum disconnector gap to withstand the recovery voltage and on the ratio C_S/C_L.
- For currents greater than 1 A, thermal effects become significant and the arc duration is dependent on the current magnitude in addition to achieving a minimum disconnector contact gap and on the ratio C_S/C_L.
- The longest arc durations at any current will occur when $C_S/C_L < 1$ and due diligence should be exercised in such cases.

Annex B
(informative)

Capacitive charging currents

Typical capacitive charging current values for station air-insulated equipment are shown in Tables B.1, B.2 and B.3.

Table B.1 – Capacitive charging currents at 245 kV and below

Equipment type	**Capacitive current (A) at**					
	72,5 kV		**145 kV**		**245 kV**	
	50 Hz	60 Hz	50 Hz	60 Hz	50 Hz	60 Hz
CT	≤ 0,04	≤ 0,04	≤ 0,04	≤ 0,04	≤ 0,04	≤ 0,04
CVT (4000 pF)	0,05	0,06	0,11	0,13	0,18	0,21
Busbars/m	$1,7 \times 10^{-4}$	2×10^{-4}	$0,32 \times 10^{-3}$	$0,39 \times 10^{-3}$	$0,54 \times 10^{-3}$	$0,65 \times 10^{-3}$

Table B.2 – Capacitive charging currents at 300 kV to 550 kV

Equipment type	**Capacitive current (A) at**					
	300 kV		**420 kV**		**550 kV**	
	50 Hz	60 Hz	50 Hz	60 Hz	50 Hz	60 Hz
CT	0,05	0,06	0,08	0,09	0,1	0,12
CVT (4 000 pF)	0,22	0,26	0,3	0,37	0,4	0,48
Busbars/m	$0,66 \times 10^{-3}$	$0,8 \times 10^{-3}$	$0,84 \times 10^{-3}$	$1,0 \times 10^{-3}$	$1,1 \times 10^{-3}$	$1,3 \times 10^{-3}$

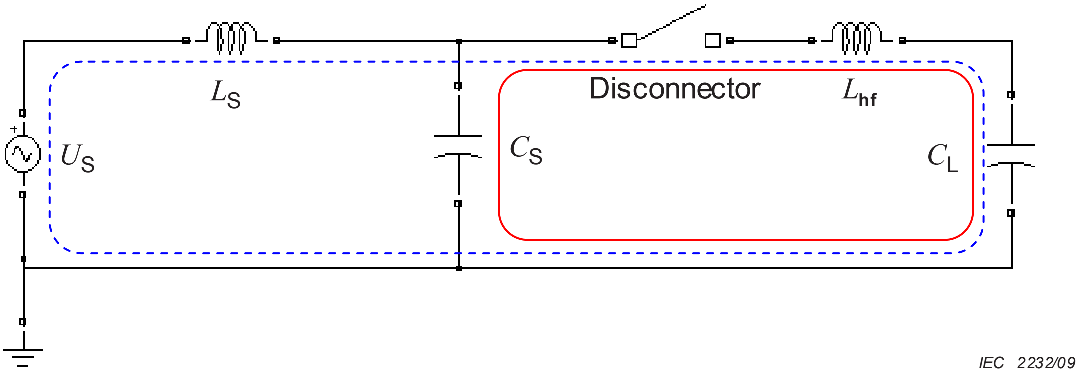
Table B.3 – Capacitive charging currents at 800 kV to 1 200 kV

Equipment type	**Capacitive current (A) at**					
	800 kV		**1 100 kV**		**1 200 kV**	
	50 Hz	60 Hz	50 Hz	60 Hz	50 Hz	60 Hz
CT	0,15	0,18	TBD	TBD	TBD	TBD
CVT (5 000 pF)	0,72	0,87	1,0	1,2	1,1	1,3
Busbars/m	$1,8 \times 10^{-3}$	$2,2 \times 10^{-3}$	$2,5 \times 10^{-3}$	3×10^{-3}	$2,8 \times 10^{-3}$	$3,3 \times 10^{-3}$
TBD = To be determined.						

Optical instrument transformers, if used, will have about the same capacitance as post insulators, i.e. about 50 pF, and the associated capacitive charging currents will be negligible.

Annex C
(informative)

Test circuits



Key

U_S	Supply side voltage	C_L	Load side capacitance
L_S	Short-circuit inductance	L_{hf}	Inductance C_S and C_L loop
C_S	Supply side capacitance		

Figure C.1 – Basic capacitive current switching circuit

The basic capacitive current switching circuit in Figure C.1 is considered to be a realistic representation of reality when the short-circuit impedance L_S is based on the short-time current for which the disconnector is rated. Upon restrike of the disconnector gap, the restriking current basically has three components:

a) high-frequency (HF) component (indicated by the solid line loop of the circuit C_S - Disconnector - L_{hf} - C_L);

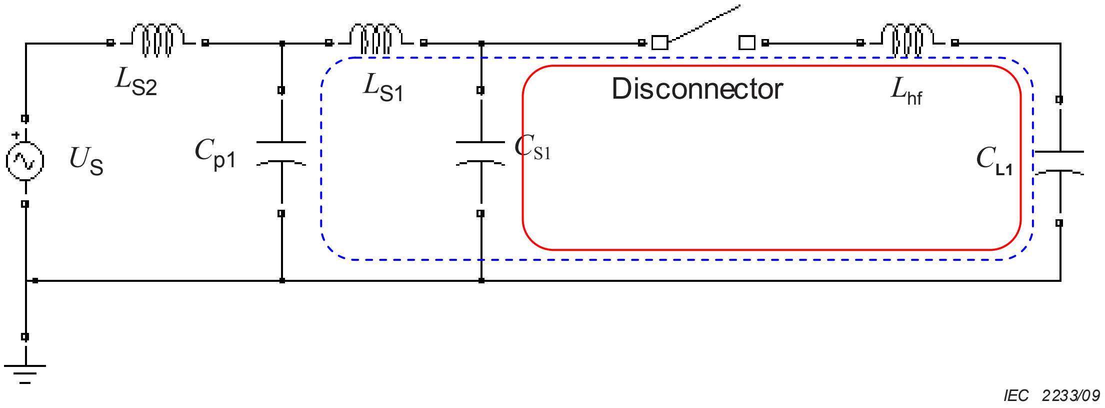
b) medium frequency (MF) component (indicated by the dashed line loop of the circuit U_S - L_S Disconnector - L_{hf} - C_L);

c) power frequency (PF) component (also in the dashed line loop of the circuit U_S - L_S Disconnector - L_{hf} - C_L).

These currents determine the thermal energy that is injected into the arc path, the consequent heating of the arc and the ultimate recovery of the gap. Each of these components have their own contribution to thermal processes in terms of amplitude and/or duration: HF (few kA, but very short duration), MF (few hundreds of amperes, longer duration), PF (few amperes but long duration).

The circuit above, however, is unpractical, because it implies that tests with only a few amperes must be done in circuits having a very strong source (must be able to supply the short-time current). Already for moderate voltages (> 145 kV) this would imply such tests are impossible.

As an alternative, the test circuit shown in Figure C.2 is proposed.



Key

U_s	Supply side voltage	C_{s1}	Supply side capacitance
L_{s2}	Test supply side inductance	C_{L1}	Load side capacitance
C_{p1}	Test supply side capacitance	L_{hf}	Inductance C_s and C_L loop
L_{s1}	Short-circuit inductance		

Figure C.2 – Alternative test circuit

In this circuit, the source can be much weaker ($L_{S2} >> L_S$), whereas all other components can be kept identical to the original circuit: $C_{S1} \cong C_s$, $C_{L1} \cong C_L$ and $L_{S1} \cong L_S$. The capacitor C_{p1} (low impedance for MF current) effectively shunts the (weak) source part of the circuit with its relatively high impedance circuit.

Simulations have been carried out, comparing the basic circuit with the alternative circuit for three values of C_{p1} (1 000 nF, 100 nF and 10 nF) and two values of C_{S1}/C_{L1} (0,1 and 1). In each of the six plots shown in Figure C.3, the drawn curves are the traces from the alternative circuit, the dashed traces (for comparison) the traces from the basic circuit. The upper trace in each of the six figures is the restriking current through the disconnector and the lower trace is the integrated current being proportional to the energy supplied by the arc to the gap.

Simulations were run with a rated (line) voltage of 245 kV, 2 A capacitive current (C_L = 45 nF). Stray-inductance L_{hf} is taken as 20 µH and $L_{S2} = 5L_S$. Reignition is considered with source at positive peak voltage and load at trapped voltage of 100 kV negative.

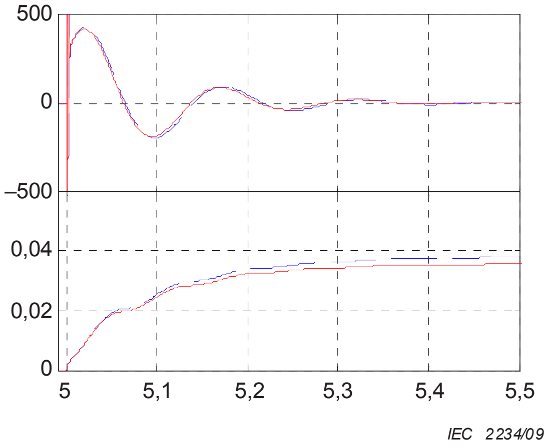
Examination of the plots shows that:

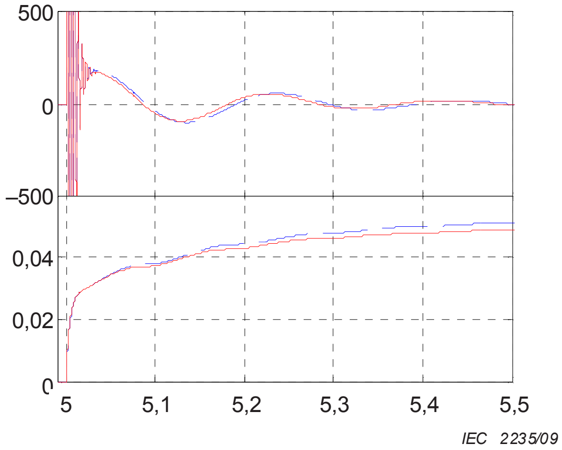
a) Roughly 50 % of the arc energy is provided by the HF current, is not dependent on the source circuit, and is released during a very short period.

b) The other 50 % is provided by the MF current, in a much longer period, depending on the disconnector's capability to interrupt this current at a zero crossing. This portion is therefore dependent on the source side topology.

c) Equivalence between basic and alternative circuit is better with high values of C_{p1}.

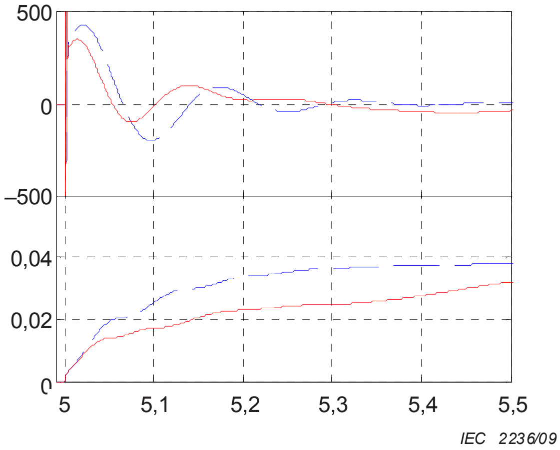
d) A value of C_{p1} of approximately five (5) times the value of C_L appears to reasonably represent the phenomena at restriking.

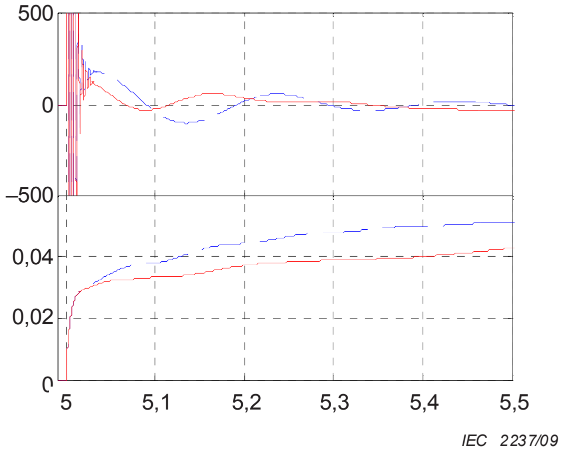




C_{S1}/C_{L1} = 0,1; C_{p1} = 1000 nF

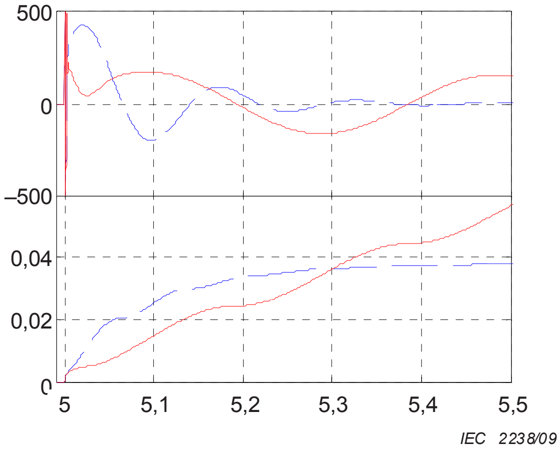
C_{S1}/C_{L1} = 1; C_{p1} = 1000 nF

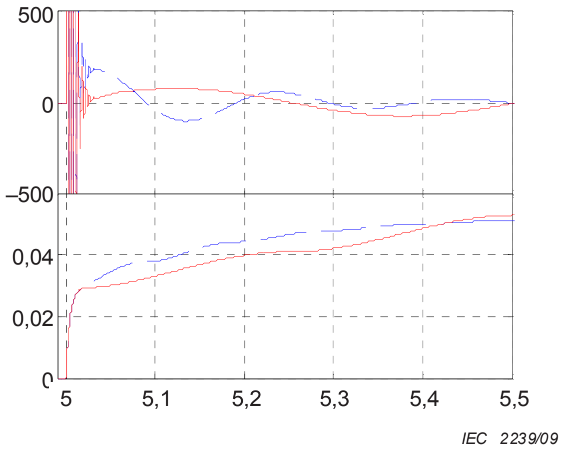




C_{S1}/C_{L1} = 0,1; C_{p1} = 100 nF

C_{S1}/C_{L1} = 1; C_{p1} = 100 nF





C_{S1}/C_{L1} = 0,1; C_{p1} = 10 nF

C_{S1}/C_{L1} = 1; C_{p1} = 10 nF

Horizontal axis in ms.

Figure C.3 – Restriking and integrated currents (in A and As, respectively) for the basic (dashed) traces) and alternative circuits (drawn traces)

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