DRAFT FOR DEVELOPMENT

DD IEC/PAS 62326-7-1:2007

Performance guide for single- and double-sided flexible printed wiring boards

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National foreword

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A review of this Draft for Development will be carried out not later than 3 years after its publication.

Notification of the start of the review period, with a request for the submission of comments from users of this Draft for Development, will be made in an announcement in the appropriate issue of *Update Standards*. According to the replies received, the responsible BSI Committee will judge whether the validity of the PAS should be extended for a further 3 years or what other action should be taken and pass their comments on to the relevant international committee.

Observations which it is felt should receive attention before the official call for comments will be welcomed. These should be sent to the Secretary of the responsible BSI Technical Committee at British Standards House, 389 Chiswick High Road, London W4 4AL.

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PERFORMANCE GUIDE FOR SINGLE- AND DOUBLE-SIDED FLEXIBLE PRINTED WIRING BOARDS

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1 Scope

This PAS provides the requirements for the single- and double-sided flexible printed wiring boards (hereinafter designated as "flexible printed board" or FPC).

In this document, an FPC means a single- or double-sided FPC prepared by lamination of a film of polyester or polyimide with copper foil(s) on one or both sides of a board including the type with no adhesive layer, and with conductor pattern formed by the subtractive method (etching of the copper foil), or possibly by the build-up method.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60326-7:1981, *Printed boards – Part 7: Specification for single- and double-sided flexible printed boards without through connections*

IEC 60326-8:1981, *Printed boards – Part 8: Specification for single- and double-sided flexible printed boards with through connections*

JPCA-TD01:2000, *Terms and definitions for printed circuits*

JPCA-BM03:2003*, Flexible printed wiring boards (adhesive and adhesiveless types)*

JIS C 5016:1994, *Test methods for flexible printed wiring boards*

JIS C 5017:1994, *Single- and double-sided flexible printed wiring boards*

JIS C 5603:1993, *Terms and definitions for printed circuits*

JIS C 6471:1995, *Test methods of copper-clad laminates for flexible printed wiring boards*

JIS C 6472:1995, *Copper-clad laminates for flexible printed wiring boards (polyester film, polyimide film)*

JIS C 6515:1998, *Copper foil for printed wiring boards*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in JIS C 5603, JIS C 5017, JIS C 5016, and JPCA-FC03 apply.

4 Test methods

The test methods used in this document as specified below shall be in conformance with JIS C 5016.

a) Test methods requiring complicated referencing procedures are reproduced in this document.

b) Tests on through connection apply only to double-sided FPCs.

c) External appearance is the only requirement specified in this document for stiffeners affixed to FPCs.

5 Performance levels

The FPCs are classified into three levels, Levels 1, 2, and 3, and an additional special level, Level X, for applications requiring special attention. They are defined as:

Level 1 – FPCs requiring "ordinary" performance;

Level 2 – FPCs requiring "high" performance;

Level 3 – FPCs requiring "extra-high" performance;

Level X – FPCs requiring special performances which do not belong to the above-mentioned three levels, and the specifications requiring an agreement between user and supplier.

A relevant level of the board is chosen for a specific application of the board. A different level can be selected for a specific section of the board when the required specification of the section is different from that of another part of the board.

6 Base materials

The base materials used in FPCs shall satisfy the requirements specified in JPCA-BM03.

7 Visual inspection

7.1 Test environment

The test environment shall meet the requirements of JIS C 5016, Clause 3.

7.2 Test specimens

The test specimens shall meet the requirements of JIS C 5016, Clause 4.

7.3 Tools for testing

A magnifying glass having a magnification of 3× to 10× shall be used for examining the appearance and the surface finish conditions of the product. Dimensions shall be measured with a scaled magnifying glass or an instrument capable of two-dimensional coordinate measuring, if necessary. Thickness shall be measured with a micrometer having an accuracy of 1 μm or better.

7.4 Preparation of limit samples

Limit samples showing the required criteria to make technical judgments may be prepared under agreement between user and supplier for the application of this document.

7.5 Description of inspection

Requirements, procedures, and illustration for visual inspections are given in 7.5.1 through 7.5.6. Requirements that are not designated for a specific performance level shall apply to all the performance Levels 1, 2 and 3.

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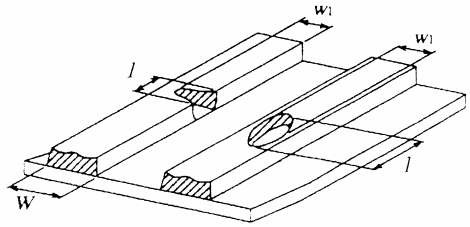
7.5.1 Visual inspection of conductor

7.5.1.1 Open and short circuit

There shall be no open and/or short circuit on FPCs.

7.5.1.2 Nicks and pinholes on conductor

a) The allowable width (w_1) and length (l) of a nick and a pinhole of the conductor reducing conductor width, as shown in Figure 1, shall meet the requirement given in Table 1 for the finished conductor width (W) (see Note 1).



NOTE 1 The width of the finished conductors should be measured at the bottom of the conductor.

Figure 1 – Nicks and pinholes in conductor

Table 1 – Allowable nicks and pinholes

Level	Nicks and pinholes
1 and 2	$w1 \leqq 1/2W$ $l \leqq 2W$
3	$w1 \leqq 1/3W$ $l \leqq W$

b) The void area on a land, as illustrated in Figure 2, shall not exceed 10 % of the effective exposed land area.

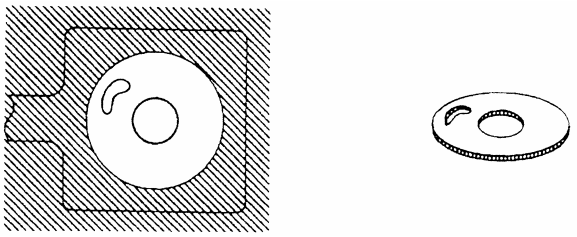


Figure 2 – Reduced area on land

c) The circumferential void of a lead insertion hole, as illustrated in Figure 3, shall not exceed one-third of the total circumference.

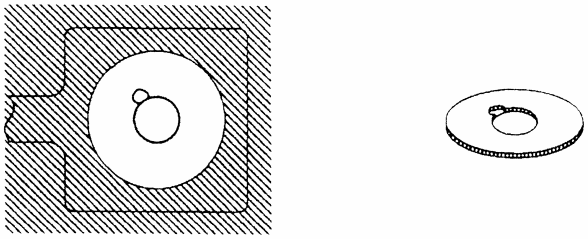


Figure 3 – Circumferential void at the component hole

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7.5.1.3 Distance between conductor/spur and nodule of conductor

The distance (s_1) or (s_2 + s_3) in Figure 4 relative to the finished conductor spacing(s) shall meet the requirement given in Table 2.

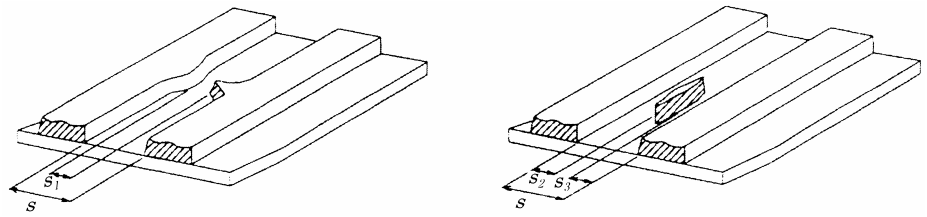

Figure 4 – Unnecessary copper between conductor/spur and nodule of conductor

Table 2 – Allowable unnecessary copper, spur and nodule between conductors

Level	Unnecessary copper, spurs and nodules, s_1 or (s_2 + s_3)
1 and 2	1/2 s_1 ≦ a or (s_2 + s_3)
3	2/3 s_1 ≦ a or (s_2 + s_3)

7.5.1.4 Unnecessary copper between conductor/spur and nodule of conductor in an open area

The spacing(s) between the board edges and the unnecessary copper or spur and nodule shall be larger than 0,125 mm in an open area where no conductor pattern is routed, as illustrated in Figure 5. The spacing(s) between the board edge and the unnecessary copper or spur and nodule shall be larger than 0,125 mm. The open area as stated in this clause shall have a width of no less than 0,375 mm.

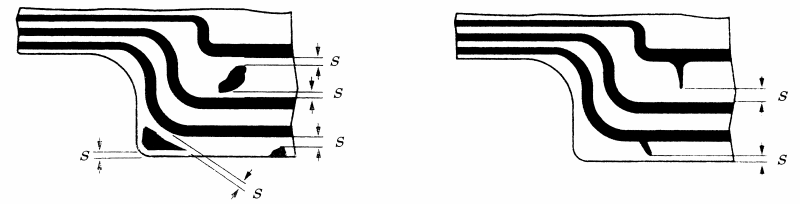

Figure 5 – Unnecessary copper, spurs and nodules in an open area and nodules of conductor corners

7.5.1.5 Etched concave surface of the conductor

Etched concave surface (d) of the conductor relative to the conductor thickness (t), as illustrated in Figure 6, shall meet the requirement given in Table 3. The concave surface shall not run across the entire width of a conductor.

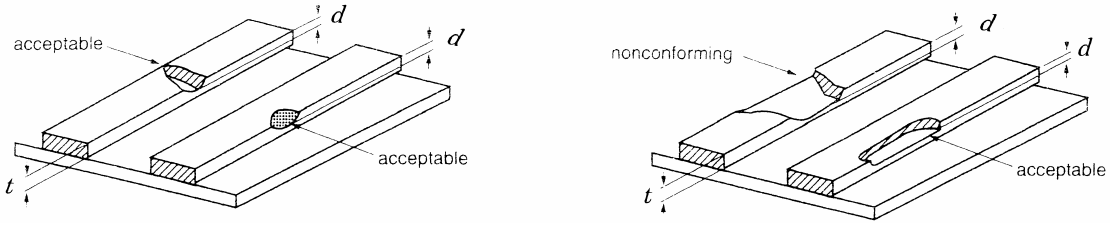

Figure 6 – Etched concave surface of the conductor and nodule at a conductor corner

Table 3 – Allowable etched concave of the surface conductor

Level	Etched concave surface of the conductor, d (t: conductor thickness)
1 and 2	$d \leqq 1/3\ t$
3	$d \leqq 1/5\ t$

7.5.1.6 Conductor delamination

The width (w_1) and length (l) of conductor delamination relative to the finished conductor width (W), as illustrated in Figure 7, shall meet the requirement given in Table 4.

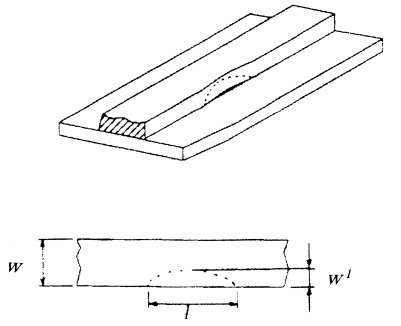

Figure 7 – Conductor delamination

Table 4 – Allowable conductor delamination

Level	Conductor delamination, length (l), width (w_1)
1	Coverlay laminated area $l \leqq W$ and $w1/W \leqq 1/3$ for flexing area $l \leqq W$ and $w1/W \leqq 1/2$ for other area
	No coverlay laminated area $l/W \leqq 1/4$ and $w_1/W \leqq 1/4$
2 and 3	There shall be no delamination in the conductor which can be observed by the naked eye

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7.5.1.7 Conductor crack

There shall be no crack in the conductor.

7.5.1.8 Scratch on conductor

A scratch on a conductor surface, as illustrated in Figure 8, indicates the damage made by a sharp metal point and is harmful to the performance of the printed circuit. The depth (d) of a scratch shall meet the requirement given in Table 5 relative to the conductor thickness (t). The scratch shall not damage the bending property of the repeatedly flexing portion.

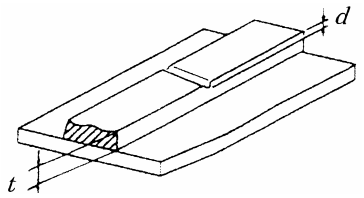


Figure 8 – Scratch on conductor

Table 5 – Allowable scratch on conductor

Level	Depth of scratch on conductor, d
1 and 2	$d \leqq 1/3\ t$
3	$d \leqq 1/5\ t$

7.5.1.9 Discoloration

Discoloration shall meet the requirement given in Table 6.

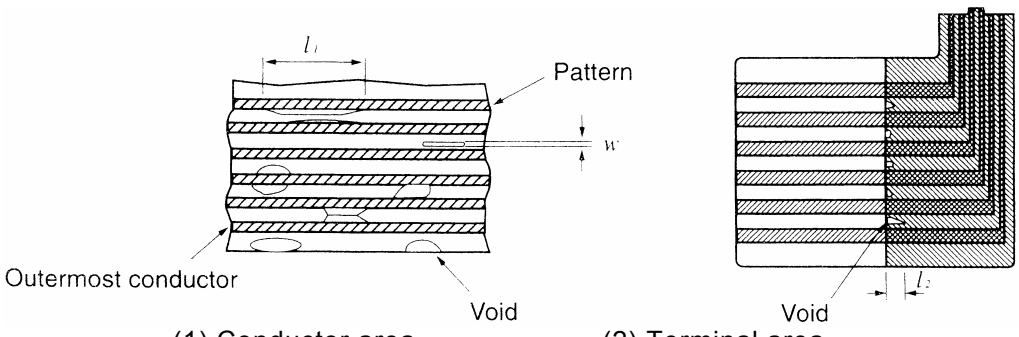
Table 6 – Allowable discoloration

Level	Discoloration
1 and 2	When discoloration is observed on a conductor laminated with coverlay, the discoloration shall be acceptable unless it is remarkably noticeable after conditioning at 40 °C with 90% RH for 96 h
3	The acceptable discoloration shall be agreed upon between user and supplier by means of a limit sample

7.5.2 Visual inspection of coverlay and covercoat

7.5.2.1 Void

Void, as illustrated in Figure 9, shall meet the requirement given in Table 7.



(1) Conductor area (2) Terminal area

Figure 9 – Voids

Table 7 – Allowable void

Level	Voids
1	A void extending over two or more conductors shall not exist. A void both on the outline edge and to a conductor shall not exist. (A void at the terminal area, as illustrated in Figure 9 (2), shall be acceptable even if it extends to two conductors) The maximum length (l_2) of a void shall be 0,3 mm
2	The length of a void (l_1) shall be no longer than 10 mm. The width of a void (w) shall be no longer than one-third of the spacing between the conductors. There shall be no void in a contact extending to two neighbouring conductors. The maximum length ($_2$) of a void shall be 0,3 mm. A void at the repeatedly bending area shall not damage the flexibility of the board
3	There shall be no void

7.5.2.2 Foreign substance

Foreign substance, as illustrated in Figure 10, shall meet the following requirements.

a) **Conductive foreign substance:** Requirements 7.5.1.3 and 7.5.1.4 of this specification shall apply to conductive foreign substances.

b) **Non-conductive foreign substance:** Non-conductive foreign substances shall meet the requirement given in Table 8.

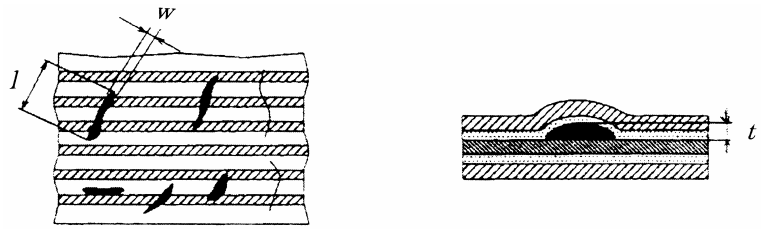


Figure 10 – Foreign substance

Table 8 – Allowable non-conductive foreign substance

Unit: mm

Level	Thickness t	Width w	Length l
Level 1	$t \leqq 0,1$	$w \leqq 0,3$	$l \leqq 3$
Level 2	$t \leqq 0,05$	$w \leqq 0,2$	$l \leqq 2$
Level 3	$t \leqq 0,05$	$w \leqq 0,05$	$l \leqq 1$ A foreign substance shall not extend to three or more conductors

7.5.2.3 Blistering and delamination

There shall be no visible blistering and delamination of coverlay or covercoat along the edge of the FPC, as illustrated in Figure 11. The covercoat shall not be peeled off when using the test tape specified in JIS C 5016, 8.5.1.

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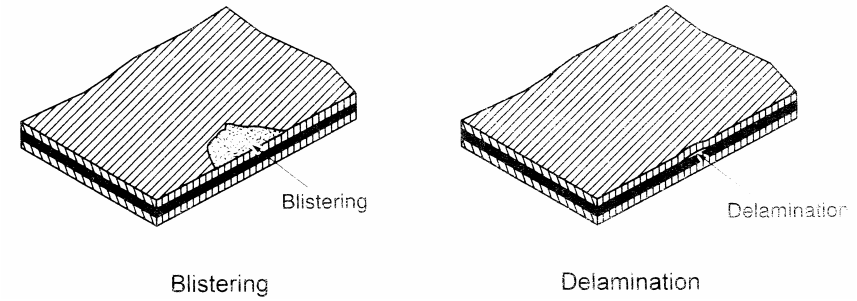
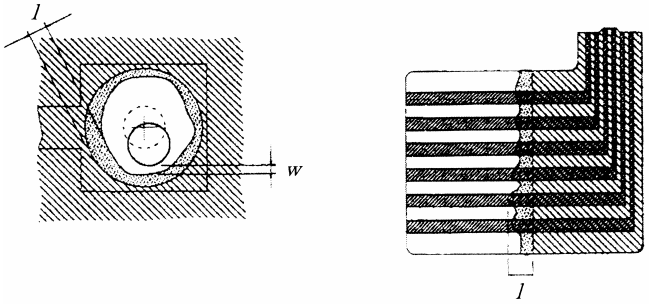


Figure 11 – Lifting and delamination of coverlay and covercoat

7.5.2.4 Squeeze-out of adhesive of coverlay, ooze-out of covercoat and photosensitive register strike

Squeeze-out of adhesive, ooze-out (l) of covercoat and photosensitive register strike, as illustrated in Figure 12, shall comply with the specification given in Table 9.

The squeeze-out and ooze-out at a land as illustrated in Figure 12-1 shall comply with the specification given in Table 10 for the effective land width (w), including possible printing and/or punching errors.



(1) Land area (2) Terminal area

Figure 12 – Allowable squeeze-out of coverlay adhesive and ooze-out of covercoat and photosensitive resist

Table 9 – Allowable squeeze-out of coverlay adhesive, and ooze-out of covercoat and photosensitive register strike

Unit: mm

Level	Squeeze-out of coverlay adhesive and ooze-out of covercoat	Ooze-out of a photosensitive register strike
1 and 2	$l \leqq 0{,}3$	—
3 3	$l \leqq 0{,}2$ $\leqq 0{,}2$	$l \leqq 0{,}1$ $\leqq 0{,}1$

Table 10 – Effective land width at a land

Level	Effective land width, w
1	Squeeze-out/ooze-out contacting the hole edge is acceptable up to one-third of the terminal hole circumference
2	0,05 mm min.
3	0,1 mm min.

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7.5.2.5 Skipping of covercoat photosensitive register strike

When tested in accordance with JIS C 5016, 10.4, no solder shall stick onto the conductor of the covercoat and photoresist in the skipped area.

7.5.3 Visual inspection of plating

7.5.3.1 Plating defect

Plating defect shall meet the requirements given in 7.5.3.1.1 and 7.5.3.1.2.

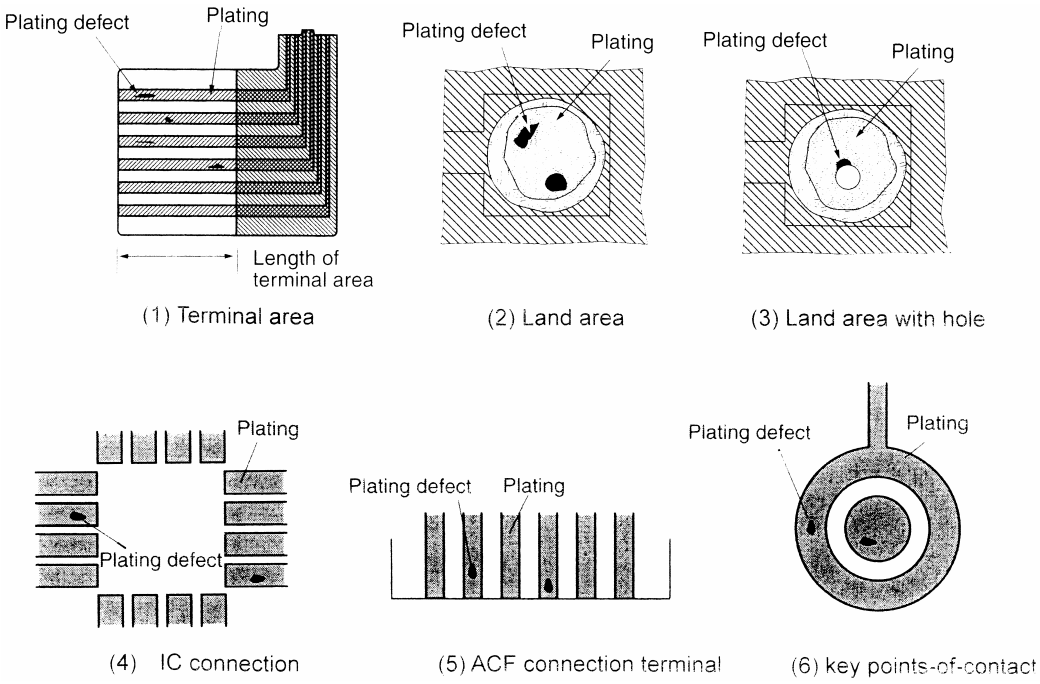

Figure 13 – Plating defects

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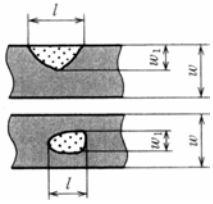
7.5.3.1.1 Gold plating

Gold plating shall meet the requirement given in Table 11.

Table 11 – Gold plating

<table>
<tr><th>Level</th><th>Gold plating</th><th>Examples in Figure 13</th></tr>
<tr><td>1</td><td>Plating defects on the land area, as shown in Figure 13 (2) and (3) shall be no larger than 10 % of the total plated area (excluding the skipped plating area for a defect caused by adhesive squeeze-out)</td><td>(2), (3)</td></tr>
<tr><td>2</td><td>The width (w_1) and length (l) of the plating defects in comparison to the finished line conductor width (w) are specified in the table below
 
Width and length of plating defects
Unit: mm
<table>
<tr><th colspan="2" rowspan="2">Item</th><th colspan="3">Finished line width, w</th></tr>
<tr><th>w < 0,30</th><th>0,30 ≦ w ≦0,45</th><th>0,45 < w</th></tr>
<tr><td rowspan="2">Terminals</td><td>Width of plating defect (w_1)</td><td>w_1 ≦1/2 w</td><td>w_1 ≦0,15</td><td>w_1 ≦1/3 w</td></tr>
<tr><td>Length of plating defect (l)</td><td colspan="3">w_1 ≦w</td></tr>
</table>
There shall be no defect of an area larger than 0,02 mm^2 for a terminal area of a large area such as a key contact</td><td>(1), (5), (6)</td></tr>
<tr><td>3</td><td>There shall be no defect such as poor contact and pit (hole or dent) that can be detected using a magnifying glass of 3× to 10× in the area of direct contact</td><td>(1), (4), (5)</td></tr>
<tr><td>X</td><td>The limit of a defect shall be agreed upon between user and supplier for special requirements</td><td>–</td></tr>
</table>

7.5.3.1.2 Solder plating (solder paste or dip solder plating including use of lead free solder)

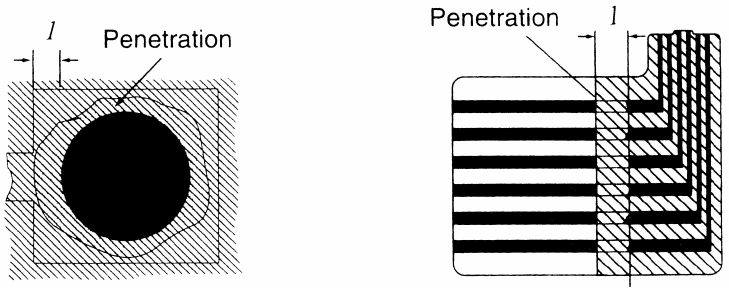
The width of a plating defect at the terminal area, as shown in Figure 13(1), shall be no larger than one-half of the finished conductor width, and the length shall not exceed the width of the conductor.

Plating defects on land area, as shown in Figures 13(2) and (3), shall be less than 10 % of the total plated area (excluding the skipped plating area caused by adhesive squeeze-out).

Plating defects contacting the edge of a component hole, as shown in Figure 13(3), shall be no larger than one-third of the circumference. The area of a plating defect shall be covered with adhesive.

7.5.3.2 Penetration of plated metal or solder plating (Solder paste or dip solder plating including the use of lead free solder)

Penetration of plated metal or solder plating, as illustrated in Figure 14, shall meet the following requirements.



(1) Land area (2) Terminal area

Figure 14 – Penetration of plated metal or solder

a) The penetrated portion (l) between conductor and coverlay (covercoat and photosensitive resist) shall meet the requirement given in Table 12, as illustrated in Figure 14.

Table 12 – Requirement for metal penetration between conductor and coverlay

Unit: mm

Level	Requirement for metal penetration, l
1	$l \leqq 0{,}5$
2	$l \leqq 0{,}3$
3	$l \leqq 0{,}1$

b) The penetrated portion between the conductor and the base film shall meet the requirement given in Table 13.

Table 13 – Requirements for metal penetration between conductor and base film

Level	Requirement for metal penetration
1	Shall meet the requirement of 7.5.1.6
2 and 3	There shall be no visible penetration

7.5.3.3 Surface condition of plated metal and solder plating

7.5.3.3.1 Gold plating

Gold plating shall meet the requirement given in Table 14.

Table 14 – Gold plating

Level	Gold plating
1 and 2	Defect, such as stain, haze, and dirt which can be easily detected by the naked eye without the use of a magnification glass should be judged on the basis of a limit sample
3	There shall be no defect, such as stain, haze, discoloration, and dirt, detectable by observation with a magnification of 10×
X	The special requirement for any specific application shall be agreed upon between user and supplier

7.5.3.3.2 Solder plating (solder paste or dip solder plating including use of lead-free solder)

There shall be no darkened appearance (blackening discoloration).

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7.5.3.3.3 Void in plated through hole

The number of plating voids illustrated in Figure 15 shall be no more than three per hole. The total area of voids for the entire hole wall (S_{sum}) for the total inner wall area of a hole (S_{total}) shall meet the requirement given in Table 15.

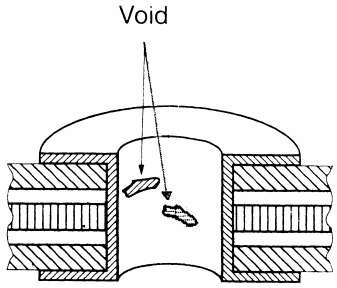

Figure 15 – Plating voids in plated-through hole

Table 15 – Allowable plating voids

Level	Total void area, S_{sum}
1 and 2	S_{sum} < 1/3 S_{total}
3	S_{sum} < 10 S_{total}

7.5.4 Visual inspection of edges of outline and holes

7.5.4.1 Tear and nick

There shall be no tear and nick except for slight cuts formed at the joining of blades which are allowed provided they are not visible without magnification, as illustrated in Figure 16.

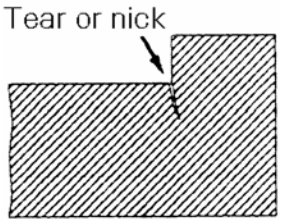

Figure 16 – Tear and nick

7.5.4.2 Burr

The height (h) of burr, as illustrated in Figure 17, shall be no larger than 0,1 mm.

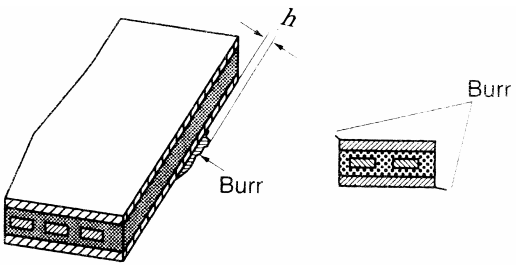

Figure 17 – Burrs

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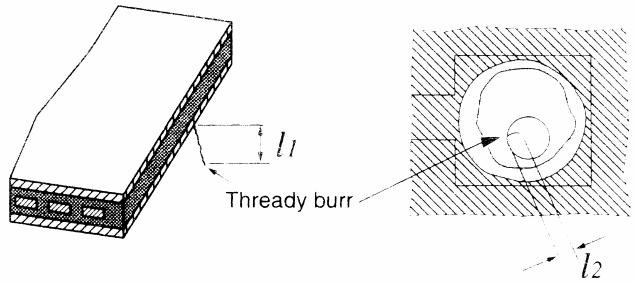
7.5.4.3 Thready burr

Two types of non-conductive thready burrs are illustrated in Figure 18. The length of thready burr at the outline edge (l_1, l_2) shall be no longer than 1,0 mm. The length of burr at the hole edge (l_2) shall be no longer than 0,3 mm.



(1) Thready burr at outline edge (2) Thready burr at hole edge

Figure 18 – Thready burrs

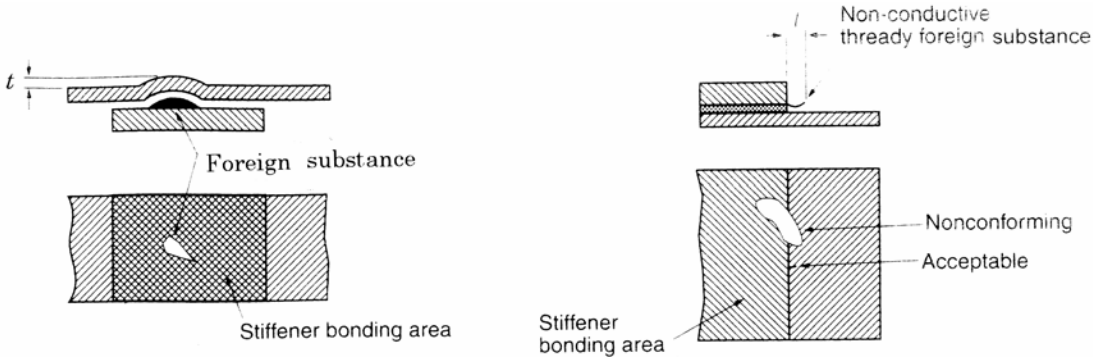
7.5.5 Visual imperfection related to stiffener bonding

7.5.5.1 Foreign substance between flexible printed board and stiffener

The bulge (t) of the FPC caused by a foreign substance sandwiched between the FPC and the stiffener, as illustrated in Figure 19, shall be no larger than 0,1 mm. The thickness of the stiffener shall also meet those specifications when the thickness of the printed board and stiffener are specified.

The size of the foreign substance shall be no larger than 5 % of the bonding area of the printed board and stiffener. There shall be no foreign substance in contact with the component hole or an outline edge of the board.

The length of a non-conductive thready foreign substance (l) protruding from the outline edge shall not exceed 1 mm.

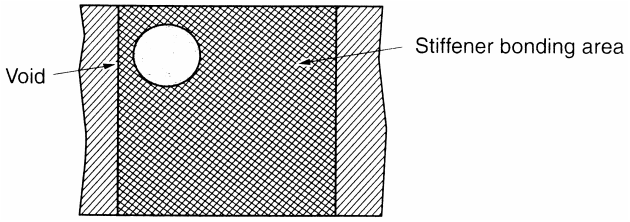


(1) Centre area of stiffener (2) Border area of stiffener

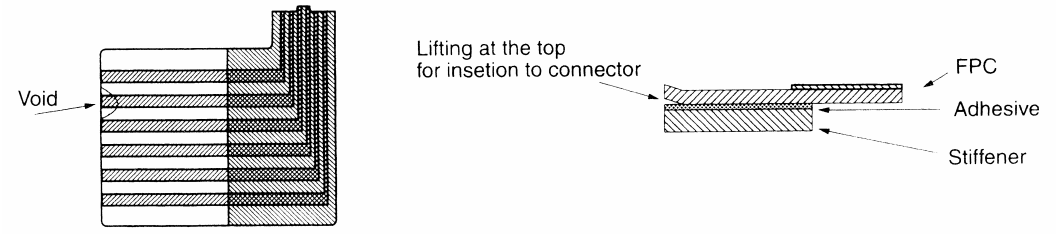
Figure 19 – Foreign substance between board and stiffener

7.5.5.2 Void between flexible printed board and stiffener

When the stiffener is bonded to FPC with thermosetting adhesive, the total area of voids, as illustrated in Figure 22, shall be no larger than 10 % of the total area of the stiffener. When other types of adhesive are used, the total area of voids shall be no larger than one-third of the stiffener area. There shall be no lifting and swelling at the tip for insertion to the connector.



(1) Centre area of stiffener



(2) Terminal area for insertion to connector

Figure 20 – Voids between board and stiffener

7.5.5.3 Defect of stiffener

7.5.5.3.1 Crack

Cracks, as illustrated in Figure 21, shall meet the requirement given in Table 16.

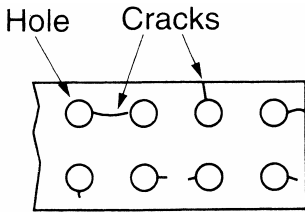


Figure 21 – Cracks

Table 16 – Cracks

Level	Cracks
1	There shall be no crack that could affect practical use
2 and 3	There shall be no crack that links two holes on the stiffener as well as a hole and the outline edge

7.5.5.3.2 Chip-off

The length (l) of a chip-off of stiffener, as illustrated in Figure 22, shall be no larger than 1 mm.

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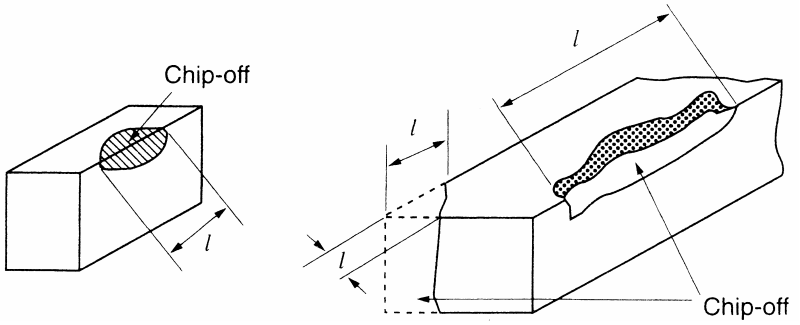

Figure 22 – Chip-off

7.5.5.3.3 Scratch

The allowable scratch shall be agreed upon between user and supplier if necessary.

7.5.5.3.4 Bow and twist

Bow and twist causing no problem in board assembly and instalment are acceptable.

7.5.6 Other visual inspection

7.5.6.1 **Fixed substance on surface** (excluding the area of exposed conductor)

7.5.6.1.1 Thermosetting adhesive

Thermosetting adhesive on the surface shall meet the requirement given in Table 17.

Table 17 – Thermosetting adhesive on surface

Level	Thermosetting adhesive on the surface
1 and 2	Cured adhesive, chip of coverlay, covercoat or fibre stuck with adhesive hardly adhered on the surface is acceptable, provided they do not fall off when rubbed with an applicator impregnated with isopropyl alcohol. The thickness including the adhesive on surface shall meet the requirement where total thickness is specified
3	There shall be no visible substance stuck to the adhesive on the surface

7.5.6.1.2 Flux residues

Flux residue on the surface shall meet the requirement given in Table 18.

Table 18 – Flux residue on surface

Level	Thermosetting adhesive on the surface
1 and 2	When the surface is rubbed with an applicator impregnated with isopropyl alcohol, the applicator shall not be stained with flux residue
3	There shall be no visible flux residue on surface

7.5.6.1.3 Residue of metal powder (solder, aluminum, copper, etc.)

The following requirement shall apply only when the metal powder falling off the board does not cause any problem in the performance of equipment mounted with the flexible printed

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circuit of the interest. The residue of the metal powder shall meet the requirement given in Table 19.

Table 19 – Residue of metal powder (solder, aluminum, copper, etc.)

Level	Residue of metal powder (solder, aluminum, copper, etc.)
1	The acceptable size and the number of metal grains shall be as follows: – for the grain diameter of 0,1 mm or larger and smaller than 0,03mm: 3 or less per product; – for the grain diameter of 0,05 mm or larger and smaller than 0,1mm: 10 or less per product
2	There shall be no visible metal powder residue
3	There shall be no metal powder residue detectable with a magnification 10×

7.5.6.1.4 Residue of adhesive

The residue of the adhesive shall meet the requirement given in Table 20.

Table 20 – Residue of adhesive

Level	Residue of adhesive
1 and 2	The acceptable size and the number of adhesive residue shall be as follows: – for the diameter of 1,0 mm or larger and smaller than 2,0 mm: 1 or less per product; – for the diameter of 0,1 mm or larger and smaller than 1,0 mm: 5 or less per product
2	There shall be no visible adhesive residue

7.5.6.2 Protrusion and dent

Wrinkle, uneven and crease which influence the characteristics on use and on the assembly process of a flexible print board are not permitted, even if there is no problem at the time of mounting and at use. A limit sample for these defects should be prepared if necessary. Examples of protrusions and dents are illustrated in Figure 23.

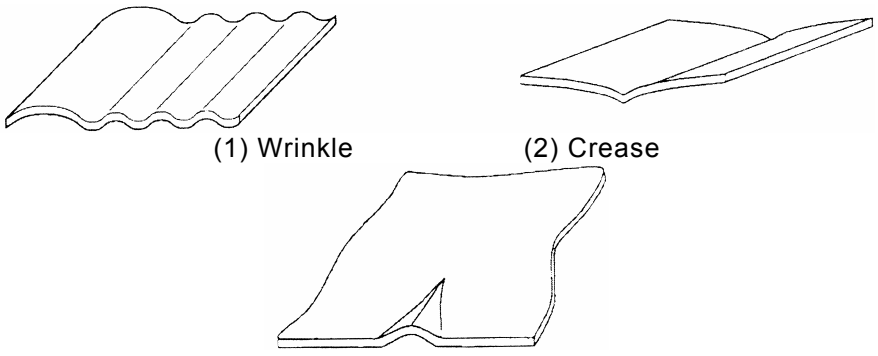

Figure 23 –Protrusion and dent on flexible printed board

7.5.6.3 Bow and twist

Bow, twist and the like, as illustrated in Figure 24, which may influence the characteristics on use and on the assembly process of a flexible print board are permitted if there is no problem at the time of mounting and at use in the field.

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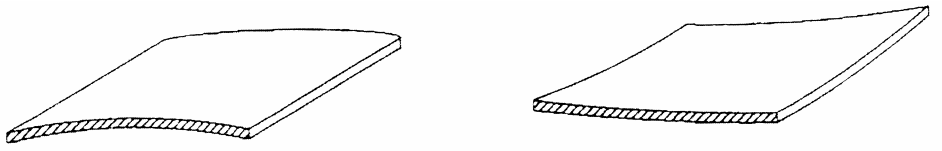

Figure 24 – Bow and twist

7.5.6.4 Conductor

Dent: Dent on a conductor, as illustrated in Figure 25, shall meet the requirement given in Table 21. Dent condition is usually difficult to judge (i.e., shape, size, and depth); accordingly, details should be agreed upon between user and supplier with reference to a limit sample prepared for evaluation.

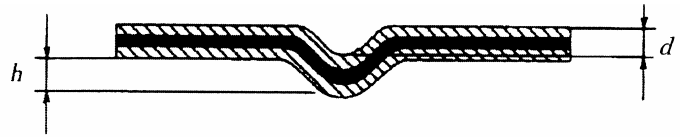

Figure 25 – Dent

Table 21 – Dent

Level	Depth of a dent, d
1 and 2	Depth (d) of a dent from the surface shall be ≦ 0,1 mm. When depth is difficult to measure, the height (h) of the back protrusion of the base film shall be regarded as equal to the depth (d) of a dent
2	There shall be no dent visible from both sides

7.5.6.5 Base film side

a) Dent: Dent on the base film, as illustrated in Figure 25, shall meet the requirement given in Table 22.

Table 22 – Dent

Level	Dent
1 and 2	Depth (d) of a dent from the surface shall be no larger than 0,1 mm. When depth is difficult to measure, the height (h) of the back protrusion of the base film shall be regarded as equal to the depth (d) of a dent
2	There shall be no dent visible from both sides

b) Scratch on base film: The depth (d) of a scratch on a base film relative to the film thickness (t), as illustrated in Figure 26, shall meet the requirement given in Table 23. There shall be no sharp pressed mark, cut, tear, or delaminated adhesive layer. These defects shall not damage the bending property of the repeatedly flexing part.

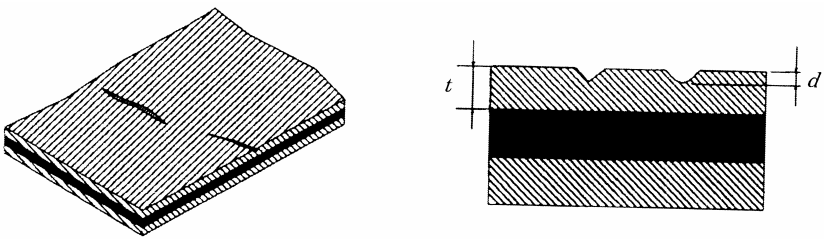

Figure 26 – Scratch on base film

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Table 23 – Allowable scratches on base film

Level	Scratch on base film
1 and 2	$d \leqq 1/3\ t$
3	$d \leqq 1/5\ t$

7.5.6.6 Visual inspection of coverlay and covercoat

a) Dent on coverlay and covercoat: Dents on coverlay and covercoat, as illustrated in Figure 25, shall meet the requirement given in Table 24.

Table 24 – Dents on coverlay and covercoat

Level	Depth of a dent, d
1 and 2	Depth (d) of a dent from the surface shall be no greater than 0,1 mm. When depth is difficult to measure, the height (h) of the back protrusion of the base film shall be regarded as equal to the depth (d) of a dent
3	There shall be no dent visible from both sides

b) Scratch on coverlay and covercoat: The depth (d) of a scratch on the coverlay and covercoat relative to the thickness (t) of coverlay or covercoat, as illustrated in Figure 26, shall meet the requirement given in Table 25. There shall be no sharp pressed mark, cut, tear, or delaminated adhesive layer on the surface of coverlay or covercoat. These defects shall not damage the bending property of the repeatedly flexing portion.

Table 25 – Requirement for scratch on coverlay and covercoat

Level	Depth of a scratch, d
1	There shall be no exposure of conductor.
2	Depth (d) $\leqq 1/3\ t$
3	Depth (d) $\leqq 1/5\ t$

NOTE The thickness of the covercoat should be calculated by subtracting the thickness of the FPC without covercoat from the total FPC thickness.

7.5.6.7 Marking

Marking shall be legible.

8 Dimensional Inspections

8.1 Measurement of dimension

Measuring methods for dimensions of the flexible printed board shall be in accordance with JIS C 5016, Clauses 3, 4 and 5 and 6.3.

8.2 External dimension

Measurement of external dimensions of the FPC shall meet the requirement given in Table 26.

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Table 26 – Tolerance of external dimension

Level	Tolerance of external dimension
1 and 2	Tolerance of the external dimension of product: – for product size smaller than 100 mm in length: ±0,30 mm; – for product size of 100 mm or larger: ±0,3 %
3	Requirement shall be agreed upon between user and supplier

8.3 Thickness

Thickness shall meet the requirements given in Table 27.

Table 27 – Thickness tolerance

Level	Thickness tolerance
1 and 2	≦ ±20 % of the total thickness of the product
3	To be agreed upon between user and supplier

8.4 Hole diameter

Hole diameter shall meet the requirement given in Table 28.

Table 28 – Hole diameter and tolerance

Unit: mm

Thickness, t	Tolerance
0,8 ≦ t	±0,20
0,2 < t < 0,8	±0,10
t ≦ 0,2	±0,05

8.5 Conductor width

Tolerances of the width of the finished conductor for designed conductor width shall meet the requirement given in Table 29.

Table 29 – Conductor width and tolerance

Unit: μm

Designed conductor width, w	Tolerance
w < 50	The requirement shall be agreed upon between user and supplier
50 ≦ w < 100	± 25
100 ≦ w < 200	± 50
200 ≦ w	± 100

8.6 Cumulative pattern pitch

Table 30 gives the cumulative pitch as illustrated in the illustration.

Table 30 – Cumulative pattern pitch and tolerance

	Conductor pitch, P µm	Tolerance of the cumulative conductor pitch %
Level 1	300 ≦ P	± 0,3 %
Level 2	150 ≦ P < 300	± 0,2 %
Level 3	100 ≦ P < 150	± 0,15 %
Level X	P < 100	To be agreed upon between user and supplier

NOTE The length of each component is as follows. Connector: 11,4 mm, IC: 4,8 mm/side, and liquid crystal display: 35,6 mm.

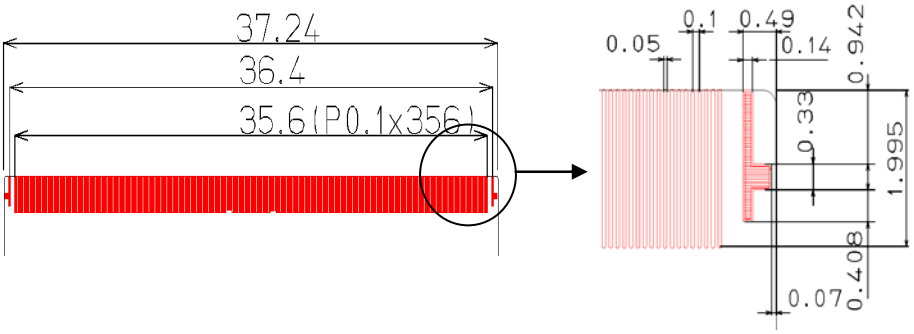

Figure a – ACF connector

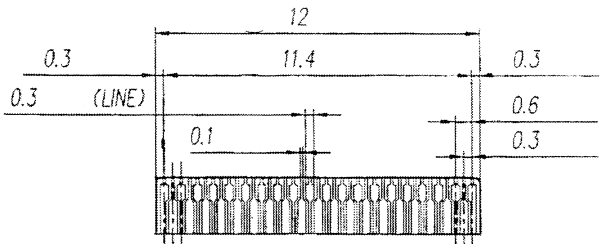

Figure b – Connector terminals

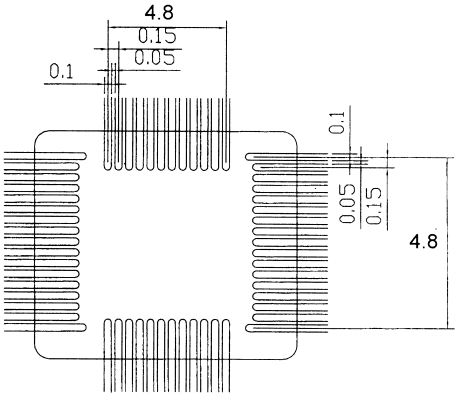

Figure c – COF terminals

Figure 27 – Cumulative pitch

8.7 Distance between hole centres

The distance between hole centres shall meet the requirements given in Table 31.

Table 31 – Tolerance of distance between hole centres

Level	Tolerance of distance between hole centers
1 and 2	For distance < 100 mm: ±0,30 100 mm ≦ for distances: ≦ 0,3 % of the distance between hole centres
3	The requirements shall be agreed upon between user and supplier

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8.8 Design minimum distance between board edge and conductor

Design minimum distance between a board edge and a conductor shall meet the requirement given in Table 32.

Table 32 – Design minimum distance between board edge and conductor

Level	Minimum distance between board edge and conductor
1 and 2	Design minimum distance between the board edge and the conductor shall not be ≦ 0,5 mm
3	The requirements shall be agreed upon between user and supplier

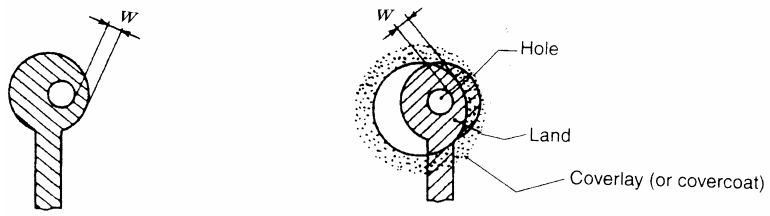
8.9 Position accuracy

8.9.1 Position accuracy of holes

Position tolerance of a finished hole to the design position data shall be no larger than ±0,3 mm for an external dimension of less than 100 mm, and shall be no larger than ±0,3 % for an external dimension of over 100 mm, but except via holes.

8.9.2 Registration of hole to land

The minimum registration accuracy of a solderable finished land width (w), as illustrated in Figure 28, shall comply with the requirement given in Table 10.



a) In the case of without coverlay (or covercoat)

b) In the case of with coverlay (or covercoat)

Figure 28 – Misregistration of hole and land

8.9.3 Registration of coverlay (or covercoat) to a land

The effective land area (S), as illustrated in Figure 29, shall comply with the requirement given in Table 10.

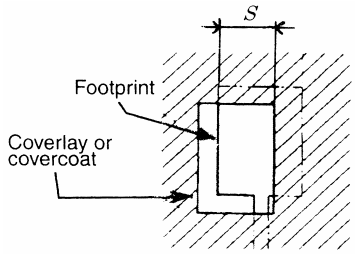


Figure 29 – Misregistration of land and coverlay (or covercoat)

Table 33 – Effective land area

Level	Effective land area, S
1 and 2	Larger than 50 % of the designed land area
3	To be agreed upon between user and supplier

8.9.4 Registration accuracy of stiffener to FPC

8.9.4.1 Hole registration

The deviation (w) between holes of the stiffener and the flexible printed circuit, as illustrated in Figure 30, shall be such that the difference (D-w) between the hole diameter (D) and the displacement (w) shall meet the tolerance requirement for the hole diameter (D).

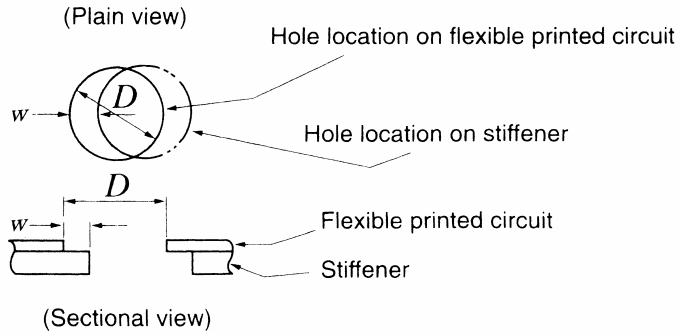


Figure 30 – Registration of holes

8.9.4.2 Displacement of the outer dimensions

The displacement (l) between outer dimensions shall meet the requirements given in Table 34, as illustrated in Figure 31.

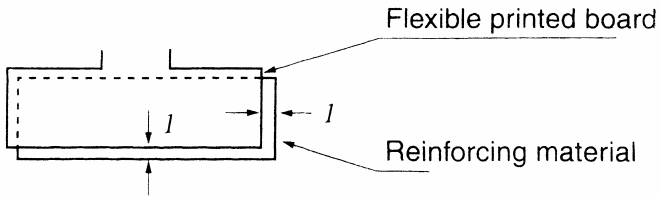


Figure 31 – The displacement of the outer dimensions

Table 34 – Allowable displacement between outlines of the stiffener and the FPC

Unit: mm

Level	Tolerance
1	/ ≦ ± 0,5
2	/ ≦ ± 0,3
3	/ ≦ ± 0,2

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8.9.5 Registration of punched outline to conductor pattern

The registration of punched outline to conductor pattern shall meet the requirement given in Table 35.

Table 35 – Registration of punched outline to conductor patterns

Level	Requirement for registration
1 and 2	The edges of the outline of the board shall not be in contact with conductors, except for plating lead(s), isolated land(s), and conductor(s) for mechanical reinforcement
3	The clearance between the outline edge and the conductor shall be no smaller than 0,1 mm, except for plating lead(s), isolated land(s) and conductor(s) for mechanical reinforcement

8.10 Registration of pressure sensitive or heat activated adhesive (including adhesive squeeze-out) to flexible printed board and stiffener

The displacement (l) of pressure-sensitive or heat-activated adhesives from the FPC and stiffener (including adhesive squeeze-out), as illustrated in Figure 32, shall be ± 0,5 mm. The registration of the adhesive at component holes shall meet the requirement for the tolerance of the hole diameter.

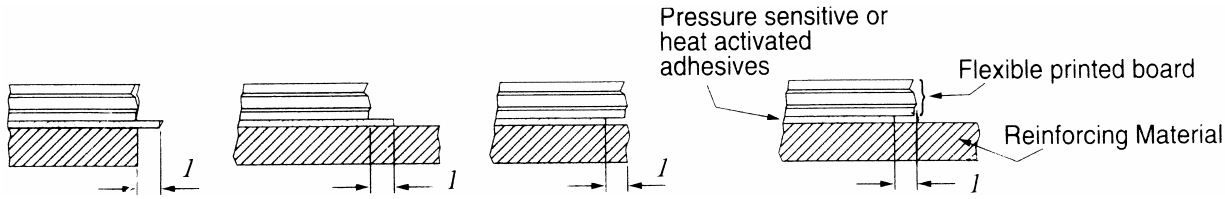

Figure 32 – Registration of pressure-sensitive or heat-activated adhesive from flexible printed board and stiffener (Including adhesive squeeze-out)

8.10.1 Plating thickness of copper plated-through holes

The thickness of the plated copper of the plated-through holes shall be 0,004 mm min.

9 Electrical performance test

The electrical performance of the FPC shall be tested in accordance with JIS C 5016. The test items and requirements are given in Table 36.

Table 36 – Electrical properties of flexible printed boards

Item No.	Item		Requirement	Test method (JIS C 5016)
9.1	Conductor resistance		Shall be agreed upon between user and supplier	7.1 (Conductor resistance)
9.2	Insulation resistance of surface layers	As received	$5 \times 10^8\ \Omega \leqq$	According to 7.6 (Insulation resistance of surface layers)
		After humidity test	Level 1: shall retain the electrical functions. Level 2: $1 \times 10^8\ \Omega \leqq$ Level 3: $5 \times 10^8\ \Omega \leqq$	9.4 (Temperature and humidity cycling test) and according to 7.6
9.3	Dielectric withstanding voltage of surface layers		There shall be no flashover when 500 V a.c. is applied.	7.5 (Dielectric withstanding voltage, surface layers)
9.4	Open circuit of the conductor		1 kΩ*	7.7.2 (Circuit continuity test)
9.5	Short circuit between conductors		$\leqq$ 100 kΩ*	7.7.1 (Circuit isolation test)
* The criteria values for open circuit and short circuit for judging the product performance may not necessarily be these values.				

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10 Mechanical performance test

The mechanical performance of FPCs shall be tested in accordance with JIS C 5016. The test items and specifications are given in Table 37.

Table 37 – Mechanical properties of flexible printed boards

Item No.	Item		Property requirements	Test method (JIS C 5016)
10.1	Peel strength	Conductor	0,49 N/mm ≦	8.1 (Peel strength)
		Coverlay	0,34 N/mm ≦	Specimen with coverlay bonded on the shiny side of the copper foil shall be tested in accordance with 8.1, method B.
		Stiffener	Thermosetting adhesives: 0,34 N/mm Pressure sensitive adhesives: 0,15 N/mm ≦	Specimen with stiffener bonded on the base film shall be tested in accordance with 8.1, method B.
10.2	Pull-out strength for plain hole and footprint		Level 1: Not specified Levels 2 and 3: 1 N/mm^2 ≦	8.2 (Pull-out strength for plain holes) and 8.3 (Pull-out strength for footprints)
10.3	Plating adhesion		There shall be no peel-off	8.4 (Plating adhesion)
10.4	Solderability		The well-wetted area shall be more than 95 % of the total plated area. This does not apply to FPCs with polyester base film	10.4 (Solderability)
10.5	Flexural endurance		FPCs with coverlay shall satisfy the specified bending radius and the bending frequency based on the repetition speed, which are agreed between user and supplier	8.6 (Flexural endurance) The rate of 1 000 cycles/min or higher is preferred to save the testing time
10.6	Bending resistance		FPCs with coverlay shall satisfy the specified bending curvature radius and the loaded bending frequency which are agreed between user and supplier	8.7 (Bending resistance)

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11 Environmental performance

The environmental test of FPCs shall be made in accordance with JIS C 5016. The test items and requirements are given in Table 38.

Table 38 – Environmental tests and requirements

Item No.	Item		Requirement	Test method JIS C 5016
11.1	Temperature cycling		Shall meet the requirements before and after the test for the items and conditions agreed upon between user and supplier	9.1 (Temperature cycling)
11.2	Humidity test	Stationary condition	Same as 11.1	9.5 (Humidity test, stationary condition)
		Temperature/ humidity cycling	Same as 11.1	9.4 (Humidity test, temperature/humidity cycling)
11.3	Thermal shock	High temperature dipping	Same as 11.1	9.3 (Thermal shock, low temperature/high temperature cycling)
		Low temperature/ high temperature cycling	Same as 11.1	9.2 (Thermal shock, low temperature/high temperature cycling)
11.4	Thermal shock resistance of connection between layers (copper plated-through hole, etc.)		The variation in connection resistance between layers (copper plated-through hole, etc.) shall be less than 20 %	10.2 (Thermal shock resistance of copper plated-through holes)
11.5	Migration		$10^8\ \Omega \leqq$	Annex B of this document
11.6	Whisker		To be agreed upon between user and supplier	Annex C of this document

12 Chemical resistance

There shall be no swell or delamination when tested in accordance with JIS C 5016, 10.5. There shall be no appreciable damage of symbol marks.

13 Cleanliness

The measuring method and the requirement shall be agreed upon between user and supplier.

14 Flame resistance

The flame resistance shall be agreed upon between user and supplier.

15 Marking, packaging, and storage

These items should normally be agreed upon between user and supplier. The items in 15.1 and 15.2 are given just as guidelines.

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15.1 Marking on products

a) Product name or product's code name

b) Name of manufacturer or the code name

15.2 Marking on package

a) Product type (name or symbol expressing the FPC shall be marked where it is readily seen)

b) Product name or its code name

c) Number of products in the package

d) Production lot number or year/month of manufacturing

e) Name of manufacturer or its code name

15.3 Packaging and storage

15.3.1 Packaging

Packaging shall meet the requirements given in Table 39.

Table 39 Requirements for packaging

Level	Requirement
1	The product shall be packaged so that it is not damaged during transportation
2	In addition to the requirement for level 1, humidity shall be controlled during storage at room temperature
3	In addition to the requirement for levels 1 and 2, any requirement agreed upon by user and supplier shall be incorporated

15.3.2 Storage

FPCs shall be stored in a storage that is equipped with suitable humidity control.

15.3.3 Handling

Annex A gives the recommendation for preventing accidents caused by the handling of FPCs by customer.

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Annex A

Handling instruction manual handling of polyimide-base FPC

A.1 Storage and handling

Wipe off moisture and/or chemical substance(s) attached to the product surface during storage and/or handling. These substances may cause discoloration and/or deterioration of the product.

The tarnish protection coating on the conductor is valid for approximately six months after production in a storage where temperature and humidity are controlled, whereas the plated and cream-solder-coated surface is valid for approximately one year.

In addition to the precautions to prevent mechanical damage to the boards caused by careless handling or stacking of boards, it is very important to protect boards against contamination by foreign substances. Oil component may be transferred from human skin to a board causing contamination, stain or discoloration when the board is handled for test or installation to an automatic processing machine. Hand cream containing silicone can cause poor adhesion of photoresist and coverlay layers.

Protection gloves shall be used to prevent contamination.

Periodical change of gloves should be observed. Generation of minute fibre dust from the gloves should be checked.

A.2 Component mounting and installation to equipment

Torque to tighten screws and caulk metal plates shall be appropriately adjusted. Too high a torque may break materials.

A.3 Soldering

A.3.1 Pre-treatment

Polyimide used as a base film of FPCs and as a coverlay absorbs moisture easily (i.e., the simple film will be saturated with water vapour in approximately 4 h if a polyimide film is left in the open air). This may readily cause blistering of the FPC by a rapid temperature change when soldering is carried out using a reflow furnace or flow soldering equipment. Pre-drying of the FPC to remove absorbed moisture should be added as a pre-treatment process before the assembly process.

Depending on the composition of the FPC, the following pre-drying conditions are recommended as given in Table A.1.

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Table A.1 – Recommended pre-drying conditions

FPC	Pattern composition	Stiffener material	Pre-drying temperature	Drying time
Single-sided	Fine patterns only (such as signal lines)	None	80 °C	30 min ≦
		Film	80 °C	1 h ≦
		Glass/epoxy board, etc.	120 °C	1 h ≦
Double-sided	Fine patterns only (such as signal lines)	None	80 °C	30 min ≦
		Film	80 °C	1 h ≦
		Glass/epoxy board, etc.	120 °C	1 h ≦
	With wide patterns (such as ground lines)	None	120 °C	30 min ≦
		Film	120 °C	1 h ≦
		Glass/epoxy board, etc.	120 °C	2 h ≦

A different drying time depending on the composition of the FPC or patterns results in a different moisture removal time from polyimide and/or adhesive layers. Pre-dried FPCs, when left in a normal environment storage (air-conditioned room), should be soldered within the same day after being taken out of storage. If soldering is to be carried out the following day, the FPC should be kept in a moisture-tight bag. The boards should be kept in the bag with silica gel, which can extend the allowable time for soldering to approximately one month (the period may vary depending on the type of bag and the amount of silica gel used). One or more hours of pre-drying should be added if manual soldering or flow soldering is made to the FPC one or more days after reflowing.

A.3.2 Soldering

When the soldering temperature is too high or soldering time is too long, separation or blistering of the FPC may occur. The land may separate if the FPC is bent or pressed too much by a soldering iron while heated. Suitable soldering conditions which are appropriate to the circuit pattern and the working location shall be selected.

Care should be taken to avoid burning while soldering. Protection gear, such as goggles, should be worn to prevent burning by scattered fine solder balls and flux.

A.4 Disposal

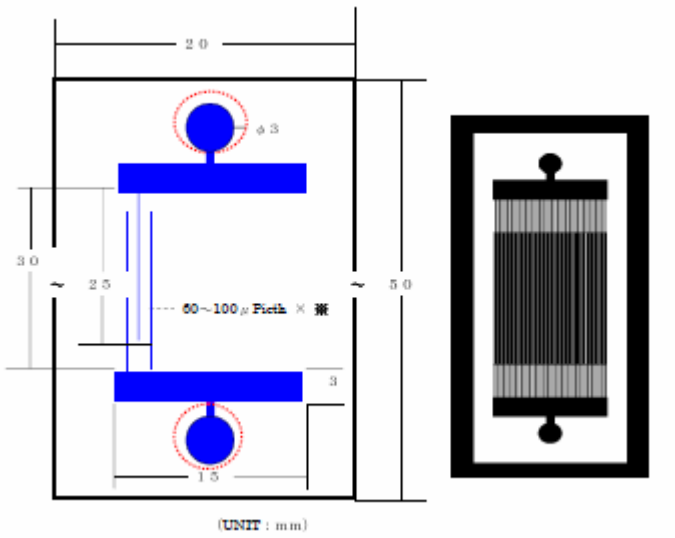
Disposal shall be carried out according to the specified procedure of disposing industrial wastes. No incineration, use of the waste for land fill, or dumping in the sea without permission should be carried out.

A.5 Adoption and switching to lead-free solder plating

When the present tin-lead solder is changed to lead-free solder for plating, short circuit and/or generation of foreign substances may occur due to whisker growth. The whisker growth on a component is affected by various factors including the material, shape and strain to the component. Careful study is needed of the actual FPC. It is necessary to use gold plating or an organic anticorrosion surface layer on the FPC if the whisker generation is strictly prohibited for reasons of reliability.

Annex B

Ion migration test

Item	Ion migration test for flexible wiring boards	
Specimen	The structure of the specimen shall be as illustrated in Figure B.1 with the details of the specimen as given below: – the material of the specimen shall be the same as that of the product to be evaluated including coverlay and covercoat; – the number of interdigits of the pattern is 75; – the line/space of the specimen shall be between 60/60 to 100/100 µm and shall be agreed upon between user and supplier; – the number of specimens to be tested shall be from 1 to 10 and be agreed upon between user and supplier.  NOTE Dotted circles indicate the openings of coverlay and covercoat. **Figure B.1 – Structure of specimen for ion migration test.**	
Test condition	• Temperature/humidity : 85 °C/85 % • Applied voltage : 15 V or 50 V d.c. , and to be agreed upon between user and supplier • Duration: 250 h, 500 h, or 1 000 h, and to be agreed upon between user and supplier	
Test equipment	The test equipment shall be capable of maintaining a temperature of 85 °C ± 2 °C and RH of 85 % ± 3 % The insulation resistance shall be measured using an insulation tester	
Conditioning	Not specified	
Measurement	Measure the insulation resistance of a specimen using the circuit described in 7.7.1 of JIS C 5016 with an applied voltage of either 15 V or 50 V d.c.	

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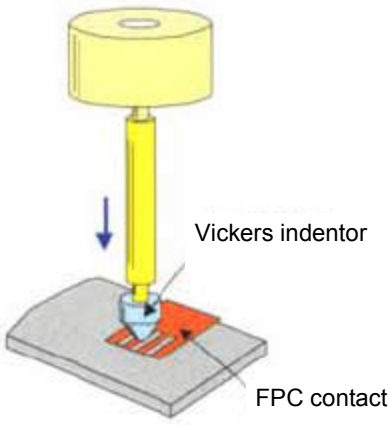
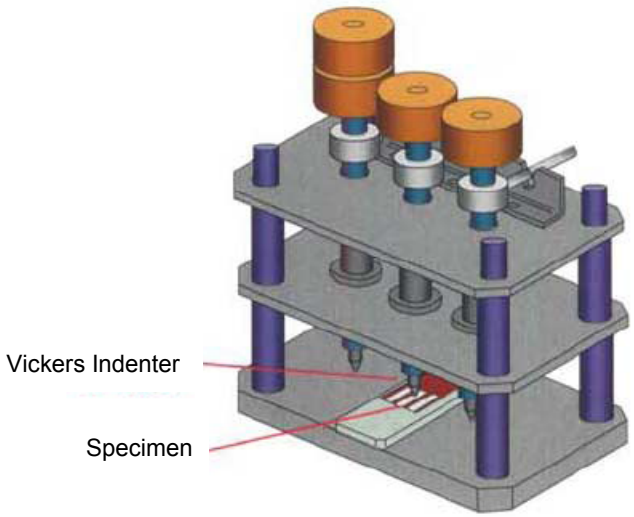
Annex C

Whisker test

Item	Whisker test for flexible printed wiring board (FPC) with an applied mechanical external stress (JPCA - YAMAICHI method)	
Specimen	The specimen is the contact section of FPC used as a mail of a connector and to be agreed upon between user and supplier The recommended number of specimens, N = 5	
Equipment	The structure of the whisker test equipment is as illustrated in Figures C.1 and C.2 An SEM (or a metallurgical microscope) (magnification of x100 or higher should be used  **Figure C.1 – The basic structure of the test equipment**  【JPCA-YAMAICHI method】 **Figure C.2 – An example of the construction of the test equipment**	

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Test condition	Temperature: Room temperature, 25 °C ± 5 °C Humidity: RH of : 55 & ± 30 % Weight: 200 g ± 10 g Test time: A recommended test time of 96 h for the first step. The time may be extended as agreed upon between user and supplier
Evaluation	Count the number of whiskers with a length of more than 50 µm using an SEM The number of whiskers shorter than 50 µm shall be agreed upon between user and supplier
Remarks	• This test is not for a quantitative and absolute test but a qualitative and relative test for whisker growth • Care should be taken that the vibration should not disturb the test. • It is desirable to perform this whisker growth test without using stiffener and/or adhesive as the whisker growth may be affected by the presence of these materials • It is also be regarded that the time required to start whisker growth may differ for a board using tin plating with the thickness and the process of tin plating employed • It shall be confirmed that the tip of the Vickers indenter is clean and free of dust • It is recommended to do an insertion test of a flexible board to a mail connector for whisker growth • Whisker growth tests under internal stresses induced by temperature humidity and/or thermal shock environmental tests may be necessary in addition to the whisker-growth test under external stress as described in this document to elucidate the whisker growth mechanism
Notes	• This test method was developed by Yamaichi Electric Works. This test method was carefully studied by the Standardization Committee of JPCA for Flexible Printed Circuit Boards and is adopted in this PAS • See the report made by Fujino of Yamaichi Electric presented at the 19th Annual Meeting of the Japan Electronics Packaging Association, March 2005

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Annex D

Additional information

Explanation of JPCA performance guide for single- and double-sided flexible printed wiring boards

This explanation does not constitute a part of this specification but should help the readers understand what is written in the text and the related issues.

I. Path to completion of this document

In 1992, JPCA prepared JPCA-FC03 to establish the requirements for the external appearance of the FPC which had not been specified before. The purpose of that standard was

- to specify the most common external appearance;
- to avoid unnecessary disputes caused by difference of concepts between the user and supplier on the external appearance of FPCs;
- to improve cost performance;
- to further advance the technology of FPCs;
- to fulfil expectations of consumers.

The contents of JPCA-FC03 was superseded by JIS C 5017 which was released in 1994.

The JPCA performance guide manual prepared at this time can be considered as a proposal for an IEC standard. At the drafting stage, we adopted the style of IEC 60326-7 and IEC 60326-8, and also referred to IPC standards, particularly IPC-FC-250A. The overall constitution of this standard, therefore, followed that of the IEC standards. The most difficult item was the ‘‘classification.’’ There was no idea of ‘‘classification’’ in JPCA-FC03 and JIS C 5017, whereas the concept of ‘‘classification’’ was essential for an IEC standard. The classification in conventional standards, including IPC documents, was based on the characteristics of the printed boards, and the classification was assigned uniquely to all the items of the printed board. This assignment of classes sometimes induces a situation that a board requires a rather high class for just part of the board for a special function, even though most of the board can perform its functions with material of a regular class requirement and does not need such a high class.

In the present document, the term ‘‘class’’ has been changed to “level’’, which is based on the levels of required performance only. A product may require, in principle, either Level 1, Level 2 or Level 3, while for some specification items a different level can also be assigned from a practical standpoint. This may be different from the usual concept of a standard; therefore, we decided to name this document a ‘‘performance guide manual’’ so that a level can be applied flexibly

JPCA-DG02-1997 (1st ed.) was also published as a joint standard by IPC as IPC/JPCA 4202 and then published as an IEC document, IEC/PAS 62133. The original JPCA-DG-02 was revised in 2004 as the 2nd edition. Flexible printed wiring boards (FPWB) have been widely used especially in cellular phones and hard-disc drives these days. Use of the fine pattern circuit, wire bonding and anisotropic conductive film (ACF) is also a common practice in the industry. It was necessary to revise the 1st edition to cope with the advanced technology. The JPCA FPC Committee had revised the document in 2004. This document is further revised as the 3rd edition of the document including the cumulative pattern pitch, and the test methods for ion migration and for whiskers are added in the annexes.

It was necessary for the industry to prepare a 3rd edition of the document by including the contents of the document published in February 2006 in the present 3rd edition of the

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document, also taking into account of the cumulative conductor pitch. Test methods for migration and whisker growth on FPC were also to be added.

The joint standard preparation of this document with IPC is not planned at this time as a frequent revision may be necessary for the industry, especially in Asian countries where most of the production is made around the world. It is considered instead to submit this information to IEC as a PAS for early dissemination of the information the industry needs.

The Japanese Government had adopted in 1995 the policy of harmonizing the JIS (Japan Industrial Standards) to ISO and IEC standards, basically translation of the ISO/IEC documents. JIS C-5017 is not a direct translation of the corresponding IEC document but the present IEC document was published years before and does not reflect the present-day technology. We need to use the present JIS C-5017 for the time being and need to wait for the revision of the IEC document by IEC/TC 91. TC 91 has a plan to revise the old documents on board materials based on proposals from national committees reflecting the present-day technology in the industry.

In view of these considerations, the present document, the 3rd edition of JPCA-DG-02, is named as the performance guide for single- and double-sided flexible printed wiring boards.

II. Supplementary explanation on each specification (item numbers being those in the text)

5 Performance level: Classification of specification and application of performance levels

Since the FPC is one type of printed board, the classification of specification items of this performance guide in the first edition (1997) was prepared in accordance with the IEC standards for printed boards. The classification of boards was drafted in harmony with the conventional JIS standards and with future international standards.

FPCs for various applications require different performance, and a specific application of a printed board often requires a higher level of performance.

FPC used for an application where the board is subject to repeated bending sometimes requires a special specification, such as: “There shall be no dents and nicks in the flexing portion.”. Some other examples of special requirements and applications for FPCs include

– dimensional accuracy (for fine circuit patterns for fine connections);
– flexural performance (for applications such as mobile phones, digital versatile disc, hard disc drives, floppy disc drives, printers, and others in which flex boards are repeatedly bent);
– cleanliness (contamination issue in hard discs);
– surface treatment (FPCs for COF).

The FPC is unique in its overall dependency in quality (reliability) and cost-on specific requirements/applications as seen from the above items. FPC cannot have only one specific ”level”, as each specification may require its own ”level”. We can select a specific requirement with a certain ”level” different from other portions of the same FPC to use it for a different application.

7.5.1.2 Nicks and pinholes on conductors

These are used to judge whether the FPC can be used without any trouble in its function (for example, at the time of component mounting and/or soldering). We added requirements for defects on lands in the first edition (1997) as problems were found in operation in the field,

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and requirements have been specified. The value of 10 % used in the specification is the most common value, which has been used in agreement between user and supplier.

7.5.1.4 Unnecessary copper between conductor/spur and nodule of conductor in an open area

We added requirements for this item in the first edition (1997), as these were the phenomena often observed. An open area is described as the space more than 0,375 mm wide. The maximum value of 0,125 mm is specified for the spacing assuming the electrical properties are not affected by this value.

7.5.2.2 Foreign substance

A non-conductive foreign substance is assumed never to cross over three conductors in the conventional specification, whereas the assumption is no more practical for a dense pattern currently used. We changed the specification to the sizes of foreign substances from the first edition (1997).

7.5.3.1.1 Gold plating

We added examples of plating errors, such as at COF and ACF connections and key contacts, and allowances specified as Levels 2 and 3.

15 Cleanliness

Non-volatile residues (NVR), organic silicone compounds, and ion contamination (including chlorine) are the new problems for hard-disc drives (HDDs) and COF applications. The user and supplier should agree to carry out analyses based on FTIR and ion chromatography.

17.3.2 Storage

Pre-drying conditions after storage were clearly indicated to maintain the heat resistance in soldering.

Additional remarks to Annexes

Annex 2 Ion migration

An ion migration test is requested in many cases of FPC especially for fine-pattern applications. A test method is provided in this document using a reasonably narrow interdigital pattern of a conductor spacing of less than 100 µm.

Annex 3 Whisker growth test

A whisker-growth test method for FPC developed by Yamaichi Electric Work is included in this document.

On the adoption of lead-free solders and the time of switching from lead-based to lead-free solders, tin-based metal plating is commonly used to replace plating of lead-tin solder to conductors in flexible boards by most of FPC manufacturers. The tin-based metal plating used as a surface treatment of a conductor brings a serious technical problem of the whisker growth on flexible boards with the possibility of short circuit between neighbouring conductors when the length of a whisker exceeds a critical length. It is now fairly well known that the whisker growth becomes significant when a stress is applied to the plated tin-based metal. It is an urgent issue to develop a reliable whisker-growth test method to estimate the possibility of operation failure of products using flexible boards. The JEITA (Japan Electronics and Information Technology Industries Association) has been extensively working to develop a whisker-growth test method on leads of components and joints on boards. JPCA is also studying whisker growth, especially on flexible boards.

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Tin-copper plating is widely used in the FPC industry for tin-based metal plating. It is known that whisker growth is affected by the induced internal stress, the thickness of Sn and other metal plating, the materials and thickness of stiffeners used, types and thickness of adhesive, and actual conditions of reflow process. At this date, it has not yet been decided to suppress whisker growth completely as whisker growth seems based on one of the distinct properties of tin. Some means are being studied for the suppression of whisker growth by various FPC manufacturers, such as annealing to relax internal stress generated in plated metal films, or reflow soldering, but no sure-cure method has been found. Whisker growth is not completely understood yet. There are reports that nodules were grown even on tin-lead plated film. FPC manufacturers do understand now that the suppression of whisker growth is very difficult, though it may not be impossible as tin-based metal is used for plating.

We added a paragraph to this edition of the design guide to call the attention of those involved in the FPC industry to whisker growth.

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