DRAFT FOR DEVELOPMENT

DD IEC/PAS
62050:2004

Board level drop test method of components for handheld electronic products

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Summary of pages

This document comprises a front cover, an inside front cover, the IEC PAS title page, a blank page, pages i and ii, pages 1 to 14, an inside back cover and a back cover.

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS

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Draft PAS	**Report on voting**
47/1753/NP	47/1791/RVN

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BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS

Introduction

The handheld electronic products fit into the consumer and portable market segments. Included in the handheld electronic products are cameras, calculators, cell phones, pagers, palm size PCs, Personal Computer Memory Card International Association (PCMCIA) cards, smart cards, mobile phones, personal digital assistants (PDAs) and other electronic products that can be conveniently stored in a pocket and used while held in user's hand.

These handheld electronic products are more prone to being dropped during their useful service life because of their size and weight. This dropping event can not only cause mechanical failures in the housing of the device but also create electrical failures in the printed circuit board (PCB) assemblies mounted inside the housing due to transfer of energy through PCB supports. The electrical failures may result from various failure modes such as cracking of circuit board, trace cracking on the board, cracking of solder interconnections between the components and the board, and the component cracks. The primary driver of these failures is excessive flexing of circuit board due to input acceleration to the board created from dropping the handheld electronic product. This flexing of the board causes relative motion between the board and the components mounted on it, resulting in component, interconnects, or board failures. The failure is a strong function of the combination of the board design, construction, material, thickness, and surface finish; interconnect material and standoff height; and component size.

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BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS

(From JEDEC Board Ballot JCB-03-38, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices)

1 Scope

The Board Level Drop Test Method is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. The purpose is to standardize the test board and test methodology to provide a reproducible assessment of the drop test performance of surface mounted components while duplicating the failure modes normally observed during product level test.

The purpose of this document is to prescribe a standardized test method and reporting procedure. This is not a component qualification test and is not meant to replace any system level drop test that maybe needed to qualify a specific handheld electronic product. The standard is not meant to cover the drop test required to simulate shipping and handling related shock of electronic components or PCB assemblies. These requirements are already addressed in JESD22-B104-B and JESD22-B110. The method is applicable to both area-array and perimeter-leaded surface mounted packages.

Correlation between test and field conditions is not yet fully established. Consequently, the test procedure is presently more appropriate for relative component performance than for use as a pass/fail criterion. Rather, results should be used to augment existing data or establish baseline for potential investigative efforts in package/board technologies.

The comparability between different test sites, data acquisition methods, and board manufacturers has not been fully demonstrated by existing data. As a result, if the data are to be used for direct comparison of component performance, matching study must first be performed to prove that the data are in fact comparable across different test sites and test conditions.

This method is not intended to substitute for full characterization testing, which might incorporate substantially larger sample sizes and increased number of drops. Due to limited sample size and number of drops specified here, it is possible that enough failure data may not be generated in every case to perform full statistical analysis.

2 Apparatus

As per JESD22-B104-B and JESDD22-B110

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3 Terms and definitions

For purposes of this standard, the following definitions shall apply

component: A packaged semiconductor device.

single-sided PCB assembly: A printed circuit board assembly with components mounted on only one side of the board

double-sided PCB assembly: A printed circuit board assembly with components mounted on top and bottom sides of the board.

handheld electronic product: A product that can conveniently be stored in a pocket (of sufficient size) and used when held in user's hand.

NOTE Included in handheld electronic products are cameras, calculators, cell phones, pagers, palm-size PCs (formerly called 'pocket organizers'), Personal Computer Memory Card International Association (PCMCIA) cards, smart cards, mobile phones, personal digital assistants (PDAs), and other communication devices.

peak acceleration: The maximum acceleration during the dynamic motion of the test apparatus.

pulse duration; acceleration interval: The time interval between the instant when the acceleration first reaches 10% of its specified peak level and the instant when the acceleration first returns to 10% of the specified peak level after having reach that peak level.

table drop height: The free-fall drop height of the drop table needed to attain the prescribed peak acceleration and pulse duration.

event: An electrical discontinuity of resistance greater than 1000 ohms lasting for 1 microsecond or longer.

event detector: A continuity test instrument capable of detecting electrical discontinuity of resistance greater than 1000 ohms lasting for 1 microsecond or longer.

4 Applicable documents

JESD22-B104-B, *Mechanical Shock*
JESD22-B110, *Subassembly Mechanical Shock*
IPC-SMT-782, *Surface Mount Design and Land Pattern Standard*
IPC-A-600, *Acceptability of Printed Boards*
J-STD-020, *Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices*
J-STD-033, *Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*
IPC-9701, *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*

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5 Test Components and Board

5.1 Components

This standard covers all area arrays and perimeter-leaded surface-mountable packaged semiconductor devices such as BGAs, LGAs, CSPs, TSOPs, and QFNs typically used in handheld electronic product. Since components with body sizes larger than 15 mm x 15 mm in size are not used in these applications, the maximum size of the component body covered in this standard is 15 mm x 15 mm. All components used for this testing must be daisy-chained. The daisy chain should either be done at the die level or by providing daisy chain links at the lead-frame or substrate level. In case of non-daisy chain die, a mechanical dummy die must be used inside the package to simulate the actual structure of the package. The die size and thickness should be similar to the functional die size to be used in application. The component materials, dimensions, and assembly processes shall be representative of typical production device.

5.2 Test board

Since the drop test performance is a function of the test board used for evaluation, this standard defines a preferred test board construction, dimensions, and material that is representative of those used in handheld electronic products. If another board construction/material better represents a specific application, the test board construction, dimensions and material should be documented. The test data generated using such a board shall be correlated at least once by generating the same data on same component using the preferred board defined in this document.

5.2.1 Preferred board construction, material, and design

The preferred test board shall use built-up multilayer technology incorporating microvias using 1+6+1 stack-up. This is required as typical PCB assemblies used in handheld electronic systems are constructed using high density, buildup technology. The test board shall have a nominal thickness of 1.0 mm. Table 1 provides the thickness, copper coverage, and the material for each layer. The dielectric materials shall meet the mechanical properties requirements as given in Table 2. The PCB shall have Organic Solderability Preservatives (OSP) as surface finish to avoid any copper oxidation before component mounting. The glass transition temperature, Tg, of each dielectric material as well as of the composite board shall be 125 ^{o}C or greater. The modulus and Tg of the dielectric materials shall be specified. The composite values (Modulus, and Tg) shall be measured on at least one representative test board at component mounting location. The boards shall be symmetric in construction about the mid-plane of the board, except for the minor differences in the top and bottom two layers.

Since a typical product board may have a combination of microvia in pad and no vias in pad for area array packages for routing purposes, it is required that such components (BGAs, CSPs, etc) be tested on board with both microvia and non-microvia PCB pads. This shall be accomplished by designing double sided boards with mirror component footprint on each side (top and bottom) of the board. The board Side A shall have microvias in pads (“via in pad”) on all component mounting pads while the board Side B shall have no microvias in pads (“no via in pads”). For board Side A, the microvias in pads shall be created with laser ablation with via diameter of 110 microns. The vias shall then be plated resulting in straight or near straight walls. The capture pad diameter shall be at least 220 microns. Although two sided boards are to be designed, the component shall only be mounted on one side at a time, resulting in two single sided assemblies (“Side A assembly” and “Side B assembly”), unless the component is anticipated for use in mirror-sided board assemblies. In that case, the components shall be mounted on each side of the board.

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5.2 Test board (cont'd)

5.2.1 Preferred board construction, material, and design)cont'd)

As perimeter-leaded devices do not typically require microvia in pad, the test board for such devices (TSOP, QFP, etc) does not need to include microvias. The board shall still be designed as double-sided with footprint of similar sized components on each side.

Although daisy-chain nets will typically not require plated though holes (PTH) other than those required for manual probe pads and connectors, the test board shall contain PTH in the component region (1.2X the area covered by component) to approximate mechanical effect of vias on actual application boards. There shall be 20 plated through holes per square centimeter in the component region. The actual location and distribution of plated through holes will depend on component size and I/O. The through holes shall have the drill diameter of 300 microns and finished plated hole diameter of 250 microns. The PTH pad diameters shall be 550 microns for the outer layer and 600 microns for the inner layers.

It is recommended that the component mounting pads on the PCB be designed as per the specification in Table 3 for area array devices. The pad design for leaded and perimeter I/O devices shall be according to IPC-SM-782 guidelines. All component attachment pads shall be non-solder-mask-defined (NSMD) with solder mask clearance of 75 microns between the edge of the pad and the edge of solder mask. Smaller clearance can be used as long as it does not cause any solder mask encroachment on pads due to mis-registration. Solder mask registration tolerance shall not exceed 50 microns

Table 1 — Test board stack-up and material

Board Layer	Thickness (microns)	Copper Coverage (%)	Material
Solder Mask	20		LPI
Layer 1	35	Pads + traces	Copper
Dielectric 1-2	65		RCC*
Layer 2	35	40% including daisy chain links	Copper
Dielectric 2-3	130		FR4†
Layer 3	18	70%	Copper
Dielectric 3-4	130		FR4†
Layer 4	18	70%	Copper
Dielectric 4-5	130		FR4†
Layer 5	18	70%	Copper
Dielectric 5-6	130		FR4†
Layer 6	18	70%	Copper
Dielectric 6-7	130		FR4†
Layer7	35	40%	Copper
Dielectric 7-8	65		RCC*
Layer 8	35	Pads + Traces + daisy chain links	Copper
Solder Mask	20		LPI

* Suggested RCC Material: Polyclad PCL-CF-400 12/35/35
† Suggested FR4 Material: NELCO N-4000-6 or equivalent

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5.2 Test board (cont'd)

5.2.1 Preferred board construction, material, and design)cont'd)

Table 2 — Mechanical property requirements for dielectric materials

Property	Unit	FR4	RCC
Tensile Strength	MPa	>100	>50
Tensile Modulus	GPa	20 ± 2	2 ± 1
Tensile Elongation	%	>3	>3
In-plane CTE (below Tg)	ppm/°C	15 ± 2	60-80
Tg	°C	>130	>130
Cu Peel	kgf/cm	>1	>1

Table 3 — Recommended test board pad sizes and solder mask openings

Component I/O Pitch (mm)	PCB Pad Diameter (mm)	Solder Mask Opening (mm)
0.50	0.28	0.43
0.65	0.30	0.45
0.75/0.80	0.35	0.50
1.00	0.45	0.60

The trace widths on the suggested test board shall be 75 microns within the component area. This includes all traces making contact with solder joint interconnect as well as all internal layers. A trace width of 100 microns shall be used for all traces outside of component region. The board shall have matching daisy chain pattern such that one or multiple nets are formed through all interconnects after component mounting. Wherever necessary, additional test points within each net shall be incorporated for failure location identification. Each additional test point shall be clearly labeled using row column format of the package. All routing and traces within and just outside the component footprint shall be done on layer 2 and layer 8 for area array packages and layer 1 and layer 8 for perimeter leaded packages.

The suggested test board shall have component mounting features such as Pin 1 identification and global/local fiducials.

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5.2 Test board (cont'd)

5.2.1 Preferred board construction, material, and design (cont'd)

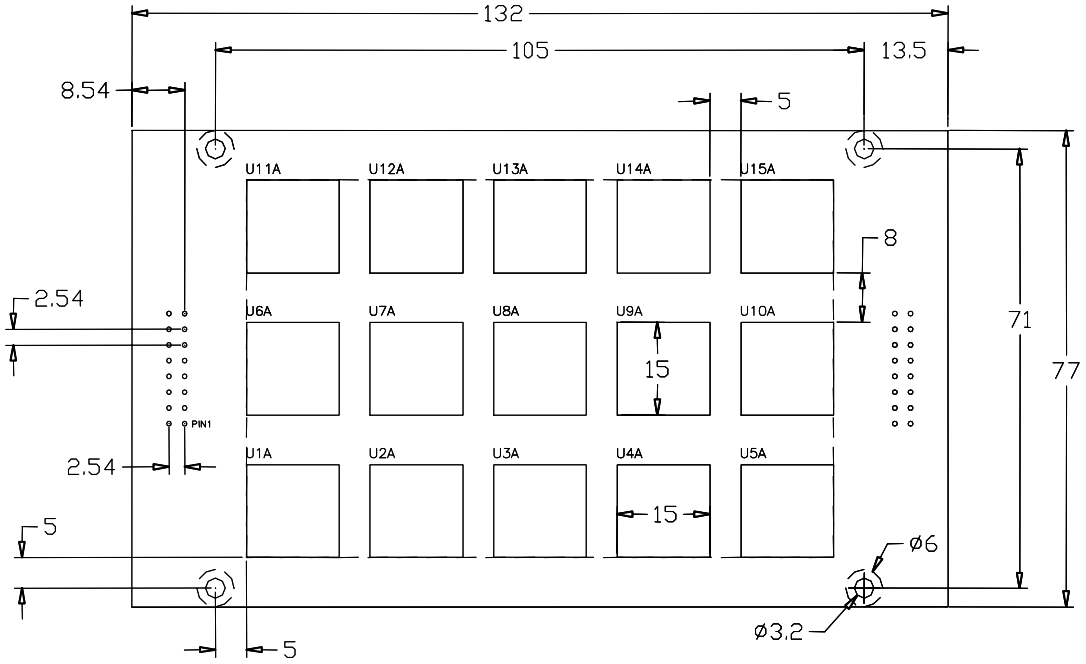

Figure 1 — Test board size and layout

Table 4 — X, Y locations for components' center (Center of lower left screw hole as datum)

Component ID	X location of component center (mm)	Y location of component center (mm)
U1	5 + CompX/2	5 + CompY/2
U2	28.75 + CompX/4	5 + CompY/2
U3	52.5	5 + CompY/2
U4	76.25 - CompX/4	5 + CompY/2
U5	100 - CompX/2	5 + CompY/2
U6	5 + CompX/2	35.5
U7	28.75 + CompX/4	35.5
U8	52.5	35.5
U9	76.25 - CompX/4	35.5
U10	100 - CompX/2	35.5
U11	5 + CompX/2	66 - CompY/2
U12	28.75 + CompX/4	66 - CompY/2
U13	52.5	66 - CompY/2
U14	76.25 - CompX/4	66 - CompY/2
U15	100 - CompX/2	66 - CompY/2
CompX & CompY: Component length and width.		

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5.2 Test board (cont'd)

5.2.2 Preferred test board size, layout, and component locations

The board footprint and layout is shown in Figure 1. The overall board size shall be 132 mm X 77 mm that can accommodate up to 15 components of same type in a 3 row by 5 column format. The maximum component size shall be 15 mm in length or width and there shall be at least 5 and 8 mm gap between the components in x- and y-direction, respectively. All 15 sites on each side of the board (top and bottom) shall have the same component footprint. A "common" footprint for multiple components can also be used if daisy chain requirements, as specified in section 6.2, are met. For example, a 9 x 9 pad array can be designed to accommodate suitably designed daisy chain components with 8 x 8, 7 x 7, 8 x 9, or any other ball array combination. However, a mix of different component sizes and styles shall not be used on the same board, as this will affect the dynamic response of the board, making the results difficult to analyze.

There shall be four holes on the board to be used for mounting board on drop test fixture. The locations of these holes are shown in Figure 1. All components must be located within the 95 mm X 61 mm box (shown by the dashed line in Figure 1) defined by the outer edges of all outer components. The outer edges of out side components (U1 through U6 and U10 through U15) shall align with the boundary of this box, guaranteeing a fixed diagonal distance of (4 mm} between the outside of screw head and component's corner closest to the screw head (components U1, U3, U5, U11, U13, and U15) irrespective of component size. The x, y location of the center of each component location is listed in Table 4, using the center of lower left screw hole as datum.

The area of the board in the length direction outside of components shall be restricted for labeling, through holes, edge fingers, and any other fixtures, if needed. Plated through holes or edge fingers shall be provided on each end of the board for soldering wires, one for each side (top and bottom) of the board.

5.3 Test board assembly

Prior to board assembly, all devices shall be inspected for missing balls or bent leads. Board thickness, warpage, and pad sizes shall also be measured using a sampling plan. A visual inspection shall be performed on all boards for solder mask registration, contamination, and daisy chain connection. It is recommended that boards should be inspected and accepted as per IPC-A-600, Class 3 acceptability criteria. One board shall also be used to measure the mechanical properties (modulus, and Tg) of the board at the component location using DMA and TMA method. It is highly recommended that the CTE of the board be also measured in X, Y, and Z direction. The mechanical property measurements are not required for every board lot, unless the fab process, material, or vendor is changed from lot to lot.

The components shall be baked according to J-STD-020 and J-STD-033 prior to board assembly. .

The test boards shall be assembled using best known methods of printed circuit assembly process, representative of production methods. At least one board shall be used to adjust board mounting process such as paste printing, placement, and reflow profile.

All assemblies shall be single side only unless the component is anticipated for use in mirror-sided board assemblies. In that case, the components shall be mounted on each side of the board.

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5.3 Test board assembly (cont'd)

A 100% X-ray inspection is recommended on assembled units to check for voids, shorts, and other abnormalities. Electrical continuity test shall also be performed on all mounted units to detect any opens or shorts.

5.4 Number of Components and Sample Size

The above board design allows up to 15 locations for component mounting and it is preferred that components be mounted on all 15 locations. Since the drop performance is a function of component location on the board, testing with components mounted on all 15 locations will provide useful information to the users of this data (OEMs) in proper layout of their product board. With board supported at 4 corners these locations cover worst case board curvature (U8 location), effect of proximity to support locations (U1, U5, U11, & U15), and various locations in-between.

Because of various design for test and design for failure analysis practices used in the industry, it is recognized that populating boards with all 15 locations may not leave enough room between components for large number of test points to properly identify the exact failure location. Therefore, options are provided for mounting just 1 or 5 components on the board using the following locations:

- 1-component configurations: Location U8
- 5-component configurations: Locations U2, U4, U8, U12, & U14

Table 5 — Quantity of test board and components required for testing

Number of components per board	Number of boards		Total number of components
	Side A Assembly (via in pad)	Side B Assembly (No via in pad)	
15	4	4	120
5	4	4	40
1	10	10	20

Since the number and size of may influence the dynamic response of the test board assembly during drop the components mounted on the board, it is required that additional data be provided whenever these 1-component or 5-component configuration is employed. The additional data shall directly compare the effect of optional component mounting (1 or 5 components) to the preferred 15-component mounting configuration. This comparison shall be provided for a component similar in size (within 20% in both length and width) to the component, which has been tested using 1- or 5-component per board configuration only.

Depending on the number of components mounted per board, Table 5 shall be used to determine the minimum quantity of assembled board required for testing and total number of components to be tested. Sample sizes greater than specified below can be used to generate statistically sufficient data.

In case of rectangular components, the longer side of the component should be parallel to the longer side of the board when mounted.

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6 Test procedure

This test method is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. This test method is not meant to address the drop test methods required to simulate shipping and handling related shock of electronic subassemblies. These requirements are addressed in JESD22-B110.

6.1 Test equipment and parameters

The shock testing apparatus shall be mounted on a sturdy laboratory table or equivalent base and leveled before use. Means shall be provided in the apparatus (such as automatic braking mechanism) to eliminate bounce and to prevent multiple shocks to the board. Figure 3 shows the typical drop test apparatus where the drop table travels down on guide rods and strikes the rigid fixture. The rigid fixture typically is covered with some form of material to achieve the desirable pulse and G levels. The bottom of the drop table is usually rounded slightly to ensure very small area of contact with the strike surface.

A base plate with standoffs (6 mm OD / 3.2 mm ID, 10 mm long) shall be rigidly mounted on the drop table. The thickness and mounting locations of the base plate shall be selected such there is no relative movement between the drop table and any part of base plate during drop testing. This plate will serve as the mounting structure for the PCB assemblies. This is pictorially shown in Figure 3. The PCB assembly shall be mounted to the base plate standoffs using 4 screws, one at each corner of the board. The board shall be mounted using four #4-40 precision shoulder screws (McMaster Carr Part # 91829A511). Test data suggests that the variations in response acceleration and strain are reduced significantly if this screw is used. Since the length of shoulder is 3.175 mm nominal, a number of washers should be placed between the screw head and the top surface of the board (nominal 1.0 mm thick) to avoid any gap between the top of the standoffs and the bottom surface of the board. Due to tolerance stack up, a small gap is still possible but this gap shall not exceed 50 microns. The use of shoulder screw eliminates the need to re-tighten screws between drops. The screws shall be tightened in diagonal pattern in the order of SW, NE, SE, and NW corners of the board. The screw shall be tightened until the shoulder of the screw bottoms out against the standoff. The number of washers used shall be the same for all four screws.

Experience with different board orientation has suggested that the horizontal board orientation with components facing down results in maximum PCB flexure and, thus, the worst orientation for failures. Therefore, this standard requires that the board shall be horizontal in orientation with components facing in downward direction during the test. Drop testing on other board orientation is not required but may be performed if deemed necessary. However, this is an additional test option and not a replacement for testing in required orientation.

This document requires JEDEC Condition B (1500 Gs, 0.5 millisecond duration, half-sine pulse), as listed in JESD22-B110 Table 1 or in JESD22-B104-B Table 1, as the input shock pulse to the printed circuit assembly. This is the applied shock pulse to the base plate and shall be measured by accelerometer mounted at the center of base plate or close to the support posts for the board. Other shock conditions, such as Condition H (2900 Gs, 0.3 millisecond duration), in addition to the required condition can also be used.

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6 Test procedure (cont'd)

6.2 Pre-test characterization

A set-up board with components mounted on it shall be used to adjust and characterize drop test parameters and board response. A lightweight accelerometer (such as Endevco model 22, 0.14 gram) should be attached with Beeswax on top of component located at position U8 to characterize the output acceleration response of the PCB assembly. It should be noted, however, that any additional mass will add significant dynamic weight to the board and may alter its dynamic response. Therefore, it is recommended that this characterization should only be done on a set-up board. In addition, a 45^0 rectangular rosette strain gage shall be mounted on this set-up board underneath position U8 on the other side (non-component) side of the board to characterize strains in x and y directions as well as the principal strain and principal strain angle. Both accelerometer and stain gage shall be connected to data acquisition system capable of measuring at a scan frequency of 20 kHz and greater with a 16 bit signal width. Additional strain gages may also be mounted at different locations on the board to fully characterize the strain response of the assembly. The board assembly shall then be mounted on the drop test fixture using four screws. The screws shall be tightened in diagonal pattern in the order of SW, NE, SE, and NW corners of the board. Additional accelerometer may also be mounted on the board assembly at or close to one of the support locations to ensure that the input pulse to the base plate is transmitted to the PCB without any distortion. The drop table shall then be raised to the height specified according to JEDEC condition and dropped on the strike surface while measuring the G level, pulse duration, and pulse shape. Multiple drops maybe required while adjusting the drop height and strike surface to achieve the specified G levels and pulse duration (1500 Gs, 0.5 millisecond half-sine pulse). It should be noted that the peak acceleration and the pulse duration is a function of not only the drop height but also the strike surface. Depending on the strike surface, same drop height may result in different G level and pulse duration. Theoretically, the drop height needed to achieve the appropriate G levels can be determined by equation below where H is the drop height and C is the rebound co-efficient (1.0 for no rebound, 2.0 for full rebound). However, this equation does not include the strike surface effect. Experiments with different strike surface may be needed to achieve the desired peak value and duration.

$$A(t) = A_o \sin\left(\frac{\pi t}{t_w}\right)$$

$$\sqrt{2gH} = \frac{2A_o}{C}\frac{t_w}{\pi}$$

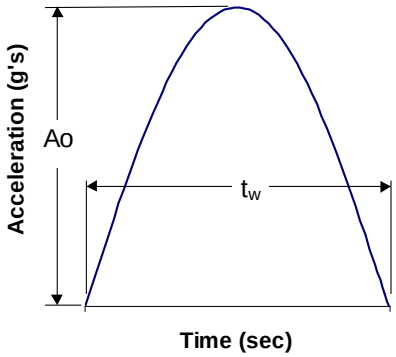

Figure 2 — Typical shock test ½ sin pulse graphic and formulas

Once the specified drop parameters (G Level, duration, and pulse shape) are achieved, the PCB response acceleration and strain shall be measured. Strain rate shall also be calculated by dividing the change in strain value by the time interval during which this change occurred. The characterized board response (acceleration, strain, and strain rate) and its variation shall be documented and provided with the test data. Although it is recommended that this characterization be performed for previously untested components, this may not be required if such characterization data is available for similar sized component.

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6 Test procedure (cont'd)

6.3 Drop testing

With test parameters adjusted and PCB response characterized, the PCB assemblies shall be prepared for drop testing. This involves soldering cables to the plated though holes on one end of the board, mounting board on the drop fixture with component facing down, and connecting cables to the event detector/data logger. Since the dynamic response of the board may be affected by the mass and stiffening of the connector, it is recommended that no connectors are used and wires are directly soldered to the board. The event detector's threshold resistance shall be set to no more than 1000 ohms. Proper strain relief should also be provided to cables/wires to avoid a failure at wires to board interconnects. All cables shall be cleared from the drop path. The initial resistance of all nets for each assembly shall be measured and logged before conducting the first drop. The drop test shall be conducted by releasing the drop table from the pre-established height. The electrical resistance of each net shall be measured in-situ during each drop and all failures shall be logged. The board shall be dropped a maximum of 30 times or until 80% of all devices have failed, whichever is earlier. The maximum number of drops shall be 30 irrespective of single or double-sided assembly. In the event that shock condition in addition to the required Condition B is used to conduct the test, the maximum number of drops shall be determined using the acceleration factor between the two conditions for similar sized components. This acceleration factor shall be reported with the test data.

During the test, the shock pulse shall be measured for each drop to ensure that input pulse remains within the specified tolerance. Adjustments in drop height or replacement of strike surface may be needed if the pulse deviates from the specified.

Depending on number of components per board, Table 5 shall be used to determine the number of boards to be tested per component type.

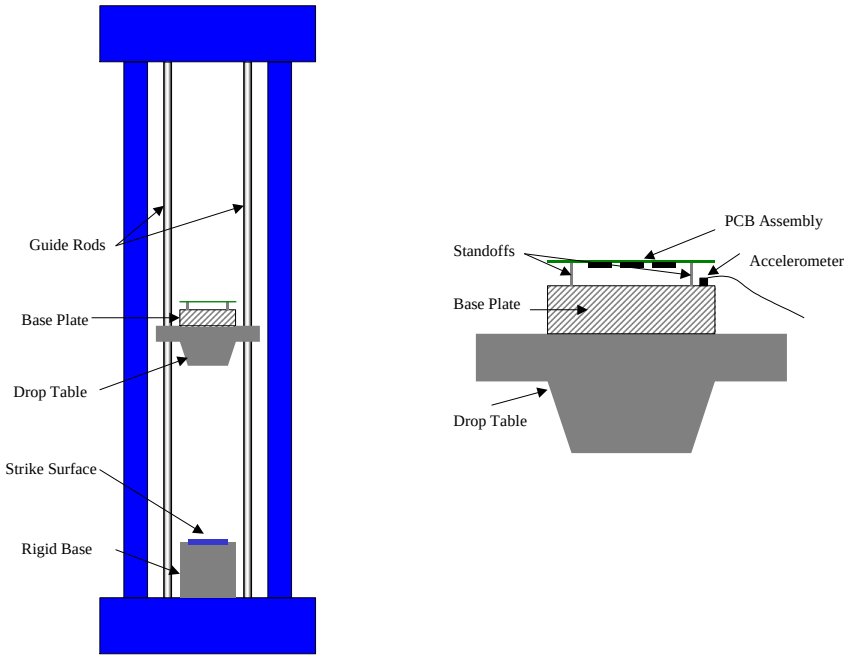

Figure 3 — Typical drop test apparatus and mounting scheme for PCB assembly

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7 Failure criteria and failure analysis

In-situ electrical monitoring of daisy chain nets for failure is required during each drop. The electrical continuity of all nets should either be detected by an event detector or by a high-speed data acquisition system. The event detector should be able to detect any intermittent discontinuity of resistance greater than 1000 ohms lasting for 1 microsecond or longer. The high-speed data acquisition system should be able to measure resistance with a sampling rate of 50,000 samples per second or greater.

Depending on the monitoring system used, the failure is defined as follows:

- event detector: The first event of intermittent discontinuity as defined above followed by 3 additional such events during 5 subsequent drops.

- high speed data acquisition: The first indication of resistance value of 100 ohms or 20% increase in resistance from the initial resistance if initial resistance is greater than 85 ohms followed by 3 additional such indications during 5 subsequent drops.

A visible partial separation of component from the test board, even without a significant increase in resistance or intermittent discontinuity, shall also be considered as a failure. This can occur if the PCB traces come off the board with component while maintaining electrical continuity.

As wires soldered to the board for electrical continuity test may also come off during the test, it is highly recommended that all electrical connections be checked once a failure in indicated to ensure that the failure is due to component to board interconnection failure.

All failures after each drop shall be logged. A total of 5 packages from the test lot shall be subjected to failure analysis to determine the root cause and to identify failure mechanism. The selection of packages should cover different locations on the board. Different methods and equipment, such as visual inspection, cross-section, dye and pry, chemical etching, SEM, and SAT can be employed to determine the root cause of failure. The failure site shall be clearly identified as “component failure”, “interconnect failure”, or “board failure”. For the purpose of this document, the “interconnect failure” is defined as any failure at a) package pad – joint interface or intermetallics, b) through joint material, and c) PCB pad-joint interface or intermetallics.

8 Reporting

All test reports shall include the following information:

- Package and PCB assembly weight
- Package geometrical details including body size, I/O, ball size, layer thickness, and die size
- Package materials including mold compound, die attach, substrate
- Board geometry, material, and material properties such as thickness, pad size, modulus, and Tg
- Board assembly details including stencil thickness, apertures, stencil material, solder alloy & paste, reflow profile, and other board assembly process details.
- Test details: drop height, strike surface, shock pulse profile

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8 Reporting (cont'd)

- Board response (Acceleration, strain, and strain rate)
- Initial resistance of daisy chain nets
- Failure detection equipment and failure criteria
- Test results including the number of drops to failure for each location on each test board, failure mechanisms, and representative pictures.
- Data analysis showing mean and standard deviation of failure data according to component groupings. Weibull and /or lognormal analysis result should also be included if sufficient quantities have failed for such analyses. Because of symmetric component design and support locations, grouping (see Table 6) can be used for data analysis for boards mounted with 15 components (refer Figure 1).

Table 6 — Component locations for test boards

Group	Number of components in the group	Component locations on the board	Sample size	
			Side A Assembly	Side B Assembly
A	4	U1, U5, U11, & U15	8	8
B	4	U2, U4, U12, & U14	8	8
C	2	U6 & U10	4	4
D	2	U7 & U9	4	4
E*	2	U3 & U13	4	4
F*	1	U8	2	2

Failure data for components in Group E and F can also be combined into one group as the PCB curvature underneath these components is expected to be very similar during the fundamental mode of vibration, as shown in the Figure 4 below. The fundamental mode results in maximum displacements and is typically most damaging. Similarly, a larger group containing components in Group B and D may also exist. It is recommended to first analyze the component reliability data at individual locations without assuming any grouping. The failure data can only be pooled together when they have been proved to be statistically equivalent.

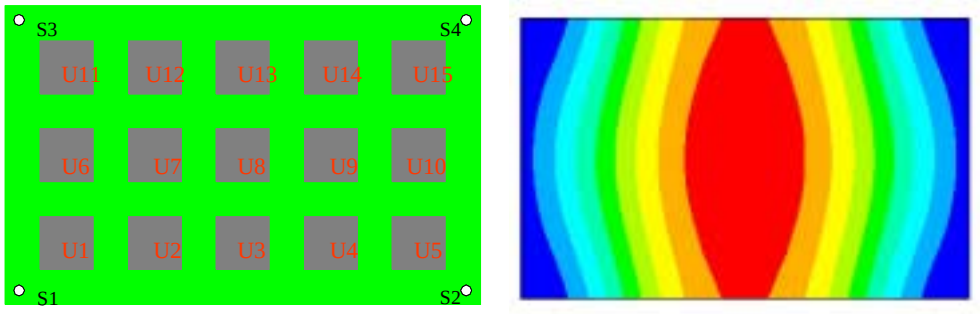

Figure 4 — Fundamental mode of vibration of PCB supported with four screws

For the cases where component design is not symmetric about X and Y-axis, the above grouping may not work. This may require additional boards to be tested to achieve the sample sizes given above.

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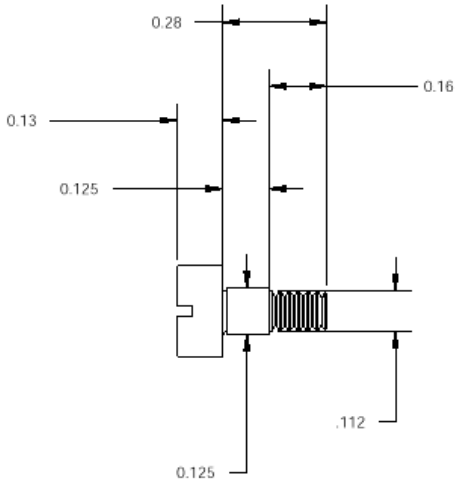
Annex A (informative) Recommended Testing Hardware

Table A.1 — Recommended hardware to mount PCB on the base plate

Standoff	Screws
Part # 91075A431*	Part #: 91829A511*
System of Measurement: Inches	Precision Shoulder
Outside Diameter: 0.25”	System of Measurement: Inches
Screw Size: #4-40	Thread: #4-40
18-8 Stainless Steel	Thread Length: 5/32”
Shape: Hex	18-8 Stainless Steel
Body Length: 3/8”	Shoulder length = 0.125”
	Head Diameter: 0.25”
	Slotted Head
	
* All part numbers are from McMaster Carr Catalog	

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