Specification for

Processor system bus interface (Eurobus A)

Committees responsible for this British Standard

The preparation of this British Standard was entrusted by the Office and Information Standards Committee (OIS/-) to Technical Committee OIS/13 upon which the following bodies were represented:

British Gas Corporation
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Business Equipment Trade Association
Central Computer and Telecommunications Agency
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Electricity Supply Industry in England and Wales
Electronic Engineering Association
Institute of Measurement and Control
Ministry of Defence
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Contents

Foreword

This British Standard was published under the direction of the Office and Information Standards Committee. It is based on the Eurobus A specification, published by the Ministry of Defence as Defence Standard 00-20, and specifies the same interface.

The text of this standard is under consideration by the International Organization for Standardization (ISO) with a view to publication as ISO 6951.

For ease of production, Figure 1 to Figure 20 have been reproduced from Ministry of Defence Standard 00-20, with alterations to Figure 2, Figure 5 and Figure 18, with the permission of the Ministry of Defence. Certain conventions are not identical to those used in British Standards.

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Summary of pages

This document comprises a front cover, an inside front cover, pages i to iv, pages 1 to 70, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

0 Introduction

0.1 General. This standard specifies the set of signal lines that constitute the bus itself, and the interfacing of devices connected to the bus.

This standard specifies protocols for the allocation of bus time to devices wishing to make transfers and for the transfer of data between devices. The standard does not, however, specify priority rules, these being left to be formulated individually for each system.

This standard specifies a full set of signalling rules to be followed by the device responsible for bus allocation and by devices conducting transfers. Appendix F gives illustrative examples of each of the possible types of transfer.

The set of electrical and signal timing requirements specified in clause **6** uniquely defines the interface that is Eurobus A. Certain mechanical requirements are specified in clause **6**, namely those that directly affect the electrical characteristics (e.g. the physical length of the bus, the spacing of device connectors on the bus, the pin pitch on connectors and the signal disposition on the connectors), but this standard does not further specify the mechanical implementation. An example of a possible mechanical implementation of Eurobus A is given in Appendix J.

Implementations of Eurobus A are possible with 8, 16, 24, 32,.... -bit data widths and devices having different data widths can operate on the same bus. Logical implementation summaries for the first four of the possible data widths are given in Appendix A to Appendix D. Appendix E specifies the connector allocation.

The group of signal lines constituting an assembled Eurobus A provides the means for the transfer of binary digital information between up to 20 devices plugged into the backplane of a single equipment shelf. Devices share the bus on a time-division multiplex basis. The length of the backplane is limited to a maximum of 460 mm. The signal lines form an asynchronous unbalanced voltage interface capable of operating at transfer rates of up to 6.5×10^6 words or bytes per second.

0.2 Data width and addressing capability. The data/address width of any device using the bus is theoretically unconstrained. However, the asynchronous protocols and addressing facilities of Eurobus A permit devices of 8, 16, 24 and 32-bit data widths to share the same bus, and when the bus is so shared, the maximum data width is that of the widest device.

The full addressing capability of the bus enables devices to address any 8-bit byte of any word in a normal address space defined by both of the following.

    a) The addressing range determined by the number of data/address bits.

    b) A two-bit extension to the foregoing a). The full two-bit extension is available on buses with non-shared width, but on shared-width buses the use of these bits is restricted.

In addition, any complete word can be addressed in a second address space of equal magnitude to the first, designated the pseudo address space.

0.3 Devices. Free choice is available to the system designer as to the devices connected to a Eurobus and the order in which they are connected. However, each bus needs to include both:

    a) an arbiter, the purpose of which is to control the time-division multiplexing of transfers on the bus;

    b) if communication with other buses if required, a bus link to each of the other buses.

Figure 1 shows an example of a bus with a number of typical devices including an arbiter and a bus link.

0.4 Bus allocation. Information is transferred between devices on a master-and-slave basis. A device bids for control of the bus by means of its starred Request line and becomes the master device for that transfer after the arbiter has allocated the bus to it. This standard specifies the protocols by which devices bid for use of the bus and by which the arbiter allocates the use of the bus to one of them. The standard does not, however, specify the algorithm used in making the selection, thus the system designer is given the choice of an allocation algorithm in order to optimize system performance.

The protocol whereby a master device may flag an interrupt to the arbiter is also specified, but the subsequent action by the arbiter is left to the system designer to define.

0.5 Bus transfers. In addition to specifying the protocols for the execution of Read cycles (in which the master addresses a device as slave and reads data from it) and Write cycles (in which the master transfers data to the addressed slave), this standard also specifies the protocol for a Vector cycle in which an address, without data, is transferred from master to slave.

Figure 1 — Eurobus with some typical devices
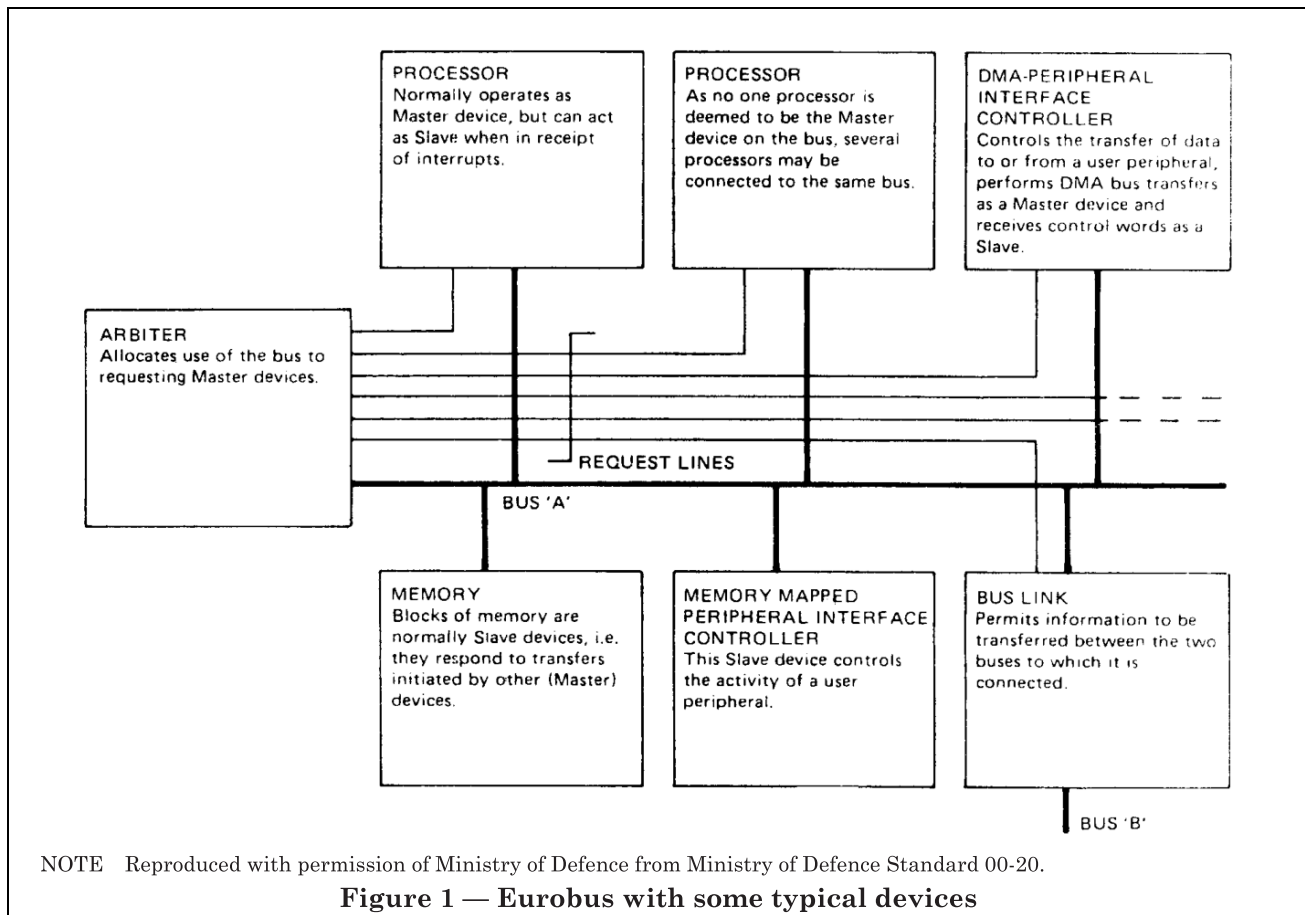
The bus allocation protocols permit a master to hold the bus for repeated use without the need to make a fresh bit for every transfer, while also giving the arbiter the ability to instruct any master to release the bus for reallocation. A master is also permitted to retain the bus for an indivisible sequence of cycles, such as a Read-Modify-Write sequence. An additional protocol is defined whereby the arbiter may abort a cycle that is deemed to have failed.

0.6 Interbus transfers. The protocols for Read, Write and Vector cycles permit a master on bus A, for example, wishing to effect a transfer with a slave on bus B, to address a bus linker on bus A as slave. The bus linker then bids for use of bus B as master and addresses the required slave on bus B. Should master devices on both buses attempt simultaneous transfers, the bus link cannot become master on either bus and a condition of deadly embrace ensues. The Eurobus protocols permit the embrace to be broken simply.

The protocols used by bus links to perform interbus addressing and data transfer are not within the scope of this standard.

0.7 Electrical requirements. The standard specifies the electrical and timing requirements that need to be obeyed by Eurobus A devices. Aspects covered within the electrical requirements include:

a) the voltage levels of the active and quiescent logic states on the bus;

b) the required characteristics of the terminations networks;

c) the required characteristics of the bus transmitters and receivers;

d) the required characteristics of the spurs to be connected to the bus.

The specified set of electrical characteristics presupposes certain bus settling times for the transitions on the signal lines. Arising from these, certain timing constraints are specified. These constraints ensure that the relevant signal lines will have settled to the appropriate state before an associated control signal transition is issued.

0.8 Commercial and military versions. Two versions of Eurobus A are specified in this standard, a version for a commercial temperature range (0 °C to 70 °C) and a version for a military temperature range (– 55 °C to 125 °C). Where the requirements are different they are separately specified for each version.

1 Scope

This British Standard specifies a processor system bus interface known as Eurobus A that is one of a family of interfaces for use in modular data acquisition, communication and control systems for military, industrial and other applications.

NOTE 1   More detailed information about the requirements specified in this standard, including the data width and addressing capability, devices connected to the bus, bus allocation, bus transfers, interbus transfers and electrical requirements, and background information are given in clause **0**.

NOTE 2   In this standard, upper case letters are used for the first letter of names of bus cycles.

NOTE 3   The titles of the publications referred to in this standard are listed on the inside back cover.

2 Definitions

For the purposes of this British Standard the following definitions apply.

2.1
address

the location of a data word, or the value on the highway during the addressing phase of any Read, Write or Vector cycle

2.2
arbiter

the device that performs the function of arbitration for the bus and is also responsible for servicing interrupts and for timing-out failed cycles and aborting them

2.3
arbitration

the means whereby use of the bus is allocated to one of the bidding devices which then becomes the master

2.4
backplane

the assembly of the bus with connectors into which spur cards may be plugged

2.5
bidding device

a device that wishes to initiate a cycle or group of cycles on a bus and that requests use of the bus

2.6
bus

the complete set of bus lines used by a particular implementation of Eurobus

2.7
bus cycle

a closed group of signals on the bus that convey information between devices connected to it. This group consists of an addressing phase, in which the master places an address on the highway for recognition by a slave and, except in Vector cycles, a subsequent data transfer phase

2.8
bus line

an electrical connection between two or more devices

2.9
bus linker

a device that plugs into two or more buses thus providing a means whereby a master on one bus may transfer information to or from a slave on another bus

2.10
bus voltage

the voltage on a bus line measured relative to the bus zero voltage reference

2.11
byte

a contiguous group of 8 bits

2.12
circuit card

a card on which various electronic components are mounted and that plugs into a Eurobus backplane as a spur

2.13
data

the information held at, written to, or read from an address

2.14
deadly embrace

the conditions when two interbus transfers, using the same bus linker, have been commenced and neither transfer can be completed

2.15
device

a functional block, occupying one or more circuit cards, that communicates with other functional blocks by means of the bus or a subset of the bus

2.16
extender panel

a circuit card that can be inserted between the bus and another circuit card to permit easy access to the latter while it is still connected to the bus

2.17
hold cycles

a sequence of cycles during which the master is not asked by the arbiter to release the bus for reallocation

2.18
highway

those bus lines used to convey data and addresses between devices on the Eurobus

2.19
indivisible operation

a sequence of bus cycles for which the correct system function can only be guaranteed if no other bus cycles occur within that sequence,
e.g. a Read-Modify-Write sequence

2.20
interbus transfer

a transfer of information between devices that uses two or more buses and one or more bus linkers

2.21
interrupt

a flag passed to the arbiter by a device in order to initiate a predetermined system-dependent function

2.22
master

the device that initiates the transfer in question

2.23
normal address space

an addressing space whose size is determined by the number of lines in the highway and that is addressable as words or bytes

2.24
protocol

the signalling rules used to convey information or commands between devices connected to the bus

2.25
pseudo address space

a second, independent addressing space whose size is determined by the number of lines in the highway and that is addressable as words only

2.26
read cycle

a bus cycle in which the master obtains a word or byte from the slave

2.27
reset

the operation whereby each device connected to the bus is put into a predetermined initial condition

2.28
retain cycle

a bus cycle at the end of which the master keeps control of the bus in order to complete an indivisible operation

2.29
settling time

the time taken for a bus line to settle unambiguously into its new logical state from its previous state

2.30
shelf

the physical structure that supports the backplane and the cards that plug into it

2.31
skew

on the assumption that two logical transitions are launched simultaneously on two bus lines, the time difference between the receipt of those transitions at a given pair of receivers on a card connected to the bus at the point in question

2.32
slave

the device that responds to the address placed on the bus by the master for the cycle in question

2.33
spur

device connected to the bus at some point between the two ends of the bus

2.34
state (of a bus line)

one of two conditions of a bus line, namely active or quiescent

2.35
vector cycle

a bus cycle in which the purpose is to pass an address from a master to a slave and in which no data transfer takes place

2.36
word

a group of bits whose number corresponds to the maximum data width that can be conveyed over the bus in a single transfer

2.37
0 V

the signal return path and, as such, the reference for all voltage measurements

NOTE   0 V is not a safety earth. Where a safety earth is referred to in this standard, it is specifically identified.

2.38
write cycle

a bus cycle in which a master writes a word or byte to a slave

3 Designation of a particular Eurobus

Each member of the Eurobus A family shall be designated using the following format.

Eurobus	address width	/A	qualifying information

The designation entries shall be determined as follows:

a) address width = 10 or 18 or 26 or 34 . . . etc., as appropriate (see note 1);

b) A designates the electrical characteristics specified in clause **6**;

c) qualifying information is additional text stating the version (see **0.8**) and, optionally, text to enable users: to identify a particular mechanical implementation.

NOTE 1   The address width is the number of highway bits, i.e. the number of data bits plus two.

NOTE 2   It is recommended that sufficient qualifying information should be provided to enable users and potential users to identify a particular mechanical implementation of Eurobus.

NOTE 3   For example, an 18-bit address implementation of Eurobus A (omitting optional qualifying information) is designated "Eurobus 18/A commercial".

4 Compliance

4.1 Full compliance of devices. Devices that are said, without qualification, to comply with this standard, shall comply with:

a) the logical requirements of clause **5**;

b) the electrical requirements of clause **6**;

c) the requirements for connector allocation (see **4.4**).

4.2 Logical compliance

4.2.1 Devices said to be logically compliant shall comply with the protocol requirements of clause **5** or with an appropriate subset of those requirements.

NOTE   For example, a slave-only device need not be capable of acting as a bidding device.

4.2.2 In an implementation said to be logically compliant, *either:*

a) the bus lines shall be used only for the purposes specified in this standard; *or*

b) if one or more of the bus lines is used for purposes not so specified;

1) normal signals on the bus between devices that, operate according to the specified protocols shall not cause any malfunction in the implementation concerned;

2) signals generated within that implementation shall not cause malfunction in devices, connected to the bus, that operate according to the protocols specified in this standard.

4.3 Electrical compliance. Devices said to be electrically compliant shall *either:*

a) comply with **6.1** and **6.2**, relating to the electrical requirements of devices; *or*

b) when incorporated into a bus, not prevent that bus from complying with **6.3**, relating to the electrical requirements of buses.

If a device is logically compliant (see **4.2**) and is electrically compliant in accordance with item b) [i.e. not in accordance with item a)], all descriptions of the device that refer to this standard shall include an explicit statement of the limitations imposed on a system into which the device may be incorporated.

4.4 Mechanical compliance. Connector allocations for data widths of 8, 16, 24 and 32 bits shall be as specified in Appendix E.

5 Protocols for Eurobus A

5.1 Preliminary

5.1.1 *General.* The set of signals constituting Eurobus A shall be as specified in **5.2**. The protocols, for use of those signals for the allocation of the bus to potential users and thereafter for effecting transfers on the bus, shall be as specified in **5.3** and **5.4**.

NOTE 1   Appendix F gives illustrative examples of the operation of the bus protocols in accordance with these requirements.

NOTE 2   Any transfer using the Eurobus protocols generally involves three devices:

a) the arbiter which:

1) grants use of the bus to a bidding device that then becomes the bus master; *or*

2) allows an existing master to continue using the bus;

b) the master device that initiates the transfer by addressing another device;

c) the device that, having recognized the address, accepts the transfer and so becomes the bus slave.

5.1.2 *Basic bus cycles.* There shall be three basic types of bus cycle (see Table 1) as follows.

    a) Read cycle in which data is read from a slave device by a master device.

    b) Write cycle in which data is written to a slave device by a master device.

    c) Vector cycle in which an address is transferred from the master device to the slave device.

NOTE   The address used by the master device to identify one of a set of locations recognized by a slave device is the only information transferred over the bus in a Vector cycle.

5.1.3 *Bus cycle variants.* The number of possible variants of each basic type shall be two, as follows:

    a) Read and Hold;

    b) Read and Retain;

    c) Write and Hold;

    d) Write and Retain;

    e) Vector and Hold;

    f) Vector and Retain.

NOTE 1   The main purpose of a Hold cycle is to allow devices that have a requirement for numerous bus cycles, e.g. processors to access the bus repeatedly without having to bid for each individual cycle. Because the use of such a cycle can delay the reallocation of the bus to another device, such cycles are only recommended where there is a high probability that the device concerned will make use of the next bus cycle.
The main purpose of Retain cycles is to enable indivisible operations to be performed, e.g. Read-Modify-Write.

NOTE 2   The differences between these variants and the basic cycles concern the time at which the bus is released by the device for reallocation by the arbiter.

NOTE 3   The bus allocation protocol is designed so that:
    a) the minimum avoidable delay is experienced when allocating an idle bus;
    b) wherever possible, bus allocation is overlapped with bus cycles in order to reduce delays;
    c) a device that requires numerous bus cycles, such as a processor, does not necessarily have to make a fresh request for each cycle;
    d) a device can perform indivisible cycles (this provides the facility necessary, for example, for the construction of a Ready-Modify-Write cycle from a Read cycle followed by a Write cycle);
    e) a device can, as an alternative to performing a Read, Write or Vector cycle, signal an Interrupt to the arbiter which is then responsible for servicing the Interrupt.

5.2 Signalling

5.2.1 *Use of bus lines.* All communication between the arbiter, devices acting as master and devices acting as slave shall be over the Eurobus protocol lines as specified in Table 1. The usage of these lines shall be such that any device, or several devices simultaneously, can cause a line to be active. If no device has caused a line to be active, that line shall be quiescent.

5.2.2 *Bit numbering.* The bit number, (N), of the most significant data and address line shall be given by:

    $N = 8p - 1$

where

    p is any positive integer.

The bit number (M) of the most significant byte address line shall be given by:

    M = the largest positive integer that is *less than* $\log_2[(N + 1)/8]$

NOTE   For example, in order to address one of two bytes in a 16-bit data word:
    $N = 15$ and
    $M < \log_2 16/18$, i.e. $M < 1$
    $\therefore M = 0$, i.e. only one byte address line is required.

5.2.3 *Byte mode address selection.* The current but master shall specify, by coding the Byte Working and Byte Address lines, as given in Table 2, the selection of either full-word working, or byte working. If full-word working is selected, the coding shall further specify the selection of pseudo or normal address space. If byte-working is selected, the coding shall further specify which byte is addressed and pseudo address space shall then be unavailable.

5.3 Address recognition protocol

5.3.1 *Data width.* The full addressing capability of the highway, $2(N + 3)$ bits provided by $\overline{\text{AdM(1)}}$, $\overline{\text{AdM(0)}}$, $\overline{\text{H(N)}}$ to $\overline{\text{H(0)}}$, is available on a bus having only devices all of equal data widths. The use of this capability shall be by the method given in Table 3 for a data width of 8 bits.

For buses that include devices having unequal data widths, the method of address allocation shall be as specified in Appendix G.

NOTE   The functioning of the bus is not dependent on this method.

5.3.2 *Recognition of address modifier bits.* Any slave device operating on a bus that it is sharing with other devices having different data width(s) from itself, shall in all instances recognize one coding and one coding only on the Address Modifier lines.

The specific codes recognized by devices of a particular data width shall, in any system, be allocated according to the following rules.

    a) The codes listed in Table 4 under the heading first block (columns 3 and 4) shall first be allocated.

    b) If further codes are required, the codes listed under the headings second block, third block and fourth block (columns 5 to 10) shall be allocated in that order.

Such codes shall be allocated by data width in order from the smallest widths to the largest width, and any code that has then been allocated shall not be available for allocation to another data width as follows.

1) If the second, third or fourth block is already allocated for recognition by 8-bit devices, 16-bit devices shall be allocated the next higher available block;

2) If the second, third or fourth block is already allocated for recognition by 8-bit or 16-bit devices, 24-bit devices shall be allocated the next higher available block.

3) If the second, third or fourth block is already allocated for recognition by 8-bit, 16-bit or 24-bit devices, 32-bit devices shall be allocated the next higher available block.

c) Any unused blocks shall be available for extending the address range of any of the devices.

5.4 Eurobus A protocol rules

5.4.1 *Preliminary*. The rules for the use of the bus lines specified and named in Table 1 shall be as specified in **5.4.2** to **5.4.6**, as follows:

a) for devices bidding for, and the arbiter granting, use of the bus; **5.4.2**, rules A1 to A12;

b) for a device acting as master selecting and communicating with a device acting as slave; **5.4.3**, rules M1 to M11;

c) for a device acting as slave responding to the master; **5.4.4**, rules S1 to S6;

d) for the arbiter aborting a bus cycle; **5.4.5**, rules C1 to C4;

e) for a device, being a bus linker, requesting deallocation of the bus; **5.4.6**, rules D1 to D2.

NOTE Within this point-numbered text the rules and conditions have been arranged and identified, in order to aid understanding, by use of a code of upper case letters, lower case letters and small roman numerals. Each rule is designated by a letter and number (e.g. "A 9"). Within each rule the alternative ("or") conditions are distinguished by lower case letters while simultaneous ("and") conditions are distinguished by small roman numerals.

5.4.2 *Rules for bus allocation*

Rule A1. When device n requires use of the bus it shall bid for the bus by holding $\overline{Rq(n)}$ active. It shall do this if and only if:

i) it is not locked (rules A7 and A12); and

ii) $\overline{BusGr}$ is quiescent; and

iii) $\overline{Rs}$ is quiescent.

Rule A2. The arbiter shall allocate the bus to one of the bidding devices by also holding the appropriate $\overline{Rq(n)}$ line active. It shall do this if and only if:

i) $\overline{Rq(n)}$ is already active; and

ii) the arbiter is not already holding a $\overline{Rq}$ line active; and

iii) $\overline{BusGr}$ is quiescent; and

iv) $\overline{BusAcq}$ is quiescent; and

v) $\overline{It}$ is quiescent; and

vi) $\overline{Bus\ Deallocate}$ is quiescent; and

vii) $\overline{CcAbort}$ is quiescent; and

viii) $\overline{Rs}$ is quiescent.

Table 1 — Eurobus A protocol lines

Signal name (abbreviations)	Number of lines	Requirements
High way lines		
Data/Address [$\overline{H(0)}$ to $\overline{H(N)}$]	$N+1$	Time division multiplexed bi-directional data and address lines. $\overline{H(0)}$ shall be associated with the least significant bit. The number of the most significant bit, $\overline{H(N)}$, shall be determined as specified in **5.2.2**
Address Modifier Bits (0), (1) [$\overline{AdM(0)}$, $\overline{AdM(1)}$]	2	Address Modifier lines. These are available and shall be used when it is required to increase the address range beyond that definable by $\overline{H(0)}$ to $\overline{H(N)}$ and also for selection between devices of different data width that share the same bus (see **5.3**)
Byte mode/address space selection lines		
Byte Working ($\overline{BytWk}$) Byte Address Bits (0) to [$\overline{BytAd(0)}$ to $\overline{BytAd(M)}$]	1 $M+1$	These lines shall be used to qualify the address on the highway in terms of the byte mode/address space selection coding (see **5.2.3**). The number of the most significant Byte Address bit, (M), shall be determined as specified in **5.2.2** If $N=7$ the Byte Working line shall remain quiescent

Table 1 — Eurobus A protocol lines

Signal name (abbreviations)	Number of lines	Requirements
Bus allocation protocol lines		
Request (n) [$\overline{\mathrm{Rq}(n)}$]	1 per potential bus master	One Request line shall be star-connected to the arbiter from each device that requires to be able to bid for bus allocation
		Request(n) line shall be activated by device(n) to signal its bid for bus allocation. The arbiter shall activate the Request line, in conjunction with the Bus Granted line, to allocate use of the bus to device(n)
Bus Granted ($\overline{\mathrm{BusGr}}$)	1	This line shall be activated by the arbiter at the same time as it activates the Request line of a particular device in order to affect a new bus allocation. The device in question shall then be the current bus master for the next transfer
		This line shall also be activated by the arbiter without activating a Request line to deallocate the current bus master (see **5.4.5**)
Bus Acquired ($\overline{\mathrm{BusAcq}}$)	1	This line shall be activated by the current bus master to signify that the bus grant has been accepted. The line shall be held active by a slave if that slave is about to activate the Bus Deallocate line
Interrupt ($\overline{\mathrm{It}}$)	1	This line shall be activated by the current bus master to indicate to the arbiter that its request is for an Interrupt cycle
Transfer control handshake lines		
Cycle Begin ($\overline{\mathrm{CcBn}}$)	1	This line shall be activated by the current master device to indicate that: a) there is a stable address on the highway and byte mode/address space selection lines; b) the Cycle Finish line (which at this point of the transfer indicates Read/Vector cycle or Write cycle) is stable
Cycle Response ($\overline{\mathrm{CcRes}}$)	1	This line shall be activated by a device to indicate that it has recognized the address on the highway and has become the current bus slave. On detecting that this line has become active the master shall remove the address from the highway
Cycle Finished ($\overline{\mathrm{CcFin}}$)	1	This bi-directional line shall be activated: a) by the current master: 1) in a Read cycle to indicate that the address has been removed: 2) in a Write cycle to identify the cycle as a Write cycle and, when released, to indicate that Write data has been removed; b) by the current slave during the transmission of Read data
Cycle Abort ($\overline{\mathrm{CcAbort}}$)	1	This line shall be activated by the arbiter to terminate an invalid bus cycle

Table 1 — Eurobus A protocol lines

Signal name (abbreviations)	Number of lines	Requirements
Reset ($\overline{\text{Rs}}$)	1	Reset line. This line shall be connected to all devices on the bus. When the line is activated by any device that is permitted to do so, it shall cause a general bus reset operation
Bus Deallocation ($\overline{\text{Bus Deallocate}}$)	1	This line shall be activated by a bus link device in order to indicate to an arbiter *either:* a) that the bus link requires a deadly embrace to be broken; *or* b) that the arbiter is required to ask the bus master to release the bus for reallocation. The state of the Cycle Response line shall be used to specify which of the indications is valid at the time the Bus Deallocate line is activated

Table 2 — Coding of byte mode/address space selection lines

$\overline{\text{BytWk}}$	$\overline{\text{BytAd}}(M)$	$\overline{\text{BytAd}}(M-1)$	. . .	$\overline{\text{BtyAd}}(0)$	Selection
Q	Q	X	X	X	The whole word ($N+1$ bits) in normal address space
Q	Acv	X	X	X	The whole word ($N+1$ bits) in pseudo address space
Acv	Q	Q	Q	Q	Least significant byte (byte 0)
Acv	Q	Q	Q	Acv	Byte 1
.	.	.	.	.	
.	.	.	.	.	in normal address space
Acv	Acv	Acv	Acv	Q	Byte $[2(M+1)-2]$
Acv	Acv	Acv	Acv	Acv	Byte $[2(M+1)-1]$

NOTE 1   In Table 2 and later tables the abbreviation "Acv" signifies the active state, and "Q" signifies the quiescent state Symbol "X" signifies that either state may exist.

NOTE 2   For values of M and N see **5.2.2**.

Table 3 — Address recognition protocol ($N = 7$)

$\overline{\text{AdMd}}(1)$	$\overline{\text{AdMd}}(0)$	Addresses	Data
Acv	Acv	Fourth block for 8-bit devices	$\overline{\text{H}(7)}$ $\overline{\text{H}(0)}$
Acv	Q	Third block for 8-bit devices	$\overline{\text{H}(7)}$ $\overline{\text{H}(0)}$
Q	Acv	Second block for 8-bit devices	$\overline{\text{H}(7)}$ $\overline{\text{H}(0)}$
Q	Q	First block for 8-bit devices	$\overline{\text{H}(7)}$ $\overline{\text{H}(0)}$

NOTE   See note 1 to Table 2.

Table 4 — Address modifier codes to be recognized by slave devices of different widths sharing the same bus

Bus data width (bits)	Device data width (bits)	Address modifier code for recognition of address block							
		First block		Second block		Third block		Fourth block	
		AdM(1)	AdM(0)	AdM(1)	AdM(0)	AdM(1)	AdM(0)	AdM(1)	AdM(0)
16	8	Q	Q	Acv	Q	Acv	Acv	—	—
	16	Q	Acv	Acv	Q	Acv	Acv	Q	Q
24	8	Q	Q	Q	Acv	Acv	Acv	—	—
	16	Q	Acv	Acv	Acv	Q	Q	—	—
	24	Acv	Q	Acv	Acv	Q	Q	Q	Acv
32	8	Q	Q	Q	Acv	Acv	Q	—	—
	16	Q	Acv	Acv	Acv	Q	Q	—	—
	24	Acv	Q	Q	Q	Q	Acv	—	—
	32	Acv	Acv	Q	Q	Q	Acv	Acv	Q

NOTE See note 1 to Table 2.

Rule A3. The arbiter shall $\overline{\text{BusGr}}$ hold active if and only if:

ai) the arbiter has made an allocation under rule A2; and

aii) $\overline{\text{Rs}}$ is quiescent;

NOTE Bus allocation is complete.

bi) or, the arbiter is not holding a $\overline{\text{Rq}}$ line active; and

bii) $\overline{\text{CcBn}}$ is active; and

biii) $\overline{\text{CcRes}}$ is quiescent; and

biv) $\overline{\text{Bus Deallocate}}$ is active; and

bv) $\overline{\text{CcRes}}$ was quiescent when $\overline{\text{Bus Deallocate}}$ became active; and

bvi) $\overline{\text{Rs}}$ is quiescent.

NOTE The arbiter deallocates the cycle that the slave has refused.

Rule A4. A bidding device shall release its $\overline{\text{Rq}}$ line if and only if:

a) $\overline{\text{BusGr}}$ is active;

b) or, $\overline{\text{Rs}}$ is active.

Rule A5. A device shall hold $\overline{\text{BusAcq}}$ active, if and only if:

ai) $\overline{\text{BusGr}}$ is active; and

aii) its $\overline{\text{Rq}}$ line is active (and it is not itself holding this line active); and

aiii) $\overline{\text{CcBn}}$ is quiescent; and

aiv) $\overline{\text{CcRes}}$ is quiescent; and

av) $\overline{\text{CcFin}}$ is quiescent; and

avi) the device is not holding the $\overline{\text{It}}$ line active; and

avii) $\overline{\text{CcAbort}}$ is quiescent; and

aviii) $\overline{\text{Rs}}$ is quiescent;

NOTE The master acquires the bus.

bi) or, $\overline{\text{CcRes}}$ is quiescent; and

bii) $\overline{\text{CcBn}}$ is active; and

biii) the signals on the highway and byte mode lines correspond to an address recognized by the device; and

biv) the device is not holding $\overline{\text{CcFin}}$ active; and

bv) the device is about to hold $\overline{\text{Bus Deallocate}}$ active according to rule D 1a or (after application of rule S1) rule D 1b; and

bvi) $\overline{\text{CcAbort}}$ is quiescent; and

bvii) $\overline{\text{Rs}}$ is quiescent.

NOTE The slave device holds $\overline{\text{BusAcq}}$ active before $\overline{\text{CcRes}}$, if it intends to ask the arbiter to remove allocation from the current master, or before $\overline{\text{Bus Deallocate}}$, if it intends to refuse the cycle.

Rule A6. Alternatively to rule A5, a device shall hold $\overline{\text{It}}$ active, and thus initiate an Interrupt cycle, if and only if:

i) $\overline{\text{BusGr}}$ is active; and

ii) its $\overline{\text{Rq}}$ line is active (and it is not itself holding this line active); and

iii)   it is not holding $\overline{\text{BusAcq}}$ active; and

iv) $\overline{\text{CcAbort}}$ is quiescent; and

v) $\overline{\text{Rs}}$ is quiescent.

> NOTE   The master generates an interrupt to the arbiter.

Rule A7. A device shall become locked if and only if:

a)   it holds $\overline{\text{BusAcq}}$ active according to rule A5a;

b) or,   it holds $\overline{\text{It}}$ active according to rule A6.

Rule A8. The arbiter shall release $\overline{\text{BusGr}}$ if and only if:

ai) $\overline{\text{BusAcq}}$ is active; and

aii) $\overline{\text{Bus Deallocate}}$ is quiescent:

> NOTE   The arbiter acknowledges bus acquisition

bi) or, $\overline{\text{It}}$ is active; and

bii) $\overline{\text{Bus Deallocate}}$ is quiescent;

> NOTE   The arbiter acknowledges an interrupt.

ci) or,   it is not holding a $\overline{\text{Rq}}$ line active; and

cii) $\overline{\text{BusAq}}$ is quiescent;

> NOTE   The arbiter completes the bus deallocation handshake.

di) or,   it is holding $\overline{\text{CcAbort}}$ active; and

dii) $\overline{\text{Bus Deallocate}}$ is quiescent;

e) or, $\overline{\text{Rs}}$ is active.

Rule A9. The arbiter shall release any $\overline{\text{Rq}}$ line it is currently holding active if and only if:

ai) $\overline{\text{BusGr}}$ is quiescent; and

aii) $\overline{\text{BusAcq}}$ is quiescent; and

aiii) $\overline{\text{It}}$ is quiescent; and

aiv)   the arbiter is not about to hold $\overline{\text{BusGr}}$ under rule A3;

> NOTE   The last allocated master has finished using the bus.

bi) or, $\overline{\text{BusGr}}$ is quiescent; and

bii)   a device holds its $\overline{\text{Rq}}$ line active; and

biii)   the arbiter is not about to hold $\overline{\text{BusGr}}$ under rule A3;

> NOTE   A device requests allocation while the allocated master is still using the bus.

c) or, $\overline{\text{Bus Deallocate}}$ is active;

> NOTE   The arbiter asks the allocated master to release the bus for reallocation.

d) or,   it is holding $\overline{\text{CcAbort}}$ active;

e) or,   Reset is active.

Rule A10. A device that is holding $\overline{\text{BusAcq}}$ active shall release it if and only if:

ai)   the current bus cycle is established (rule M5); and

aii)   the device's $\overline{\text{Rq}}$ line is active; and

aiii)   it does not wish to hold the bus for further cycles;

> NOTE   The master relinquishes the bus unilaterally.

bi) or,   the current bus cycle is established (rule M5); and

bii)   the device's $\overline{\text{Rq}}$ line is quiescent; and

biii)   it does not require to retain the bus for an indivisible operation;

> NOTE   The arbiter asks the master to release the bus.

ci) or,   the current cycle is refused (rule M6);and

cii)   it is not holding $\overline{\text{CcBn}}$ active; and

ciii)   it is not holding $\overline{\text{CcFin}}$ active;

> NOTE   The master releases the bus in a Deallocate cycle.

di) or,   it is holding $\overline{\text{Bus Deallocate}}$ active; and

(dii)   it is slave for the current cycle;

> NOTE   The onus is on the slave to guarantee that $\overline{\text{BusAcq}}$ is active when $\overline{\text{Bus Deallocate}}$ becomes active (see rules A10a, A10b, S1 and D1b).

ei) or,   it is holding $\overline{\text{Bus Deallocate}}$ active; and

eii)   it has refused to become slave for the current cycle; and

eiii) $\overline{\text{BusGr}}$ is active;

f) or, $\overline{\text{CcAbort}}$ is active;

g) or, $\overline{\text{Rs}}$ is active.

Rule A11. A device that is holding $\overline{\text{It}}$ active shall release it if and only if:

(a) $\overline{\text{BusGr}}$ is quiescent;

> NOTE   The handshake completes the Interrupt cycle.

(b) or, $\overline{\text{CcAbort}}$ is active;

(c) or, $\overline{\text{Rs}}$ is active.

Rule A12. A device shall cease to be locked if and only if:

a)   it completes a cycle as master (rules M9b, M9c and M11a) when $\overline{\text{BusAcq}}$ is quiescent;

NOTE   This is the end of a cycle in which the master released the bus for reallocation.

b) or, it releases $\overline{\text{BusAcq}}$ (rules A10a and A10b) after completion of one cycle as master (rules M9b, M9c and M11a) and before commencement of another (rule M1);

NOTE   The master releases the bus for reallocation following a Hold cycle or a Retain cycle.

c) or, it releases $\overline{\text{It}}$ under rule A11a;

NOTE   This is the end of Interrupt cycle.

di) or, it completes a cycle as slave in a Write cycle or a Vector cycle (rules S4a and S4c); and

dii)   it is not holding $\overline{\text{It}}$ active;

NOTE   This condition releases the lock following the abortion of a master cycle.

e) or, it releases $\overline{\text{BusAcq}}$ under rule A10c;

NOTE   This release is after deallocation.

f) or, $\overline{\text{Rs}}$ is active.

5.4.3 *Rules for devices acting as master*

Rule M1. The master shall commence a cycle if and only if:

i)   it is holding $\overline{\text{BusAcq}}$ active; and

ii) $\overline{\text{CcBn}}$ is quiescent; and

iii) $\overline{\text{CcRes}}$ is quiescent; and

iv) $\overline{\text{CcFin}}$ is quiescent; and

v) $\overline{\text{CcAbort}}$ is quiescent; and

vi) $\overline{\text{Rs}}$ is quiescent.

NOTE   The cycle starts after bus free.

Rule M2. The master shall hold the highway and byte mode lines to form an address if and only if:

i)   the cycle is commenced (rule M1);and

ii) $\overline{\text{CcAbort}}$ is quiescent; and

iii) $\overline{\text{Rs}}$ is quiescent.

Rule M3. The master shall hold $\overline{\text{CcFin}}$ active if and only if:

ai)   the cycle is commenced (rule M1); and

aii) $\overline{\text{CcAbort}}$ is quiescent; and

aiii)   it wishes to perform a Write cycle; and

aiv) $\overline{\text{Rs}}$ is quiescent;

NOTE   This is the beginning of a Write cycle.

bi) or, the cycle is established (rule M5); and

bii)   it is not holding an address; and

biii)   it wishes to perform a Read cycle; and

biv) $\overline{\text{CcAbort}}$ is quiescent; and

bv) $\overline{\text{Rs}}$ is quiescent.

NOTE   The address has been removed from the bus in a Read cycle.

Rule M4. The master shall hold $\overline{\text{CcBn}}$ active if and only if:

ai)   it is holding $\overline{\text{BusAcq}}$ active; and

aii)   it is holding an address; and

aiii)   it is holding $\overline{\text{CcFin}}$ active; and

aiv)   it wishes to perform a Write cycle; and

av) $\overline{\text{CcAbort}}$ is quiescent; and

avi) $\overline{\text{Rs}}$ is quiescent;

NOTE   The Write address is on the bus.

bi) or, it is holding $\overline{\text{BusAcq}}$ active; and

bii)   it is holding an address; and

biii)   it wishes to perform a Read cycle; and

biv) $\overline{\text{CcAbort}}$ is quiescent; and

bv) $\overline{\text{Rs}}$ is quiescent;

NOTE   The Read address is on the bus.

ci) or, it is holding $\overline{\text{BusAcq}}$ active; and

cii)   it is holding an address; and

ciii)   it wishes to perform a Vector cycle; and

civ) $\overline{\text{CcAbort}}$ is quiescent; and

cv) $\overline{\text{Rs}}$ is quiescent.

NOTE   The Vector address is on the bus.

Rule M5. The master shall regard the cycle commenced under rule M2 as established if and only if $\overline{\text{CcRes}}$ is active.

NOTE   The slave has accepted the address.

Rule M6. The master shall regard the cycle commenced under rule M1 as refused if and only if:

i)   the master's $\overline{\text{Rq}}$ line is quiescent; and

ii) $\overline{\text{BusGr}}$ is active.

NOTE   This is a bus deallocation.

Rule M7. The master shall release an address if and only if:

a)   the cycle is established (rule M5);

b) or, the cycle is refused (rule M6);

c) or, $\overline{\text{CcAbort}}$ is active;

d) or, $\overline{\text{Rs}}$ is active.

Rule M8. The master shall hold the highway lines to form Write data if and only if:

i) the cycle is established (rule M5); and

ii) it wishes to perform a Write cycle; and

iii) $\overline{\text{CcAbort}}$ is quiescent; and

iv) $\overline{\text{Rs}}$ is quiescent.

Rule M9. The master shall release $\overline{\text{CcBn}}$ if and only if:

ai) it is not holding an address; and

aii) it is holding Write data on the highway;
NOTE This event occurs in a Write cycle.

bi) or, it is not holding $\overline{\text{CcFin}}$ active; and

bii) $\overline{\text{CcFin}}$ is active; and

biii) $\overline{\text{CcRes}}$ is quiescent; and

biv) it has accepted the signals on the highway as Read data; and

bv) $\overline{\text{CcAbort}}$ is quiescent;
NOTE This event occurs in a Read cycle.

ci) or, it is not holding an address; and

cii) it wishes to perform a Vector cycle; and

ciii) $\overline{\text{CcRes}}$ is active; and

civ) $\overline{\text{CcAbort}}$ is quiescent;
NOTE This event occurs in a Vector cycle.

di) or, the current cycle is refused (rule M6); and

dii) it is not holding $\overline{\text{CcFin}}$ active; and

diii) it is not holding an address;
NOTE This event occurs in bus deallocation.

ei) or, $\overline{\text{CcAbort}}$ is active; and

eii) it is not holding $\overline{\text{CcFin}}$ active; and

eiii) it is not holding an address;

fi) or, $\overline{\text{CcAbort}}$ is active; and

fii) it is holding Write data;

gi) or, $\overline{\text{Rs}}$ is active; and

gii) it is not holding $\overline{\text{CcFin}}$ and

giii) it is not holding an address;

hi) or, $\overline{\text{Rs}}$ is active; and

hii) it is holding Write data.

Rule M10. The master shall release Write data from the highway if and only if:

ai) $\overline{\text{CcRes}}$ is quiescent; and

aii) $\overline{\text{CcBn}}$ is quiescent;
NOTE The slave accepts Write data.

b) or, $\overline{\text{CcAbort}}$ is active;

c) or, $\overline{\text{Rs}}$ is active.

Rule M11. The master shall release $\overline{\text{CcFin}}$ if and only if;

ai) it is not holding $\overline{\text{CcBn}}$ active; and

aii) it is not holding Write data; and

aiii) the cycle is established (rule M5); and

aiv) $\overline{\text{CcAbort}}$ is quiescent;
NOTE This is the final handshake in a Write cycle.

bi) or, it is holding $\overline{\text{CcBn}}$ active; and

bii) $\overline{\text{CcRes}}$ is quiescent; and

biii) the cycle is established (rule M5);
NOTE This event occurs in the middle of a Read cycle.

ci) or, the current cycle is refused (rule M6); and

cii) it is not holding an address;
NOTE This event occurs while a Write cycle is being deallocated.

di) or, $\overline{\text{CcAbort}}$ is active; and

dii) it is not holding an address;

ei) or, $\overline{\text{CcAbort}}$ is active; and

eii) it is not holding Write data;

fi) or, $\overline{\text{Rs}}$ is active; and

fii) it is not holding an address;

gi) or, $\overline{\text{Rs}}$ is active; and

gii) it is not holding Write data.

5.4.4 *Rules for devices acting as slave*

Rule S1. A device shall hold $\overline{\text{CcRes}}$ active if and only if:

i) $\overline{\text{CcBn}}$ is active; and

ii) $\overline{\text{BusGr}}$ is quiescent; and

iii) the signals on the highway and byte mode lines correspond to an address recognized by the device; and

iv) the device is not refusing to become slave for the current cycle (rule D1a); and

v) the device is not holding $\overline{\text{CcFin}}$ active, and

vi) $\overline{\text{CcAbort}}$ is quiescent; and

vii) $\overline{\text{Rs}}$ is quiescent.

Rule S2. The slave shall hold Read data on the highway if and only if:

i) $\overline{\text{CcFin}}$ is active; and

ii) $\overline{\text{CcFin}}$ was not active when it held $\overline{\text{CcRes}}$ active; and

iii) $\overline{\text{CcAbort}}$ is quiescent; and

iv) $\overline{\text{Rs}}$ is quiescent.

NOTE   This event occurs in a Read cycle.

Rule S3. The slave shall hold $\overline{\text{CcFin}}$ active if and only if:

i) $\overline{\text{CcFin}}$ is active; and

ii) $\overline{\text{CcFin}}$ was not active when it held $\overline{\text{CcRes}}$ active; and

iii) $\overline{\text{CcAbort}}$ is quiescent; and

iv) $\overline{\text{Rs}}$ is quiescent.

NOTE   This event occurs in a Read cycle.

Rule S4. The slave shall release $\overline{\text{CcRes}}$ if and only if:

ai) it is not holding $\overline{\text{CcFin}}$ active; and

aii) $\overline{\text{CcFin}}$ is active; and

aiii) $\overline{\text{CcFin}}$ was active when it held $\overline{\text{CcRes}}$ active; and

aiv) $\overline{\text{CcBn}}$ is quiescent; and

av) it is not holding $\overline{\text{BusAcq}}$ active; and

avi) it has accepted the signals on the highway as Write data; and

avii) $\overline{\text{CcAbort}}$ is quiescent;

NOTE   The slave has accepted the data in a Write cycle.

bi) or, it is holding Read data on the highway; and

bii) it is holding $\overline{\text{CcFin}}$ active; and

biii) it is not holding $\overline{\text{BusAcq}}$ active;

NOTE   The slave signals the presence of Read data on the bus.

ci) or, $\overline{\text{CcFin}}$ is quiescent; and

cii) $\overline{\text{CcBn}}$ is quiescent; and

ciii) $\overline{\text{CcAbort}}$ is quiescent; and

civ) it is not holding $\overline{\text{BusAcq}}$ active;

NOTE   This is the final handshake in a Vector cycle.

d) or, $\overline{\text{CcAbort}}$ is active;

e) or, $\overline{\text{Rs}}$ is active.

Rule S5. The slave shall release Read data from the highway if and only if:

a) $\overline{\text{CcBn}}$ is quiescent;

NOTE   The master has accepted the Read data.

bi) or, $\overline{\text{CcAbort}}$ is active; and

bii) $\overline{\text{CcRes}}$ is quiescent;

ci) or, $\overline{\text{Rs}}$ is active; and

cii) $\overline{\text{CcRes}}$ is quiescent.

Rule S6. The slave shall release $\overline{\text{CcFin}}$ if and only if:

ai) $\overline{\text{CcBn}}$ is quiescent; and

aii) it is not holding Read data; and

aiii) $\overline{\text{CcAbort}}$ is quiescent;

NOTE   This is the final handshake in a Read cycle.

bi) or, it is not holding Read data; and

bii) $\overline{\text{CcAbort}}$ is active;

ci) or, it is not holding Read data; and

cii) $\overline{\text{Rs}}$ is active.

5.4.5 *Rules for abortion of cycles*

Rule C1. The arbiter shall hold $\overline{\text{CcAbort}}$ active if and only if it detects that:

ai) there has been an infringement of any of the rules A5, A6, A10 or A11 (see **5.4.2**) and

aii) $\overline{\text{CcBn}}$ is quiescent; and

aiii) $\overline{\text{CcRes}}$ is quiescent; and

aiv) $\overline{\text{CcFin}}$ is quiescent; and

av) $\overline{\text{Rs}}$ is quiescent;

bi) or, there has been an infringement of any of the rules of **5.4.3** or **5.4.4**; and

bii) $\overline{\text{It}}$ is quiescent; and

biii) $\overline{\text{Rs}}$ is quiescent;

ci) or, there has been an infringement of any of the rules A5, A6, A10 or A11; and

cii) there has been an infringement of any of the rules of **5.4.3** or **5.4.4**; and

ciii) $\overline{\text{Rs}}$ is quiescent.

Rule C2. The arbiter shall release $\overline{\text{CcAbort}}$ if and only if:

ai) it is not holding any $\overline{\text{Rq}}$ line active; and

aii) it is not holding $\overline{\text{BusGr}}$ active; and

aiii) $\overline{\text{BusAcq}}$ is quiescent; and

aiv) $\overline{\text{It}}$ is quiescent; and

av) $\overline{\text{CcBn}}$ is quiescent; and

avi) $\overline{\text{CcRes}}$ is quiescent; and

avii) $\overline{\text{CcFin}}$ is quiescent; and

aviii) $\overline{\text{Bus Deallocate}}$ is quiescent;

b) or, $\overline{\text{Rs}}$ is active.

Rule C3. Failure to comply with a rule within the time specified by the system designer for a particular implementation of an arbiter shall be an infringement of that rule.

NOTE   The specified time may be included in the qualifying information in the bus designation (see clause **3**).

Rule C4. A device shall regard a Read, Write or Vector cycle or an Interrupt as valid if and only if it has completed its action under rule A11a, M9b, M9c, M11a, S4a, S4c, or S6a, as appropriate.

NOTE   Rule C1 does not imply that any given Eurobus arbiter need be capable of detecting all possible infringements of the rules.

5.4.6 *Roles for bus deallocation*

Rule D1. A device shall hold $\overline{\text{Bus Deallocate}}$ active if and only if:

ai) $\overline{\text{BusGr}}$ is quiescent; and

aii) it is not holding $\overline{\text{CcRes}}$ active; and

aiii) it is holding $\overline{\text{BusAcq}}$ active under rule A5b: and

aiv) the device is refusing to become (and is not already) slave for the current cycle; and

av) $\overline{\text{CcAbort}}$ is quiescent; and

avi) $\overline{\text{Rs}}$ is quiescent;

NOTE   The device asks the arbiter to deallocate the bus.

bi) or, it is holding $\overline{\text{BusAcq}}$ active under rule A5b; and

bii) $\overline{\text{CcRes}}$ is active; and

biii) $\overline{\text{CcAbort}}$ is quiescent; and

biv) $\overline{\text{Rs}}$ is quiescent.

NOTE   The device asks the arbiter to remove allocation from the master.

Rule D2. A device shall release $\overline{\text{Bus Deallocate}}$ if and only if $\overline{\text{BusAcq}}$ is quiescent.

5.4.7 *Rules for data transfer.* Data shall be transferred over the least significant w highway lines where w is the notional width of the data in bits. The more significant highway lines shall be quiescent.

For example, on a 16-bit bus (N in Table 1 is 15), 8-bit bytes shall be transferred over the least significant 8 bus lines, H(0) to H(7) inclusive, and the remaining lines, $\overline{\text{H(8)}}$ to $\overline{\text{H(15)}}$, shall be quiescent.

6 Electrical and timing requirements

6.1 Electrical requirements

6.1.1 *General.* Eurobus A shall operate over an electrically unbalanced voltage interface using a positive logic convention. All signals shall be referred to the bus 0 V connections which therefore need to meet stringent noise limits.

NOTE 1   The requirements for line and spur characteristics and connector pin allocation ensure good 0 V integrity.

NOTE 2   When devices are connected to the bus, the shunt impedance of each spur alters both line impedance and propagation velocity. Assuming that the shunt impedance is mainly capacitive, the line impedance and propagation velocity fall.

6.1.2 *Power supplies to the backplane*

6.1.2.1 For the commercial version, the power supply shall be 5 ± 0.15 V.

6.1.2.2 For the military version, the power supply shall be 5 ± 0.25 V.

NOTE   For particular implementations of Eurobus A, additional power supplies may be defined and included.

6.1.3 *Eurobus A logic states*

NOTE   The positive logic convention coupled with the use of active low bus signals ensures that gated-off transmitters and open circuits contribute quiescent states to the bus lines. Any gated-on transmitter contributes an active state to the bus line to which it is connected.

6.1.3.1 *Active signal.* A bus line shall be active when its voltage relative to the bus 0 V connections is not less than -0.5 V and not more than 0.8 V.

6.1.3.2 *Quiescent signal.* A bus line shall be quiescent when its voltage relative to the bus 0 V connections is not less than 2 V and not more than the upper limit of the power supply voltage (see **6.1.2**).

6.1.3.3 *Undefined bus voltages.* The meaning of bus line voltages outside the active and quiescent ranges shall be undefined. Devices connected to the bus, except in fault conditions, shall obey the appropriate rules while the voltages on the bus lines remain within the defined limits and the transitions between those limits comply with **6.3.3**.

6.1.4 *Current convention.* Conventional current flowing from a bus line into a spur shall be positive. Conventional current flowing from a spur into a bus line shall be negative.

6.1.5 *Eurobus bus line characteristics*

6.1.5.1 *Bus length.* The bus length shall not exceed 460 mm, including any track on an end terminator/spur card (see **6.1.6.2**).

6.1.5.2 *Inter-spur distance (spur pitch).* The distance between any two spurs on one bus shall not be less than 15 mm.

6.1.5.3 *Number of spurs.* The number of spurs that are connected directly to a given bus shall not exceed 20.

6.1.5.4 *Bus line impedance.* The effective characteristic impedance of any given bus line when spurs as specified in **6.1.7** are connected at the minimum inter-spur pitch shall not fall below 20 Ω.

6.1.5.5 *Cross talk.* The physical implementation of bus lines shall be such that the noise signal induced in any bus line as a result of cross talk from other lines shall not exceed 300 mV under worst case conditions.

NOTE 1   This requirement does not include connector cross talk, which is limited by the defined connector pin allocations (see also Appendix E).

NOTE 2   A specific implementation of the bus lines that complies with **6.1.5** given in cross section in Appendix H.

NOTE 3   An example of a particular mechanical implementation is given in Appendix J.

6.1.6 *Bus line termination*

6.1.6.1 *Networks.* All bus lines, except Request line, shall be terminated at both ends using networks as shown in Figure 2.

The networks shall be fitted directly to the printed circuit backplane, in which case they shall be fitted within 40 mm of an end of the bus, or on cards that are plugged into the bus, as specified in **6.1.6.2**.

Resistors shall comply with the general requirements of BS CECC 40100 and have the properties given in Table 6, throughout the operational temperature range. Diodes (D1; D2 and D3 in Figure 2) shall be fast-switching diodes complying with the general requirements of BS CECC 50000 and have the properties given in Table 7. The requirement for forward recovery voltage shall apply to the value determined as described in IEC 147-2B:1970.

The series inductance of each clamping circuit via the series diode (D1 in Figure 2) and the clamp reference capacitor (C2) to the 0 V rail shall be less than 20 nH.

Capacitor C2 shall be a ceramic or other high-frequency capacitor with better than ± 60 % tolerance.
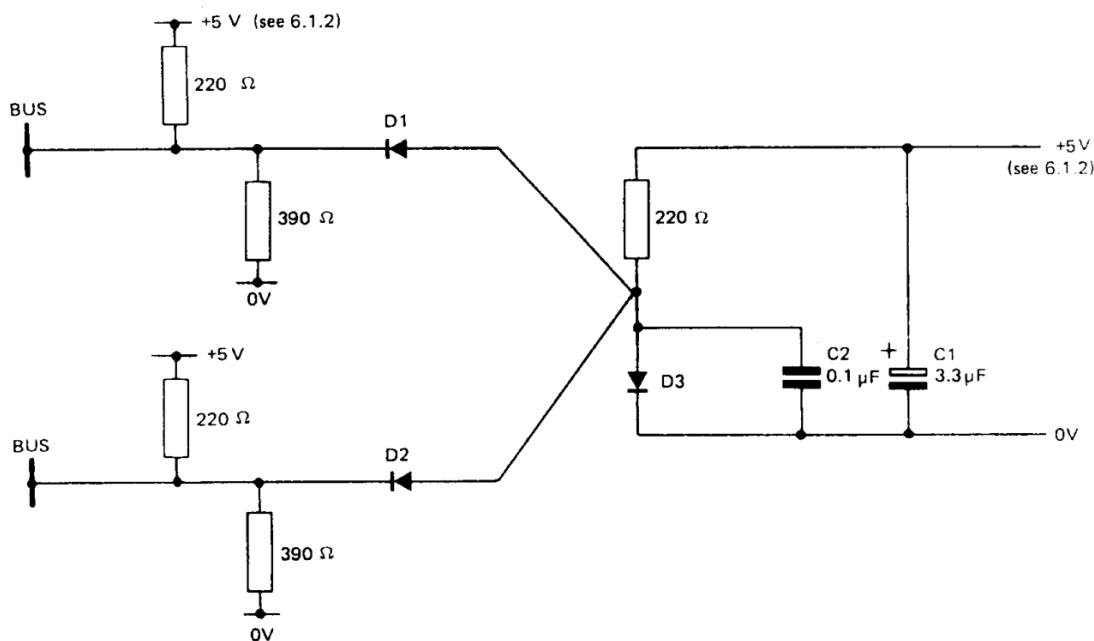
NOTE 1   The diode clamp rail may be shared by up to 10 terminations.
NOTE 2   Reproduced with permission of Ministry of Defence from Ministry of Defence Standard 00-20, with minor alterations.

Figure 2 — Bus terminations

6.1.6.2 *General terminator card.* This type of terminator card, if fitted, shall be fitted in an end slot or within 20 mm of it. The length of the spur track from the bus connector to the termination network shall not exceed 50 mm. The bus on this type of card shall not be connected to other spurs on the card.

When determined as described in **6.1.7.6**, the connector inductance shall not exceed 15 nH.

The total series inductance, including the connector, in the 0 V path between the 0 V reference on the bus and the 0 V reference of a termination network shall not exceed I, in nH, given by:

$$I = 50/N$$

where

N is the number of bus lines terminated by the network.

NOTE   This requirement is inclusive of the 0 V connections to the 5 V decoupling capacitor, C1 on Figure 2.

6.1.6.3 *End terminator/spur card*, (see also **6.1.7.5**). This type of terminator card, if fitted, shall be fitted in an end slot of the bus. The termination networks shall be fitted on the card at the end of the bus that is remote from the connector. The length of the bus on the card shall be included in the total length of the bus.

NOTE 1   Spurs may be attached to the bus between the connector and the termination (see **6.1.7.5**).

When determined as described in **6.1.7.6**, the connector inductance shall not exceed 15 nH.

The total series inductance, including the connector in the 0 V path between the 0 V reference on the bus and the 0 V reference of a termination network shall not exceed I, in nH, given by:

$$I = 50/N$$

where

N is the number of bus lines terminated by the network.

NOTE 2   This requirement is inclusive of the 0 V connections to the 5 V decoupling capacitor, C1 on Figure 2.

6.1.6.4 *Request line termination.* Each of the Request lines shall be terminated at the arbiter by a resistor in the range 171 Ω to 242 Ω to the power supply (see Table 1).

NOTE   This range accommodates resistors rated at 180 Ω ± 5 % and 220 Ω ± 10 %.

6.1.7 *Spurs connected to the bus*

6.1.7.1 *Impedance.* The impedance of the whole spur, including connector, track and interface devices etc., shall not fall outside the limits specified in **6.1.7.2** to **6.1.7.8**.

NOTE 1   This is to ensure that:
a) the active and quiescent levels fall within the specified values;
b) bus settling time is controlled.

NOTE 2   At each device, the majority of the bus lines will be connected to a transmitter and a receiver via the bus connector and track on the card carrying the appropriate circuitry. The combined characteristics of each spur are important from the viewpoint of bus loading.

Table 5 — Identification of symbols

Symbol	Significance
T_A	Ambient temperature
I_F	Forward current during test
V_R	Reverse voltage applied
f	Frequency at which capacity is determined
V_{cc}	Supply voltage (see **6.1.2**)
V_{IH}	High level input voltage
V_{IL}	Low level input voltage
I_{IH}	High level input current
I_{IL}	Low level input current
I_{OL}	Low level output current
I_{OHX}	Leakage current
V_{OH}	Output voltage, high
V_{BUS}	Voltage on the bus line

NOTE   Current flowing into a pin of the device under test is defined as positive.

Table 6 — Termination network resistor ratings

Resistor value (nominal)	Tolerance	Minimum dissipation	
		Commercial version	Military version
Ω	%	mW	mW
220	± 5	135	155
390	± 5	35	35

Table 7 — Termination network diode characteristics

Characteristic	Test conditions	Max. value
Forward voltage V_F	T_A = 25 °C I_F = 20 mA	1.0 V
Diode capacity C_d	T_A = 25 °C V_R = 0 V f = 1 MHz	3.0 pF
Forward recovery voltage V_{FR}	T_A = 25 °C I_F = 10 mA Rise time of current pulse t_r = 20 ns	1.75 V

NOTE   See Table 5 for the significance of the symbols.

6.1.7.2 *D.C. limits.* The d.c. parameters shall be as given in Table 8 to Table 11.

NOTE   This requirement ensures that the active (low) and quiescent (high) levels remain within the specified limits (**6.1.3**) for up to 20 spurs.

6.1.7.3 *A.C. limits: general spur card.* A general spur card can be fitted in any slot along the length of the bus but the total combined capacitive load presented to a given bus line by a general spur shall not exceed 23 pF.

NOTE   This load includes the connector, track on the card, and the shunt capacity of any transmitters and receivers connected to the spur.

The total combined inductive load presented to a given bus line by a given spur, excluding the connector, shall not exceed 40 nH.

6.1.7.4 *A.C. limits: end spur card.* An end spur card, if fitted, shall only be fitted in a slot that is adjacent to and within 50 mm of either a bus termination, if the latter is fitted directly to the backplane, or an end slot on the bus that carries a general terminator card (see **6.1.6.2**).

The total combined capacitative and inductive loads presented to a given bus line by this type of spur shall not exceed 50 pF (including connector) and 50 nH (excluding connector) respectively.

6.1.7.5 *A.C. limits: end terminator/spur card.* An end terminator/spur card that carries both bus termination networks and spurs (see Figure 3), if fitted, shall only be fitted in an end slot on the bus.

The characteristics of spurs on such a card shall comply with **6.1.7.3** and **6.1.5.2**. The characteristic impedance of bus lines on this type of card shall not fall below 20 Ω and their length shall be included in the total length of the bus.

6.1.7.6 *A.C. limits: connector.* The self inductance of a pair of adjacent connector pins when they are short circuited at the points where they would normally join track on the card or bus assembly shall not exceed 15 nH.

6.1.7.7 *A.C. limits:* 0 V *series inductance.* The total series inductance, including the connector, in the 0 V path between a transmitter package and the reference on the bus shall not exceed *I*, in nH, given by:

$$I = 50/N$$

where

   N is the number of bus transmitters in that package.

NOTE 1   For example, where 20 transmitters share a 0 V path the effective series inductance of that path is required not to exceed 2.5 nH.

NOTE 2   As a guide to the layout of bus line spur track on cards in order that the required a.c. parameters might be achieved, the following information is offered.

Where higher capacity track is used, e.g. buried track at about 0.15 pF/mm, the maximum track length is usually limited by the maximum general spur capacity of 23 pF, after addition of bus transceiver and connector shunt capacities, to approximately 50 mm.

Where lower capacity track is used, e.g. surface track at about 0.09 pF/mm, the maximum track length is usually limited by the maximum general spur inductance of 40 nH to approximately 70 mm.

The lengths for end spur cards are likely to be limited by the maximum inductance to approximately 125 mm for buried track and approximately 100 mm for surface track.

Appendix K describes an extender panel that can be plugged into a device complying with **6.1.7**, without degradation of the performance of the device or of the bus.

6.1.8 *Bus transmitters and receivers.* The characteristics of Eurobus A transmitters and receivers shall comply with the appropriate limits given in Table 8 to Table 13.

NOTE   Because most of the bus lines are connected to a transmitter and a receiver at each spur, the combined characteristics of a transmitter/receiver pair are more significant than the characteristics of an individual transmitter or receiver.

Where a given bus line is connected to a transmitter or a receiver at a given spur, the characteristics of that transmitter or receiver shall fall within the limits specified for a transmitter/receiver pair.

Where a given bus line is connected to more than one transmitter or receiver at a given spur, the combined effect of the transmitters and receivers shall *either:*

   a) fall within the limits specified for a single transmitter/receiver pair; *or*

   b) be taken into account when determining whether the maximum number of spurs available to the particular implementation of the bus needs to be reduced below that nominally available. (See **6.3** for assembled bus requirements.)

Unless otherwise stated in this standard, all requirements shall be complied with over the full operational temperature range for the version of the bus in question (see **0.8**) and over the appropriate supply voltage tolerances given in Table 8.

6.1.9 *Bus transceiver characteristics (of devices on cards plugged into the bus).* The bus transceiver characteristics shall be as given in Table 8 to Table 11. For the properties given in Table 9, Table 10 and Table 11, the values shall be determined as described in BS 9400.

Table 8 — Power supply ranges at the bus transmitters and receivers

| Characteristics | Bus version | Limit | |
		Min.	Max.
Supply voltage V_{cc}	Commercial	V 4.75	V 5.25
Supply voltage V_{cc}	Military	4.5	5.5

Typical
bus line
on
backplane

TERMINATION
NETWORK

Spurs to bus transmitters/
receivers on card

NOTE   Reproduced with permission of Ministry of Defence from Ministry of Defence Standard 00-20.

Figure 3 — End terminator/spur card
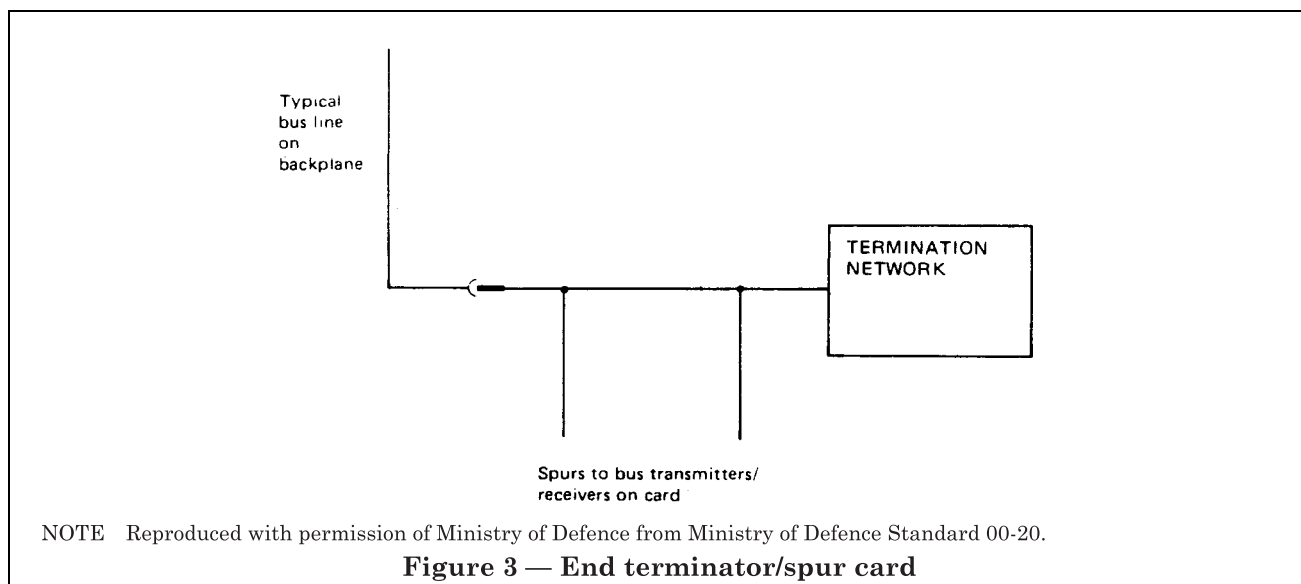
Table 9 — D.C. characteristics of the bus transmitter/receiver pair

Characteristics	Methods of test	Limit (max.)	BS 9400 method
High state input current I_{IH}	$V_{IH} = 2.4$ V Transmitters off $V_{cc,min} \leqslant V_{cc} \leqslant V_{cc,max}$	300 A	2004
	$V_{IH} = 5.25$ V Transmitters off $V_{cc,min} \leqslant V_{cc} \leqslant V_{cc,max}$	1 mA	2004
Low state input current $- I_{IL}$	$V_{IL} = 0.4$ V Transmitters off $V_{cc,min} \leqslant V_{cc} \leqslant V_{cc,max}$	200 A	2003

Table 10 — D.C. characteristics of the bus receiver

Characteristic	Methods of test	Limit		BS 9400 method
		Min.	Max.	
High state input current I_{IH}	$V_{IH} = 2.4$ V $V_{cc,min} \leqslant V_{cc} \leqslant V_{cc,max}$	—	300 A	2004
	$V_{IH} = 5.25$ V $V_{cc,min} \leqslant V_{cc} \leqslant V_{cc,max}$	—	1 mA	2004
Low state input current $- I_{IL}$ (all bus lines except Reset)	$V_{IL} = 0.4$ V $V_{cc,min} \leqslant V_{cc} \leqslant V_{cc,max}$	—	200 A	2003
Low state input current $- I_{IL}$ (Reset line only)	$V_{IL} = 0.4$ V $V_{cc,min} \leqslant V_{cc} \leqslant V_{cc,max}$	—	400 A	2003
Low state input voltage V_{IL}		—	0.8 V	2000
High state input voltage V_{IH}		2 V	—	2000

Table 11 — D.C. characteristics of the bus transmitter

| Characteristic | Methods of test | Limit | | BS 9400 method |
		Min.	Max.	
Low state output current I_{OL} (all bus lines except Request and Reset)	Commercial version Military version	48 mA 50 mA	— —	2016
Low state output current I_{OL} (Request lines only)	Commercial version Military version	29 mA 30 mA	— —	2016
Low state output current I_{OL} (Reset line only)	Commercial version Military version	54 mA 56 mA	— —	2016
High state leakage I_{OHX}	$V_{OH} = 2.4$ V	—	100 µA	2013
Low state output voltage V_{OL}	at rated I_{OL} min.	—	0.5 V	2016

Table 12 — A.C. noise rejection of the bus receiver

| Characteristic | Methods of test | Limit | |
		Min.	Max.
A.C. noise rejection[a]	See Appendix M	See Appendix M	
Pulse width		15 ns	—
Pulse height (positive-going) or depth (negative-going)		1 V	—

[a] The a.c. noise rejection requirement specified applies to the cycle control lines, namely Bus Grant, Cycle Begin, Cycle Response, Cycle Finish, and to Cycle Abort, See also **6.3.4**.

6.2 Maximum number of transmitters and receivers on a line.
The maximum number of spurs that shall be connected to Eurobus A is 20.

NOTE 1   This requirement assumes full compliance of spurs, lines and transmitters. The number is determined by the combined characteristics of transmitters, receivers and the interconnection method. They include:

a) the physical construction of the bus line;

b) the current-sinking capability of the transmitter elements;

c) the current sourced by receivers to an active (low) input state or required by receivers from a quiescent (high) input stage;

d) the shunt impedance due to spurs including the interface devices so connected;

e) the series inductance in the 0 V returns from transceivers to the bus reference 0 V.

NOTE 2   The noise immunity of the bus will depend to some extent on the precise switching levels of the logic family or families connected to it. However, as a corollary of the electrical requirements, the minimum d.c. noise immunities under worst case conditions are:

a) bus line quiescent: greater than 400 mV;

b) bus line active: greater than 300 mV.

6.3 Electrical compliance of the assembled bus

6.3.1 *Conditions for compliance.* When the bus has been assembled with the appropriate complement of spurs, it shall comply with **6.3.2** to **6.3.5**.

Table 13 — A.C. requirements of the bus transmitter

| Characteristic | Methods of test | Limit | |
		Min.	Max.
Rise time T_R from + 0.8 V to + 3.0 V when transmitter is turned off	Test circuit as shown in Figure 4	10 ns	25 ns
Fall time T_F from + 3.0 V to 0.8 V when transmitter is turned on	Test circuit as shown in Figure 4	5 ns	25 ns
Transient sink current	See Appendix M	60 mA	—

NOTE   Reproduced with permission of Ministry of Defence from Ministry of Defence Standard 00-20.

Figure 4 — Test circuit
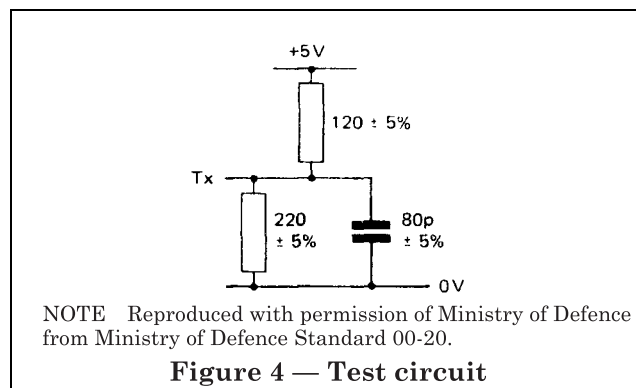
6.3.2 *D.C. limits.* In order to ensure that the quiescent logic level remains within the specified region, the total current drawn from a line that needs to be supplied by the terminations shall not exceed the limits given in Table 14.

Table 14 — Current drawn from a bus line in the quiescent state

Bus version	Conditions	Limit (max.)
		mA
Commercial	0 °C to + 70 °C V_{BUS} = 2.4 V	7.2
Military	− 55 °C to + 125 °C V_{BUS} = 2.4 V	5.0

In order to ensure that the active logic level remains within the specified region, the total current output from the various devices, excluding terminations, to an active bus line shall not exceed the limits given in Table 15.

Table 15 — Current output to a bus line in the active state

Bus version	Conditions	Limit (max.)
		mA
Commercial	0 °C to + 70 °C V_{BUS} = 0.4 V	− 4
Military	− 55 °C to + 125 °C V_{BUS} = 0.4 V	− 4
NOTE The a.c. limits shown in Figure 5 are primarily concerned with the quality of the waveforms on the bus lines and the ability of devices connected to the bus to reject internally induced noise on those waveforms.		

6.3.3 *Bus waveforms.* If any spurs and/or bus connections do not comply with **6.3.2** fully, the physical characteristics of the bus and the number of spurs that may be connected to it shall be adjusted so that *after assembly* the bus waveforms shall comply with the following requirements.

Any perturbations on a positive or negative edge shall be less than 1.0 V amplitude and less than 15 ns pulse width (see Figure 5). The waveform shall comply with the limits given in Table 16 and shown in Figure 5.

6.3.4 *Bus receiver noise immunity.* The performance of the receiver shall be within the limits given in Table 10 when noise within the limits given in Table 16 and shown in Figure 5 is present at the input.

NOTE 1   When the bus receiver is implemented using discrete components or a simple transistor-transistor logic (TTL) (or similar) receiver, compliance with **6.3.4** ensures that perturbations, within the limits given in Table 16 and shown in Figure 5, do not cause any change in the receiver output signal that might cause malfunction in any module logic using the receiver.

NOTE 2   When the bus receiver is part of a more complex integrated circuit, compliance with **6.3.4** ensures that perturbations within the bounds given in Table 16 and shown in Figure 5 do not cause erroneous signals to be output to the module logic connected to it.

Table 16 — Properties of waveform

Parameter	Limit (max.)
Amplitude of perturbation, V	1.0 V
Width of perturbation, t_1	15 ns
Rise time, t_r	35 ns
Fall time, t_f	25 ns

6.3.5 *Connector allocations.* The allocation of bus signals to connector pins shall be as specified for 8, 16, 24 and 32-bit data width buses in Appendix E.

6.4 Timing

NOTE   The operation of the Eurobus protocols, as defined by the rules of **5.4**, is theoretically independent of constraints on the timing of events. In practice, however, an event at one device is not immediately perceived by another device on the bus and two events occurring simultaneously at one device on the bus may not be perceived simultaneously by another. This occurs as a result of the finite propagation and settling times of the signals on the bus lines.

The propagation and settling times are determined by the physical length of the bus, the electrical requirements specified, the quality of the match between the bus terminations and the effective characteristic impedance of the bus lines, and the detection thresholds of the receiving circuits, etc.

It is therefore necessary to impose timing constraints that specify the minimum time that shall elapse between the fulfilment of all the logical conditions necessary to enable certain events, according to the bus rules and the occurrence of the event itself. In each case the rule, the time and the reason for the constraint is given in **6.4.1** and **6.4.2**.

Events on which no constraints are placed may take place as soon as the device generating the event has perceived that the conditions enabling that event have been met. Detailed examples are given in Appendix L.

6.4.1 *Settling times.* Assuming that the specified electrical requirements are complied with and in order to guarantee that the bus lines whose state has been changed by one event (e.g. when the master holds an address on the bus) have stabilized before a device recognizes that another event has occurred (e.g. when the master holds $\overline{CcBn}$ active to signal the presence of an address on the bus), appropriate delays shall be applied to the second event. The amount of delay required shall depend on whether the first event involves a quiescent to active or active to quiescent change.

NOTE   In general the delays are:
   a) 25 ns where the first event involves quiescent to active transitions only;
   b) 35 ns where the first event involves any active to quiescent transitions.
The detailed requirements are specified in **6.4.2**.

6.4.2 *Timing.* Timing shall be according to the values given in Table 17 where the protocol rules are identified in column 1 by the designations used in clause **5**.

6.5 Power supply failure

6.5.1 *Bus supplies*

6.5.1.1 + 5 V *bus supply*. Failure of the + 5 V bus supply shall be assumed to render the bus inoperable.

6.5.1.2 *Other bus supplies.* Failure of any other bus supplies shall only effect those devices that use the supply or supplies concerned.

6.5.2 *Card supplies*

6.5.2.1 *Effect of failure on the system.* The failure of one (or more) of the power supplies to or on a given card shall not result in damage to other cards in the system that use the supplies concerned.

6.5.2.2 *Effect on card.* The spur loading presented to the bus shall not fall outside the limits specified in **6.1.7** in the event of one or more of the supplies to a given card failing and the card remaining connected to the bus.
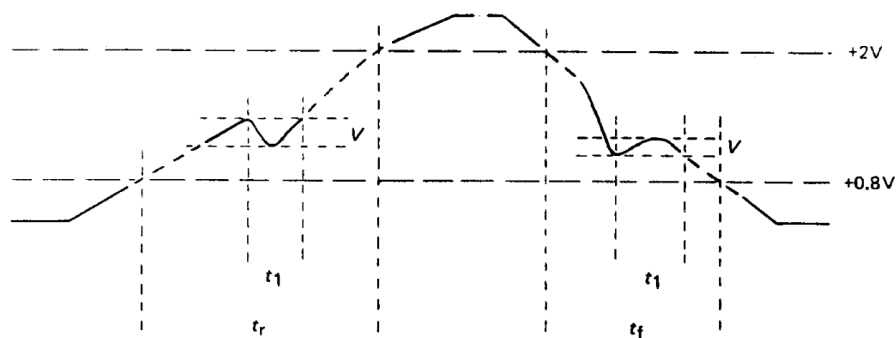
NOTE   Reproduced with permission of Ministry of Defence from Ministry of Defence Standard 00-2, with minor alterations.

Figure 5 — Signal edge characteristics

Table 17 — Eurobus A timing

Rule	Event	Minimum delay	Reason
		ns	
A2	Arbiter holds $\overline{\text{BusGr}}$ active while holding a $\overline{\text{Rq}}$ line active	35	$\overline{\text{Rs}}$ $\overline{\text{CcAbort}}$ etc. are required to settle before the bus is granted
A3b	Arbiter holds $\overline{\text{BusGr}}$ with no request line held	35	The released $\overline{\text{Rq(n)}}$ (rule A9c) is required to settle before $\overline{\text{BusGr}}$ for deallocation is issued
A5aii	Device tests $\overline{\text{Rq(n)}}$ after releasing it in response to $\overline{\text{BusGr}}$ becoming active	35	Rule A4a requires all devices to release their $\overline{\text{Rq}}$ lines in response to $\overline{\text{BusGr}}$ active. $\overline{\text{Rq}}$ lines shall be allowed to settle to the quiescent state before they are tested to determine bus allocation
A5a, iii, iv, v, vii, viii	The master acquires the bus after perceiving the bus free condition	35	$\overline{\text{CcBn}}$, $\overline{\text{CcRes}}$, $\overline{\text{CcFin}}$ and $\overline{\text{CcAbort}}$ are required to settle before the bus is acquired by a new master
A6	Device n tests $\overline{\text{Rq(n)}}$ after releasing it in response to $\overline{\text{BusGr}}$ becoming active	35	As for rule A5
A8d	Arbiter releases $\overline{\text{BusGr}}$ after holding $\overline{\text{CcAbort}}$ active	25	It is required that devices are informed of the fault condition before the arbiter generates an event that would normally occur as a result of a handshake

Table 17 — Eurobus A timing

Rule	Event	Minimum delay	Reason
		ns	
A8e	Arbiter releases $\overline{\text{BusGr}}$ after holding $\overline{\text{Rs}}$ active	25	It is required that devices are informed of the reset condition before the arbiter generates an event that would normally occur as a result of a handshake. No delay is required if $\overline{\text{Rs}}$ is activated by a device other than the arbiter
A9d	Arbiter releases a $\overline{\text{Rq(n)}}$ after holding $\overline{\text{Rs}}$ active	25	As for rule A8d
A9e	Arbiter releases a $\overline{\text{Rq(n)}}$ line after holding $\overline{\text{Rs}}$ active	25	As for rule A8e
A10d	Slave releases $\overline{\text{BusAcq}}$ after holding $\overline{\text{Bus Deallocate}}$ active	25	Guarantees that the arbiter perceives $\overline{\text{Bus Deallocate}}$ active before $\overline{\text{BusAcq}}$ quiescent
A10a A10b	Master releases $\overline{\text{BusAcq}}$ in response to $\overline{\text{CcRes}}$ becoming active	25	Ensures that $\overline{\text{BusAcq}}$ is not released before the cycle is established at all devices
M3b	Master holds $\overline{\text{CcFin}}$ active after releasing the address in a Read cycle	35	The bus lines to be used for data are required to be quiescent before the master signals that the address has been removed by holding $\overline{\text{CcFin}}$
M4a M4b M4c	Master holds $\overline{\text{CcBn}}$ active after holding an address, including $\overline{\text{CcFin}}$ in a Write cycle	25	The address lines (and $\overline{\text{CcFin}}$, if held active) are required to settle before the master signals the presence of an address by holding $\overline{\text{CcBn}}$
M7a M9a	Master releases $\overline{\text{CcBn}}$ after releasing an address (M9ai) and holding Write data (M9aii)	35 25	The lines used to convey data are required to settle after releasing the address (35 ns) and holding the Write data (25 ns), before $\overline{\text{CcBn}}$ is released to signal the presence of Write data. The minimum time of 35 ns applies if the master holds the Write data within 10 ns of releasing the address, since both periods need to be satisfied
M9c M9d M9e M9g	Master releases $\overline{\text{CcBn}}$ after releasing the address	35	The appropriate lines are required to settle to the quiescent state before $\overline{\text{CcBn}}$ is released to signal that the address has been removed
M11a M11e M11g	Master releases $\overline{\text{CcFin}}$ after releasing Write data	35	The highway lines are required to settle to the quiescent state before $\overline{\text{CcFin}}$ is released to signal the removal of Write data

Table 17 — Eurobus A timing

Rule	Event	Minimum delay	Reason
		ns	
M11d M11f	Master releases $\overline{\text{CcFin}}$ after releasing the address	35	The address lines are required to settle to the quiescent state before $\overline{\text{CcFin}}$ is released to signal that the address has been removed
S4b	Slave releases $\overline{\text{CcRes}}$ after holding Read data	25	The highway lines are required to settle before $\overline{\text{CcRes}}$ is released to signal the presence of Read data
S6a S6b S6c	Slave release $\overline{\text{CcFin}}$ after releasing Read data	35	The highway lines are required to settle before $\overline{\text{CcFin}}$ is released to signal the removal of Read data
C2a	Arbiter releases $\overline{\text{CcAbort}}$ after the bus has been freed	35	All the released lines are required to settle before the arbiter releases $\overline{\text{CcAbort}}$. The arbiter may release $\overline{\text{CcAbort}}$ without delay following the fulfilment of the appropriate conditions if it was not holding any other line active when it held $\overline{\text{CcAbort}}$ active
D1a	Slave holds $\overline{\text{Bus Deallocate}}$ on detecting $\overline{\text{BusGr}}$ quiescent	35	Ensures that all the master devices can detect $\overline{\text{BusGr}}$ quiescent before the arbiter holds it active again to signal cycle refusal
D1b	Slave holds $\overline{\text{Bus Deallocate}}$ after holding $\overline{\text{CcRes}}$	25	Ensures that $\overline{\text{CcRes}}$ is received by the Arbiter before $\overline{\text{Bus Deallocate}}$, thus distinguishing a request for the arbiter to ask the master to release the bus for reallocation as soon as possible from a cycle refusal
D2	Slave releases $\overline{\text{Bus Deallocate}}$ after perceiving that $\overline{\text{BusAcq}}$ has been released	35	Ensures that $\overline{\text{BusAcq}}$ has settled before the slave releases $\overline{\text{Bus Deallocate}}$
—	$\overline{\text{Rs}}$ released after being held active	5×10^4	To give time for all actions consequent on reset to be completed before $\overline{\text{Rs}}$ is released

Appendix A Eurobus 10/A logical implementation

A.1 General

This appendix summarizes the Eurobus 10/A implementation of clause **5** relating to highway width and normal/pseudo address space selection.

A.2 Highway

According to **5.2** and **5.3**, the set of highway lines used by a device of 8-bit data width is as follows.

a) Eight data/address lines, $\overline{H(0)}$ to $\overline{H(7)}$, providing for an addressing capability of 256 8-bit words.

b) Two address modifier lines, $\overline{AdM(0)}$ to $\overline{AdM(1)}$. These lines are available for extending the addressing capability up to a maximum of 1 024 8-bit words, but in implementations where an 8-bit data width device shares a bus with wider devices, the requirements of **5.3** apply, and the address range is restricted to 256, 512 or 768 words.

A.3 Normal/pseudo address space selection

According to **5.2.3**, the Byte Address Line, $\overline{BytAd(0)}$, is used alone in this implementation to distinguish accesses to normal address space from accesses to pseudo address space. The Byte Working line is quiescent.

The coding of the Byte Address line is interpreted as given in Table 18.

Table 18 — Eurobus 10/A byte address code

$\overline{BytAd(0)}$	Meaning
Q	Word of 8 bits in normal address space
Acv	Word of 8 bits in pseudo address space
NOTE See note 1 to Table 2.	

Appendix B Eurobus 18/A logical implementation

B.1 General

This appendix summarizes the Eurobus 18/A implementation of clause **5** relating to highway width, byte working and normal/pseudo address space selection.

B.2 The highway

According to **5.2** and **5.3**, the set of highway lines available to devices using the bus is as follows.

a) 16 data/address lines, $\overline{H(0)}$ to $\overline{H(15)}$, providing for an addressing capability of 64k 16-bit words (k = 1 024 words).

b) Two address modifier lines, $\overline{AdM(0)}$ and $\overline{AdM(1)}$. These lines are available for extending the addressing capability up to a maximum of 256k words, but in implementations where a 16-bit data-width device shares a bus with wider or narrower devices, the requirements of **5.3** apply, and the address range is restricted to 64k, or 128k or 192k words.

B.3 Byte mode and normal/pseudo address space selection

According to **5.2.3**, the meanings of the Byte Working and Byte Address codes in the Eurobus 18/A implementation are as given in Table 19.

Table 19 — Eurobus 18/A byte address code

$\overline{BytWk}$	$\overline{BytAd(0)}$	Meaning
Q	Q	Word of 16 bits in normal address space
Q	Acv	Word of 16 bits in pseudo address space
Acv	Q	Least significant byte in normal address space
Acv	Acv	Most significant byte in normal address space
NOTE See note 1 to Table 2.		

Appendix C Eurobus 26/A logical implementation

C.1 General

This appendix summarizes the Eurobus 26/A implementation of clause **5** relating to highway width, byte working and normal/pseudo address space selection.

C.2 The highway

According to **5.2** and **5.3**, the set of highway lines available to devices using the bus is as follows.

a) 24 data/address lines, $\overline{H(0)}$ to $\overline{H(23)}$, providing for an addressing capability of 16M 24-bit words ($M = 1\ 024^2$ words).

b) Two address modifier lines, $\overline{AdM(0)}$ and $\overline{AdM(1)}$. These lines are available for extending the addressing capability up to a maximum of 64M words, but in implementations where a 24-bit data-width device shares a bus with wider or narrower devices, the requirements of **5.3** apply, and the address range is restricted to 16M, 32M or 48M words.

C.3 Byte mode and normal/pseudo address space selection

According to **5.2.3** the meanings of the Byte Working and Byte Address codes in the Eurobus 26/A implementation are as given in Table 20.

Table 20 — Eurobus 26/A byte address code

$\overline{BytWk}$	$\overline{BytAd(1)}$	$\overline{BytAd(0)}$	Meaning
Q	Q	X	Word of 24 bits in normal address space
Q	Acv	X	Word of 24 bits in pseudo address space
Avc	Q	Q	Byte 0 (least significant) in normal address space
Acv	Q	Acv	Byte 1 in normal address space
Acv	Acv	X	Byte 2 (most significant) in normal address space
NOTE See note 1 to Table 2.			

Appendix D Eurobus 34/A logical implementation

D.1 General

This appendix summarizes the Eurobus 34/A implementation of clause **5** relating to the highway width, byte working and normal/pseudo address space selection.

D.2 The highway

According to **5.2** and **5.3**, the set of highway lines available to devices using the bus is as follows.

a) 32 data/address lines, $\overline{H(0)}$ to $\overline{H(31)}$, providing for an addressing capability of 4G 32-bit words ($G = 1\ 024^3$ words).

b) Two address modifier lines, $\overline{AdM(0)}$ to $\overline{AdM(1)}$. These are available for extending the addressing capability up to a maximum of 16G words, but in implementations where a 32-bit data-width device shares a bus with narrower devices, the requirements of **5.3** apply, and the address range is restricted to 4G, 8G or 12G words.

D.3 Byte mode and normal/pseudo address space selection

According to **5.2.3** the meanings of the Byte Working and Byte Address codes in the Eurobus 34/A implementation are as given in Table 21.

Table 21 — Eurobus 34/A byte address code

$\overline{BytWk}$	$\overline{BytAd(1)}$	$\overline{BytAd(0)}$	Meaning
Q	Q	X	Word of 32 bits in normal address space
Q	Acv	X	Word of 32 bits in pseudo address space
Acv	Q	Q	Byte 0 (least significant) in normal address space
Acv	Q	Acv	Byte 1, in normal address space
Acv	Acv	Q	Byte 2, in normal address space
Acv	Acv	Acv	Byte 3 (most significant) in normal address space
NOTE See note 1 to Table 2.			

Appendix E Connector allocation

E.1 Eurobus 10/A

The Eurobus 10/A signals shall be assigned to two rows of pins not more than a nominal 5.04 mm apart on a 2.54 mm pitch connector as given in Table 22 and this allocation ensures:

a) adequate 0 V integrity;

b) adequate freedom from cross-talk between bus signals.

NOTE   Where a particular hardware implementation is intended to support Eurobus 10/A devices only, pins that are unused may be allocated to other purposes. However, it is strongly recommended that due consideration should be given to the allocation of the pins concerned on the connectors for other Eurobus implementations to achieve maximum interchangeability of plug-in cards.

Table 22 — Eurobus 10/A allocation of connector pins to signals

First row	Signal	Second row	Signal
Pin No. 01	$\overline{H(0)}$	Pin No. 01	$\overline{H(1)}$
Pin No. 02	$\overline{H(2)}$	Pin No. 02	$\overline{H(3)}$
Pin No. 03	$\overline{H(4)}$	Pin No. 03	+ 5 V
Pin No. 04	0 V[a]	Pin No. 04	$\overline{H(5)}$
Pin No. 05	$\overline{AdM(1)}$	Pin No. 05	—
Pin No. 06	—	Pin No. 06	$\overline{AdM(0)}$
Pin No. 07	$\overline{Rs}$	Pin No. 07	0 V
Pin No. 08	$\overline{H(6)}$	Pin No. 08	—
Pin No. 09	—	Pin No. 09	—
Pin No. 10	0 V	Pin No. 10	$\overline{CcAbort}$
Pin No. 11	$\overline{BytAd}$	Pin No. 11	$\overline{H(7)}$
Pin No. 12	—	Pin No. 12	$\overline{BusGr}$
Pin No. 13	$\overline{BytWk}$	Pin No. 13	—
Pin No. 14	—	Pin No. 14	$\overline{BusAcq}$
Pin No. 15	0 V	Pin No. 15	—
Pin No. 16	$\overline{CcBn}$	Pin No. 16	+ 5 V
Pin No. 17	—	Pin No. 17	$\overline{It}$
Pin No. 18	—	Pin No. 18	—
Pin No. 19	$\overline{Rq}$	Pin No. 19	—
Pin No. 20	—	Pin No. 20	—
Pin No. 21	0 V	Pin No. 21	—
Pin No. 22	$\overline{BusDeallocate}$	Pin No. 22	$\overline{CcRes}$
Pin No. 23	—	Pin No. 23	0 V
Pin No. 24	—	Pin No. 24	—
Pin No. 25	$\overline{CcFin}$	Pin No. 25	—
Pin No. 26	+ 5 V	Pin No. 26	—
Pin No. 27	—	Pin No. 27	—
Pin No. 28	—	Pin No. 28	—
Pin No. 29	0 V	Pin No. 29	—
Pin No. 30	—	Pin No. 30	—
Pin No. 31	—	Pin No. 31	—
Pin No. 32	Earth[b]	Pin No. 32	—

[a] It is recommended that a leading connection should be used for pin No. 04 on the first row.
[b] It is recommended that provision should be made to earth the front panel of all cards, and that a leading connection should be used.

E.2 Eurobus 18/A

The Eurobus 18/A signals shall be assigned to two rows of pins not more than a nominal 5.04 mm apart on a 2.54 mm pitch connector as given in Table 23 and this allocation ensures:

a) adequate 0 V integrity;

b) adequate freedom from cross-talk between bus signals.

NOTE   Where a particular hardware implementation is intended to support Eurobus 18/A devices only (see Table 22) and possibly Eurobus 10/A devices subject to compatible usage of spare pins on the implementation or implementations concerned, pins that are unused may be allocated to other purposes. However, it is strongly recommended that due consideration should be given to the allocation of the pins concerned on the connectors for other Eurobus implementations to achieve maximum interchangeability of plug-in cards.

Table 23 — Eurobus 18/A allocation of connector pins to signals

First row	Signal	Second row	Signal
Pin No. 01	$\overline{H(0)}$	Pin No. 01	$\overline{H(1)}$
Pin No. 02	$\overline{H(2)}$	Pin No. 02	$\overline{H(3)}$
Pin No. 03	$\overline{H(4)}$	Pin No. 03	+ 5 V
Pin No. 04	0 V[a]	Pin No. 04	$\overline{H(5)}$
Pin No. 05	$\overline{AdM(1)}$	Pin No. 05	—
Pin No. 06	—	Pin No. 06	$\overline{AdM(0)}$
Pin No. 07	$\overline{Rs}$	Pin No. 07	0 V
Pin No. 08	$\overline{H(6)}$	Pin No. 08	—
Pin No. 09	—	Pin No. 09	—
Pin No. 10	0 V	Pin No. 10	$\overline{CcAbort}$
Pin No. 11	$\overline{BytAd}$	Pin No. 11	$\overline{H(7)}$
Pin No. 12	—	Pin No. 12	$\overline{BusGr}$
Pin No. 13	$\overline{BytWk}$	Pin No. 13	—
Pin No. 14	$\overline{H(8)}$	Pin No. 14	$\overline{BusAcq}$
Pin No. 15	0 V	Pin No. 15	$\overline{H(9)}$
Pin No. 16	$\overline{CcBn}$	Pin No. 16	+ 5 V
Pin No. 17	—	Pin No. 17	$\overline{It}$
Pin No. 18	—	Pin No. 18	—
Pin No. 19	$\overline{Rq}$	Pin No. 19	—
Pin No. 20	—	Pin No. 20	—
Pin No. 21	0 V	Pin No. 21	—
Pin No. 22	$\overline{BusDeallocate}$	Pin No. 22	$\overline{CcRes}$
Pin No. 23	$\overline{H(10)}$	Pin No. 23	0 V
Pin No. 24	$\overline{H(12)}$	Pin No. 24	$\overline{H(11)}$
Pin No. 25	$\overline{CcFin}$	Pin No. 25	$\overline{H(13)}$
Pin No. 26	+ 5 V	Pin No. 26	—
Pin No. 27	—	Pin No. 27	—
Pin No. 28	$\overline{H(14)}$	Pin No. 28	$\overline{H(15)}$
Pin No. 29	0 V	Pin No. 29	—
Pin No. 30	—	Pin No. 30	—
Pin No. 31	—	Pin No. 31	—
Pin No. 32	Earth[b]	Pin No. 32	—

[a] It is recommended that a leading connection should be used for pin No. 04 on the first row.
[b] It is recommended that provision should be made to earth the front panel of all cards, and that a leading connection should be used.

Example. Table 24 gives the connector allocation used on a specific implementation of Eurobus 18/A on double Eurocard, 160 mm × 233.4 mm, complying with BS 5954.

In this implementation the bus is assigned to the lower (B) connector of the pair on the card when viewed from the front, component side to the right.

Table 24 — Example of Eurobus 18/A signal allocations in an actual implementation

Row a	Signal	Row c	Signal
Pin No. 01	$\overline{H(0)}$	Pin No. 01	$\overline{H(1)}$
Pin No. 02	$\overline{H(2)}$	Pin No. 02	$\overline{H(3)}$
Pin No. 03	$\overline{H(4)}$	Pin No. 03	+ 5 V
Pin No. 04	0 V (leading)	Pin No. 04	$\overline{H(5)}$
Pin No. 05	$\overline{AdM(1)}$	Pin No. 05	—
Pin No. 06	$\overline{Fa}$	Pin No. 06	$\overline{AdM(0)}$
Pin No. 07	$\overline{Rs}$	Pin No. 07	0 V
Pin No. 08	$\overline{H(6)}$	Pin No. 08	$\overline{FaRs}$
Pin No. 09	—	Pin No. 09	− 5 V
Pin No. 10	0 V	Pin No. 10	$\overline{CcAbort}$
Pin No. 11	$\overline{BytAd}$	Pin No. 11	$\overline{H(7)}$
Pin No. 12	− 12 V	Pin No. 12	$\overline{BusGr}$
Pin No. 13	$\overline{BytWk}$	Pin No. 13	+ 12 V
Pin No. 14	$\overline{H(8)}$	Pin No. 14	$\overline{BusAcq}$
Pin No. 15	0 V	Pin No. 15	$\overline{H(9)}$
Pin No. 16	$\overline{CcBn}$	Pin No. 16	+ 5 V
Pin No. 17	Address	Pin No. 17	$\overline{It}$
Pin No. 18	Selection	Pin No. 18	
Pin No. 19	$\overline{Rq}$	Pin No. 19	Address Selection
Pin No. 20	—	Pin No. 20	
Pin No. 21	0 V	Pin No. 21	
Pin No. 22	$\overline{BusDeallocate}$	Pin No. 22	$\overline{CcRes}$
Pin No. 23	$\overline{H(10)}$	Pin No. 23	0 V
Pin No. 24	$\overline{H(12)}$	Pin No. 24	$\overline{H(11)}$
Pin No. 25	$\overline{CcFin}$	Pin No. 25	$\overline{H(13)}$
Pin No. 26	+ 5 V	Pin No. 26	—
Pin No. 27	Inrush Control leading	Pin No. 27	—
Pin No. 28	$\overline{H(14)}$	Pin No. 28	$\overline{H(15)}$
Pin No. 29	0 V	Pin No. 29	—
Pin No. 30	—	Pin No. 30	+ 24 V
Pin No. 31	0 V (analogue, leading)	Pin No. 31	
Pin No. 32	Earth (leading)	Pin No. 32	− 24 V

E.3 Eurobus 26/A

The Eurobus 26/A signals shall be assigned to two rows of pins not more than a nominal 5.04 mm apart on a 2.54 mm pitch connector as given in Table 25 and this allocation ensures:

a) adequate 0 V integrity;

b) adequate freedom from cross-talk between bus signals.

NOTE Where a particular hardware implementation is intended to support Eurobus 26/A devices only, and possibly Eurobus 10/A and 18/A devices subject to compatible usage of spare pins on the implementation or implementations concerned, pins that are unused may be allocated to other purposes, However, it is strongly recommended that due consideration should be given to the allocation of the pins concerned on the connectors for other Eurobus implementations to achieve the maximum interchangeability of plug-in cards.

Table 25 — Eurobus 26/A allocation of connector pins to signals

First row	Signal	Second row	Signal
Pin No. 01	$\overline{H(0)}$	Pin No. 01	$\overline{H(1)}$
Pin No. 02	$\overline{H(2)}$	Pin No. 02	$\overline{H(3)}$
Pin No. 03	$\overline{H(4)}$	Pin No. 03	+ 5 V
Pin No. 04	0 V[a]	Pin No. 04	$\overline{H(5)}$
Pin No. 05	$\overline{AdM(1)}$	Pin No. 05	$\overline{BytAd(0)}$
Pin No. 06	—	Pin No. 06	$\overline{AdM(0)}$
Pin No. 07	$\overline{Rs}$	Pin No. 07	0 V
Pin No. 08	$\overline{H(6)}$	Pin No. 08	—
Pin No. 09	—	Pin No. 09	—
Pin No. 10	0 V	Pin No. 10	$\overline{CcAbort}$
Pin No. 11	$\overline{BytAd(1)}$	Pin No. 11	$\overline{H(7)}$
Pin No. 12	—	Pin No. 12	$\overline{BusGr}$
Pin No. 13	$\overline{BytWk}$	Pin No. 13	—
Pin No. 14	$\overline{H(8)}$	Pin No. 14	$\overline{BusAcq}$
Pin No. 15	0 V	Pin No. 15	$\overline{H(9)}$
Pin No. 16	$\overline{CcBn}$	Pin No. 16	+ 5 V
Pin No. 17	—	Pin No. 17	$\overline{It}$
Pin No. 18	—	Pin No. 18	—
Pin No. 19	$\overline{Rq}$	Pin No. 19	—
Pin No. 20	—	Pin No. 20	—
Pin No. 21	0 V	Pin No. 21	—
Pin No. 22	$\overline{BusDeallocate}$	Pin No. 22	$\overline{CcRes}$
Pin No. 23	$\overline{H(10)}$	Pin No. 23	0 V
Pin No. 24	$\overline{H(12)}$	Pin No. 24	$\overline{H(11)}$
Pin No. 25	$\overline{CcFin}$	Pin No. 25	$\overline{H(13)}$
Pin No. 26	+ 5 V	Pin No. 26	$\overline{H(16)}$
Pin No. 27	$\overline{H(22)}$	Pin No. 27	$\overline{H(17)}$
Pin No. 28	$\overline{H(14)}$	Pin No. 28	$\overline{H(15)}$
Pin No. 29	0 V	Pin No. 29	$\overline{H(18)}$
Pin No. 30	$\overline{H(23)}$	Pin No. 30	$\overline{H(19)}$
Pin No. 31	$\overline{H(21)}$	Pin No. 31	$\overline{H(20)}$
Pin No. 32	Earth[b]	Pin No. 32	0 V

[a] It is recommended that a leading connection should be used for pin No. 04 on the first row.
[b] It is recommended that provision should be made to earth the front panel of all cards, and that a leading connection should be used.

E.4 Eurobus 34/A

The Eurobus 34/A signals shall be assigned to two rows of pins not more than a nominal 5.04 mm apart on 2.54 mm pitch connectors as shown in Table 26 and Table 27 and this allocation ensures:

a) adequate 0 V integrity;

b) adequate freedom from cross-talk between bus signals.

NOTE   Eurobus 34/A requires more connections than can be allocated to a single 64-way connector; it is therefore recommended that the additional signals should be allocated to a second connector on the card concerned.

The allocations shown in Table 26 and Table 27 assume that the connectors are mounted such that the pin No. 1 end of the connector, whose allocation is shown in Table 26, is adjacent to but at an unspecified distance from the pin No. 32 end of the connector whose allocation is shown in Table 27. These connectors could, for example, be the B (lower) and A (upper) connectors respectively on a double Eurocard.

Where a particular hardware implementation is intended to support Eurobus 34/A devices only, and possibly Eurobus 10/A, 18/A and 26/A devices, subject to compatible usage of spare pins and connectors on the implementations concerned, pins that are unused may be allocated to other purposes. However, it is strongly recommended that due consideration should be given to the allocation of the pins concerned on the connectors for other Eurobus implementations to achieve the maximum interchangeability of plug-in cards.

Table 26 — Eurobus 34/A allocation of connector B pins to signals

First row	Signal	Second row	Signal
Pin No. 01	$\overline{H(0)}$	Pin No. 01	$\overline{H(1)}$
Pin No. 02	$\overline{H(2)}$	Pin No. 02	$\overline{H(3)}$
Pin No. 03	$\overline{H(4)}$	Pin No. 03	+ 5 V
Pin No. 04	0 V[a]	Pin No. 04	$\overline{H(5)}$
Pin No. 05	$\overline{AdM(1)}$	Pin No. 05	$\overline{BytAd(0)}$
Pin No. 06	—	Pin No. 06	$\overline{AdM(0)}$
Pin No. 07	$\overline{Rs}$	Pin No. 07	0 V
Pin No. 08	$\overline{H(6)}$	Pin No. 08	—
Pin No. 09	—	Pin No. 09	—
Pin No. 10	0 V	Pin No. 10	$\overline{CcAbort}$
Pin No. 11	$\overline{BytAd(1)}$	Pin No. 11	$\overline{H(7)}$
Pin No. 12	—	Pin No. 12	$\overline{BusGr}$
Pin No. 13	$\overline{BytWk}$	Pin No. 13	—
Pin No. 14	$\overline{H(8)}$	Pin No. 14	$\overline{BusAcq}$
Pin No. 15	0 V	Pin No. 15	$\overline{H(9)}$
Pin No. 16	$\overline{CcBn}$	Pin No. 16	+ 5 V
Pin No. 17	—	Pin No. 17	$\overline{It}$
Pin No. 18	—	Pin No. 18	—
Pin No. 19	$\overline{Rq}$	Pin No. 19	—
Pin No. 20	—	Pin No. 20	—
Pin No. 21	0 V	Pin No. 21	—
Pin No. 22	$\overline{BusDeallocate}$	Pin No. 22	$\overline{CcRes}$
Pin No. 23	$\overline{H(10)}$	Pin No. 23	0 V
Pin No. 24	$\overline{H(12)}$	Pin No. 24	$\overline{H(11)}$
Pin No. 25	$\overline{CcFin}$	Pin No. 25	$\overline{H(13)}$
Pin No. 26	+ 5 V	Pin No. 26	$\overline{H(16)}$
Pin No. 27	$\overline{H(22)}$	Pin No. 27	$\overline{H(17)}$
Pin No. 28	$\overline{H(14)}$	Pin No. 28	$\overline{H(15)}$
Pin No. 29	0 V	Pin No. 29	$\overline{H(18)}$
Pin No. 30	$\overline{H(23)}$	Pin No. 30	$\overline{H(19)}$
Pin No. 31	$\overline{H(21)}$	Pin No. 31	$\overline{H(20)}$
Pin No. 32	Earth[b]	Pin No. 32	0 V

[a] It is recommended that a leading connection should be used for pin No. 04 on the first row.
[b] It is recommended that provision should be made to earth the front panel of all cards, and that a leading connection should be used.

Table 27 — Eurobus 34/A allocation of connector A pins to signals

First row	Signal	Second row	Signal
Pin No. 01	—	Pin No. 01	—
Pin No. 02	—	Pin No. 02	—
Pin No. 03	—	Pin No. 03	—
Pin No. 04	—	Pin No. 04	—
Pin No. 05	—	Pin No. 05	—
Pin No. 06	—	Pin No. 06	—
Pin No. 07	—	Pin No. 07	—
Pin No. 08	—	Pin No. 08	—
Pin No. 09	—	Pin No. 09	—
Pin No. 10	—	Pin No. 10	—
Pin No. 11	—	Pin No. 11	—
Pin No. 12	—	Pin No. 12	—
Pin No. 13	—	Pin No. 13	—
Pin No. 14	—	Pin No. 14	—
Pin No. 15	—	Pin No. 15	—
Pin No. 16	—	Pin No. 16	—
Pin No. 17	—	Pin No. 17	—
Pin No. 18	—	Pin No. 18	—
Pin No. 19	—	Pin No. 19	—
Pin No. 20	—	Pin No. 20	—
Pin No. 21	—	Pin No. 21	—
Pin No. 22	—	Pin No. 22	—
Pin No. 23	—	Pin No. 23	—
Pin No. 24	—	Pin No. 24	—
Pin No. 25	—	Pin No. 25	—
Pin No. 26	+ 5 V	Pin No. 26	$\overline{H(24)}$
Pin No. 27	$\overline{H(30)}$	Pin No. 27	$\overline{H(25)}$
Pin No. 28	—	Pin No. 28	0 V
Pin No. 29	0 V	Pin No. 29	$\overline{H(26)}$
Pin No. 30	$\overline{H(31)}$	Pin No. 30	$\overline{H(27)}$
Pin No. 31	$\overline{H(29)}$	Pin No. 31	$\overline{H(28)}$
Pin No. 32	—	Pin No. 32	0 V

Appendix F Examples of application of protocol rules

F.1 General

Some examples of the application of the Eurobus protocol rules in the allocation of the bus to a requesting device are given in this Appendix A. A device to which the bus is granted may use it either for a Read, Write or Vector cycle, or to generate an Interrupt. Examples of Read, Write and Vector cycles are given in **F.6**, **F.7** and **F.8**.

The examples cover allocation of an idle bus, or a bus in use following a previous allocation, and of a bus being held or retained by the current master. They are illustrative and do not cover all possible cases.

NOTE   In the figures contained in this appendix as illustrative examples, the following conventions apply:
a) waveforms on the bus lines are shown high when quiescent and low when active;
b) when a particular line can be held active by two devices at any time, the period during which the line is active due to one device only is shown in a broken line;
c) periods during which the state of a line may change at an undefined time relative to other transmissions shown, are shown by hatching.

F.2 Allocation of an idle bus

The sequence of actions for the allocation of an idle bus is shown in Figure 6 and given in Table 28.
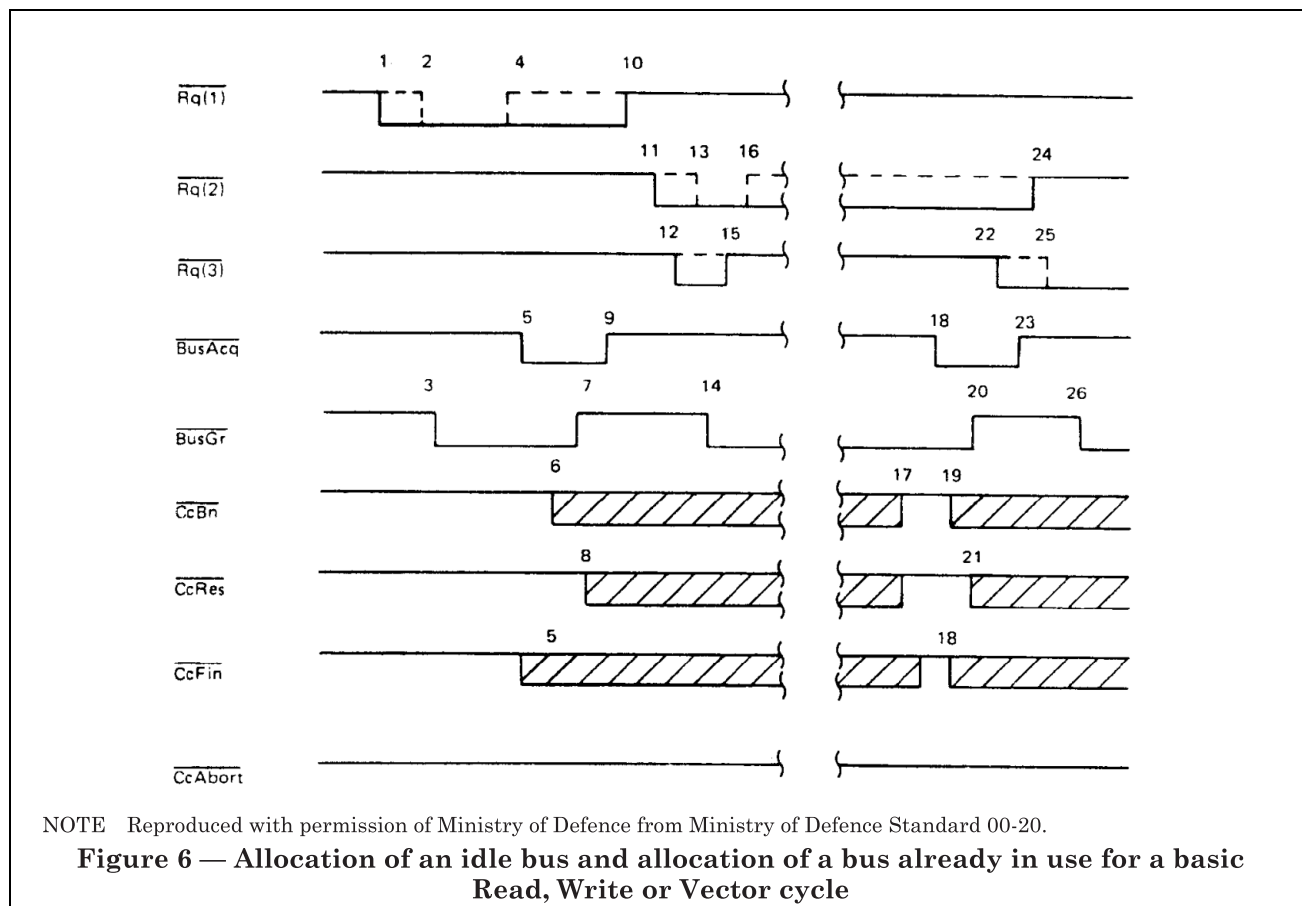

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Figure 6 — Allocation of an idle bus and allocation of a bus already in use for a basic Read, Write or Vector cycle

Table 28 — Allocation of an idle bus

Rule	Event	Comment
A1	1	A device (device 1) makes it request by holding $\overline{Rq(1)}$ active
A2	2	Because $\overline{BusAcq}$, $\overline{It}$ and $\overline{BusDeallocate}$ are quiescent, the arbiter is able to grant the request immediately, and does so by holding $\overline{Rq1}$ active
A3	3	The arbiter holds $\overline{BusGr}$ active to indicate that the allocation has been made (rule A3a)
A4	4	In response to $\overline{BusGr}$ becoming active all devices bidding for the bus are required to withdraw their requests for bus allocation. After a fixed time (see **6.4**), the bidding devices examine the state of their $\overline{Rq}$ lines to determine which device has been granted use of the bus
A5a	5	The selected device recognizes that:
		a) its $\overline{Rq}$ line is still active;
		b) the bus is free ($\overline{CcBn}$, $\overline{CcRes}$, $\overline{CcFin}$ and $\overline{CcAbort}$ are all quiescent) and responds
M1 M2		by activating $\overline{BusAcq}$ and holding the address on the bus. On activating $\overline{BusAcq}$, the device becomes locked (rule A7a) and can no longer place requests
M4a, b or c	6	The master activates $\overline{CcBn}$
A8a	7	In response to $\overline{BusAcq}$ active, the arbiter releases the $\overline{BusGr}$ line as an indication to bidding devices that they may replace any outstanding requests
S1	8	The cycle is established when the selected slave activates $\overline{CcRes}$. In order to guarantee a finite quiescent period on $\overline{BusGr}$, $\overline{CcRes}$ is not activated while $\overline{BusGr}$ is active
A10a	9	The master releases $\overline{BusAcq}$ in basic Read, Write and Vector cycles when the cycle is established. The arbiter may now arbitrate outstanding requests. The master does not place further requests until it ceases to be locked (rule A12a), however

F.3 Reallocation of a bus being used for a basic cycle

The sequence of actions for reallocation of a bus being used for a basic cycle is shown in Figure 6 and is given in Table 29.

Table 29 — Reallocation of a bus being used for a basic cycle

Rule	Event	Comment
A9a	10	In response to event 9, the arbiter releases $\overline{\mathrm{Rq(1)}}$.
A1	11, 12	Devices make bids for the bus by activating their $\overline{\mathrm{Rq}}$ lines while $\overline{\mathrm{BusGr}}$ is quiescent.
A2	13	The arbiter grants the device 2 request by holding $\overline{\mathrm{Rq(2)}}$ active.
A3	14	The arbiter sets $\overline{\mathrm{BusGr}}$ active to indicate that the allocation has been made.
A4	15, 16	In response to $\overline{\mathrm{BusGr}}$, all devices bidding for the bus are required to withdraw their request for bus allocation. After a fixed time (see **6.4**), bidding devices examine the state of their $\overline{\mathrm{Rq}}$ lines to determine which device has been granted use of the bus.
M5a M1 et seq	17	Nothing further happens until the device detects that $\overline{\mathrm{CcBn}}$, $\overline{\mathrm{CcRes}}$, $\overline{\mathrm{CcFin}}$ and $\overline{\mathrm{CcAbort}}$ are all quiescent.
	18	The selected device recognizes that its $\overline{\mathrm{Rq}}$ line is still active and responds by activating $\overline{\mathrm{BusAcq}}$ and holding the address, on the bus. The device is now locked (rule A7a).
M4a, b or c	19	The appropriate cycle may now proceed ($\overline{\mathrm{CcBn}}$ active).
A7a	20	In response to $\overline{\mathrm{BusAcq}}$ active, the arbiter releases the $\overline{\mathrm{BusGr}}$ line as an indication to devices that they may replace any outstanding requests.
S1	21	The slave holds $\overline{\mathrm{CcRes}}$ active on recognition of the address.
A1	22	Device 3 replaces its outstanding request.
A10a	23	$\overline{\mathrm{BusAcq}}$ is released, for basic Read, Write and Vector cycles only, as soon as the master cycle is established ($\overline{\mathrm{CcRes}}$ active). The arbiter may now arbitrate outstanding requests.
A9a or A9b	24	As a result of 22 or 23, whichever happens first, the arbiter releases $\overline{\mathrm{Rq(2)}}$.
A2	25	The arbiter grants use of the bus to device 3 by holding $\overline{\mathrm{Rq(3)}}$ active.
A3	26	The arbiter sets $\overline{\mathrm{BusGr}}$ active to indicate that the allocation has been made.

F.4 Reallocation of a bus being used for a Hold cycle or Retain cycle

Figure 7 shows a typical sequence of actions. Device 1 requests a cycle that turns out to be a Hold cycle, and the bus is held for several cycles by device 1. Device 2 then makes its bid for the bus which is released by device 1 as soon as possible. The events are given in Table 30.
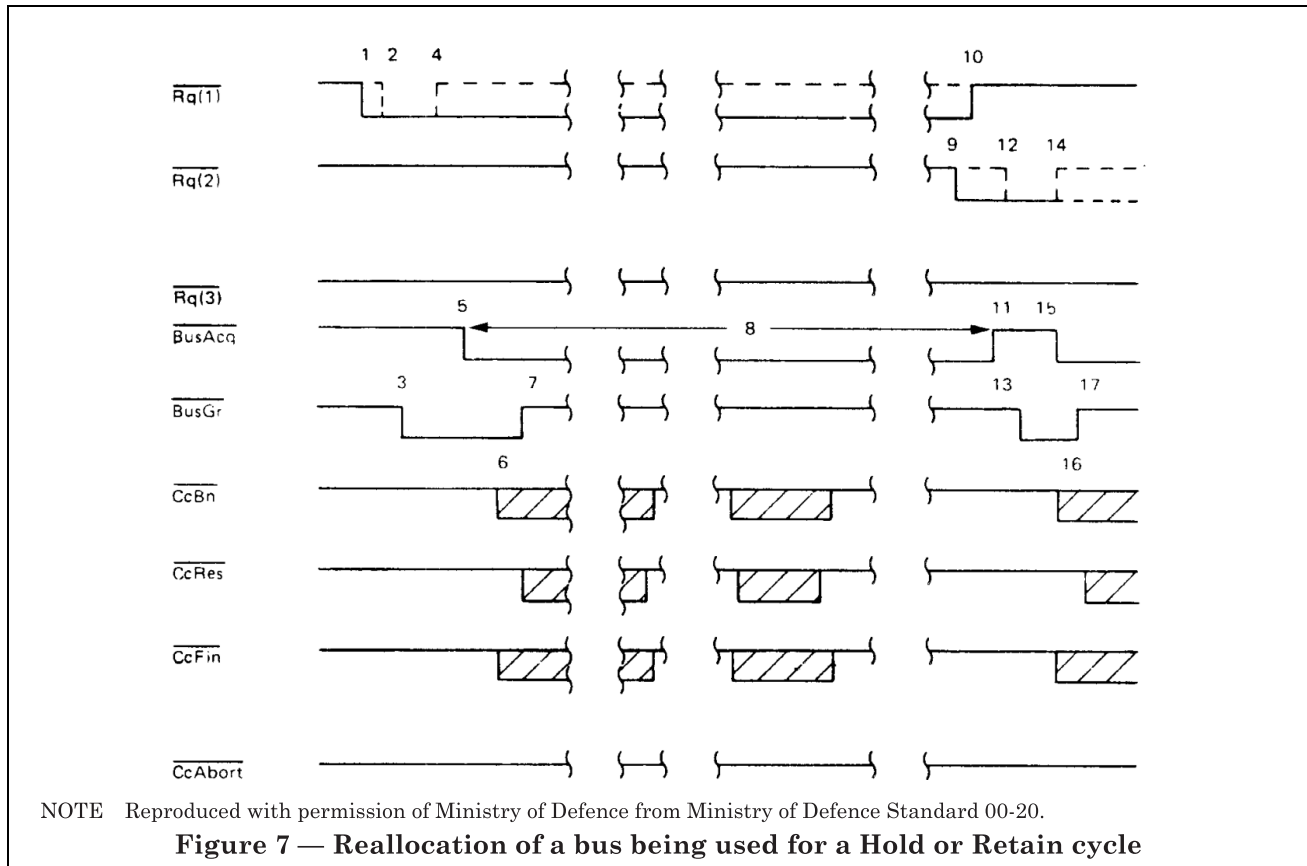

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Figure 7 — Reallocation of a bus being used for a Hold or Retain cycle

Table 30 — Reallocation of a bus being used for a Hold or Retain cycle

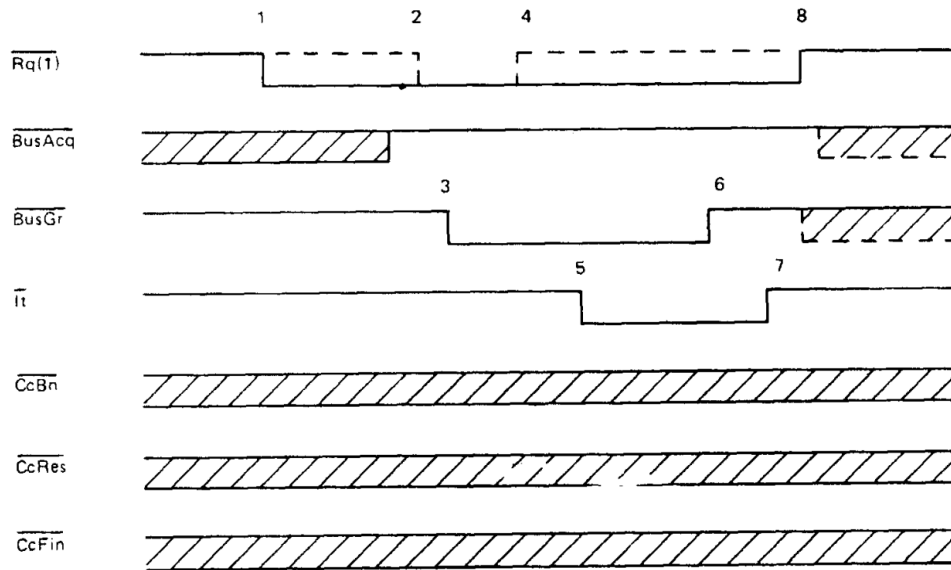| Rule	Event	Comment
A1	1	The would-be master (device 1) makes its request by holding $\overline{Rq(1)}$ active
A2	2	Because $\overline{BusAcq}$, $\overline{It}$ and $\overline{BusDeallocate}$ are quiescent, the arbiter is able to grant the request immediately, and does so by also holding $\overline{Rq(1)}$ active
A3	3	The arbiter holds $\overline{BusGr}$ active to indicate that the allocation has been made
A4	4	In response to $\overline{BusGr}$ active all bidding devices are required to withdraw their requests for bus allocation. After a fixed time (see **6.4**) the bidding devices examine the state of their $\overline{Rq}$ lines to determine which device has been granted use of the bus
A5a	5	Device 1 recognizes that: a) its $\overline{Rq}$ line is still active; b) $\overline{CcBn}$, $\overline{CcRes}$, $\overline{CcFin}$ and $\overline{CcAbort}$ are all quiescent and responds by holding $\overline{BusAcq}$ active. It therefore becomes locked (rule A7a) and is the bus master
M1	6	The appropriate cycle may now proceed
A8a	7	In response to $\overline{BusAcq}$ active, the arbiter releases $\overline{BusGr}$ as an indication to devices that they may replace any outstanding requests
M1	8	During event 8, device 1 may use the bus repeatedly without further requests for access. Since it is holding $\overline{BusAcq}$ active it continues to be locked between cycles
A1	9	Device 2 requests use of the bus by holding $\overline{Rq(2)}$ active
A9b	10	As a result of event 9, the arbiter removes the allocation from device 1 by releasing $\overline{Rq(1)}$
A10b	11	Device 1 is required to release $\overline{BusAcq}$ in response to $\overline{Rq(1)}$ becoming quiescent. If device 1 has just started a cycle when $\overline{Rq(1)}$ is removed, it is required to continue the cycle until it is established ($\overline{CcRes}$ received by device 1) at which point the $\overline{BusAcq}$ signal is released[a] (If device 1 has just started a Retain cycle when $\overline{Rq(1)}$ is removed, it is permitted to hold $\overline{BusAcq}$ low until the sequence of indivisible cycles has been completed or aborted.)
A2	12	The arbiter grants use of the bus to device 2 by holding $\overline{Rq(2)}$ active
A3	13	The arbiter indicates that the bus has been granted
A4	14	As event 4
A5	15	As event 5
M1, S1	16	As event 6
A8a	17	As event 7

[a] If device 3 had made a request between events 9 and 11, it might have been granted use of the bus, dependent on the relevant priorities of devices 2 and 3, and also on the specific arbitration algorithm in use.

As soon as it had released $\overline{BusAcq}$ at event 11, device 1 could have made a new request for use of the bus because it was not locked in a cycle. If device 1 had been part way through an established Hold cycle it would have released $\overline{BusAcq}$ in response to the arbiter releasing $\overline{Rq(1)}$ but would have remained locked and unable to place requests until the cycle had been completed (rule A12a).

The rules require the arbiter always to wait for $\overline{BusAcq}$ to be released by the current master before reallocating the bus. The delay imposed is only potentially significant following a Hold or Retain cycle where the arbiter may have to ask for use of the bus, i.e. events 10, 11 and 12 in this example.

F.5 Interrupt cycle

Individual devices signal interrupts to the arbiter by indicating acceptance of a bus grant with the $\overline{\text{It}}$ line instead of the $\overline{\text{BusAcq}}$ line. A typical sequence of actions is shown in Figure 8 and the events are given in Table 31.

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Figure 8 — Interrupt cycle

Table 31 — Interrupt cycle

Rule	Event	Comment
A1	1	The bidding device (device 1) makes its request by holding $\overline{Rq(1)}$ active[a]
A2	2	Provided that $\overline{BusAcq}$, $\overline{It}$ and $\overline{BusDeallocate}$ are quiescent, the arbiter is able to grant the request, and does so by also holding $\overline{Rq(1)}$ active
A3	3	The arbiter holds $\overline{BusGr}$ active to indicate that bus allocation has been made
A4	4	In response to event 3, all bidding devices are required to withdraw their requests. After a fixed time (see **6.4**), the bidding devices examine the state of their $\overline{Rq}$ lines to determine which device has been granted use of the bus
A6	5	The interrupting device holds the $\overline{It}$ line active. It is now locked (rule A7b) and can place no further requests
A8b	6	The arbiter releases $\overline{BusGr}$ to indicate acceptance of the interrupt. Bidding devices may now replace outstanding requests[b]
A11a	7	Device 1 completes the handshake by releasing the $\overline{It}$ line. It ceases to be locked (rule A12c) and can place requests again
A9a	8	The arbiter releases the $\overline{Rq(1)}$ line in response to event 7

NOTE   The master device does not need to wait for bus free before activating the $\overline{It}$ line because the Interrupt cycle does not use the $\overline{CcBn}$, $\overline{CcRes}$, $\overline{CcFin}$ lines.

[a] A device having already been granted use of the bus for a master/slave cycle is required to release the bus and re-request bus allocation in order to participate in an Interrupt cycle.

[b] If the arbiter wishes to grant itself use of the bus after event 7 in order to flag the interrupt to a processor (or processors), it may release $\overline{Rq(1)}$ after it releases $\overline{BusGr}$ at event 6 in this example.

F.6 Read cycle

A typical sequence of actions for a Read cycle is shown in Figure 9. The events are given in Table 32.
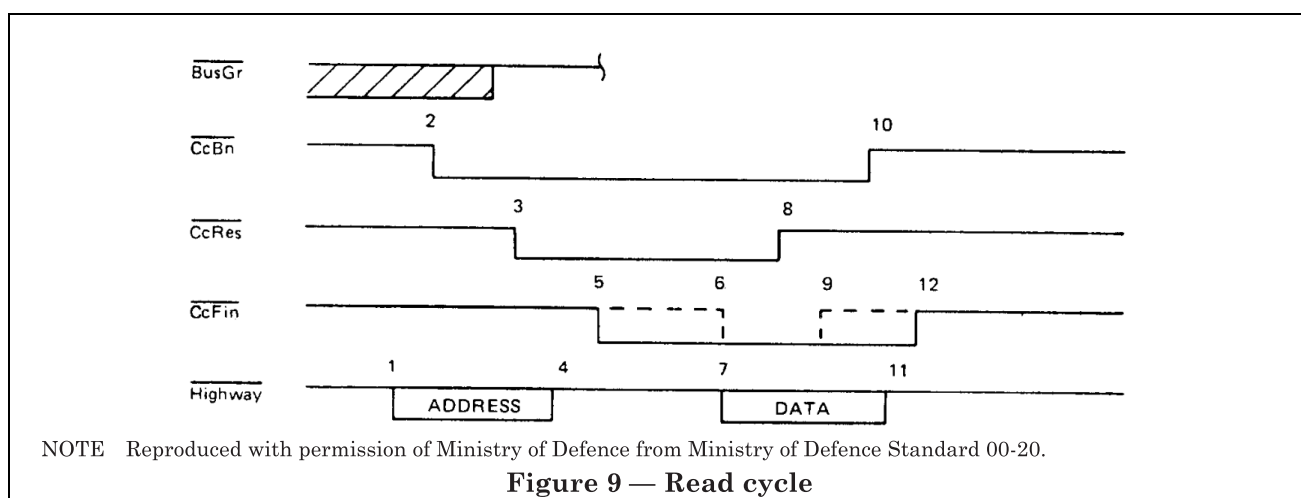
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Figure 9 — Read cycle

Table 32 — Read cycle

Rule	Event	Comment
M1, M2	1	The master detects that the bus is free and holds the address on the bus
M4b	2	The master holds $\overline{\text{CcBn}}$ active to signal that the address is available
S1	3	The slave holds $\overline{\text{CcRes}}$ active to indicate that it has recognized the address and this may now be released from the bus. The rules require that this signal is not to be issued while $\overline{\text{BusGr}}$ is active
M5, M7a	4	The master releases the address from the bus in response to event 3
M3b	5	The master holds $\overline{\text{CcFin}}$ active to indicate that the address has been released, and that the highway is ready to take the Read data from the slave
S3	6	At some time after event 5 and before event 8, the slave also holds $\overline{\text{CcFin}}$ active[a]
S2	7	The slave puts the Read data on the highway
S4b	8	$\overline{\text{CcRes}}$ is released by the slave to indicate that the data is available
M11b	9	The master releases the $\overline{\text{CcFin}}$ line. This action can take place at any time between event 8 and event 10
M9b	10	The master releases the $\overline{\text{CcBn}}$ line to indicate that the data has been accepted and may be removed from the highway. Provided that the master is not still holding $\overline{\text{BusAcq}}$ active it ceases to be locked (rule A12a) and may place requests for the bus
S5a	11	The slave releases the data from the highway
S6a	12	The slave releases the $\overline{\text{CcFin}}$ line to indicate that the data has been released

NOTE   The address comprises the signal on the data, address modifier and byte mode lines (see Table 1). Data comprise the data bits only.
[a] Event 6 may occur before or after event 7.

F.7 Write cycle

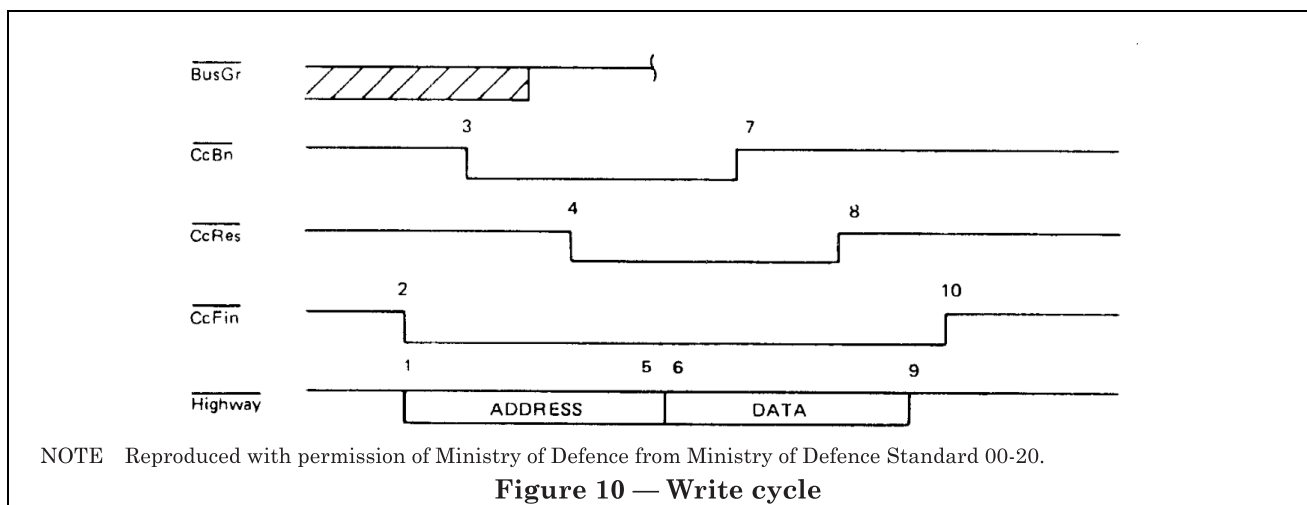A typical sequence of actions for a Write cycle is shown in Figure 10. The events are given in Table 33.

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Figure 10 — Write cycle

Table 33 — Write cycle

Rule	Event	Comment
M1, M2	1	The master detects that the bus is free and holds the address on the bus
M3a	2	The master holds $\overline{\text{CcFin}}$ active to indicate a Write cycle
M4a	3	The master holds $\overline{\text{CcBn}}$ active to signal that the address is available
S1	4	The slave holds $\overline{\text{CcRes}}$ active to indicate that it has recognized the address and this may now be released from the bus. The rules require that this signal is not issued while $\overline{\text{BusGr}}$ is active
M5, M7a	5	The master releases the address
M8	6	The master puts Write data on the highway
M9a	7	$\overline{\text{CcBn}}$ is released by the master to indicate that the data is available
S4a	8	The slave device releases $\overline{\text{CcRes}}$ to signal that the data has been accepted and may be released from the highway. Should the slave device have been left locked after an aborted cycle, it is now unlocked (rule A12d) and may place requests for the bus again
M10a	9	The master releases the Write data from the highway.
M11a	10	$\overline{\text{CcFin}}$ is released by the master device to indicate that the data has been released. Provided that the master is not still holding $\overline{\text{BusAcq}}$ active, it ceases to be locked (rule A12a) and can place requests for the bus

F.8 Vector cycle

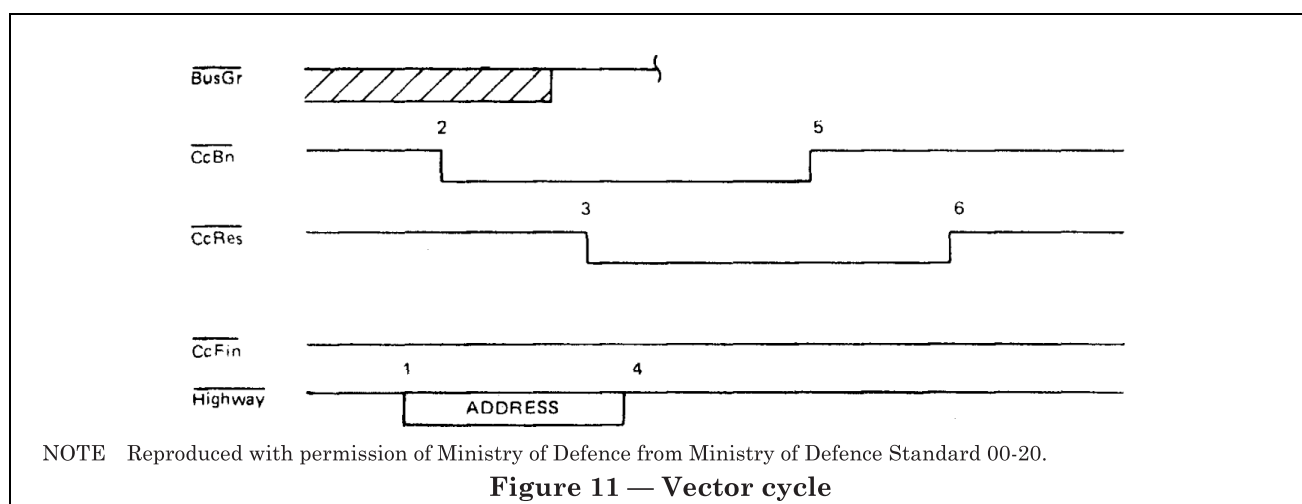A typical sequence of actions for a Vector cycle is shown in Figure 11. The events are given in Table 34.

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Figure 11 — Vector cycle

Table 34 — Vector cycle

Rule	Event	Comment
M1,M2	1	The master detects that the bus is free and holds the address on the bus
M4c	2	The master holds $\overline{\text{CcBn}}$ active to signal that the address is available
S1	3	The slave holds $\overline{\text{CcRes}}$ active to indicate that it has recognized the address and this may now be released from the bus. The rules require that this signal is not issued while $\overline{\text{BusGr}}$ is active
M5, M7a	4	The master releases the address from the bus
M9c	5	$\overline{\text{CcBn}}$ is released by the master to indicate that the address has been released. Provided that the master is not still holding $\overline{\text{BusAcq}}$ active, it ceases to be locked (rule A12a) and may place requests for the bus
S4c	6	In response to event 5, the slave device releases $\overline{\text{CcRes}}$. Should the slave device have been left locked after an aborted cycle, it is now unlocked (rule A12d) and may place requests for the bus again

F.9 Examples of the use of cycle abort

F.9.1 *General.* The $\overline{\text{CcAbort}}$ line is normally used to terminate a cycle that for some reason has failed. The most probable failure is a failure to respond, and an example of this is given as example 8. The arbiter will also hold $\overline{\text{CcAbort}}$ active if it detects any other invalid operation.

A permissible secondary use of $\overline{\text{CcAbort}}$ is to implement a memory protection facility, and an example of this is also given, as example 9.

F.9.2 *Orderly termination of uncompleted cycle.* A typical sequence of actions, in which $\overline{\text{CcAbort}}$ is used to terminate a failed cycle after the arbiter time-out period has expired, is shown in Figure 12. The cycle taken as an example is a Read cycle. The events are given in Table 35.
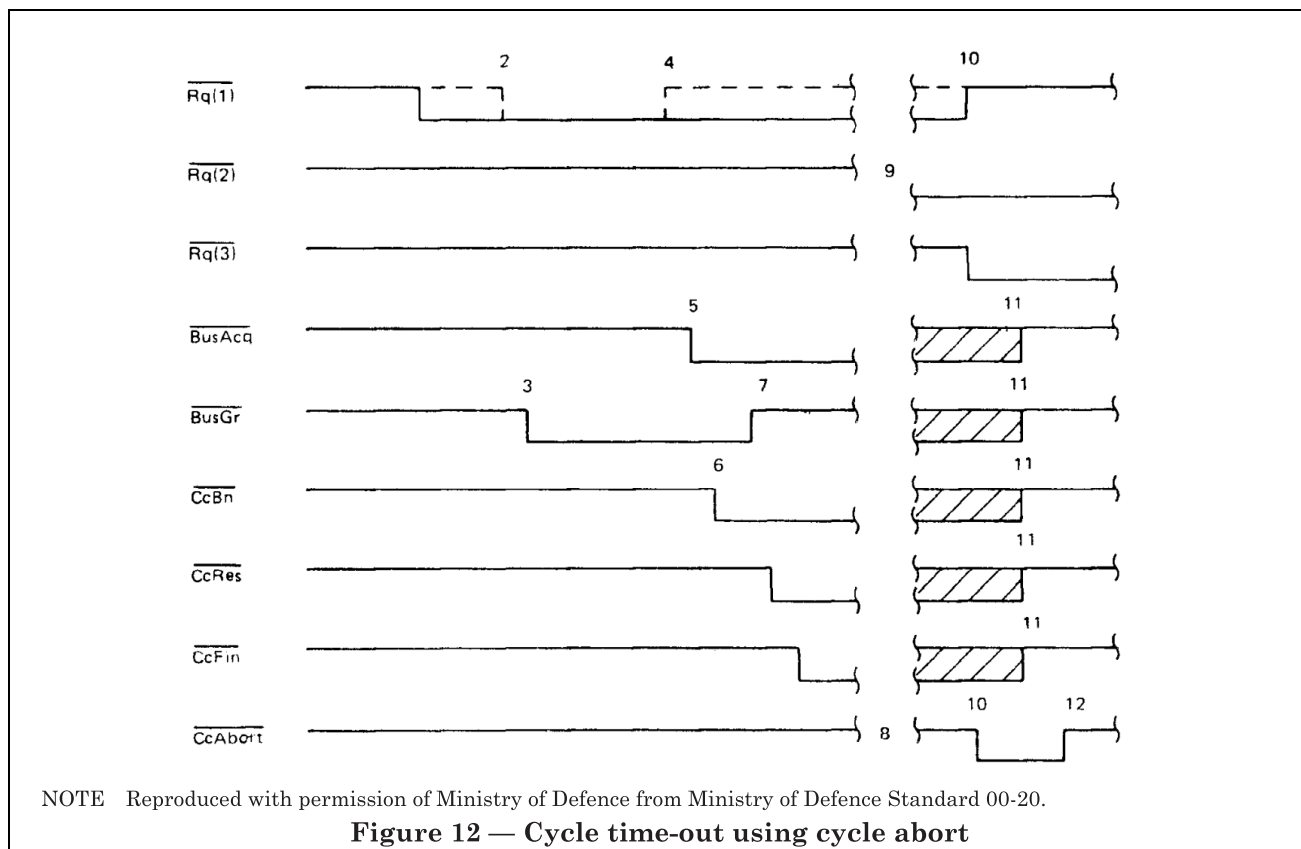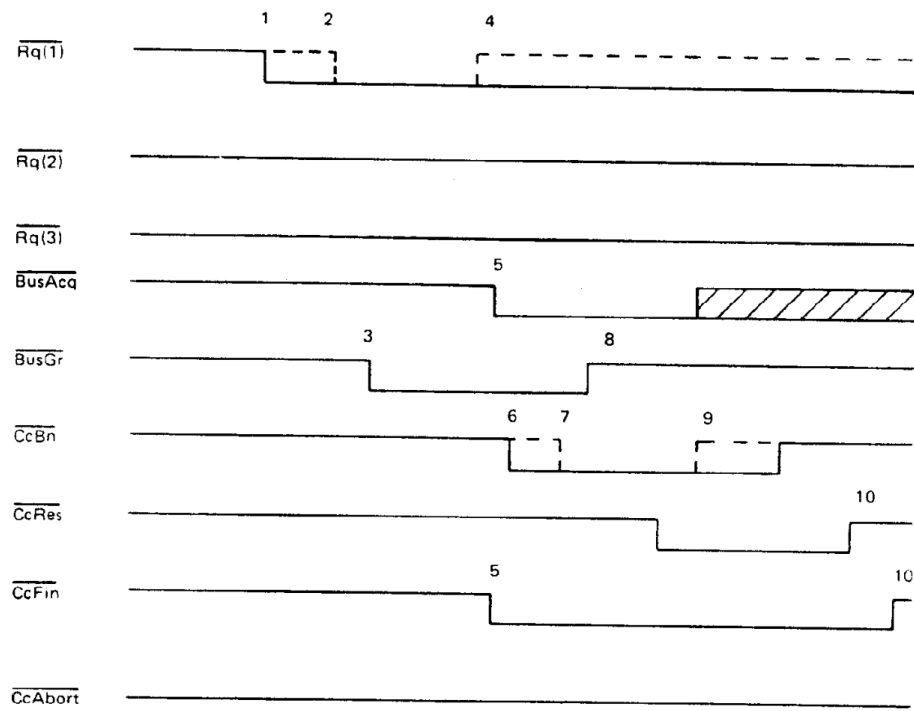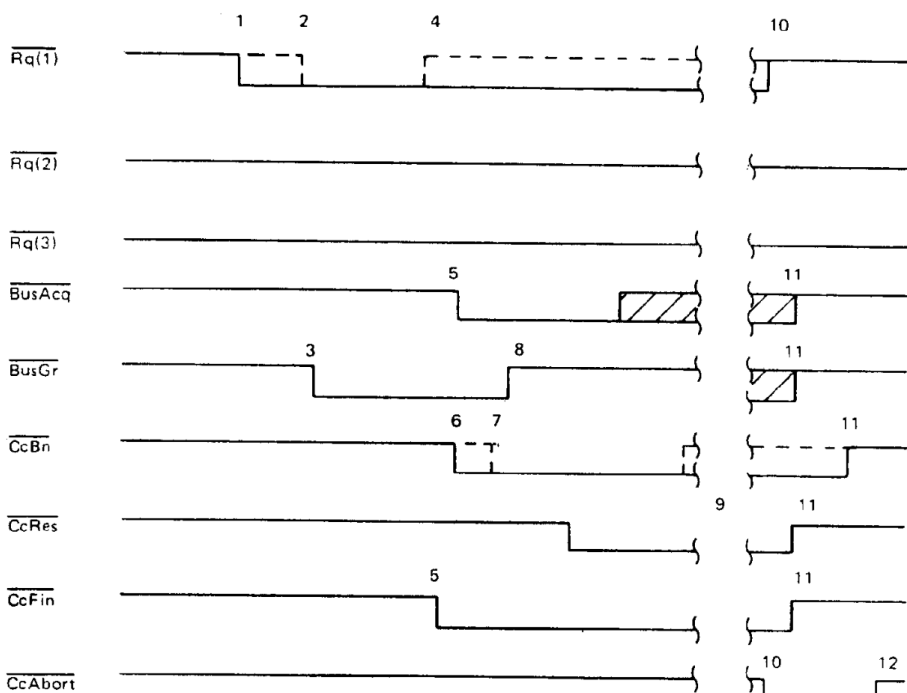

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Figure 12 — Cycle time-out using cycle abort

Table 35 — Cycle time-out using cycle abort

Rule	Event	Comment
A1	1	Device 1 makes its request by setting $\overline{\text{Rq(1)}}$ active
A2, A3	2, 3	The arbiter grants the request by holding $\overline{\text{Rq(1)}}$ active and then holding $\overline{\text{BusGr}}$ active
A4	4	Devices release their request lines
A5a, M1	5, 6	The bus is acquired and the appropriate master cycle commences. The master is now locked
A8	7	Arbiter releases $\overline{\text{BusGr}}$ in response to event 5
S4b	8	It is assumed that for some reason the bus locks up here
A1	9	It is assumed that another device signals a request during the time-out period
C3, C1b	10	The time-out implemented in the arbiter expires and the arbiter holds $\overline{\text{CcAbort}}$ active
A10c, M9d, M10b, S4d, and possibly S5b and S6b	11	All master and slave devices are required to release their cycle control lines, but bidding devices not involved in the aborted cycle need not remove outstanding requests
C2	12	In response to event 11, the arbiter releases $\overline{\text{CcAbort}}$. The arbiter is now able to grant the bus to either device 2 or device 3, but device 1 remains locked and unable to bid for the bus (rule A1) until it has acted as slave in a Write or Vector cycle (rule A12d)

F.9.3 *Memory protection device using cycle abort.* The cycle abort facility may also be used, indirectly, by a memory protection device. This device is connected to the bus lines and examines all accesses within its defined address range. A typical sequence of actions is shown in Figure 13. The events are given in Table 36.

(a) Cycle allowed by protection device

(b) Cycle not allowed by protection device

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Figure 13 — Memory protect using cycle abort

Table 36 — Memory protect using cycle abort

Rule	Event	Comment
A1	1	Device 1 makes its request by holding $\overline{Rq(1)}$ active
A2, A3	2, 3	The arbiter grants the request by holding $\overline{Rq(1)}$ active and $\overline{BusGr}$ active
A4	4	All requests are removed
A5a, M1, M2, M3a, M4a	5,6	Master 1 acquires the bus and commences the required (Write) cycle
—	7	$\overline{CcBn}$ is held active by the memory protection device
A8a	8	In response to event 5 the arbiter releases $\overline{BusGr}$ CYCLE ALLOWED [see Figure 13(a)]
	9, 10	After the cycle has been validated, the memory protection device releases $\overline{CcBn}$. This can occur at any point in the region shown. The cycle then proceeds normally and terminates in the usual way CYCLE NOT ALLOWED [see Figure 13(b)]
—	9	If the protection device does not validate the cycle, it continues to hold $\overline{CcBn}$ active
C4, C1a, A9d	10	The arbiter times out the transfer, activates $\overline{CcAbort}$ and releases the allocation of device 1
M11c, S4d, and possibly M10b	11	In response to $\overline{CcAbort}$, all devices connected to the bus are required to release their cycle control signals
C2	12	The arbiter releases $\overline{CcAbort}$ in response to the bus signals being released. Device 1 (the device that attempted the forbidden Write cycle) remains locked until freed under rule A12d

F.10 Multiple bus operation

F.10.1 *General.* Eurobus is designed to permit several buses to be interlinked by means of bus links. A linker card is required on each bus and a special interconnection between those cards provides a uni-directional or bi-directional link (see Figure 14).

The scheme outlined in Figure 14 constitutes an example only, since the means whereby information is conveyed between a bus linker card on one bus and a bus linker card on another bus does not fall within the scope of this standard (see clause **1**).

The implementation of links is not covered by this standard, but a bus line, $\overline{Bus\ Deallocate}$, is provided to make multiple bus operation possible. It is used by a linker addressed as or acting as a slave in the following circumstances.

a) The linker recognizes that it is being addressed as a slave but the linker on the remote bus cannot become master on the remote bus.

This state can occur for either of the following two reasons.

1) The most probable reason is that the linker on the remote bus has also recognized an address. Clearly the cycle on either the local bus or the remote bus needs to be terminated to resolve the deadly embrace thus created.

2) A less likely reason is that the linker on the remote bus is unable to become bus master in a reasonable time, for example, because the remote bus has locked up and is being timed out for cycle abortion, and there is a danger that the local bus arbiter will time out.

In neither case it is desirable that the cycle should be terminated by a cycle abort with consequent locking of the current master. $\overline{\text{Bus Deallocate}}$ is used to request termination of the cycle in an orderly manner.

b) The linker has established the cycle as slave (rule S1). Under the Eurobus protocol rules the current master is able to hold the bus indefinitely if no other device places a request for bus allocation. $\overline{\text{Bus Deallocate}}$ is used to ask the arbiter to withdraw allocation from the current master and thus enable the companion linker to release the remote bus for reallocation.

Examples of these two uses of $\overline{\text{Bus Deallocate}}$ are given in **F.10.2** and **F.10.3**. They are illustrative and do not cover all possible situations.
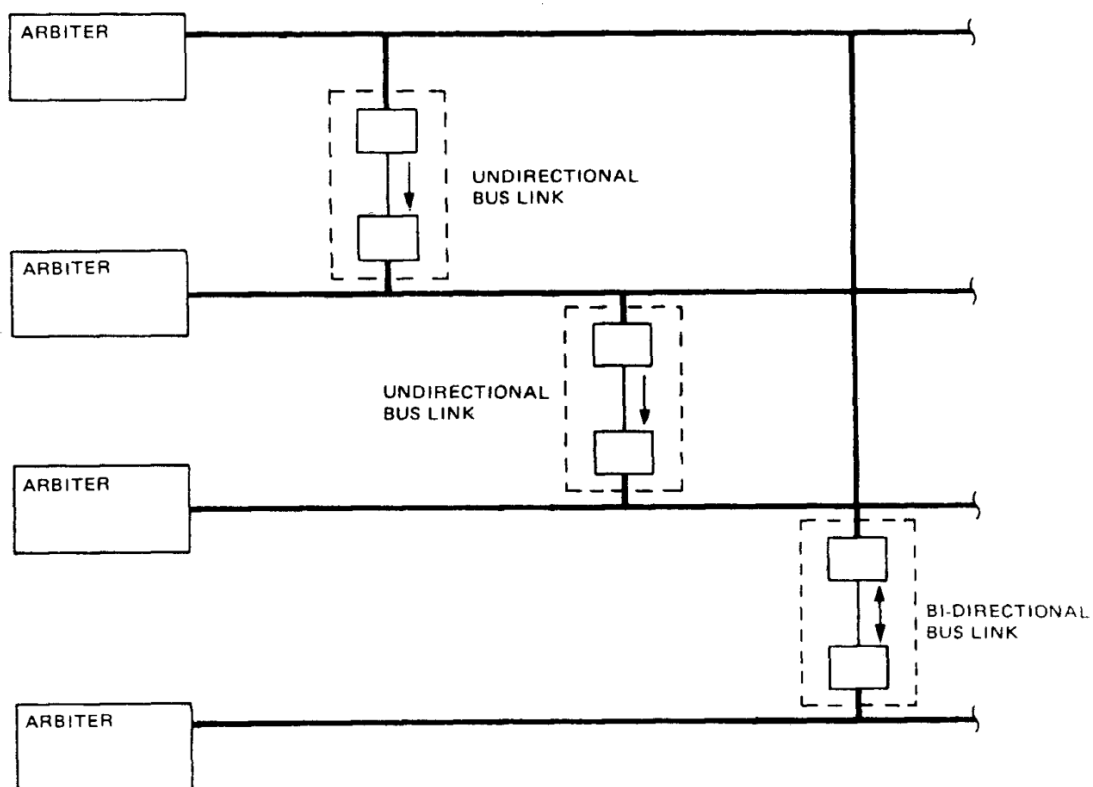
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Figure 14 — Multiple buses

F.10.2 *Resolution of deadly embrace.* A typical sequence of actions for the resolution of a deadly embrace is shown in Figure 15 and the events are given in Table 37. In this case $\overline{\text{Bus Deallocate}}$ is held active instead of $\overline{\text{CcRes}}$ by the addressed device.

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Figure 15 — Resolution of deadly embrace
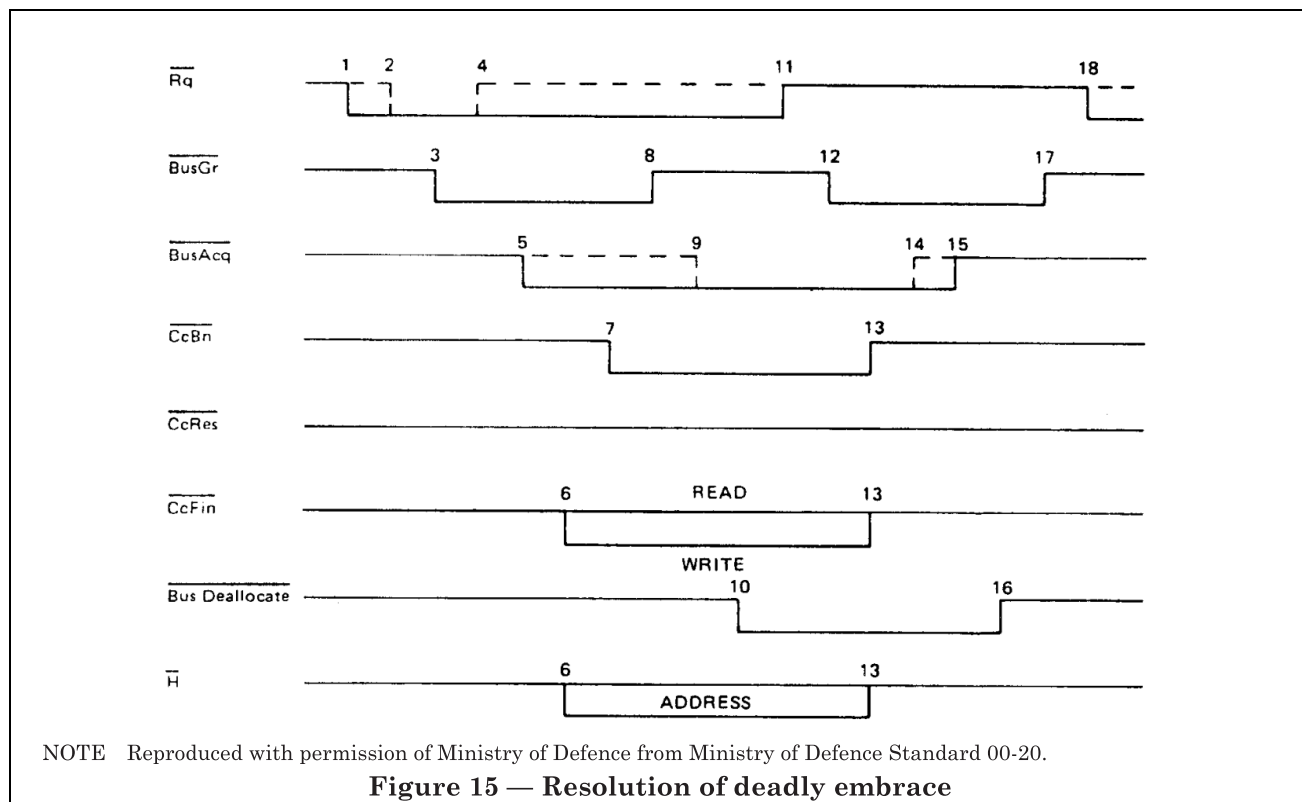
Table 37 — Resolution of deadly embrace

Rule	Event	Comment
A1	1	A device places a request for the bus by holding its $\overline{\text{Rq}}$ line active
A2, A3	2, 3	The arbiter grants the bus
A4	4	The device releases its $\overline{\text{Rq}}$ line and ascertains that it has been granted the bus
A5a	5	The device acquires the bus and becomes master
M1, M2 and possibly M3a	6	The master holds the address on the bus and holds $\overline{\text{CcFin}}$ active if it intends to carry out a Write cycle
M4	7	The master holds $\overline{\text{CcBn}}$ active
A8a	8	In response to event 5, the arbiter releases $\overline{\text{BusGr}}$
A5b	9	The linker recognizes its address on the bus and holds $\overline{\text{BusAcq}}$ active. This may occur before or after event 8
D1a	10	The linker is unable to respond because of conditions on the remote bus. It refuses the cycle by holding $\overline{\text{Bus Deallocate}}$ active instead of $\overline{\text{CcRes}}$. The rules require that this does not happen while $\overline{\text{BusGr}}$ is active
A9c	11	The arbiter releases the $\overline{\text{Rq}}$ line
A3b	12	The arbiter holds $\overline{\text{BusGr}}$ active following event 11
M6, M7b, M9d and possibly M11c	13	The master responds to events 11 and 12 by releasing the address, $\overline{\text{CcFin}}$ (if held) and $\overline{\text{CcBn}}$
A10c	14	After event 13, the master releases $\overline{\text{BusAcq}}$ and ceases to be locked
A10e	15	The linker also responds to event 12 by releasing $\overline{\text{BusAcq}}$. This could occur before or after, event 14
D2	16	When the linker perceives that $\overline{\text{BusAcq}}$ is quiescent it releases $\overline{\text{Bus Deallocate}}$
A8c	17	The arbiter responds to the last of events 14 and 15, i.e. $\overline{\text{BusAcq}}$ quiescent, by releasing $\overline{\text{BusGr}}$
A1	18	The deallocated master may bid again as soon as $\overline{\text{BusGr}}$ is quiescent. No device may bid while $\overline{\text{BusGr}}$ is active (rule A4)

F.10.3 *Request for allocation to be removed from current master.* A typical sequence of actions for request for allocation to be removed from current master is shown in Figure 16 and the events are given in Table 38. In this case $\overline{\text{Bus Deallocate}}$ is held active while $\overline{\text{CcRes}}$ is active.
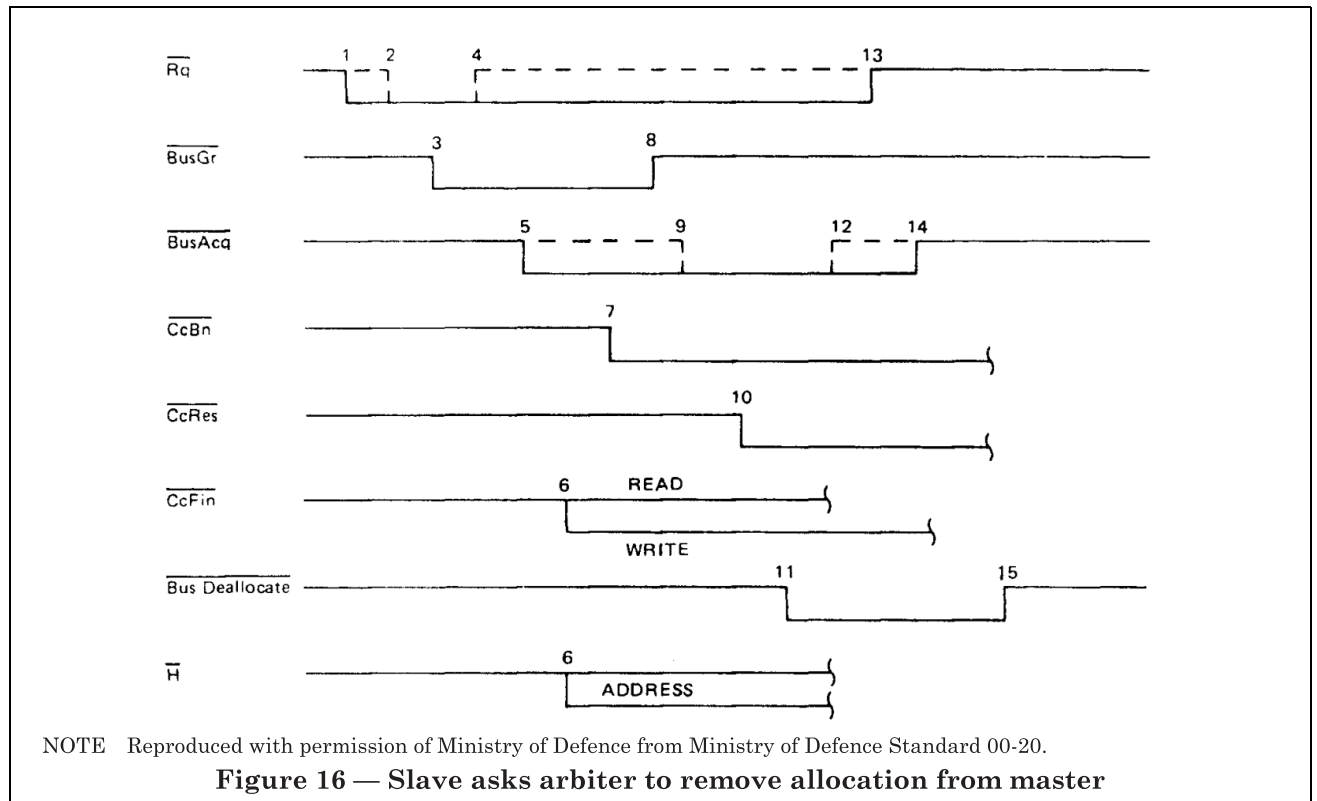

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Figure 16 — Slave asks arbiter to remove allocation from master

Table 38 — Slave asks arbiter to remove allocation from master

Rule	Event	Comment
A1	1	A device places a request for the bus
A2, A3	2, 3	The arbiter grants the bus
A4	4	The device releases its $\overline{\text{Rq}}$ line and ascertains that it has been granted the bus
A5a	5	The device acquires the bus and becomes master
M1, M2 and possibly M3a	6, 7	The master holds the address on the bus and holds $\overline{\text{CcBn}}$ active
A8a	8	The arbiter releases $\overline{\text{BusGr}}$ in response to event 5
A5b	9	The linker recognizes its address on the bus and holds $\overline{\text{BusAcq}}$ active. This may occur before or after event 8 but needs to occur before event 10
S1	10	The linker holds $\overline{\text{CcRes}}$ active, becoming slave
D1b	11	The linker holds $\overline{\text{Bus Deallocate}}$ active to obtain release of the bus
A10d	12	The linker releases $\overline{\text{BusAcq}}$ having guaranteed compliance with rule D1bi at event 11
A9c	13	In response to event 11, the arbiter releases the request line. Since $\overline{\text{CcRes}}$ is active, however, it does not hold $\overline{\text{BusGr}}$ active
A10b	14	The master may have already released $\overline{\text{BusAcq}}$ after $\overline{\text{CcRes}}$ became active. If not, it does so in response to event 13 in the normal way (i.e. either at once or as soon as the last cycle of an indivisible operation is established)
D2	15	The tinker releases $\overline{\text{Bus Deallocate}}$ in response to $\overline{\text{BusAcq}}$ becoming quiescent. The arbiter is now able to grant the bus to a requesting device

Appendix G Method of address allocation for mixed data widths

G.1 General

This appendix describes a logical consistent method of address allocation for cases where a system designer is faced with a need to mix devices of various data widths on the same bus. The functioning of the bus is not dependent on this allocation, but other methods leave a risk of incompatibility between implementations. With unequal data widths the addressing range is restricted.

G.2 Method

In the case of a 16-bit data-width bus (see Table 39), there is provision for 16-bit and 8-bit devices. The Address Recognition protocol allocates the address block selected by $\overline{\text{AdM(1)}}$ quiescent, $\overline{\text{AdM(0)}}$ quiescent, to 8-bit devices and the block selected by $\overline{\text{AdM(1)}}$ quiescent, AdM(0) active, to 16-bit devices. If further address blocks are needed for 8-bit devices, the second block to be allocated is the block selected by $\overline{\text{AdM(1)}}$ active, $\overline{\text{AdM(0)}}$ quiescent, and the third block $\overline{\text{AdM(1)}}$ active, $\overline{\text{AdM(0)}}$ active. If further blocks are needed for 16-bit devices, the second block is selected by $\overline{\text{AdM(1)}}$ active, $\overline{\text{AdM(0)}}$ quiescent, the third by $\overline{\text{AdM(1)}}$ active $\overline{\text{AdM(0)}}$ active, and the fourth by $\overline{\text{AdM(1)}}$ quiescent, $\overline{\text{AdM(0)}}$ quiescent; but, if any of these blocks has already been allocated for use by 8-bit devices, it is omitted from the blocks that can be allocated for use by 16-bit devices.

The principles recommended for the 16-bit bus are applicable to 24-bit and 32-bit buses, as illustrated by the values given in Table 40 and Table 41.

Table 39 — Address recognition protocol ($N = 15$)

$\overline{\text{AdMd}(1)}$	$\overline{\text{AdMd}(0)}$	Addresses		Data
Acv	Acv	Third block for 16-bit devices if no 8-bit devices in this block		$\overline{\text{H}(15)}$ $\overline{\text{H}(8)}$
			Third block for 8-bit devices	$\overline{\text{H}(7)}$ $\overline{\text{H}(0)}$
Acv	Q	Second block for 16-bit devices if no 8-bit devices in this block		$\overline{\text{H}(15)}$ $\overline{\text{H}(8)}$
			Second block for 8-bit devices	$\overline{\text{H}(7)}$ $\overline{\text{H}(0)}$
Q	Acv	First block for 16-bit devices		$\overline{\text{H}(15)}$ $\overline{\text{H}(8)}$
				$\overline{\text{H}(7)}$ $\overline{\text{H}(0)}$
Q	Q	Fourth block for 16-bit devices if no 8-bit devices		$\overline{\text{H}(15)}$ $\overline{\text{H}(8)}$
			First block for 8-bit devices	$\overline{\text{H}(7)}$ $\overline{\text{H}(0)}$

Table 40 — Address recognition protocol ($N = 23$)

$\overline{AdMd(1)}$	$\overline{AdMd(0)}$	Addresses			Data
Acv	Acv	Second block for 24-bit devices if no 16-bit or 8-bit devices in this block			$\overline{H(23)}$ $\overline{H(16)}$
			Second block for 16-bit devices if no 8-bit devices in this block		$\overline{H(15)}$ $\overline{H(8)}$
				Third block for 8-bit devices	$\overline{H(7)}$ $\overline{H(0)}$
Acv	Q	First block for 24-bit devices			$\overline{H(23)}$ $\overline{H(16)}$
					$\overline{H(15)}$ $\overline{H(8)}$
					$\overline{H(7)}$ $\overline{H(0)}$
Q	Acv	Fourth block for 24-bit devices if no 16-bit devices or no 8-bit devices in this block			$\overline{H(23)}$ $\overline{H(16)}$
			First block for 16-bit devices		$\overline{H(15)}$ $\overline{H(8)}$
				Second block for 8-bit devices if no 16-bit devices	$\overline{H(7)}$ $\overline{H(0)}$
Q	Q	Third block for 24-bit devices if no 16-bit or 8-bit devices in this block			$\overline{H(23)}$ $\overline{H(16)}$
			Third block for 16-bit devices if no 8-bit devices		$\overline{H(15)}$ $\overline{H(8)}$
				First block for 8-bit devices	$\overline{H(7)}$ $\overline{H(0)}$

Table 41 — Address recognition protocol ($N = 31$)

$\overline{AdMd(1)}$	$\overline{AdMd(0)}$	Addresses				Data
Acv	Acv	First block for 32-bit devices				$\overline{H(31)}$ $\overline{H(24)}$
						$\overline{H(23)}$ $\overline{H(16)}$
						$\overline{H(15)}$ $\overline{H(8)}$
						$\overline{H(7)}$ $\overline{H(0)}$
Acv	Q	Fourth block for 32-bit devices if no 24-bit devices and no 8-bit or 16-bit devices in this block				$\overline{H(31)}$ $\overline{H(24)}$
			First block for 24-bit devices			$\overline{H(23)}$ $\overline{H(16)}$
				Second block for 16-bit devices if no 24-bit devices and no 8-bit devices in this block		$\overline{H(15)}$ $\overline{H(8)}$
					Third block for 8-bit devices if no 24-bit devices	$\overline{H(7)}$ $\overline{H(0)}$
Q	Acv	Third block for 32-bit devices if no 16-bit devices and no 8-bit or 24-bit devices in this block				$\overline{H(31)}$ $\overline{H(24)}$
			Third block for 24-bit devices if no 16-bit devices and no 8-bit devices in this block			$\overline{H(23)}$ $\overline{H(16)}$
				First block for 16-bit devices		$\overline{H(15)}$ $\overline{H(8)}$
					Second block for 8-bit devices if no 16-bit devices	$\overline{H(7)}$ $\overline{H(0)}$
Q	Q	Second block for 32-bit devices if no 8-bit devices and no 16-bit or 24-bit devices in this block				$\overline{H(31)}$ $\overline{H(24)}$
			Second block for 24-bit devices if no 8-bit devices and no 16-bit devices in this block			$\overline{H(23)}$ $\overline{H(16)}$
				Third block for 16-bit devices if no 8-bit devices		$\overline{H(15)}$ $\overline{H(8)}$
					First block for 8-bit devices	$\overline{H(7)}$ $\overline{H(0)}$

Appendix H Example of Eurobus backplane construction

A cross section through a typical Eurobus backplane is shown in Figure 17.

NOTE 1   The power planes (including 0 V) extend more than 3.8 mm beyond the inverse lands around their peripheries, except where different supplies share the same plane.

NOTE 2   At least four pads are required for the connection of + 5 V supply to the 5 V plane.

NOTE 3   At least five pads are required for connection of 0 V return to each 0 V plane.

NOTE 4   The diameter of inverse lands on the 0 V and + 5 V planes is less than 2.4 mm.

NOTE 5   Tracks are on a 2.54 mm pitch.
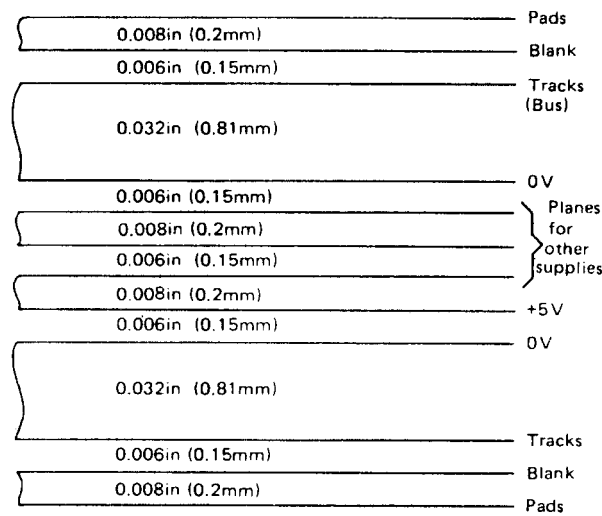
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Figure 17 — Backplane cross section

Appendix J Mechanical option 1: Forced air convection cooled double Eurocard for UK Ministry of Defence use with Eurobus 18/A

J.1 General

The objective of this particular mechanical implementation of Eurobus 18/A is to facilitate the design of a range of functional electronic modules, based on the physical requirements specified, that can be used in a wide range of forced air convection cooled systems, equipments and applications. This appendix is not part of the specification of Eurobus A.

J.2 Dimensions

J.2.1 *Panel size* (see Figure 18, Figure 19 and Figure 20). The panel size is as follows:

   a) height = 233.4 mm (nominal);

   b) depth = 160 mm (nominal);

   c) thickness = 1.8 mm (maximum).

NOTE   This is a standard depth double Eurocard from the Eurocard series, see BS 5954.

J.2.2 *Panel pitch.* Panels are mounted at a pitch corresponding to an integral multiple of 2.54 mm. The minimum pitch is 15.24 mm.

J.2.3 *Component height* (see Figure 18). The component height above the panel face does not exceed a value that is 6.24 mm less than the panel pitch, i.e. the maximum component height on panels mounted at the minimum pitch is 9 mm.

J.2.4 *Protrusions from non-component side of panel.* The height of soldered joints or other fittings on the non-component side shall not exceed 2 mm.

J.2.5 *Panel thickness.* The panel thickness is 1.6 ± 0.2 mm.

J.2.6 *Panel bow.* Panel bow does not exceed 1.5 mm when measured at the centre of the bow relative to the level at the outside edges with the plane of the panel vertical.

J.2.7 *Proximity of copper track to edges of panel.* The minimum distance between copper track and the upper end lower edges of the panel is 6.5 mm.

J.3 Thermal density

The recommended maximum heat dissipation from a single panel is 10 W. Higher dissipation is permissible, but it is essential that the user-information associated with such a panel states clearly the actual dissipation and identifies hot spot areas on the panel, if any.

J.4 Cooling

Cooling is by forced air convection, the air flow direction being from bottom to top of the panel. For optimum cooling, it is recommended that dual-in-line and other large components are mounted with their longer axes parallel to the direction of air-flow.

J.5 Input/output connectors

The panel has two 64-way connectors, complying with IEC 603-2:1980, for connector designation 603-2 IEC-C096-M, fitted on the rear edge in the positions shown in Figure 19 and Figure 20. Each connector is the male half of a two-part connector.

In order to ensure interchangeability of panels, it is recommended that jigs are used to position the connectors correctly relative to the lower edge of the panel and to each other during assembly.

The upper connector is designated A and the lower connector B. The two rows of pins on each connector are designated a and c respectively, row a being closest to the panel. The pins are numbered 1 to 32 in each row, pin No. 1 being nearest to the top of the panel in both cases (see Figure 18).

Table 42 and Table 43 give the signals and their pin allocations on the two connectors.
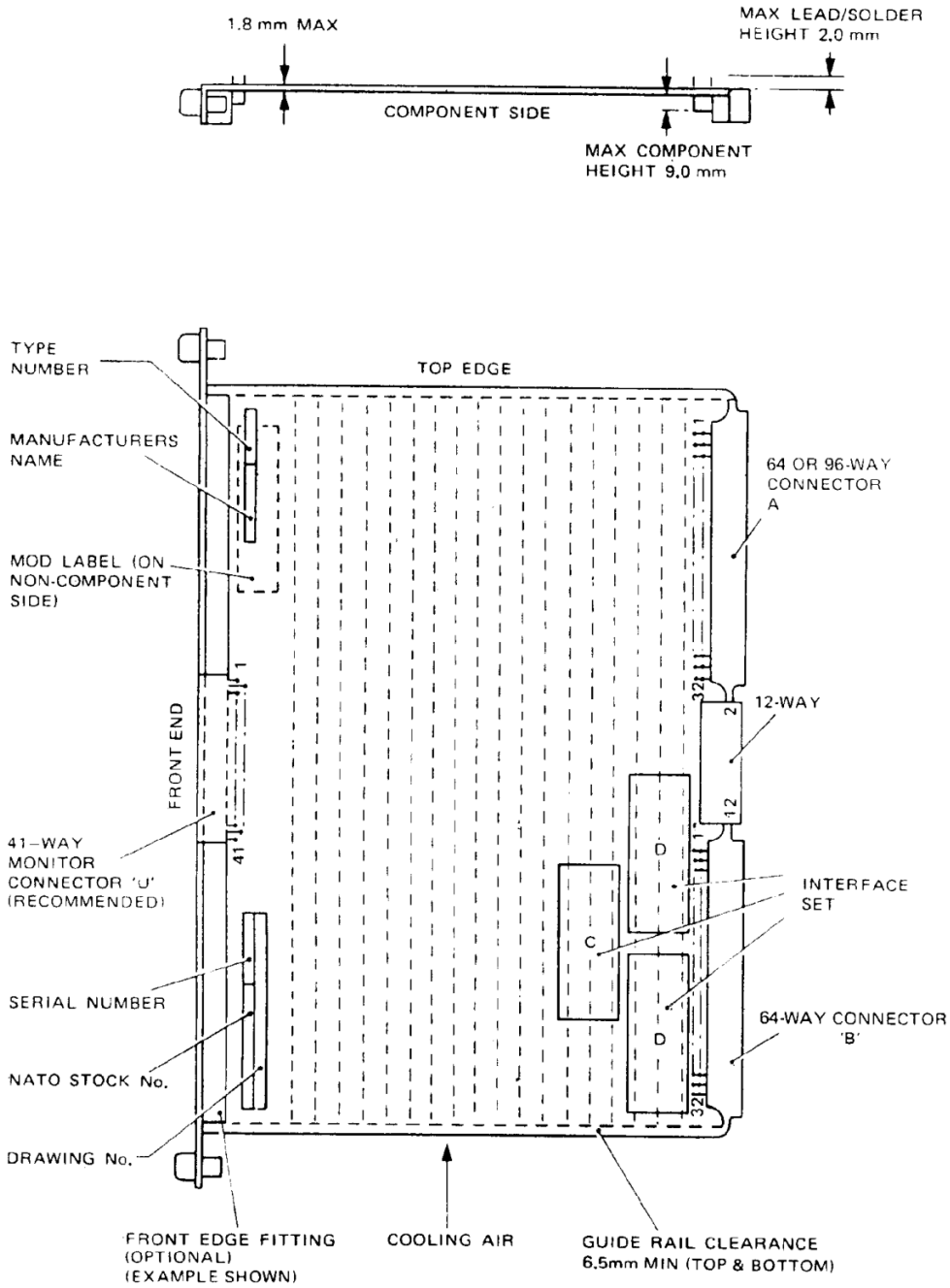
NOTE   Reproduced with permission of Ministry of Defence from Ministry of Defence Standard 00-20, with minor alterations.

Figure 18 — MOD standard forced air convection cooled double Eurocard for Eurobus 18/A

Table 42 — Input/output connector A

Row a	Signal	Row c	Signal
Pin No. 01	$\overline{\text{ExtCk}}$	Pin No. 01	$\overline{\text{InCk}}$
Pin No. 02	0 V	Pin No. 02	0 V
Pin No. 03		Pin No. 03	
Pin No. 04		Pin No. 04	
Pin No. 05		Pin No. 05	
Pin No. 06		Pin No. 06	
Pin No. 07		Pin No. 07	
Pin No. 08		Pin No. 08	
Pin No. 09		Pin No. 09	
Pin No. 10		Pin No. 10	
Pin No. 11		Pin No. 11	
Pin No. 12		Pin No. 12	
Pin No. 13		Pin No. 13	
Pin No. 14		Pin No. 14	
Pin No. 15		Pin No. 15	
Pin No. 16		Pin No. 16	
Pin No. 17		Pin No. 17	
Pin No. 18		Pin No. 18	
Pin No. 19		Pin No. 19	
Pin No. 20		Pin No. 20	
Pin No. 21		Pin No. 21	
Pin No. 22		Pin No. 22	
Pin No. 23		Pin No. 23	
Pin No. 24		Pin No. 24	
Pin No. 25		Pin No. 25	
Pin No. 26		Pin No. 26	
Pin No. 27		Pin No. 27	
Pin No. 28		Pin No. 28	
Pin No. 29		Pin No. 29	
Pin No. 30		Pin No. 30	
Pin No. 31		Pin No. 31	
Pin No. 32		Pin No. 32	

NOTE   The pins not allocated to specific signals in this table are for peripheral equipment use. It is recommended that attention should be paid to the organization of signals so that ribbon cable can be used.

J.6 Monitor connector

It is recommended that a monitor connector is fitted in the centre of the front edge, see Figure 18 to Figure 20.

If fitted, this connector is designated U and is the female half of a 41-pin two-part connector complying with BS 9525 (Pattern 9525 N0001). Pin No. 1 is located nearest to the top of the panel (see Figure 18) and is allocated to + 5 V which is monitored via a 470 Ω/0.125 W series resistor. Pin No. 41 is allocated to 0 V and pin No. 40 is allocated to an active low panel reset $\overline{\text{Pn1Rs}}$. (This may in turn generate or monitor the Bus Reset $\overline{(\text{Rs})}$ signal at the panel designer's discretion.)

Table 43 — Input/output connector B

Row a	Signal	Row c	Signal
Pin No. 01	$\overline{H(0)}$	Pin No. 01	$\overline{H(1)}$
Pin No. 02	$\overline{H(2)}$	Pin No. 02	$\overline{H(3)}$
Pin No. 03	$\overline{H(4)}$	Pin No. 03	+ 5 V
Pin No. 04	0 V (leading)	Pin No. 04	$\overline{H(5)}$
Pin No. 05	$\overline{AdM(1)}$	Pin No. 05	—
Pin No. 06	$\overline{Fa}$	Pin No. 06	$\overline{AdM(0)}$
Pin No. 07	$\overline{Rs}$	Pin No. 07	0 V
Pin No. 08	$\overline{H(6)}$	Pin No. 08	$\overline{FaRs}$
Pin No. 09	—	Pin No. 09	– 5 V
Pin No. 10	0 V	Pin No. 10	$\overline{CcAbort}$
Pin No. 11	$\overline{BytAd}$	Pin No. 11	$\overline{H(7)}$
Pin No. 12	– 12 V	Pin No. 12	$\overline{BusGr}$
Pin No. 13	$\overline{BytWk}$	Pin No. 13	+ 12 V
Pin No. 14	$\overline{H(8)}$	Pin No. 14	$\overline{BusAcq}$
Pin No. 15	0 V	Pin No. 15	$\overline{H(9)}$
Pin No. 16	$\overline{CcBn}$	Pin No. 16	+ 5 V
Pin No. 17	Address Selection	Pin No. 17	$\overline{It}$
Pin No. 18	Address Selection	Pin No. 18	Address Selection
Pin No. 19	$\overline{Rq}$	Pin No. 19	Address Selection
Pin No. 20	—	Pin No. 20	Address Selection
Pin No. 21	0 V	Pin No. 21	Address Selection
Pin No. 22	$\overline{Bus\ Deallocate}$	Pin No. 22	$\overline{CcRes}$
Pin No. 23	$\overline{H(10)}$	Pin No. 23	0 V
Pin No. 24	$\overline{H(12)}$	Pin No. 24	$\overline{H(11)}$
Pin No. 25	$\overline{CcFin}$	Pin No. 25	$\overline{H(13)}$
Pin No. 26	+ 5 V	Pin No. 26	—
Pin No. 27	Inrush Control (leading)	Pin No. 27	—
Pin No. 28	$\overline{H(14)}$	Pin No. 28	$\overline{H(15)}$
Pin No. 29	0 V	Pin No. 29	—
Pin No. 30	—	Pin No. 30	+ 24 V
Pin No. 31	0 V (analogue, leading)	Pin No. 31	—
Pin No. 32	Earth (leading)	Pin No. 32	– 24 V

NOTE 1   Under certain extreme circumstances, positions on this connector may be allocated to signals other than those specified above. The rules governing such reallocation are stated below in order of preference.

a) Spare pins may be allocated to user signals.

b) The ± 24 V and analogue 0 V pins, if not required for their assigned purposes, may be allocated to user signals including different power supplies if required.

c) The – 5 V pin, if not required for its assigned purpose, may be allocated to another power supply if required.

d) The Address selection pins, if not required for their assigned purposes, may be allocated to user signals.

It is strongly recommended that due consideration is given to the incompatibility with other panels that will result if a modified signal allocation is used.

NOTE 2   It is recommended that leading pins are used where shown, provided that compatibility is maintained between male and female connectors in order that cards may be interchanged with cards of a similar type that do not use leading pins.

The allocation of other connections on the optional monitor connector is at the equipment designer's discretion.

J.7 Front edge fitting option

Panels are provided with four holes along the front edge for attaching a panel or other retention/extraction device (see Figure 18 to Figure 20); this device is known as a front edge fitting.

To enable a developed panel type to be used in a wide range of applications, any individual panel type may be fitted with one of a number of front edge fittings designed to suit specific applications.

J.8 Panel fittings

J.8.1 *General.* The front edge fitting is an optional item and may be added to a panel according to system requirements. The different types of assembly are described in **J.8.2** and **J.8.3**.

J.8.2 *Basic panel.* A basic panel is a panel assembly with its components and connectors that is fully functional and testable, but that is not fitted with a front edge fitting. A basic panel is known by a type number with an upper case suffix letter (A, B, C... etc.) added to define the particular functional variant. In the case of a memory panel, the latter indicates the amount of storage capacity according to the number of memory elements fitted, Where no random access memories (RAMs) or programmable read only memories (PROMs) are fitted initially the panel is referenced by the type number only.

To complete the defining reference for a basic panel, a hyphenated letter or group of letters is added to indicate the component category according to the particular manufacturer's standard procedures.

A basic Panel, e.g. 4 501 A-C, where -C would indicate commercial grade components, may be held as a stock item after being fully tested against the appropriate test specification. An appropriate drawing set defines the panel for manufacturing purposes and a NATO stock number may be allocated if required.

J.8.3 *Full panel.* A full panel comprises a basic panel, as described in **J.8.1**, to which a front edge fitting may have been added. Two digits are added to indicate the front edge fitting used; /00 for no front edge fitting; /01 for front edge fitting 'Y', etc.

An example of a complete reference for a full panel is 4 501 A-C/01 which defines panel type 4 501, variant A, with commercial components used, and front edge fitting type Y.

4 501	A	-C	/01
Panel	Variant	Component	Front edge
type no.		level	fitting

The method of fitting front edge fitting is defined in the drawing sets for the front edge fittings (see Figure 19 and Figure 20).

J.9 Labelling

Each panel carries the following identification information:

　　a) type reference number (see **J.8.1**) or, exceptionally, the module part number;

　　b) manufacturer's serial number;

　　c) NATO stock reference number (if applicable);

　　d) modification record label;

　　e) manufacturer's name;

　　f) manufacturer's drawing number and issue reference

The locations of these labels is as shown in Figure 18. The alphanumerics for items d), e) and f) may optionally be printed in copper.

J.10 Lamp indicator

Facilities are provided for mounting an indicator lamp on the component side of the panel adjacent to the monitor connector U at the front. The lamp itself is mounted on the panel with the light-emitting face pointing forwards. A green light-emitting diode (LED) is specified to provide an indication of status, as required, without the necessity for a lamp test switch.

The front edge fitting provided for a full panel includes a suitable cut-out to allow visual access to the indicator lamp from the front.

Further indicator lamps may be fitted to panels if required, however a non-standard front edge fitting will be required to permit visual access.

Appendix K Extender panel

K.1 General

The use of any panel that extends the length of unterminated spur track is certain to affect bus waveforms adversely by imposing additional reflections and impedance mismatches.

For these general reasons, the passive extender panel whose characteristics are described in **K.2** may be used between 0 °C and 70 °C.
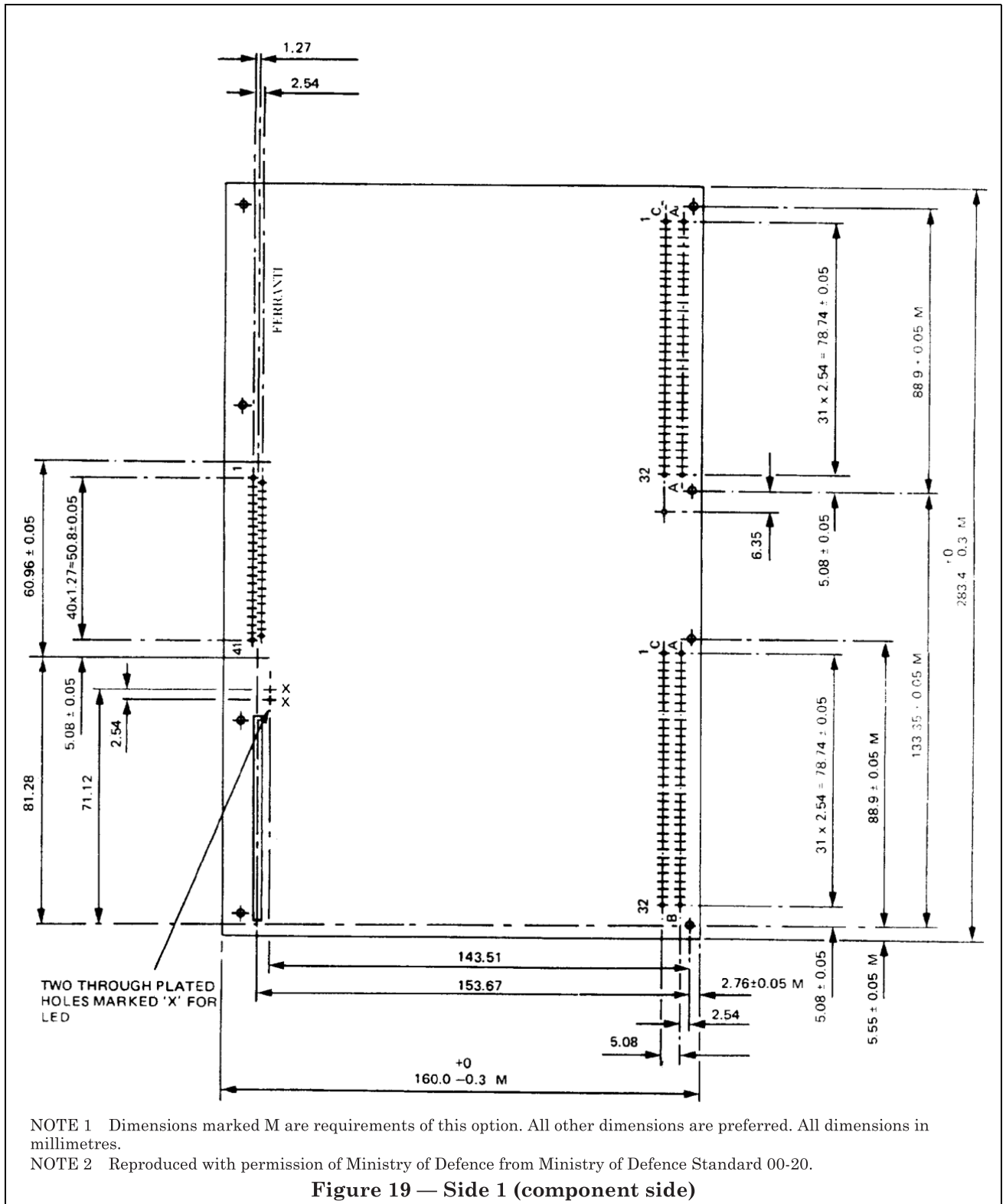
K.2 Extender panel characteristics

K.2.1 *Line impedance.* The characteristic impedance of bus lines on a passive extender is $25 \, ^{+10}_{-5} \, \Omega$.

K.2.2 *Line length.* The physical length of bus lines on a passive extender does not exceed 300 mm.

Appendix L Examples of the application of Eurobus A timing requirements

Table 44 gives the minimum delays permitted by the timing rules from one event to another on Eurobus A.

In practice, a recipient will need to observe a change before responding to it and therefore minimal delays of 0 ns, which generally correspond to an asynchronous handshake response, are extremely unlikely to occur in practice.
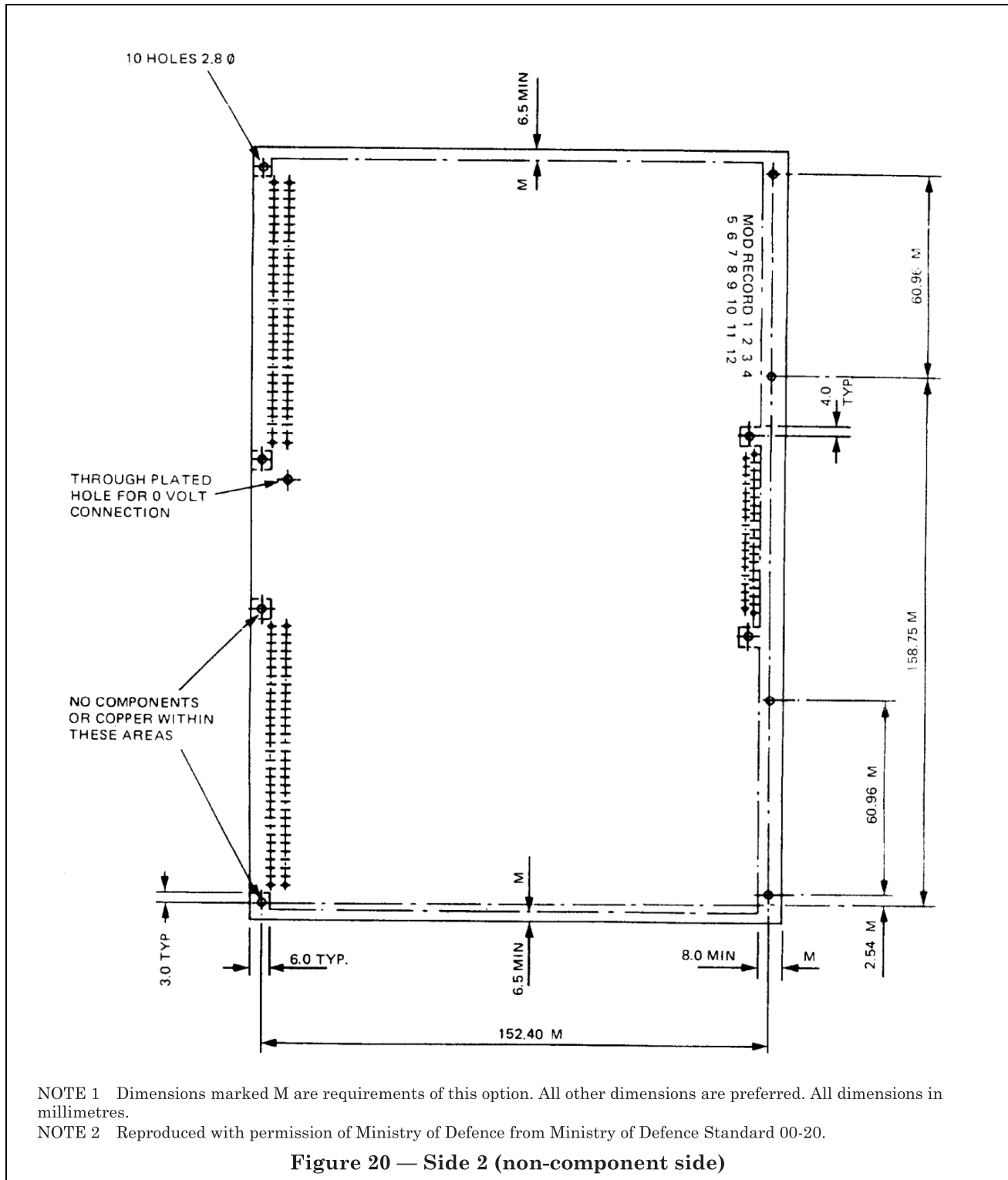
NOTE 1   Dimensions marked M are requirements of this option. All other dimensions are preferred. All dimensions in millimetres.
NOTE 2   Reproduced with permission of Ministry of Defence from Ministry of Defence Standard 00-20.

Figure 19 — Side 1 (component side)

NOTE 1 Dimensions marked M are requirements of this option. All other dimensions are preferred. All dimensions in millimetres.
NOTE 2 Reproduced with permission of Ministry of Defence from Ministry of Defence Standard 00-20.

Figure 20 — Side 2 (non-component side)

Table 44 — Minimal delays complying with timing requirements

Parameter	Minimum time	Parameter	Minimum time
	ns		ns
Bus Allocation Devices bid for use of the bus by holding their $\overline{\text{Rq}}$ lines active according to rule A1. (Rule A1)		Time from slave holding $\overline{\text{CcRes}}$ active to the same slave holding $\overline{\text{BusDeallocate}}$ active. (Rule D1b)	25
Time for last of $\overline{\text{BusAcq}}$, $\overline{\text{It}}$, $\overline{\text{BusDeallocate}}$ or $\overline{\text{CcAbort}}$ becoming quiescent to the arbiter holding $\overline{\text{BusGr}}$ active. (Rule A3)	35	Time from the slave holding $\overline{\text{BusDeallocate}}$ active to the same slave releasing $\overline{\text{BusAcq}}$. (Rules D1b and A10d)	25
Time from the arbiter holding $\overline{\text{Rq(n)}}$ active to the arbiter holding $\overline{\text{BusGr}}$ active. (Rule A3a)	0	Time from the slave holding $\overline{\text{BusDeallocate}}$ active to the same slave releasing $\overline{\text{CcRes}}$. (Rules D1b and S4)	25
Time from the arbiter holding $\overline{\text{BusGr}}$ active to all devices releasing their $\overline{\text{Rq}}$ lines. (Rule A4a)	0	Time from the slave perceiving $\overline{\text{BusAcq}}$ quiescent to the same slave releasing $\overline{\text{BusDeallocate}}$. (Rule D2)	35
Time from any device releasing its $\overline{\text{Rq}}$ line in response to the arbiter holding $\overline{\text{BusGr}}$ active to the same device examining its $\overline{\text{Rq}}$ line to test for allocation. (Rule A5aii)	35	*Bus Deallocate Cycle* Time from the slave recognizing the address on the bus to the same slave holding $\overline{\text{BusAcq}}$ active. (Rule A5b)	0
Time from "Bus Free" to the allocated master holding $\overline{\text{BusAcq}}$ active, assuming that the bus was not free when $\overline{\text{BusGr}}$ became active. (Rules A5aiii, aiv, av, avii, aviii)	35	Time from $\overline{\text{BusGr}}$ being released by the arbiter, to a slave (e.g. Bus Linker) holding $\overline{\text{BusDeallocate}}$ active. (Rule D1a)	35
Time from $\overline{\text{BusGr}}$ being held active by the arbiter to the master holding $\overline{\text{BusAcq}}$ active, assuming that the bus is free. (Rule A5i)	35	Time from $\overline{\text{BusDeallocate}}$ becoming active to the arbiter releasing $\overline{\text{Rq(n)}}$. (Rule A9c)	0
Time from $\overline{\text{BusAcq}}$ being held active by the master to the arbiter releasing $\overline{\text{BusGr}}$. (Rule A8a)	0	Time from the arbiter, releasing $\overline{\text{Rq(n)}}$ to the arbiter holding $\overline{\text{BusGr}}$ active. (Rule A3b)	35
Time from the arbiter releasing $\overline{\text{BusGr}}$ to bidding devices activating $\overline{\text{Rq}}$ lines. (Rule A1)	0	Time from the arbiter holding $\overline{\text{BusGr}}$ active to the master releasing $\overline{\text{BusAcq}}$. (Rules M6 and A10c)	0
Identification of Retain Cycle Time from slave recognizing the address on the bus to the same slave holding $\overline{\text{BusAcq}}$ active. (Rule A5b)	0	Time from the arbiter holding $\overline{\text{BusGr}}$ active to the master releasing $\overline{\text{CcFin}}$ in a Write cycle. (Rules M6 and M11c)	0
		Time from the arbiter holding $\overline{\text{BusGr}}$ active to the master releasing the address. (Rules M6 and M7b)	0
		Time from the arbiter holding $\overline{\text{BusGr}}$ active to the slave releasing $\overline{\text{BusAcq}}$ after resetting its address recognition logic. (Rule A10e)	0

Table 44 — Minimal delays complying with timing requirements

Parameter	Minimum time	Parameter	Minimum time
	ns		ns
Time from the master releasing $\overline{\text{CcFin}}$ in a Write cycle to the same master releasing $\overline{\text{CcBn}}$. (Rule M9d)	35	Time from the master holding $\overline{\text{CcFin}}$ active to the slave holding Read data on the highway. (Rule S2)	0
Time from the master releasing the address to the same master releasing $\overline{\text{CcBn}}$. (Rule M9d)	35	Time from the slave holding Read data on the highway to the same slave releasing $\overline{\text{CcRes}}$. (See notes 1 and 2.) (Rule S4bi)	25
Time from the slave perceiving $\overline{\text{BusAcq}}$ quiescent to the same slave releasing $\overline{\text{BusDeallocate}}$. (Rule D2)	35	Time from the slave releasing $\overline{\text{CcRes}}$ to the master releasing $\overline{\text{CcBn}}$. (See note 2.) (Rule M9b)	0
Time from the arbiter perceiving $\overline{\text{BusAcq}}$ quiescent to the arbiter releasing $\overline{\text{BusGr}}$. (Rule A8c)	0	Time from the master releasing $\overline{\text{CcBn}}$ to the slave releasing the Read data. (Rule S5a)	0
Read Cycle		Time from the slave releasing the Read data to the same slave releasing $\overline{\text{CcFin}}$. (Rule S6a)	35
Time from the master holding $\overline{\text{BusAcq}}$ active to the same master holding an address. (Rule M2)	0	The Read cycle is complete and the bus is free.	
Time from the master holding an address to the same master holding $\overline{\text{CcBn}}$ active. (Rule M4b)	25	NOTE 1 At some time between the master holding $\overline{\text{CcFin}}$ active and the slave releasing $\overline{\text{CcRes}}$, the slave shall also hold $\overline{\text{CcFin}}$ active. (Rule S4bii)	
Time from the arbiter releasing $\overline{\text{BusGr}}$ to the addressed slave holding $\overline{\text{CcRes}}$ active. (Rule S1ii)	0	NOTE 2 At some time between the slave releasing $\overline{\text{CcRes}}$ and the master releasing $\overline{\text{CcBn}}$, the master shall also release $\overline{\text{CcFin}}$. (Rule M11b)	
Time from the master holding $\overline{\text{CcBn}}$ active to the slave holding $\overline{\text{CcRes}}$ active. (Rule S1i)	0	*Write Cycle*	
Time from the slave holding $\overline{\text{CcRes}}$ active to the master releasing the address. (Rules M5, M7a)	0	Time from the master holding $\overline{\text{BusAcq}}$ active to the same master holding $\overline{\text{CcFin}}$ active. (Rule M3a)	0
Time from the slave holding $\overline{\text{CcRes}}$ active to the master releasing $\overline{\text{BusAcq}}$. (Rules A10a, A10b)	25	Time from the master holding $\overline{\text{BusAcq}}$ active to the same master holding an address. (Rule M2)	0
Time from the master releasing the address to the same master holding $\overline{\text{CcFin}}$ active. (See note 1.) (Rule M3b)	35	Time from the master holding $\overline{\text{CcFin}}$ active to the same master holding $\overline{\text{CcBn}}$ active. (Rule M4aiii)	25
		Time from the master holding an address on the highway to the same master holding $\overline{\text{CcBn}}$ active. (Rule M4aiii)	25

Table 44 — Minimal delays complying with timing requirements

Parameter	Minimum time	Parameter	Minimum time
	ns		ns
Time from the arbiter releasing $\overline{\text{BusGr}}$ to the addressed slave holding $\overline{\text{CcRes}}$ active. (Rule S1ii)	0	Time from the master holding an address to the same master holding $\overline{\text{CcBn}}$ active. (Rule M4c)	25
Time from the master holding $\overline{\text{CcBn}}$ active to the addressed slave holding $\overline{\text{CcRes}}$ active. (Rules S1i)	0	Time from the arbiter releasing $\overline{\text{BusGr}}$ to the slave holding $\overline{\text{CcRes}}$ active. (Rule S1ii)	0
Time from the slave holding $\overline{\text{CcRes}}$ active to the master releasing the address. (Rules M5, M7a)	0	Time from the master holding $\overline{\text{CcBn}}$ active to the slave holding $\overline{\text{CcRes}}$ active. (Rule S1i)	0
Time from the slave holding $\overline{\text{CcRes}}$ active to the master holding the Write data on the highway. (Rule M8)	0	Time from the slave holding $\overline{\text{CcRes}}$ active to the master releasing the address. (Rules M5, M7a)	0
Time from the slave holding $\overline{\text{CcRes}}$ active to the master releasing $\overline{\text{BusAcq}}$. (Rules A10a, A10b)	25	Time from the slave holding $\overline{\text{CcRes}}$ active to the master releasing $\overline{\text{BusAcq}}$. (Rules A10a, A10b)	25
Time from the master releasing the address to the same master releasing $\overline{\text{CcBn}}$. (Rule M9ai)	35	Time from the master releasing the address to the same master releasing $\overline{\text{CcBn}}$. (Rule M9c)	35
Time from the master holding the Write data to the same master releasing $\overline{\text{CcBn}}$. (Rule M9aii)	25	Time from the master releasing $\overline{\text{CcBn}}$ to the slave releasing $\overline{\text{CcRes}}$. (Rule S4c)	0
(The above two periods may be overlapped.)		The Vector cycle is now complete and the bus is free.	
Time from the master releasing $\overline{\text{CcBn}}$ to the slave releasing $\overline{\text{CcRes}}$. (Rule S4a)	0	*Interrupt Cycle*	
Time from the slave releasing $\overline{\text{CcRes}}$ to the master releasing the Write data. (Rule M10)	0	Time from the arbiter holding $\overline{\text{Rq(n)}}$ active to the arbiter holding $\overline{\text{BusGr}}$ active. (Rule A3)	0
Time from the master releasing the Write data to the same master releasing $\overline{\text{CcFin}}$. (Rule M11a)	35	Time from the arbiter holding $\overline{\text{BusGr}}$ active to all devices releasing their $\overline{\text{Rq}}$ lines. (Rule A4a)	0
The Write cycle is complete and the bus is free.		Time from any device releasing its $\overline{\text{Rq}}$ line in response to the arbiter holding $\overline{\text{BusGr}}$ active to the same device examining its $\overline{\text{Rq}}$ line to test for allocation. (Rule A6ii)	35
Vector Cycle		Time from device examining its $\overline{\text{Rq}}$ line to test for allocation to the device holding $\overline{\text{It}}$ active. (Rule A6)	0
Time from the master holding $\overline{\text{BusAcq}}$ active to the same master holding an address. (Rule M2)	0	Time from device holding $\overline{\text{It}}$ active to the arbiter releasing $\overline{\text{BusGr}}$. (Rule A8b)	0

Table 44 — Minimal delays complying with timing requirements

| Parameter	Minimum time	Parameter	Minimum time
	ns		ns
Time from arbiter releasing $\overline{\text{BusGr}}$ to device releasing $\overline{\text{It}}$. (Rule A11)	0	Time from the arbiter holding $\overline{\text{CcAbort}}$ to the master releasing Write data. (Rule M10b)	0
Cycle Abort		Time from the master releasing Write data to the master releasing $\overline{\text{CcBn}}$, if held. (Rule M9f)	0
In the event of a Cycle Abort, master and slave devices are required to release any active bus lines according to the rules laid out in **5.4**.		Time from the master releasing Write data to the master releasing $\overline{\text{CcFin}}$. (Rule M10e)	35
This subclause covers Cycle Abort timing under the headings arbiter, master and slave.		*Slave*	
Arbiter		Time from the slave releasing Read data (and $\overline{\text{CcRes}}$, if held) to the same slave releasing $\overline{\text{CcFin}}$ in response to $\overline{\text{CcAbort}}$. (Rule S6b)	35
Time from the arbiter holding $\overline{\text{CcAbort}}$ active to the arbiter releasing any other lines it may be holding active. (Rules A8d, A9d, A10f)	25		
Time from release of last cycle control line to release of $\overline{\text{CcAbort}}$. (Rule C2)	35	*Reset*	
Master		In response to the $\overline{\text{Rs}}$ line becoming active, all devices connected to the bus shall release all address (data lines are a subset) and cycle control lines that they may be holding active, according to the rules laid down in **5.4**.	
Time from the arbiter holding $\overline{\text{CcAbort}}$ active to the master releasing $\overline{\text{BusAcq}}$. (Rule A10f)	0		
Time from the arbiter holding $\overline{\text{CcAbort}}$ active to the master releasing $\overline{\text{It}}$. (Rule A11b)	0	Time from $\overline{\text{Rs}}$ becoming active to release of address, Read or Write data.	0
Time from the arbiter holding $\overline{\text{CcAbort}}$ active to the master releasing an address, including $\overline{\text{CcFin}}$ in a Write cycle. (Rules M7c, M11d)	0	Time from release of the last of any data or address lines to the release of the last of any corresponding cycle control line(s).	35
Time from the master releasing an address (including $\overline{\text{CcFin}}$ in a Write cycle) to the same master releasing $\overline{\text{CcBn}}$ in response to $\overline{\text{CcAbort}}$. (Rules M9eii, M11d)	35	The period for which the $\overline{\text{Rs}}$ line shall be active to reset all devices connected to the bus.	5×10^4

Appendix M Bus receiver a.c. noise rejection

M.1 when triangular positive-going and negative-going pulses, as defined in Figure 21(a) and Figure 21(b), are applied to the device in a circuit as shown in Figure 22, the output from the device shall not enter the threshold window [0.8 V to 2.0 V for transistor transistor logic (TTL)] from either side.

NOTE 1   Movement of the output signal to one or other of these threshold levels from outside the window does not constitute non-compliance.

NOTE 2   The test load needs to be appropriate to the purpose of the output under examination and would normally be specified by the device manufacturer. It is not possible to specify a single test load applicable to all potential bus receiver circuits.

NOTE 3   The pulse generator needs to be able to generate pulses whose base line is displaced from 0 V by a d.c. offset, V_{OFS}.
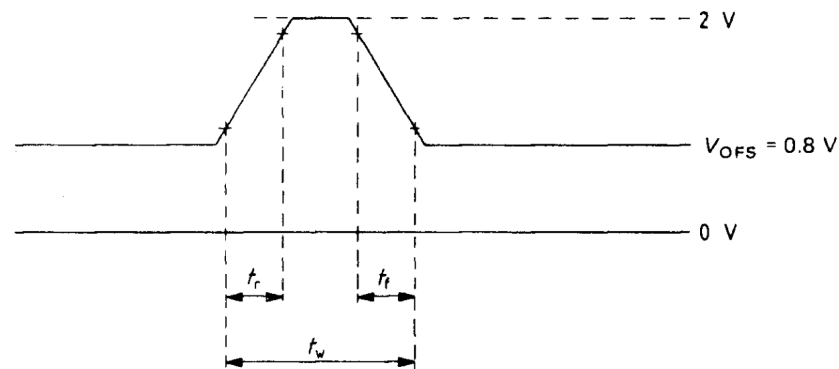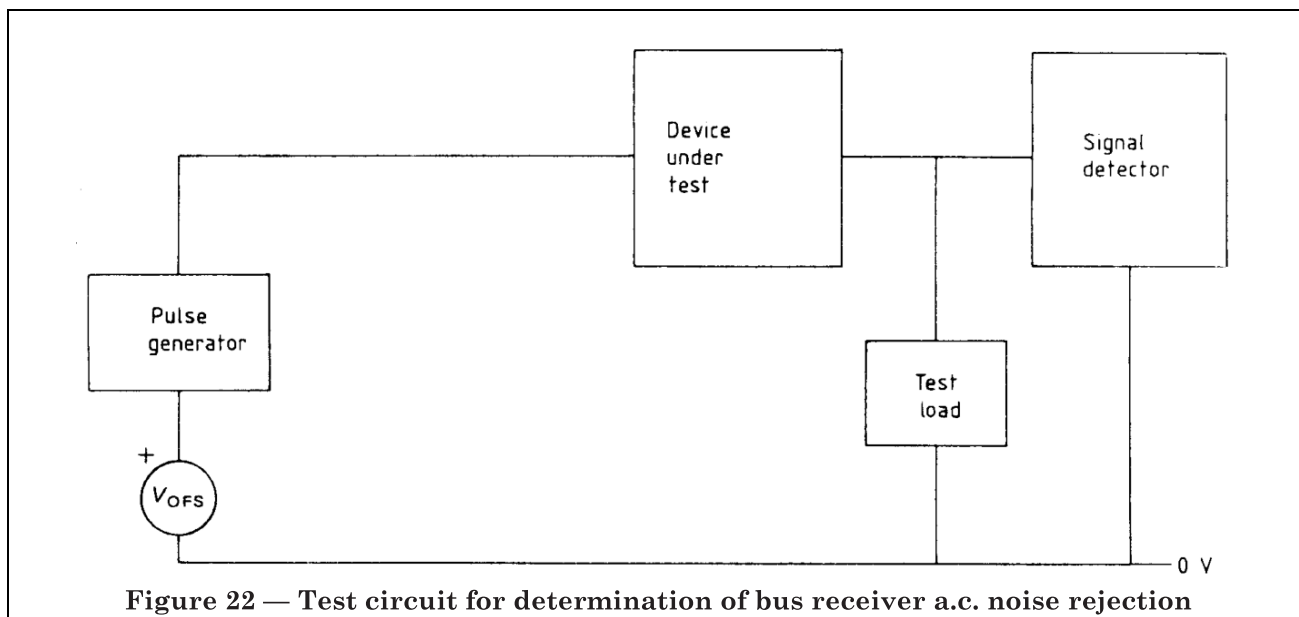

(a) Positive-going pulse
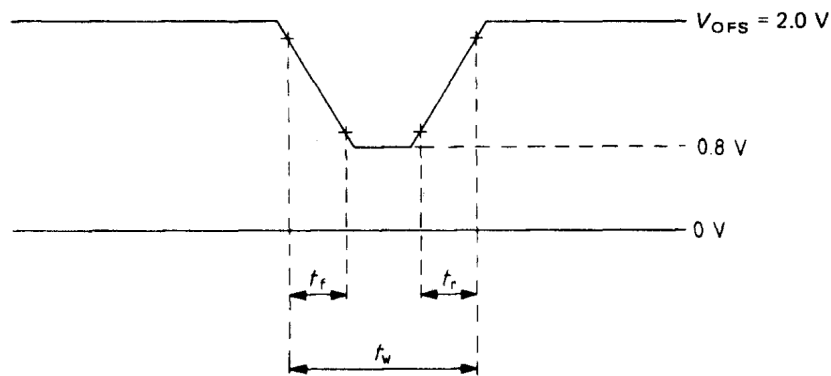
(b) Negative-going pulse

NOTE   The following limits apply:

t_{r}(10 % to 90 %)   =   7.0 ns (max.)

t_{r}(90 % to 10 %)   =   7.0 ns (max.)

t_{w} = 15.0 ns (min.)

Figure 21 — Test pulses

Figure 22 — Test circuit for determination of bus receiver a.c. noise rejection

Appendix N Test circuit and waveform for determination of transient sink current (see Figure 13)

N.1 Test circuit

Use a test circuit as shown in Figure 23 and an input appropriate to the device under test (D.U.T.).

NOTE   A complex large scale integration (LSI) device or simple line driver will probably require different inputs or sequences.

N.2 Waveform

Use a test waveform as shown in Figure 24, with V_{OUT} no greater than 0.75 V and T_{FALL} no greater than 26 ns.
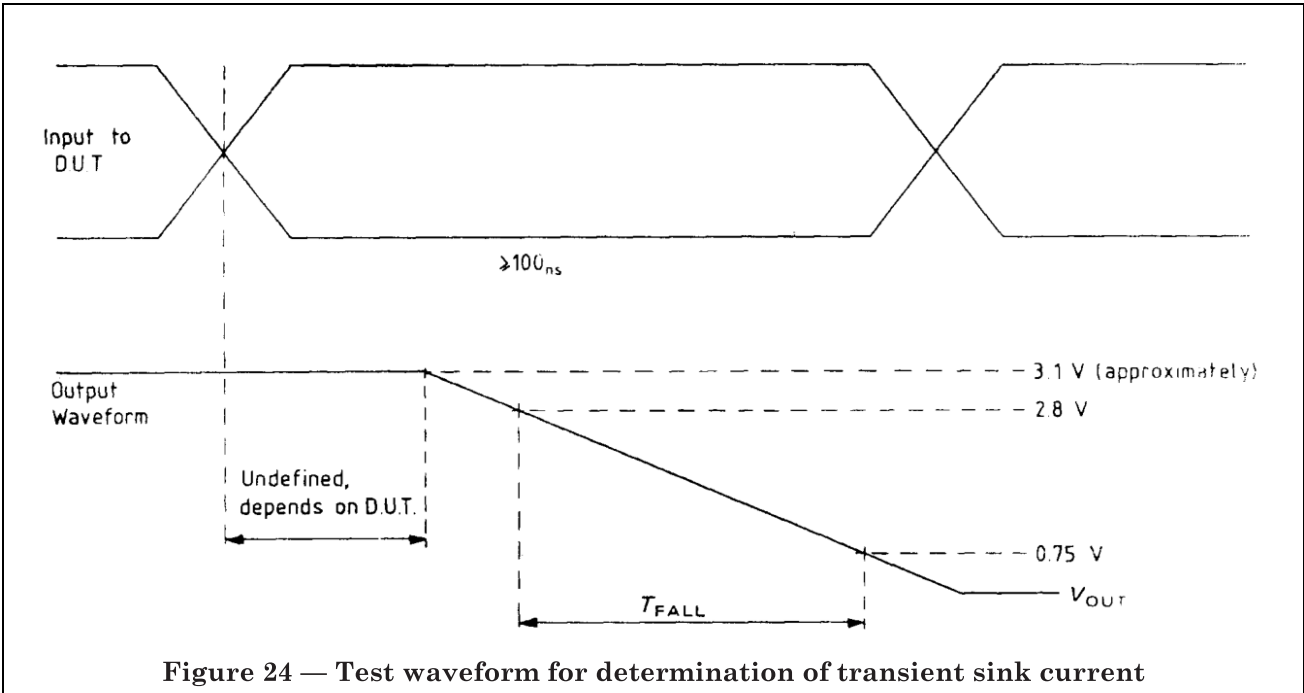

Figure 23 — Test circuit for determination of transient sink current
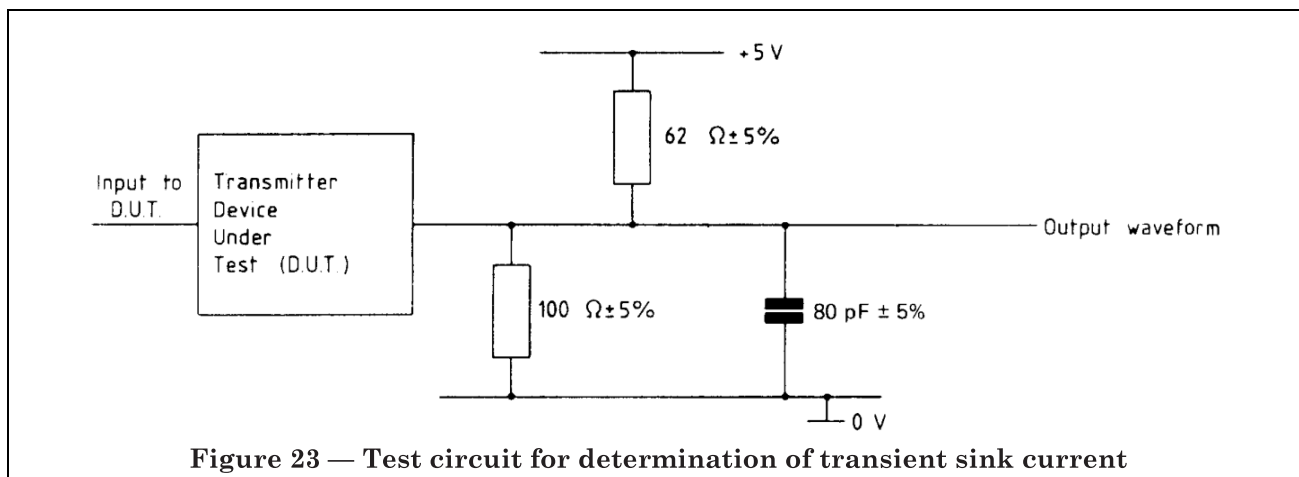
Figure 24 — Test waveform for determination of transient sink current

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Publications referred to

BS 5954, *Specification for dimensions of panels and racks for electronic equipment.*

BS 9400, *Integrated electronic circuits and micro-assemblies of assessed quality: generic data and methods of test.*

BS 9525 N0001: Issue 2, *Multi-contact two-part printed board electrical connectors of assessed quality with replaceable contacts and through board solder, solder for wire, wire wrap or crimp terminations — full plus additional assessment.*

BS CECC 40100, *Harmonized system of quality assessment for electronic components. Sectional specification: Fixed low power non-wirewound resistors.*

BS CECC 50000, *Harmonized system of quality assessment for electronic components. Generic specification: Discrete semiconductor devices.*

IEC 147, *Essential ratings and characteristics of semiconductor devices and general principles of measuring methods.*

IEC 147-2, *General principles of measuring methods.147-2B. Second supplement.*

IEC 603, *Connectors for frequencies below 3 MHz for use with printed boards.*

IEC 603-2:1980, *Two-part connectors for printed board, for basic grid of 2.54 mm (0.1 in), with common mounting features.*

Ministry of Defence Standard 00-20. Eurobus A specification.

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