BS ISO 18257:2016

BSI Standards Publication

Space systems — Semiconductor integrated circuits for space applications — Design requirements

bsi.

National foreword

This British Standard is the UK implementation of ISO 18257:2016.

The UK participation in its preparation was entrusted to Technical Committee ACE/68, Space systems and operations.

A list of organizations represented on this committee can be obtained on request to its secretary.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

Published by BSI Standards Limited 2016

ISBN 978 0 580 87096 5

ICS 49.140

Compliance with a British Standard cannot confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 30 November 2016.

Amendments/corrigenda issued since publication

Date	Text affected

BS ISO 18257:2016

INTERNATIONAL STANDARD

ISO 18257

First edition
2016-11-15

Space systems — Semiconductor integrated circuits for space applications — Design requirements

Systèmes spatiaux — Circuits intégrés semi-conducteurs d'applications spatiales — Exigences de conception

Reference number
ISO 18257:2016(E)

ISO copyright office
Ch. de Blandonnet 8 • CP 401
CH-1214 Vernier, Geneva, Switzerland
Tel. +41 22 749 01 11
Fax +41 22 749 09 47
copyright@iso.org
www.iso.org

Contents

Page

Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents).

Any trade name used in this document is information given for the convenience of users and does not constitute an endorsement.

For an explanation on the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see the following URL: www.iso.org/iso/foreword.html.

The committee responsible for this document is ISO/TC 20, *Aircraft and space vehicles*, Subcommittee SC 14, *Space systems and operations*.

Introduction

Normative design requirements of semiconductor integrated circuits for space applications largely determine the reliability of an integrated circuit (IC) and its adaptability to space environment, thereby affecting the reliability of space systems. IC tests and experiments based on product specification only can provide a comprehensive evaluation of its reliability. Once applied to space systems, the design flaws will directly affect the implementation of aerospace engineering. The development of design requirements for semiconductor ICs for space applications can ensure its reliability and space suitability from its very source to meet the space application requirements.

INTERNATIONAL STANDARD ISO 18257:2016(E)

Space systems — Semiconductor integrated circuits for space applications — Design requirements

1 Scope

This document specifies the basic design requirements for semiconductor ICs for space applications, including its design process, as well as required tasks and requirements of each stage. Requirements of specific circuit design are not included.

2 Normative references

The following documents are referred to in text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967-2, *Integrated circuits — Measurement of electromagnetic emissions*

IEC 62132, *Integrated circuits — Measurement of electromagnetic immunity*

IEC 62215-3:2013, *Integrated circuits — Measurement of impulse immunity — Part 3: Non-synchronous transient injection method*

IEEE 1149.1, *IEEE standard for test access port and boundary — Scan architecture*

3 Terms and definitions

For the purposes of this document, the terms defined in ISO 10795 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— IEC Electropedia: available at http://www.electropedia.org/

— ISO Online browsing platform: available at http://www.iso.org/obp

3.1
programmable logic device
PLD
hardware-programmable device

EXAMPLE FPGA, CPLD, etc.

3.2
suitability
degree to which a product meets its requirements

3.3
environment adaptability
ability to achieve the entire product's intended functions, performance and (or) capacity for protecting itself under various environments within its life cycle

3.4
testability
ability to perform function and performance testing of the circuit, position the failure of the circuit and select qualified circuit chip as soon as possible

4 Abbreviated terms

ASIC	application specific integrated circuit
BIST	built-in self test
CMOS	complementary metal oxide semiconductor
DFT	design for test
DRC	design rule checking
EMC	electro-magnetic compatibility
ERC	electrical rule checking
ESD	electrostatic discharge
FPGA	field programmable gate array
IC	integrated circuit
I/O	input/output
IP	intellectual property
JFET	junction field effect transistor
MOSFET	metallic oxide semiconductor field effect transistor
NMOS	N-channel metal oxide semiconductor
RAM	random access memory
RC	resistance capacitance
ROM	read only memory
RTL	register transfer level
SAR ADC	successive approximation register analogue digital converter
SCR	silicon controlled rectifier
SEL	single event latch-up
SET	single event transient
SEU	single event upset
SOI	silicon on insulator
SOS	silicon on sapphire

5 General requirements

General requirements in designing semiconductor ICs for space applications include:

a) process conducted under a fault-tolerant system with design requirements;

NOTE 1 Special implements are allowed for different types of ICs for space applications.

b) adherence to existing standards and regulations during the design process;

c) feasibility and risk analysis of requirements from aerospace customer to validate the rationality of its functional and performance requirements;

d) conversion of users' requirements into design input, which may involve the following steps:

1) derating the design criteria;

NOTE 2 Derate on the basis of nominal stress according to the stress of the circuit. The key is the level and effects. Derating can improve reliability, but takes into consideration issues such as reliability, size, weight and cost.

2) applying fault-tolerant design and adopting rational use of redundant technology;

3) ensuring the characteristics of the orbit thermal environment for reliable thermal design;

4) considering radiation hardness to ensure grade requirements, if necessary;

5) taking note of the life of customer's requirements (mean time to failure);

e) decomposition of the design input requirements to each design stage according to its tasks.

NOTE 3 Implement and validate each step until all objectives and requirements of a semiconductor IC for space applications are achieved.

6 Design process

6.1 Overview

IC designs generally include architecture design, logic design, circuit design and layout design. In order to ensure the validity of the design, computer simulation and verification of its results at each stage are necessary. Figure 1 illustrates the IC design flow.

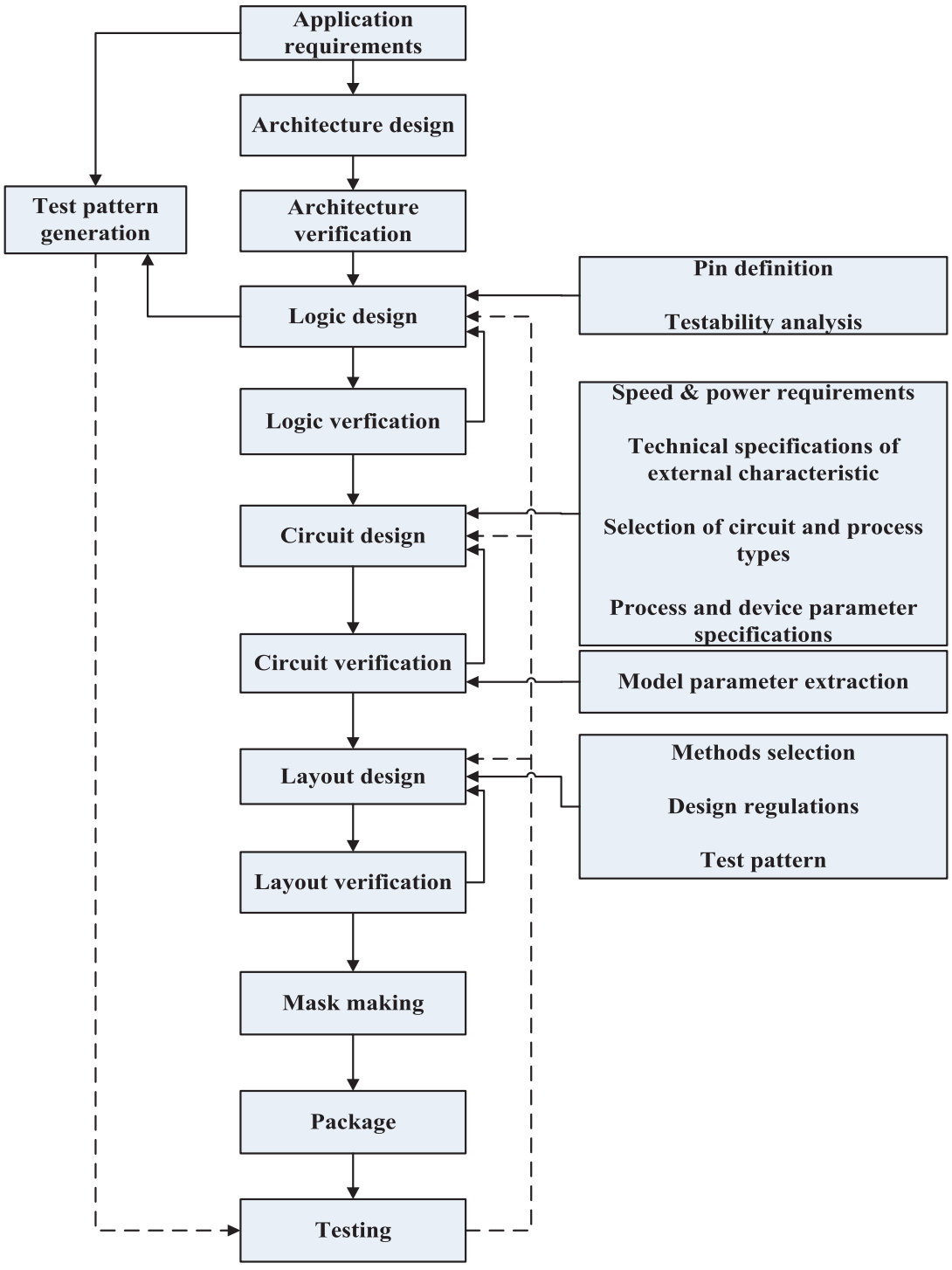

Figure 1 — Integrated circuit design flow diagram

In designing semiconductor ICs for space applications, designers have to follow a general IC design process to convert users' general and special requirements (i.e. user-oriented features, performance and reliability requirements, etc.) into design input, thereby accomplishing the design goals of each stage to meet the overall requirements. Figure 2 illustrates the decomposition of tasks in the design process of semiconductor IC for space applications.

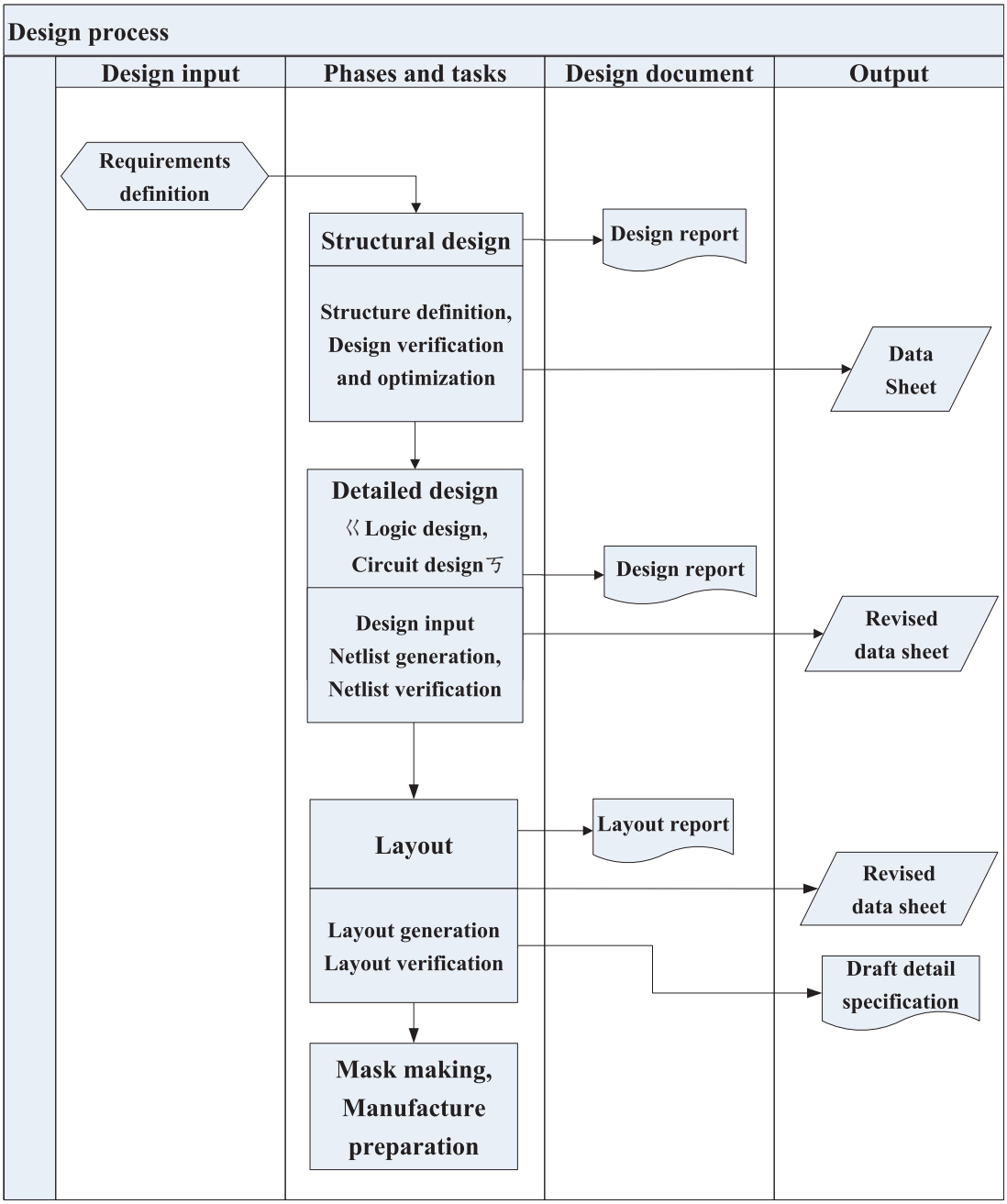

Figure 2 — Decomposition of tasks in designing semiconductor IC for space applications

6.2 Design input

A design input document will be formed after completing the requirements definition. Design input generally includes (modifications are allowed according to specific circuit requirements) the following:

a) system division, system configuration and operating mode;

b) system interface, external device communication protocols, including memory-mapped register;

c) operating frequency range;

d) constraints of electrical parameter;

e) functional requirements;

f) application algorithm;

g) reset and power dissipation requirements;

h) error handling;

i) testing mode;

j) fault coverage requirements of digital circuit testing;

k) key signal timing;

l) constraints of the normal working environment;

m) constraints of the special space working environment, which includes

   1) space radiation,

   2) heat dissipation in vacuum, and

   3) in-space charging effects (i.e. ESD, latch-up);

n) power dissipation budget;

o) physical and mechanical constraints include: pin distribution, size, packaging;

p) reusability and additional features of the product;

q) new technologies;

r) intellectual property of design;

s) IP cores that are necessary and with verification.

6.3 Design phases and tasks

6.3.1 Architecture design

6.3.1.1 Overview

Finding an architecture design that offers efficient functionality at minimal cost, while meeting users' objectives and constraints, is important.

6.3.1.2 Design content

The following is the architecture design process.

a) Define the chip architecture, verify and record the completion of functions of the basic module, as well as interfaces and interactions.

b) Select and validate the chip architecture.

c) Ensure that all definitions and selections are in accordance with the documents made in the definition phase.

d) Ensure that the output includes:

   1) a simulation model,

   2) the results verification, and

   3) a preliminary datasheet.

The datasheet shall conform to the requirements of Annex A.

Verification: For example, complex digital circuit research and development will be realized through FPGA sample or tested by simulation; digital circuit code coverage requirements; requirements for hardware and software interaction; applications of the code rules.

6.3.1.3 Design verification

The following is the architectural design verification process.

a) Verify whether the defined architecture meets demands through appropriate simulation and analysis techniques.

b) Complete independent verification.

c) Finish the primary placement and routing after the hardware unit is connected, making sure each unit is placed effectively under the given constraints.

NOTE Does not apply to PLD design.

d) Put in place a back-up plan, in case conflicts occur (i.e. power dissipation and speed, performance, pin number and package size, complexity and area).

e) Establish a final system design.

f) Complete the initial datasheet.

6.3.2 Logic design and circuit design

6.3.2.1 Overview

In this stage, the high-level system design is transmitted and transformed to unit-level architecture description with the chosen technology library, and the input information of the next phase, such as layout constraints, placement and routing, and product testing and detailed pin description, etc. are generated. Logic design and circuit design are included. For digital circuits, verified gate-level netlist is generated; while for analogue circuit, verified transistor-level netlist is generated.

6.3.2.2 Design content

The following is the logic design and circuit design process.

a) Provide complete details of the circuit architecture.

b) Identify testability description and product testing methods, including extent of fault coverage.

c) Identify circuit and layout, which are considered together for simulation design.

d) Test concept of definition during design input and synthesis stage (i.e. scan path, testability logic, test points, test bus and boundary scan).

e) Identify radiation-hardened concept through design and synthesis stage, when applicable.

f) Implement step-by-step verification plans and verify the results obtained.

g) Validate pin leads and connection plans, paying special attention to technical constraints (i.e. power dissipation supply and pin definition).

h) Select buffers according to I/O requirements.

i) Ensure that output includes

1) updated datasheet (including output pin), and

2) updated design database (including netlist, layout constraints, product testing and testing vectors).

6.3.2.3 Design verification

The following is the logic design and circuit design verification process.

a) Verify parasitic data and delay data of the assessment layout.

b) Use the testing method from system design to complete the gate-level simulation, such as formal verification and static timing analysis.

NOTE 1 Does not apply to pure analogue circuits, but applies to digital parts of a hybrid circuit, such as A/D converter and D/A converter.

c) Verify critical parameters such as bias voltage, operating point, frequency, dynamic, linear range, and modify the timing.

d) Complete functional verification, including verification of interface.

NOTE 2 It applies to analogue circuit design and analogue part of a hybrid circuit.

e) If the simulation of the whole mode cannot be completed at the top level (such as operating time limit), simulation of typical mode is allowed.

f) From the results of simulation of a typical model, verification and analysis can be applied to other models.

g) Verify the realized testing concepts, such as scan path design, testability design DFT logic, measurement points and test bus.

h) Verify the radiation-hardened concept at the netlist level.

i) Verify defined typical power dissipation.

j) Upload the parameters of the preliminary datasheet according to results obtained.

k) Generate test vectors and verify the fault coverage requirements.

l) Complete parameter sensitivity analysis.

NOTE 3 It applies to analogue circuit design and analogue part of a hybrid circuit.

6.3.3 Layout design

6.3.3.1 Overview

Transforming a circuit design into a layout design, as well as its verification, are important parts in the physical realization of an IC design, serving as the transition from the design phase to its manufacture.

6.3.3.2 Design content

The following is the layout design process.

a) Determine chip placement.

NOTE 1 This does not apply to PLDs.

b) Complete the placement and routing, ensuring that all constraints are considered.

c) Complete netlist optimization according to timing and design rules.

NOTE 2 Only applies to digital ASIC design.

d) Generate power dissipation distribution.

e) Generate clock distribution.

NOTE 3 Does not apply to analogue ASIC design.

f) Insert core and pad power, as well as other testing pins.

g) Determine the size of die.

NOTE 4 Does not apply to PLD design.

h) Generate a bonding diagram, ensuring that constraints of package wire are considered.

NOTE 5 Does not apply to PLD design.

i) Ensure that the output contains

1) an updated datasheet,

2) an updated design database (including layout imitation netlist of the target requirements and related parasitic information), and

3) a draft detail specification.

6.3.3.3 Design verification

The following is the layout verification process.

a) Perform a design rule checking (DRC).

b) Perform an electrical rule checking (ERC) if user requests and crosstalk sensitivity shall be checked as well.

c) Extract the netlist from the layout.

d) Verify the consistency between the gate-level netlist and the layout by comparing the layout and the circuit schematic.

e) Verify the functional consistency between the pre-layout netlist and the post-layout netlist through simulation and formal methods.

f) Extract parasitic information.

g) Complete the comprehensive layout verification through anti-standard simulation and timing analysis.

h) Check clock jitter and delay.

NOTE 1 Does not apply to PLD design.

i) Check I/O-related timing.

j) Check chip power dissipation.

NOTE 2 Does not apply to PLD design.

k) Describe timing performance of the circuit (i.e. maximum clock frequency, clock duty factor, input set-up and its holding time, output propagation delay).

l) Update the data table.

6.4 Mask making, package and testing

Once the design is complete, prototype manufacturing begins. It involves mask making, package and testing. The following is the prototype manufacturing process.

a) Transform correct layout data into data format that is acceptable to the mask system.

b) Submit basic device electrical parameters and process parameter documents according to design requirements for manufacturers to produce and package.

c) Test circuit function and its performance parameters by conducting irradiation tests and reliability tests according to requirements of the detail specification to ensure that the product meets the requirements.

7 Detailed requirements

7.1 Architectural design requirements

The detailed architectural design requirements are provided in the list below, while the design guidance is provided in Annex B.

Architectural design requirements include:

a) semiconductor chips subdivided into basic functions or modules, with each interface, function and interaction identified and recorded;

b) architecture definition divided into process definition, transistor-level or gate-level mapping;

c) algorithm and schematics, including realization of functional parameters;

d) independent chip modules at different positions with each sub-function identified;

NOTE Sub-functions can be compiled as core against other designs.

e) clock reset program to ensure correct data transmission of clock domains and asynchronous clock part;

f) generated model as input for subsequent detailed design.

7.2 Logic design and circuit design requirements

Code design shall meet the following specifications when designing digital circuits.

a) Initial ports state shall be stable and informed.

b) Comprehensive design principles shall

1) avoid level-sensitive transparent latches and combination of feedback loops when describing combinational logic,

2) have individual temporal logic blocks that can only be triggered by one clock transition within each timing logic block, and

3) employ synchronous design when describing the design.

c) Asynchronous logic shall be avoided when designing register transfer level (RTL) code. If asynchronous logic has to be employed, synchronizer among asynchronous interfaces is needed to ensure reliability of the design.

d) An internal logic unit clock generated by employing independent clock management unit, which supports independent reset unit to synchronize the reset input signal in generating the required reset signal of the internal logic unit.

e) Internal logic unit shall prohibit the use of tri-state bus and combined ring to ensure higher testing coverage of DFT design and circuit reliability.

7.3 Layout design requirements

Layout design requirements include:

a) a reliable circuit with the smallest footprint;

b) layout design that meets process design regulations from technology vendors;

c) die corner design, die seal ring design, wide metal slotting and other design criteria with the following specifications:

   1) die corner with a 45° metal wiring in chip corner;

   NOTE 1 The size of the die corner is determined by chip size.

   2) die seal ring (from substrate to pdiff, contact, metal1, via1 until the highest level of metal) to protect the chip against the blade when cutting;

   3) wide metal slotting with 45° corner to alleviate the pressure caused by current density in the metal (slotted placement shall be consistent with current direction);

d) placement and routing that addresses signal harassment;

   NOTE 2 Follow the principle of reducing parasitic parameters.

e) overall chip power design that employs vertical and horizontal grid wiring to ensure that every memory bit could obtain V_{DD} and V_{SS} from the power grid;

   NOTE 3 Design the power cord width of the word line direction according to the array stored number to achieve the supply capacity when all units operating line are open at the same time.

f) trace width spacing, through-hole diameter and hole line spacing that minimize trace lengths and number of through-holes.

7.4 Package design requirements

7.4.1 Package structure design requirements

Package structure design requirements include:

a) an adhesive or bonding surface on the package, the size of which is determined according to the chip size;

   NOTE 1 Ensure that there is enough space so that the bonding process does not affect the chip's electrical performance.

b) bonding wires configured according to pad size, pitch and pin orientation;

   NOTE 2 Ensure that functional pads can be smoothly extracted and step width between bonding wires meet bonding requirements.

c) melt seal ring that matches the size of the case and meets requirements;

d) case thickness that ensures mechanical strength.

7.4.2 Packaging technology design requirements

Packaging technology design requirements include:

a) bonding wires that meet requirements on thickness, length and bonding strength;

NOTE 1 Avoid cross phenomenon when arranging bonding wires.

b) melt seal ring with sufficient space left inside and outside to avoid short circuit caused by solder splash;

NOTE 2 Take full account of solder overflow when designing the melt seal ring.

c) a technology design verified through technology experiments, ensuring the feasibility of the design when necessary.

7.4.3 Packaging electrical simulation analysis requirements

Packaging electrical simulation analysis requirements include:

a) simulation software to extract important electrical performance parameters to meet device performance requirements;

b) optimized layout design to make sure parasitic parameters meet design requirements;

NOTE 1 Take full account of the effects of placement and routing on R, L, C parasitic parameters.

NOTE 2 Adjust placement and routing design to reduce parasitic parameters when some of them are high.

c) simulation software for three-dimensional bonding simulation analysis to ensure the feasibility of bonding technology, when necessary.

NOTE 3 Take full account of the effects of the thickness and length of bonding wire on circuit performance when necessary.

7.4.4 Packaging thermal simulation analysis

Packaging thermal simulation analysis requirements include:

a) thermal simulation software for a full assessment of the thermal performance of a package;

b) junction temperature not exceeding allowable value;

NOTE 1 Consider adding a heat sink at the back when the chip's power dissipation is high to improve the cooling capacity of the shell.

c) an optimized shell structure to improve thermal performance when thermal performance is insufficient.

7.5 Reliability design requirements

7.5.1 Overview

ICs for space application require high reliability. The aim of reliability design is to guarantee circuit functionality and performance parameters, improve circuit's capacity of antistatic, anti-latch up, anti-interference, and resistance to adverse environment, extend life of product, and reduce failure rate. Increase the design margin when it could affect reliability.

7.5.2 Reliability design requirements

Reliability design shall employ an optimized design technology and efficient maintenance to reduce product failure, as well as achieve objectives at minimal cost while meeting functional requirements.

Reliability design requirements include:

a) technologically mature design to meet overall technical performance requirements;

b) simplified design, taking into consideration relevant standards and regulations;

c) derating design and redundant technology criteria;

d) fault-tolerance approach and anti-transient stress design to ensure the stability and reliability of the product;

e) thermal design suited for space environment;

f) protection against harsh environment (which should include overload, vibration, shock, temperature, humidity, vacuum, fungus, salt atmosphere, dust and electrostatic, electromagnetic radiation, etc.) that meets environmental standards;

g) design rules according to the features of a circuit application software;

h) a microchip supporting several functions which can make the failure rate of the entire system lower;

i) packaging designed to minimize failure rate.

7.5.3 Antistatic design requirements

Antistatic design shall comply with the following requirements when applicable.

a) The aim of antistatic is to provide low resistance discharge path for electrostatic charge. Discharge resistor shall be as low as possible to withstand highest possible instantaneous power.

b) Antistatic protection circuit shall occupy the smallest area possible on the chip. Antistatic design on full chip is necessary, including at least ESD clamp circuit between power and ground, ESD protection circuit between input and output pads.

c) On the promise that the operation of circuit is guaranteed, selected trigger voltage should be relatively low to be triggered easily.

d) ESD rating shall be tested to guarantee the required value.

7.5.4 Low-power design requirements

Low-power design could be developed in the system level, logic level, board level, layout and process level. From its source, power dissipation can be mainly divided into two parts, dynamic power and static power dissipation. Low-power design shall meet the following requirements:

a) low power dissipation to ensure functionality and performance;

b) low dynamic power dissipation.

To ensure functionality, performance and reliability, reduce power dissipation by using lower supply voltage, reducing circuit load capacitance and circuit average flip rate, as well as clock frequency. Lower supply voltage can sometimes reduce the hardness against interference, so it shall be balanced.

7.5.5 Parameter modification and design margin optimization requirements

In parameter modification and design margin optimization:

a) take into account the impact on the circuit performance under worst conditions when the negative and positive of the operating voltage and temperature pull partial;

b) take into account the impact on circuit performance when device parameters scatter during manufacturing process;

c) select the design parameters through analysing the worst conditions of analogue circuit (increase margin when reliability could be affected).

7.5.6 Electromagnetic compatibility design requirements

Electromagnetic compatibility design requirements include:

a) interference sources, sensitive sources and coupling paths;

   Pay attention to interference sources such as high-speed logic circuits, high-speed clock circuits, as well as sensitive circuits such as microprocessors and low-level analogue circuits. Any factor which influences EMC should be minimized.

b) separation between digital and analogue circuits;

c) controlled capacitance coupling and inductive coupling;

d) mode of signal grounding in the ground plane design;

e) connection to the shield enclosure and heat sink;

f) conducted emission and conducted immunity that meet requirements;

g) radiated emissions and radiated immunity that meet requirements.

EMC verification and test shall follow IEC 62215-3:2013, IEC 61967-2, and IEC 62132.

7.5.7 Radiation-hardened design requirements

To meet the requirements of circuit functionality and performance, design hardening aims to realize a radiation-hardened circuit design without any design complexity and power dissipation. Hardening activities shall be undertaken during the circuit design process, as well as at system level, circuit level and layout to enhance the radiation hardness of the circuit.

The radiation-hardened assurance design of semiconductor ICs for space applications can meet circuit requirements through design hardening and technical hardening. Follow these steps.

a) Verify the radiation-hardened requirements of the customer and determine whether to adopt technical hardening.

b) Verify the technical library if technical hardening is preferred.

   Design hardening programs shall take full account of the feasibly of the technical process.

c) Evaluate the circuit radiation hardness by performing an irradiation test when necessary:

   1) Establish or use scientific, faultless single particle test, as well as total dose testing method.

   2) Verify the particle type and dose of tests according to circuit application environment and radiation hardness.

   3) Establish test data calculating systems and evaluation models of SEU, SET and SEL.

4) Accomplish tests according to requirements and obtain the estimated target.

7.6 Testability design requirements

Testability design requirements include:

a) pre-inserted dedicated test architectures in key parts or peripheral interface of the chip during the design process;

An automatic test equipment will evaluate the inserted test architectures or scan chains for their functionality and performance, as well as carry out testing coverage analysis and failure orientation and detect the defects and failures during layout design and prototype production to ensure the correctness.

b) a test architecture and dynamic detection point inserted during the design process to ensure testability of local design and internal circuit;

c) test vectors of circuits automatically generated according to testing rules, methods, as well as fault models;

NOTE 1 Evaluate the testing coverage to assist in the improvement of the test architecture.

e) boundary scan design (compliant with IEEE 1149.1);

NOTE 2 Clock and reset pins need a boundary scan cell (at least an observe cell), while power and ground pins do not need a boundary scan design.

f) built-in memory in the self-testing design;

NOTE 3 Choose the appropriate algorithm according to the memory type to cover as many types of fault as possible. Take note that testing coverage and testing area need compromise.

g) scan chain design;

NOTE 4 Determine the number of scan chains according to circuit scale and ensure that the testing coverage meets requirements.

Annex A
(normative)

Datasheet

A.1 Goals and objectives

Gather all technical data from system design to final design verification as input for application and procurement.

A.2 Scope and content

The scope and content of the datasheet includes:

a) circuit name, number and release date on each page;

b) description of all the features and constraints of the circuit such as detailed interface description, register definitions and memory map;

c) system overview of the circuit, and the description of its application under typical system environment, including application block diagram;

d) detailed description of all features and modes of operation;

e) detailed description of the signal interface, including definition of all signals, tests and power pins, as well as signal and functions of its signal polarity;

f) description of signals in groups according to their functions;

g) definition of all electrical data and mechanical data, as well as related application conditions:

   1) absolute maximum range includes reliability index of storage temperature, operating temperature, supply voltage, maximum pin input current, total dose, SEU, latch-up electrostatic discharge, etc.;

   2) DC parameters include voltage, leakage current, pin capacitance and output current;

   3) typical value of static and dynamic power dissipation in lower frequency operation;

   4) AC parameters include set-up and hold time, cycle time, output delay, tri-state delay, and relevant waveform;

   5) evidence of related timing characteristics of reference signal edge;

   6) package description includes pin configuration, package diagram with pin number and signal name including mechanical drawing of package thermal characteristics such as thickness of the material and heat transfer coefficient.

Annex B
(informative)

Guidance

B.1 Architectural design guidance

The topology architecture is designed according to the function and parameter requirements of the circuit. Typical topology architectures of semiconductor ICs are as follows:

a) complementary bipolar amplifier architecture is recommended for high-speed broadband amplifying;

b) high-impedance input architecture (i.e. JFET) is recommended for weak signal process amplifying;

c) PN junction isolation amplifier architecture is recommended for low-speed, low-accuracy and low-power amplifying;

d) linear regulator architecture is recommended for low-noise and ripple power supplying;

e) switching regulator architecture is recommended for high-efficiency power supplying;

f) Flash ADC architecture is recommended for high-speed analogue-to-digital conversion;

g) Σ-Δ ADC architecture is recommended for high-precision analogue-to-digital conversion;

h) SAR ADC architecture is recommended for medium speed and accuracy, low-power consumption and no transmission delay analogue-to-digital conversion.

These architectures are recommended but not required. With the development of new technologies, new architectures can be used.

B.2 Logic and circuit design guidance

Based on the understanding of the design requirements and the existing conditions, fully consider the logic design principles, and take into account the following guidance.

a) A trade-off between area and speed means to achieve the minimum area in the guarantee speed premise. The main design methods include “ping-pong” operation, pipeline operation, time division multiplexing, logic multiplexing, serial-parallel conversion operation, asynchronous clock domain data synchronization, reset operation.

b) The top-down system design is suggested.

c) Adopt a synchronous design. The main signal is caused by trigger. Divide the clock domain in the whole system well, then try to use the clock in the same clock domain as the time-driven, take in account these clock lines, interferences and delays.

d) Code comments must be concise and clear and explanatory notes should be extensive.

e) Too many levels within the module design of code should be avoided. At the same time, the excessive detail function description in the top-level documents should be avoided.

B.3 Layout design guidance

The following are the layout design guidelines.

a) Aluminium lines should be short and wide, and could not have cross connections.

b) Grounding holes should be as large as possible.

c) The overlap between the aluminium line and the connector hole shall be proper.

d) Connection mode shall be reduced with diffused strip, as much as possible.

e) Units with similar parameters should be placed in adjacent areas; geometric architecture should be as symmetrical as possible, the symmetry should not be sacrificed for a more convenient wiring.

f) Hierarchical design guidance

The layout should be designed according to the hierarchical model. According to the repeatability and functional unit, the layout is divided then each unit layout is designed and the general drawing is generated.

g) Minimization design guidance

It is important to use the silicon area fully, and increase the rate of finished products within the process conditions permission. The layout area should be as small as possible and close to the square, in order to reduce the occupied area of each circuit.

h) Reduce the number of isolation zone

The isolation frame takes up a lot of chip area for PN junction isolation zone. The number of the isolation zone should be reduced, whenever possible.

i) Prevent the parasitic effect

1) The epitaxial layer of the resistance island should be connected to the highest potential, and the isolation tank should be connected to the lowest negative potential, which is necessary for guaranteeing the PN isolation effect.

2) The input and output terminals should be separated away as far as possible.

3) The exothermic unit or the position where the most power is consumed (i.e. resistance) should be placed in the centre of the chip to make the temperature distribution uniform.

B.4 Package design guidance

The following are the package design guidelines.

a) The reliability design of bonding, including the bonding wire and the bonding solder joints should be considered, especially the effects of the high temperature aging on the brittleness of the bonding.

b) The adhesion strength of the chip, especially the shear stress on the chip with the elevated work temperature, should be considered. So the thermal shock and mechanical vibration should be done.

c) Hermetic seal is preferred. For hermetically sealed devices, a vacuum test should be considered.

d) The residual gas and water vapour content should be considered, and no harmful gases exist in the cavity.

e) Take full account of the heat dissipation requirements of the power circuit.

f) Take account of the solderability of the pins and the corrosion of the pins and package.

g) Unless otherwise specified, the following architectures, materials and processes are prohibited:

1) use of pure tin or silver, as well as use of zinc, chromium and electroless nickel as a final finish;

Pure tin is prohibited on leads and cases as a final finish. Unless specified, zinc and chromium is prohibited on leads and cases as a final finish. Electroless nickel shall not be used as the undercoat on flexible or semi-flexible leads and shall be permitted only on rigid leads or package elements other than leads.

2) tin welding seal;

3) use of organic or polymeric materials in sealed components for mounting heat conduction or conformal;

4) beam lead structure;

5) use of desiccant in components;

6) non-hermetic and vacuum package process;

7) thermal diffusion bonding for aluminium-silicon bonding wires;

Bonds should not be covered by gel.

8) laser inscribing.

Laser inscribing from the back of SOS (silicon on sapphire) is allowed.

h) Unless otherwise specified, caution is needed for the following processes:

1) when using ultrasonic cleaning processes;

Power time and other parameter should be tested and verified fully.

2) when the bond process wire metal is different from the die pad area;

If the wire metal for the bonding process is different from the die pad area, this process should be qualified. The qualification test shall contain at least a high-temperature stock, SEM inspection and bond strength. The samples after high-temperature storage should fulfil the requirements of the bond strength specification.

3) when using fritted glass to mount dies.

B.5 Antistatic design guidance

Antistatic design guidelines include:

a) Guidelines for the design of the whole chip ESD protection circuit:

1) Analyse the circuit characteristics

Analyse how to supply power for the digital source, simulation source, and the connection between analogue module and the digital module. Analyse the characteristics of each I/O unit to confirm whether there is a special port.

2) Master the process

After process analysis (including the device breakdown voltage and so on), determine the ESD design window. Be familiar with the maximum current density of polysilicones, metals, contact holes, through holes, parasitic resistance and parasitic capacitance of the metal, contact holes, through holes, the metal thickness, square resistance, current density and other parameters.

3) Choose the suitable ESD protection device

Firstly, analyse the various device characterizations such as device failure voltage, trigger voltage, type of diode, characteristics of capacitance, resistance and inductance. Then according to the characteristics of I/O port and power supply, the suitable ESD protection device is chosen to satisfy the ESD requirements.

4) Design the ESD protection unit

Generally, use the ESD protection architecture mentioned above. If the design requirements cannot be met (i.e. the parasitic value is too large or the leakage is insufficient), it is necessary to design a protection unit again according to the actual requirements.

5) The ESD protection scheme for the whole chip

According to steps 1) and 4), each port and each ESD path are designed. The reasonable layout of the power line and the shape, size of ESD units are designed.

b) Design window for protection circuit

According to the device parameters supplied by process line and each port operating voltage range, the ESD protection circuit design window is determined.

c) The choice of protection device

ESD protection circuit such as resistance, diode, thin-gate MOSFET, thick-field oxide layer devices, bipolar transistor and thyristor (SCR) are commonly used.

d) Protection circuit design

The kinds of ESD protection circuit include input, output, the connection between the power and the ground (or between the positive and negative power).

1) Two-stage protection architecture is usually adopted for input ESD protection circuit. The size of the first stage protection circuit should be greater than the smallest process size of the ESD design, while the size of the second stage protection circuit is 1/10 of the first stage.

2) The parasitic diode of the output level buffer can be directly used as the output level ESD protection circuit.

3) For analogue input port, if the impact of the resistance is large, the resistance of the two-stage input ESD protection architecture can be decreased.

4) The diode, SCR, and the ESD protection circuit based on RC trigger can be used between the power and the ground. The reverse breakdown voltage of diode is high, the protection effect is poor. The effect of SCR is best, however, the hold voltage of SCR supplied by the foundry should be ensured to be higher than the power supply voltage or far larger than the trigger current supplied by the circuit working power. The ESD protection circuit based on RC trigger does not start during normal work. Where electrostatic appears, ESD protection can quickly start. The on-state resistance is very small, which can protect the ESD very well.

5) JFETs are more sensible to ESD, so a good protection for it should be designed.

B.6 Low-power design guidance

The methods for reducing the static power consumption include reducing the leakage current leakage, sub-threshold current, substrate current. The methods for reducing the dynamic power consumption include reducing the switching power and internal power dissipation. The details are as follows:

a) Pay attention to the division between software and hardware, memory optimization and dynamic voltage management in system level low power design;

b) Parallel processing, pipeline processing and distributed processing, as well as the clock-gating, operand isolation and power management method can be used to reduce the power consumption in architecture level low power design;

c) Common factor extraction, process mapping, transistor size changing, buffer insertion, phase adjustment, pin replacement and factorization methods can be used in logic level low power design;

d) Dynamic logic, transmission gate logic, asynchronous logic architecture can be used to reduce power consumption in circuit level low power design;

e) Reducing the interconnect capacitance and using the power focusing automatic layout can be used in low power layout design;

f) The logic type selection, optimization process to reduce the capacitance, voltage scaling can be mainly considered in processing level low power design. The voltage scaling refers to the reducing of supply voltage to achieve the purpose of reducing power consumption. It is the realization of dynamic voltage management in system level.

B.7 Parameter modification and margin design guidance

In the design process, computer aided design can be used for parameter modification and margin design to meet the needs of all kinds of disparity. The optimal parameters and the most reliable scope of work are selected to ensure that the design and production of the chip can satisfy the actual request. Mainly with the circuit tolerance analysis and circuit/layout optimization design, the centre value is adjusted, and the limits of tolerance is optimized to ensure that the circuit can work normally even there are fluctuations in the production process or changes in the actual work environment.

a) Temperature offset

In the design process, the key parameters can be simulated in the whole temperature range to verify the circuit temperature performance. When needed, the ultimate temperature can be increased if the model allows.

b) Supply voltage offset

The supply voltage is fluctuating in the actual work. In the design process the supply voltage is usually offset ±10 % to verify the circuit performance under the supply voltage fluctuating conditions. For the devices in which the supply voltage is greater than 10 V, it is needed to pull partially ±20 %.

c) Packaging and testing offset conditions simulation

For high-speed and high-precision circuits, packaging and testing conditions can affect the circuit test results. In the circuit design process, the effects of packaging and testing conditions on the performance of the circuit should be considered.

d) The other functional offset simulation

For D/A converters and other devices, the allowed input signal frequency range is large. It is needed to simulate under multiple frequency point within and without the frequency range when design the circuit in order to ensure the devices can meet the design requirements in the whole frequency range containing parasitic parameters simulation, compare with pre simulation data of ideal model should be carried out according to rules provided by process. This is especially important for high frequency circuit.

e) Process angle offset

There is the deviation between actual production process and the ideal situation. Generally, the process angle is used to describe the deviation actual production process. It is needed to simulate the influence

of the process angle on the circuit performance to ensure that the simulation results meet the design requirements.

f) Post layout simulation

Focusing on the physical layout, the parasitic parameters (R, L, C, etc.) extraction should be carried out according to the process rules. The post layout simulation should be carried out based on the parasitic parameters, then based on the comparison with the results of the ideal model the parameter design should be modified.

B.8 Electro-magnetic compatibility (EMC) design guidance

EMC design guidelines include:

a) Rapid changes of voltage and current should be avoided. Special attention should be paid to the strongest interference source, such as the clock signal in digital circuits;

b) Pay special attention to the sensitive circuits and interference coupling, for example low level analogue signal;

c) Take fully consideration of the impact of ground line on the common impedance coupling;

d) Take into account the ground design and the path selection, minimize the ground loop current. The methods of reducing the common mode voltage or increasing ground loop impedance can be used to reduce ground loop current;

e) Balance circuit should be used to suppress the interference of the ground loop;

f) The signal grounding mode, such as single point grounding, multi-point grounding, mixed grounding and so on, should be considered when making choice.

   1) It is simple for single point grounding in series, however common impedance coupling may come into being;

   2) There is no common impedance coupling for single point grounding in parallel, but there are too many ground wires;

   3) It shall be ensure that the ground impedance is very small for multi-point grounding, or there will be common impedance coupling;

   4) The ground loop circuit should be avoided for mixed grounding.

B.9 Radiation-hardened design guidance

According to the kinds of radiation and radiation sensitive parameters, the corresponding measures against irradiation should be taken.

a) For total dose radiation hardened design, it is needed to reduce leakage current caused by radiation. The methods include annular transistor, P+ protection ring around NMOS devices, and so on.

   1) Considering annular without edge gate architecture to prevent the edge leakage current;

   2) The architecture of P+ protection ring around NMOS can prevent the field oxide leakage current effectively, but it will increase the area as the cost.

b) In addition to process hardening such as epitaxial silicon, SOI to overcome the single event latch-up effect, the design hardening methods includes charge supplement, temporal filtering, redundancy

and error detection, correction code, and so on to prevent SEL, SEU and SET. The latter two methods are suggested.

1) For charge supplement, with improving the circuit node power which means increasing the characterizing threshold of high level the circuit ability against single event effect is improved. In addition the ability against single event effect can be improved with increasing the area of transistor;

2) For temporal filtering, it is to separate the single event effects in time scale, such as "RC filtering", to eliminate the single event effect eventually. However, it will affect the speed of the circuit. LC filter is smaller and easier to put inside the microcircuit;

3) For the spatial redundancy, it is through the use of three modular redundancy to improve the ability of single event effect hardness for digital ICs. However, it will be at the cost of area increasing by three times. It needs to optimizing to achieve a reasonable area requirements;

4) The code methods such as parity code can improve the ability against the single event effects;

5) For the CMOS circuit the architecture reinforcement design method can be adopted, such as double ring protecting architecture can improve the ability to against the single event effects.

B.10 Testability design guidance

Design for testability mainly includes scan path test, built-in self test (BIST) and boundary scan test.

a) Scan path test

1) Scan test requires that each scan cell is under controllable and observable state. The main unit of scan test architecture is scan flip-flop. The most commonly used flip-flop is the D-flip-flop with multiplexer and latch with scanning port;

2) In the original inputs, all the clock inputs and asynchronous resets must be able to measure;

3) The clock signal cannot be used as the input signal trigger;

4) Three state buses must be controllable during the scan test mode.

b) Built-in self test

1) Built-in self test vectors are produced by the circuit itself. The circuit also has independent architecture to determine the test results correct or not. The BITS method can be used for RAM, ROM and flash test, and mainly used for RAM.

2) For built-in self test, additional circuits including the vector generator, BITS controller and response analyser are needed.

3) The BIST circuit as a part of logic circuit usually inserted in RTL. It needs to synthesize with other logic together.

c) Boundary scan test

1) The boundary scan test architecture is built according to IEEE 1149.1;

2) With boundary scan test architecture, the vector input and response on the connection between the parts under test is analysed;

3) When testing for a single core logic, the logic can be initialized and the test architecture of itself can be used;

4) The flip-flops are connected to form a scan chain (equivalent to shift register). Considering the cost of hardware, the partial scan method, such as minimized scanning overhead can be used to make the testability of the chip reach the highest level.

Bibliography

[1] ISO 10795, *Space systems — Programme management and quality — Vocabulary*

ICS 49.140
Price based on 24 pages

This page deliberately left blank

British Standards Institution (BSI)

BSI is the national body responsible for preparing British Standards and other standards-related publications, information and services.

BSI is incorporated by Royal Charter. British Standards and other standardization products are published by BSI Standards Limited.

About us

We bring together business, industry, government, consumers, innovators and others to shape their combined experience and expertise into standards -based solutions.

The knowledge embodied in our standards has been carefully assembled in a dependable format and refined through our open consultation process. Organizations of all sizes and across all sectors choose standards to help them achieve their goals.

Information on standards

We can provide you with the knowledge that your organization needs to succeed. Find out more about British Standards by visiting our website at bsigroup.com/standards or contacting our Customer Services team or Knowledge Centre.

Buying standards

You can buy and download PDF versions of BSI publications, including British and adopted European and international standards, through our website at bsigroup.com/shop, where hard copies can also be purchased.

If you need international and foreign standards from other Standards Development Organizations, hard copies can be ordered from our Customer Services team.

Copyright in BSI publications

All the content in BSI publications, including British Standards, is the property of and copyrighted by BSI or some person or entity that owns copyright in the information used (such as the international standardization bodies) and has formally licensed such information to BSI for commercial publication and use.

Save for the provisions below, you may not transfer, share or disseminate any portion of the standard to any other person. You may not adapt, distribute, commercially exploit, or publicly display the standard or any portion thereof in any manner whatsoever without BSI's prior written consent.

Storing and using standards

Standards purchased in soft copy format:

- A British Standard purchased in soft copy format is licensed to a sole named user for personal or internal company use only.
- The standard may be stored on more than 1 device provided that it is accessible by the sole named user only and that only 1 copy is accessed at any one time.
- A single paper copy may be printed for personal or internal company use only.

Standards purchased in hard copy format:

- A British Standard purchased in hard copy format is for personal or internal company use only.
- It may not be further reproduced – in any format – to create an additional copy. This includes scanning of the document.

If you need more than 1 copy of the document, or if you wish to share the document on an internal network, you can save money by choosing a subscription product (see 'Subscriptions').

Reproducing extracts

For permission to reproduce content from BSI publications contact the BSI Copyright & Licensing team.

Subscriptions

Our range of subscription services are designed to make using standards easier for you. For further information on our subscription products go to bsigroup.com/subscriptions.

With **British Standards Online (BSOL)** you'll have instant access to over 55,000 British and adopted European and international standards from your desktop. It's available 24/7 and is refreshed daily so you'll always be up to date.

You can keep in touch with standards developments and receive substantial discounts on the purchase price of standards, both in single copy and subscription format, by becoming a **BSI Subscribing Member**.

PLUS is an updating service exclusive to BSI Subscribing Members. You will automatically receive the latest hard copy of your standards when they're revised or replaced.

To find out more about becoming a BSI Subscribing Member and the benefits of membership, please visit bsigroup.com/shop.

With a **Multi-User Network Licence (MUNL)** you are able to host standards publications on your intranet. Licences can cover as few or as many users as you wish. With updates supplied as soon as they're available, you can be sure your documentation is current. For further information, email subscriptions@bsigroup.com.

Revisions

Our British Standards and other publications are updated by amendment or revision.

We continually improve the quality of our products and services to benefit your business. If you find an inaccuracy or ambiguity within a British Standard or other BSI publication please inform the Knowledge Centre.

Useful Contacts

Customer Services
Tel: +44 345 086 9001
Email (orders): orders@bsigroup.com
Email (enquiries): cservices@bsigroup.com

Subscriptions
Tel: +44 345 086 9001
Email: subscriptions@bsigroup.com

Knowledge Centre
Tel: +44 20 8996 7004
Email: knowledgecentre@bsigroup.com

Copyright & Licensing
Tel: +44 20 8996 7070
Email: copyright@bsigroup.com

BSI Group Headquarters

389 Chiswick High Road London W4 4AL UK

bsi.