BS ISO 17987-4:2016

BSI Standards Publication

Road vehicles — Local Interconnect Network (LIN)

Part 4: Electrical physical layer (EPL) specification 12 V/24 V

bsi.

National foreword

This British Standard is the UK implementation of ISO 17987-4:2016.

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Road vehicles — Local Interconnect Network (LIN) —

Part 4: Electrical physical layer (EPL) specification 12 V/24 V

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Partie 4: Spécification de la couche électrique physique (EPL) 12V/24V

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents).

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For an explanation on the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see the following URL: www.iso.org/iso/foreword.html.

The committee responsible for this document is ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 17987 series can be found on the ISO website.

Introduction

ISO 17987 (all parts) specifies the use cases, the communication protocol and physical layer requirements of an in-vehicle communication network called Local Interconnect Network (LIN).

The LIN protocol as proposed is an automotive focused low speed universal asynchronous receiver transmitter (UART) based network. Some of the key characteristics of the LIN protocol are signal-based communication, schedule table based frame transfer, master/slave communication with error detection, node configuration and diagnostic service transportation.

The LIN protocol is for low-cost automotive control applications, for example, door module and air condition systems. It serves as a communication infrastructure for low-speed control applications in vehicles by providing:

— signal-based communication to exchange information between applications in different nodes;

— bit rate support from 1 kbit/s to 20 kbit/s;

— deterministic schedule table-based frame communication;

— network management that wakes up and puts the LIN cluster into sleep state in a controlled manner;

— status management that provides error handling and error signalling;

— transport layer that allows large amount of data to be transported (such as diagnostic services);

— specification of how to handle diagnostic services;

— electrical physical layer specifications;

— node description language describing properties of slave nodes;

— network description file describing behaviour of communication;

— application programmer's interface.

ISO 17987 (all parts) is based on the open systems interconnection (OSI) Basic Reference Model as specified in ISO/IEC 7498-1 which structures communication systems into seven layers.

The OSI model structures data communication into seven layers called (top down) *application layer* (layer 7), *presentation layer*, *session layer*, *transport layer*, *network layer*, *data link layer* and *physical layer* (layer 1). A subset of these layers is used in ISO 17987 (all parts).

ISO 17987 (all parts) distinguishes between the services provided by a layer to the layer above it and the protocol used by the layer to send a message between the peer entities of that layer. The reason for this distinction is to make the services, especially the application layer services and the transport layer services, reusable also for other types of networks than LIN. In this way, the protocol is hidden from the service user and it is possible to change the protocol if special system requirements demand it.

ISO 17987 (all parts) provides all documents and references required to support the implementation of the requirements related to the following.

— ISO 17987-1: This part provides an overview of the ISO 17987 (all parts) and structure along with the use case definitions and a common set of resources (definitions, references) for use by all subsequent parts.

— ISO 17987-2: This part specifies the requirements related to the transport protocol and the network layer requirements to transport the PDU of a message between LIN nodes.

— ISO 17987-3: This part specifies the requirements for implementations of the LIN protocol on the logical level of abstraction. Hardware-related properties are hidden in the defined constraints.

— ISO 17987-4: This part specifies the requirements for implementations of active hardware components which are necessary to interconnect the protocol implementation.

— ISO/TR 17987-5: This part specifies the LIN application programmers interface (API) and the node configuration and identification services. The node configuration and identification services are specified in the API and define how a slave node is configured and how a slave node uses the identification service.

— ISO 17987-6: This part specifies tests to check the conformance of the LIN protocol implementation according to ISO 17987-2 and ISO 17987-3. This comprises tests for the data link layer, the network layer and the transport layer.

— ISO 17987-7: This part specifies tests to check the conformance of the LIN electrical physical layer implementation (logical level of abstraction) according to this document.

INTERNATIONAL STANDARD ISO 17987-4:2016(E)

Road vehicles — Local Interconnect Network (LIN) —

Part 4:
Electrical physical layer (EPL) specification 12 V/24 V

1 Scope

This document specifies the 12 V and 24 V electrical physical layers (EPL) of the LIN communications system.

The electrical physical layer for LIN is designed for low-cost networks with bit rates up to 20 kbit/s to connect automotive electronic control units (ECUs). The medium that is used is a single wire for each receiver and transmitter with reference to ground.

This document includes the definition of electrical characteristics of the transmission itself and also the documentation of basic functionality for bus driver devices.

All parameters in this document are defined for the ambient temperature range from −40 °C to 125 °C.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61000-4-2, *Electromagnetic compatibility (EMC) — Part 4-2: Testing and measurement techniques — Electrostatic discharge immunity test*

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— IEC Electropedia: available at http://www.electropedia.org/

— ISO Online browsing platform: available at http://www.iso.org/obp

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BR_Range_20K
LIN systems which operate at speeds up to 20 kbit/s

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BR_Range_20K 12 V
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3.2 Symbols

%	percentage
µs	microsecond
C'_{LINE}	line capacitance
C_{BUS}	total bus capacitance
C_{MASTER}	capacitance of master node
C_{RXD}	RXD capacitance (LIN receiver, RXD capacitive load condition)
C_{SLAVE}	capacitance of slave node
d^2V/dt^2	second derivative of voltage ($Volt^2$ per $second^2$)
di/dt	instantaneous rate of current change (amps per second)
D_{ser_int}	serial internal diode at transceiver IC
D_{ser_master}	serial master diode
$F_{TOL\_RES\_MASTER}$	master bit rate deviation from nominal bit rate
$F_{TOL\_RES\_MASTER\_A}$	master bit rate deviation from nominal bit rate in BR_Range_20K systems
$F_{TOL\_RES\_MASTER\_B}$	master bit rate deviation from nominal bit rate in BR_Range_10K systems
$F_{TOL\_RES\_SLAVE}$	slave bit rate deviation from nominal bit rate
$F_{TOL\_RES\_SLAVE\_A}$	slave bit rate deviation from nominal bit rate in BR_Range_20K systems
$F_{TOL\_RES\_SLAVE\_B}$	slave bit rate deviation from nominal bit rate in BR_Range_10K systems
$F_{TOL\_RES\_SLAVE\_1}$	slave node 1 bit rate deviation from nominal bit rate
$F_{TOL\_RES\_SLAVE\_2}$	slave node 2 bit rate deviation from nominal bit rate
$F_{TOL\_SLAVE\_to\_SLAVE}$	slave to slave bit rate deviation
F_{TOL_SYNCH}	slave node bit rate deviation from master node bit rate after synchronization
$F_{TOL\_SYNCH\_A}$	slave node bit rate deviation from master node bit rate after synchronization in BR_Range_20K systems
$F_{TOL\_SYNCH\_B}$	slave node bit rate deviation from master node bit rate after synchronization in BR_Range_10K systems

$F_{TOL\_SYNCH\_1}$	slave node 1 bit rate deviation from master node bit rate after synchronization
$F_{TOL\_SYNCH\_2}$	slave node 2 bit rate deviation from master node bit rate after synchronization
$F_{TOL\_UNSYNCH}$	slave node bit rate deviation from nominal bit rate before synchronization
$F_{TOL\_UNSYNCH\_A}$	slave node bit rate deviation from nominal bit rate before synchronization in BR_Range_20K systems
$F_{TOL\_UNSYNCH\_B}$	slave node bit rate deviation from nominal bit rate before synchronization in BR_Range_10K systems
I_{BUS}	current into the ECU bus line
I_{BUS_LIM}	current limitation for driver dominant state driver on $V_{BUS} = V_{BAT\_max}$ into ECU bus line
$I_{BUS\_NO\_BAT}$	current at ECU bus line when V_{BAT} is disconnected
$I_{BUS\_NO\_GND}$	current at ECU bus line when V_{GND_ECU} is disconnected
$I_{BUS\_PAS\_dom}$	current at ECU bus line when driver off (passive) at dominant LIN bus level
$I_{BUS\_PAS\_rec}$	current at ECU bus line when driver off (passive) at recessive LIN bus level
GND_{Device}	GND of ECU
kΩ	kilo ohm
kbit/s	kilo bit per second
LEN_{BUS}	total length of LIN bus line
LIN_{Bus}	LIN network
ms	millisecond
nF	nano farad
pF	pico farad
pF/m	pico farad per meter (line capacitance)
R_{BUS}	total bus-resistor including all slave and master resistors $R_{BUS} = R_{MASTER}\|\|R_{SLAVE\_1}\|\|R_{SLAVE\_2}\|\|$ to $\|\|R_{SLAVE\_N}$
R_{MASTER}	master resistor
R_{pull_up}	pull-up resistor
R_{SLAVE}	slave resistor
t_{BFS}	byte field synchronization time
t_{BIT}	basic bit times
t_{EBS}	earliest bit sample time
t_{rx_pd}	propagation delay of receiver

t_{rx_sym}	symmetry of receiver propagation delay rising edge propagation delay of receiver
t_{LBS}	latest bit sample time
$t_{rx\_pdf(1)}$	propagation delay time of receiving node 1 at falling (recessive to dominant) LIN bus edge
$t_{rx\_pdf(2)}$	propagation delay time of receiving node 2 at falling (recessive to dominant) LIN bus edge
$t_{rx\_pdr(1)}$	propagation delay time of receiving node 1 at rising (dominant to recessive) LIN bus edge
$t_{rx\_pdr(2)}$	propagation delay time of receiving node 2 at rising (dominant to recessive) LIN bus edge
t_{SR}	sample window repetition time
$TH_{Dom(max)}$	max. dominant threshold of receiving node (Volt)
$TH_{Dom(min)}$	min. dominant threshold of receiving node (Volt)
$TH_{Rec(max)}$	max. recessive threshold of receiving node (Volt)
$TH_{Rec(min)}$	min. recessive threshold of receiving node (Volt)
V	voltage
V_{ANODE}	voltage at the anode of the diode
V_{BAT}	voltage across the ECU supply connectors
$V_{BATTERY}$	voltage across the vehicle battery connectors
V_{BUS}	voltage on the LIN bus
V_{BUS_CNT}	centre point of receiver threshold
V_{BUS_rec}	receiver recessive voltage
$V_{CATHODE}$	voltage at the cathode of the diode
$V_{GND\_BATTERY}$	battery ground voltage
V_{GND_ECU}	voltage on the local ECU ground connector with respect to vehicle battery ground connector ($V_{GND\_BATTERY}$)
V_{HYS}	receiver hysteresis voltage
V_{Rec}	recessive voltage
$V_{SerDiode}$	voltage drop at the serial diodes
V_{Shift_BAT}	battery shift
$V_{Shift\_Difference}$	difference between battery shift and GND shift
V_{Shift_GND}	GND shift
V_{SUP}	voltage at transceiver supply pins

$V_{SUP\_NON\_OP}$	voltage which the device is not destroyed; no guarantee of correct operation
V_{th_dom}	receiver threshold voltage of the recessive to dominant LIN bus edge
V_{th_rec}	receiver threshold voltage of the dominant to recessive LIN bus edge
$\Delta F/F_{MASTER}$	deviation of node bit rate from the master node bit rate
$\Delta F/F_{Nom}$	deviation from nominal bit rate
τ	time constant
Ω	ohm

3.3 Abbreviated terms

AC	alternate current
API	application programmers interface
ASIC	application specific integrated circuit
BFS	byte field synchronization
DC	direct current
EBS	earliest bit sample
ECU	electronic control unit
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPL	electrical physical layer
ESD	electrostatic discharge
EVT	event
GND	ground
LBS	latest bit sample
Max.	maximum
Min.	minimum
OSI	open systems interconnection
RC	RC time constant τ ($\tau = C_{BUS} \times R_{BUS}$)
RX	Rx pin of the transceiver
RXD	receive data
SR	sample window repetition
TRX	transceiver
Tx	Tx pin of the transceiver

TXD transmit data

Typ. typical

UART universal asynchronous receiver transmitter

4 Conventions

ISO 17987 (all parts) and ISO 14229-7 are based on the conventions specified in the OSI Service Conventions (see ISO/IEC 10731) as they apply for physical layer, protocol, network and transport protocol and diagnostic services.

5 Electrical physical layer requirements

5.1 Bit rate deviation

The bit rate deviation of the LIN medium describes the bit rate deviation from a referenced bit rate. It is the sum of the following parameters:

— inaccuracy of setting the bit rate (systematic failure due to granularity of the configurable bit rate);

— clock deviation over temperature and supply voltage range;

— clock source stability of the slave node starting from the end of the sync byte field up to the end of the entire LIN frame (last sampled bit) when performing synchronization;

— bit time measurement failure of the slave node;

— clock source stability of the master node starting from the end of the sync byte field up to the end of the entire LIN frame (last transmitted bit).

On-chip clock may achieve a frequency deviation of better than ±14 % with internal calibration. This bit rate deviation better than ±14 % is sufficient to detect a break field in the message stream. The subsequent bit rate adaptation using the sync byte field ensures the proper reception and transmission of the message. The on-chip oscillator shall allow for accurate bite rate measurement and generation for the remainder of the message frame, taking into account effects of anything, which affects the bit rate, such as temperature and voltage drift during operation.

The bit rates on the LIN bus are specified in the range of 1 kbit/s to 20 kbit/s. The specific bit rate used on a LIN bus is defined as the nominal bit rate, F_{Nom}.

In case a non-LIN electrical physical layer (e.g. ISO 11898-1, ISO 11898-2) is used, the bit rate may have to be adjusted.

5.1.1 12 V LIN systems: Parameters

Table 1 defines the bit rate deviation from nominal bit rate.

Table 1 — Bit rate deviation from nominal bit rate

Number	Bit rate deviation	Name	$\Delta F/F_{Nom}$
Param 1	Master node (deviation from nominal bit rate)	$F_{TOL\_RES\_MASTER}$	<±0,5 %
Param 2	Slave node without making use of synchronization (deviation from nominal bit rate)	$F_{TOL\_RES\_SLAVE}$	<±1,5 %
Param 3	Deviation of slave node bit rate from the nominal bit rate before synchronization; relevant for nodes making use of synchronization and direct break detection. This parameter is microprocessor-based nodes with sync/break detection that is triggering the auto-bauding processing in software. It insures that the break is detected.	$F_{TOL\_UNSYNCH}$	<±14 %

Table 2 defines the slave node bit rate deviation from master node bit rate.

Table 2 — Slave node bit rate deviation from master node bit rate

Number	Bit rate deviation	Name	$\Delta F/F_{MASTER}$
Param 4	Deviation of slave node bit rate from the master node bit rate after synchronization; relevant for nodes making use of synchronization; any slave node shall stay within this deviation for all fields of a frame which follow the sync byte field.	F_{TOL_SYNCH}	<±2 %

Table 3 defines the bit rate deviation for slave to slave communication.

Table 3 — Bit rate deviation for slave to slave communication

Number	Bit rate deviation	Name	$\Delta F/F_{MASTER}$
Param 5	For communication between any two nodes (i.e. data stream from one slave to another slave), their bit rate shall not differ by more than $F_{TOL\_SLAVE\_to\_SLAVE}$. The following condition shall be checked for: a) $\lvert F_{TOL\_RES\_SLAVE\_1} - F_{TOL\_RES\_SLAVE\_2}\rvert < F_{TOL\_SLAVE\_to\_SLAVE}$; b) $\lvert F_{TOL\_SYNCH\_1} - F_{TOL\_SYNCH\_2}\rvert < F_{TOL\_SLAVE\_to\_SLAVE}$; c) $\lvert(F_{TOL\_RES\_MASTER} + F_{TOL\_SYNCH\_1}) - F_{TOL\_RES\_SLAVE\_2}\rvert < F_{TOL\_SLAVE\_to\_SLAVE}$.	$F_{TOL\_SLAVE\_to\_SLAVE}$	<±2 %

5.1.2 24 V LIN systems: Parameters

The required accuracy is dependent on the used bit rate range. See Table 15 and also ISO 17987-2.

Table 4 defines the bit rate deviation from nominal bit rate in BR_Range_20K systems.

Table 4 — Bit rate deviation from nominal bit rate in BR_Range_20K systems

Number	BR_Range_20K bit rate deviation	Name	$\Delta F/F_{Nom}$
Param 39	master node (deviation from nominal bit rate. The nominal bit rate F_{Nom} is defined in the LIN description file).	$F_{TOL\_RES\_MASTER\_A}$	<±0,3 %
Param 40	slave node without making use of synchronization (deviation from nominal bit rate) For communication between any two nodes, their bit rate shall not differ by more than ±0,6 %.	$F_{TOL\_RES\_SLAVE\_A}$	<±0,3 %
Param 41	deviation of slave node bit rate from the nominal bit rate before synchronization; relevant for nodes making use of synchronization and direct break field detection.	$F_{TOL\_UNSYNCH\_A}$	<±14 %

Table 5 defines the bit rate deviation for slave nodes from master node in BR_Range_20K systems.

Table 5 — Bit rate deviation for slave nodes from master node in BR_Range_20K systems

Number	BR_Range_20K bit rate deviation	Name	$\Delta F/F_{MASTER}$
Param 42	Deviation of slave node bit rate from the master node bit rate after synchronization; relevant for nodes making use of synchronization; any slave node shall stay within this deviation for all fields of a frame which follow the sync byte field.	$F_{TOL\_SYNCH\_A}$	<±0,6 %
Param 43	For communication between any two nodes (i.e. data stream from one slave to another slave), their bit rate shall not differ by more than $F_{TOL\_SLAVE\_to\_SLAVE}$. The following condition shall be checked for: a) $\lvert F_{TOL\_RES\_SLAVE\_1} - F_{TOL\_RES\_SLAVE\_2}\rvert < F_{TOL\_SLAVE\_to\_SLAVE}$; b) $\lvert F_{TOL\_SYNCH\_1} - F_{TOL\_SYNCH\_2}\rvert < F_{TOL\_SLAVE\_to\_SLAVE}$; c) $\lvert (F_{TOL\_RES\_MASTER\_A} + F_{TOL\_SYNCH\_1}) - F_{TOL\_RES\_SLAVE\_2}\rvert < F_{TOL\_SLAVE\_to\_SLAVE}$.	$F_{TOL\_SLAVE\_to\_SLAVE}$	<±0,6 %

Table 6 defines the Bit rate deviation from nominal bit rate in BR_Range_10K systems.

Table 6 — Bit rate deviation from nominal bit rate in BR_Range_10K systems

Number	BR_Range_10K bit rate deviation	Name	$\Delta F/F_{Nom}$
Param 44	master node (deviation from nominal bit rate. The nominal bit rate F_{Nom} is defined in the LDF).	$F_{TOL\_RES\_MASTER\_B}$	<±0,5 %
Param 45	slave node without making use of synchronization (deviation from nominal bit rate) For communication between any two nodes, their bit rate shall not differ by more than ±2,0 %.	$F_{TOL\_RES\_SLAVE\_B}$	<±1,5 %
Param 46	deviation of slave node bit rate from the nominal bit rate before synchronization; relevant for nodes making use of synchronization and direct break field detection.	$F_{TOL\_UNSYNCH\_B}$	<±14 %

Table 7 defines the bit rate deviation for slave nodes from master node in BR_Range_10K systems.

Table 7 — Bit rate deviation for slave nodes from master node in BR_Range_10K systems

Number	BR_Range_10K bit rate deviation	Name	$\Delta F/F_{MASTER}$
Param 47	Deviation of slave node bit rate from the master node bit rate after synchronization; relevant for nodes making use of synchronization; any slave node shall stay within this deviation for all fields of a frame which follow the sync byte field.	$F_{TOL\_SYNCH\_B}$	<±2,0 %
Param 48	For communication between any two nodes (i.e. data stream from one slave to another slave), their bit rate shall not differ by more than $F_{TOL\_SLAVE\_to\_SLAVE}$. The following condition shall be checked for: a) $\lvert F_{TOL\_RES\_SLAVE\_1} - F_{TOL\_RES\_SLAVE\_2}\rvert < F_{TOL\_SLAVE\_to\_SLAVE}$; b) $\lvert F_{TOL\_SYNCH\_1} - F_{TOL\_SYNCH\_2}\rvert < F_{TOL\_SLAVE\_to\_SLAVE}$: c) $\lvert(F_{TOL\_RES\_MASTER\_B} + F_{TOL\_SYNCH\_1}) - F_{TOL\_RES\_SLAVE\_2}\rvert < F_{TOL\_SLAVE\_to\_SLAVE}$.	$F_{TOL\_SLAVE\_to\_SLAVE}$	<±2,0 %

5.2 Timing requirements

5.2.1 Bit timing

If not otherwise stated, all bit times in this document use the bit timing of the master node as a reference.

5.2.2 Synchronization procedure

The sync byte field consists of the fixed data 55_{16} inside a byte field. The synchronization procedure shall be based on time measurement between falling edges of the pattern. The falling edges are available in distances of 2 bit, 4 bit, 6 bit and 8 bit times which allows a simple calculation of the basic bit times, t_{BIT}.

Figure 1 shows the sync byte field.

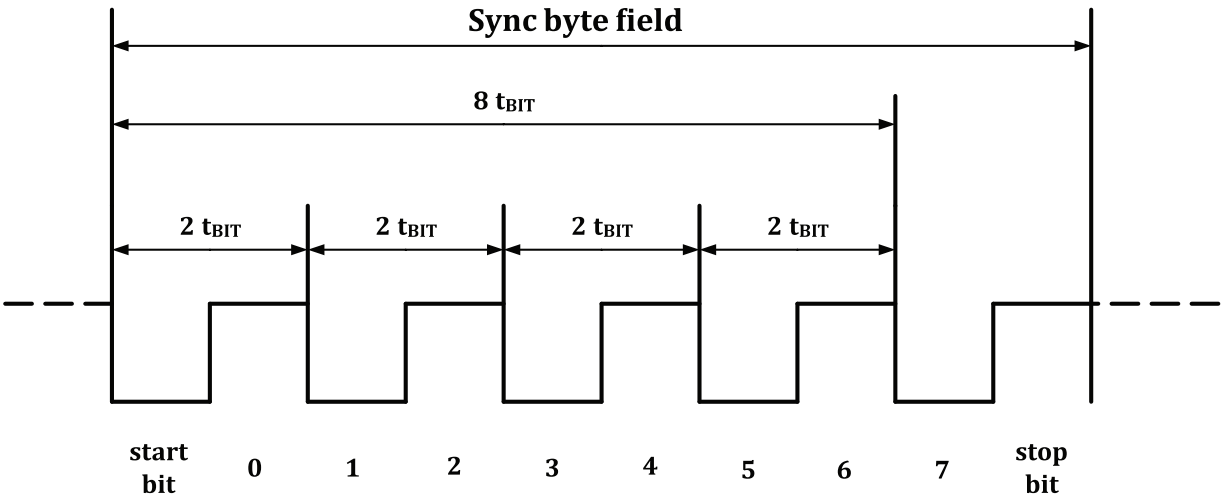


Figure 1 — Sync byte field

5.2.3 Bit sample timing

The bits of a byte field shall be sampled according to the following specification. In Figure 2, the bit sample timing of a byte field is illustrated. The corresponding timing parameters are listed in Table 8.

A byte field shall be synchronized at the falling edge of the start bit. The byte field synchronization (BFS) shall have an accuracy of t_{BFS}.

All methods for start bit sampling that met the byte field synchronization t_{BFS} are allowed.

After the byte field synchronization on the falling edge of the start bit, the data bit itself shall be sampled within the window between the earliest bit sample (EBS) time, t_{EBS}, and the latest bit sample (LBS) time, t_{LBS}. The latest bit sample time, t_{LBS}, depends on the accuracy of the byte field synchronization, t_{BFS}. The dependency between t_{LBS} and t_{BFS} is given in Formula (1):

$$t_{LBS} = 10/16\ t_{BIT} - t_{BFS} \quad (1)$$

The following bits shall be sampled within the same range as the sample window of the first data bit with the sample window repetition time, t_{SR}, respectively. The sample window repetition time, t_{SR}, is specified from the EBS of the former bit (n-1) to the EBS of the current bit; see Formula (2):

$$t_{SR} = t_{EBS(n)} - t_{EBS(n-1)} = t_{LBS(n)} - t_{LBS(n-1)} = t_{BIT} \quad (2)$$

Table 8 — Bit sample timing

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
Param 6	t_{BFS}	—	1/16	2/16	t_{BIT}	Value of accuracy of the byte field detection
Param 7	t_{EBS}	7/16	—	—	t_{BIT}	Earliest bit sample time, $t_{EBS} \leq t_{LBS}$
Param 8	t_{LBS}	—	—	—	t_{BIT}	Latest bit sample [see Formula (1)], $t_{LBS} \geq t_{EBS}$

For devices, which make use of more than one sample per bit, the bit sample majority shall determine the bit data. Furthermore, the sample majority shall be between the EBS and the LBS.

Table 9 defines the bit sample timing example.

Table 9 — Bit sample timing example

UART/SCI cycles per t_{BIT}	t_{BFS}	t_{EBS}	$t_{LBS} = 10/16\ t_{BIT} - t_{BFS}$
16	1/16 t_{BIT}	7/16 t_{BIT}	9/16 t_{BIT}
8	1/8 t_{BIT} (=2/16 t_{BIT})	4/8 t_{BIT} (=8/16 t_{BIT})	4/8 t_{BIT} (=8/16 t_{BIT})

Figure 2 shows the bit sample timing.

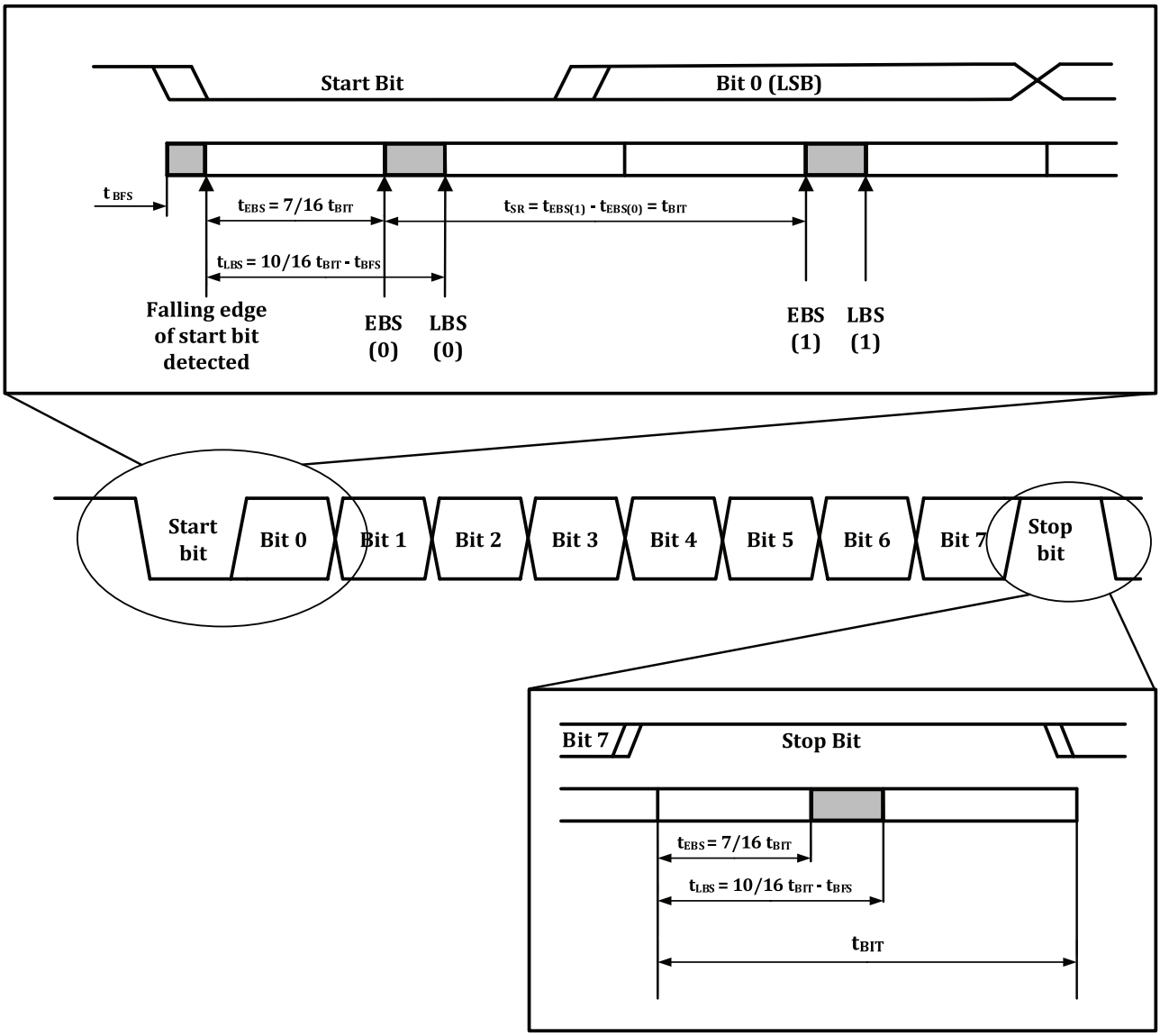


Figure 2 — Bit sample timing

5.3 Line driver/receiver

5.3.1 General configuration

The bus line driver/receiver is based on ISO 9141. It consists of the bidirectional bus line LIN which is connected to the driver/receiver of every bus node, and is connected via a termination resistor and a diode to the positive transceiver supply voltage, V_{SUP} (see Figure 3). The diode is mandatory to prevent an uncontrolled power supply of the ECU from the bus in case of a "loss of battery".

It is important to note that the LIN specification refers to the voltages at the external electrical connections of the electronic control unit (ECU), and not to ECU internal voltages. In particular, the parasitic voltage drops of reverse polarity diodes shall be taken into account when designing a LIN transceiver circuit.

5.3.2 Definition of supply voltages for the physical interface

V_{BAT} denotes the supply voltage at the connector of the ECU. Electronic components within the unit may see an internal supply V_{SUP} being different from V_{BAT} (see Figure 3). This can be the result of protection

filter elements and dynamic voltage changes on the bus. This shall be taken into consideration for the implementation of semiconductor products for LIN.

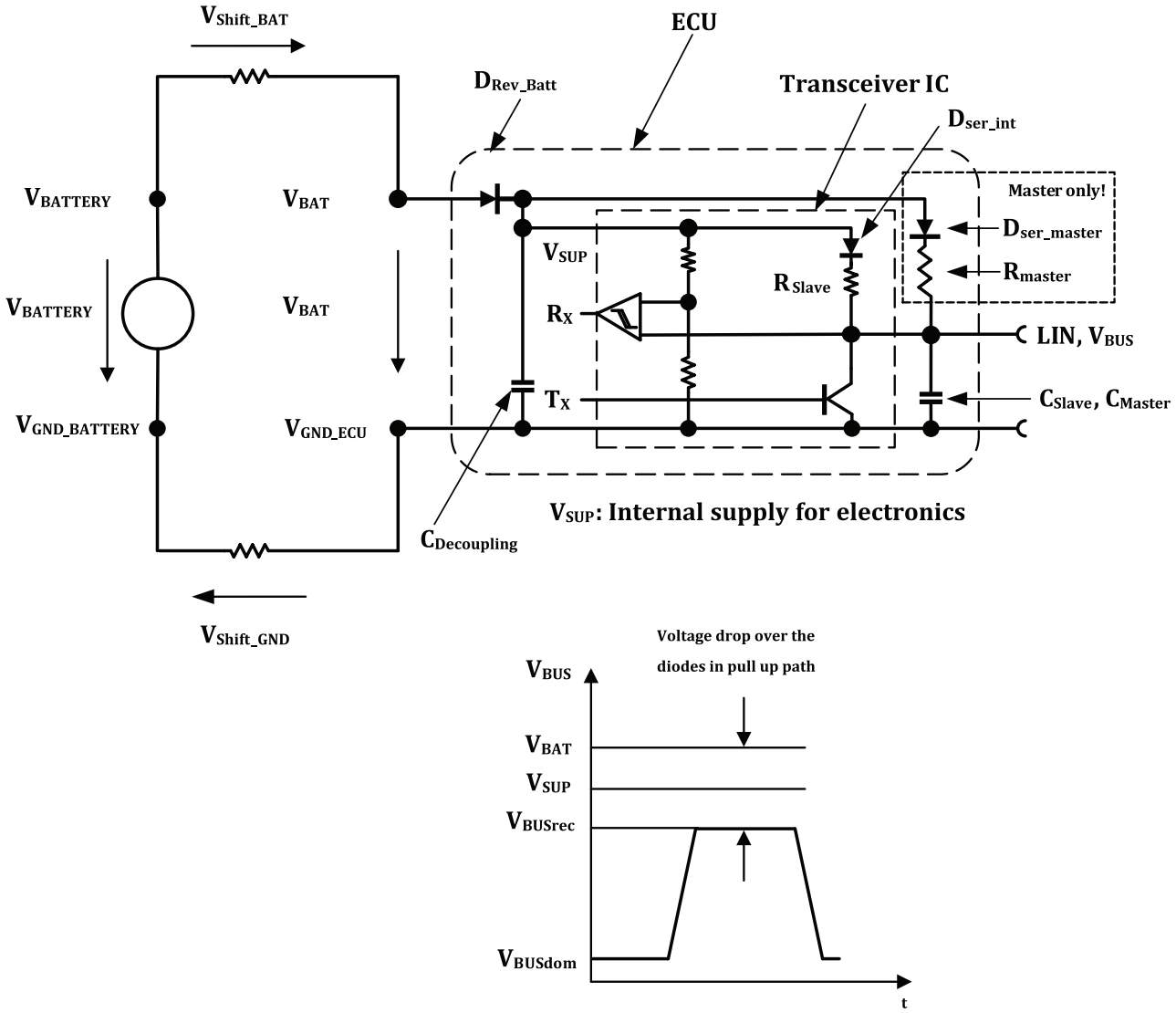


Figure 3 — Illustration of the difference between external supply voltage, V_{BAT}, and the internal supply voltage, V_{SUP}

5.3.3 Signal specification

Figure 4 shows the voltage levels on the bus line.

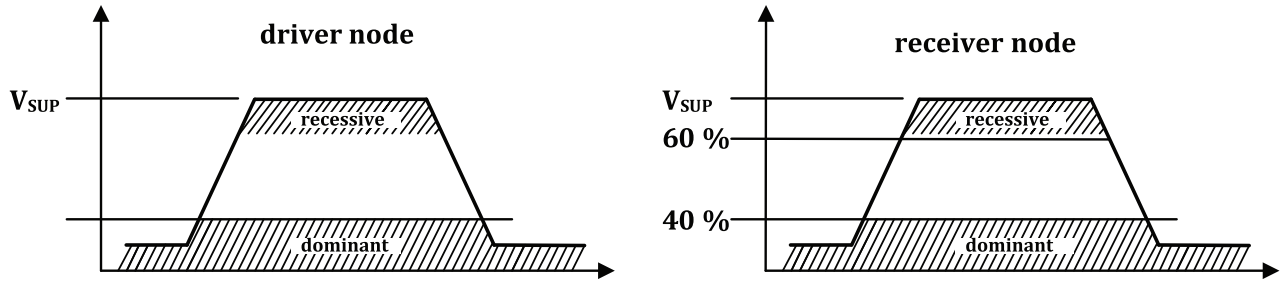
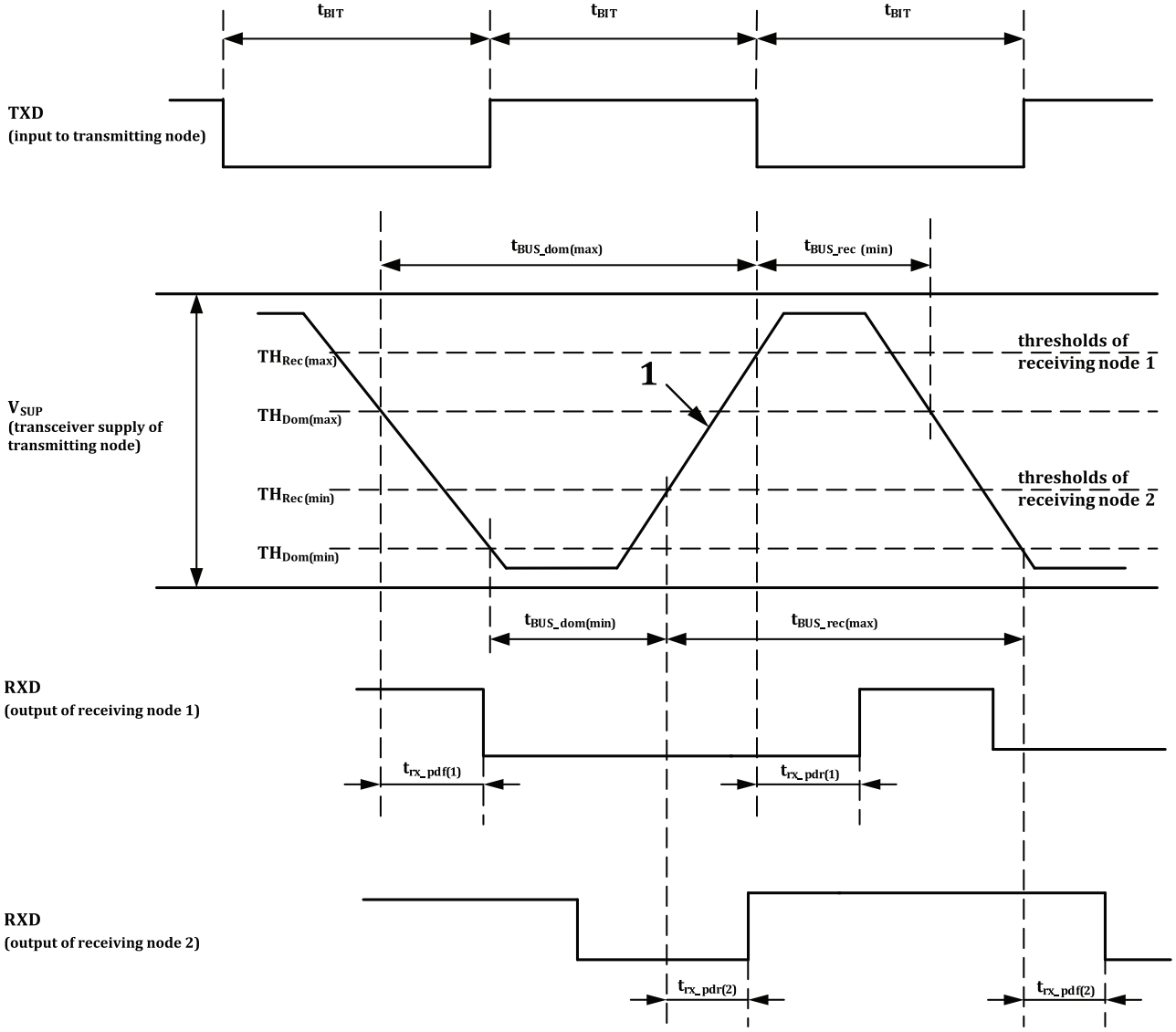


Figure 4 — Voltage levels on the bus line

For a correct transmission and reception of a bit, it shall be asserted that the signal is available with the correct voltage level (dominant or recessive) at the bit sampling time of the receiver. Ground shifts as well as drops in the supply voltage shall be taken into consideration as well as symmetry failures in the propagation delay. Figure 5 shows the timing parameters that impact the behaviour of the LIN bus. The minimum and maximum values of the different parameters are listed in the following tables.



Key

1 LIN bus signal

Figure 5 — Definition of bus timing parameters

5.3.4 12 V LIN systems: Electrical parameters

5.3.4.1 DC parameters

The electrical DC parameters of the LIN electrical physical layer and the termination resistors are listed in Tables 10 and 11, respectively. Unless otherwise specified, all voltages are referenced to the local ECU ground and positive currents flow into the ECU.

In case of an integrated resistor/diode network, no parasitic current paths shall be formed between the bus line and the ECU-internal supply (V_{SUP}), for example by ESD elements.

Table 10 defines the electrical DC parameters of the LIN electrical physical layer.

Table 10 — Electrical DC parameters of the LIN electrical physical layer

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
Param 9	V_{BAT}[a]	8	—	18	V	ECU operating voltage range
Param 10	V_{SUP}[b]	7,0	—	18	V	Supply voltage range
Param 11	$V_{SUP\_NON\_OP}$	−0,3	—	40	V	Voltage range within which the device is not destroyed; no guarantee of correct operation
Param 12	I_{BUS_LIM}[c]	40	—	200	mA	Current limitation for driver dominant state driver on $V_{BUS} = V_{BAT\_max}$[d]
Param 13	$I_{BUS\_PAS\_dom}$	−1	—	—	mA	Input leakage current at the receiver including pull-up resistor as specified in Table 11 Param 26 driver off $V_{BUS} = 0$ V $V_{BAT} = 12$ V
Param 14	$I_{BUS\_PAS\_rec}$	—	—	20	µA	Driver off $8\ V < V_{BAT} < 18\ V$ $8\ V < V_{BUS} < 18\ V$ $V_{BUS} \geq V_{BAT}$
Param 15	$I_{BUS\_NO\_GND}$	−1	—	1	mA	Control unit disconnected from ground $GND_{Device} = V_{SUP}$ $0\ V < V_{BUS} < 18\ V$ $V_{BAT} = 12$ V Loss of local ground shall not affect communication in the residual network.
Param 16	$I_{BUS\_NO\_BAT}$	—	—	100	µA	V_{BAT} disconnected V_{SUP} = GND $0 < V_{BUS} < 18$ V Node shall sustain the current that can flow under this condition. Bus shall remain operational under this condition.
Param 17	V_{BUSdom}	—	—	0,4	V_{SUP}	Receiver dominant state
Param 18	V_{BUSrec}	0,6	—	—	V_{SUP}	Receiver recessive state
Param 19	V_{BUS_CNT}	0,475	0,5	0,525	V_{SUP}	$V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$[e]
Param 20	V_{HYS}	—	—	0,175	V_{SUP}	$V_{HYS} = V_{th\_rec} - V_{th\_dom}$

[a] V_{BAT} denotes the supply voltage at the connector of the control unit and may be different from the internal supply, V_{SUP}, for electronic components (see 5.3.2).

[b] V_{SUP} denotes the supply voltage at the transceiver inside the control unit and may be different from the external supply, V_{BAT}, for control units (see 5.3.2).

[c] I_{BUS}: current flowing into the node.

[d] A transceiver shall be capable to sink at least 40 mA. The maximum current flowing into the node shall not exceed 200 mA under DC conditions to avoid possible damage.

[e] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

[f] V_{ANODE}: voltage at the anode of the diode. $V_{CATHODE}$: voltage at the cathode of the diode.

[g] $V_{BATTERY}$: voltage across the vehicle battery connectors. V_{GND_ECU}: voltage on the local ECU ground connector with respect to vehicle battery ground connector ($V_{GND\_BATTERY}$).

[h] This constraint refers to duty cycle D1 and D2 only.

Table 10 *(continued)*

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
Param 21	$V_{SerDiode}$	0,4	0,7	1,0	V	Voltage drop at the serial diodes D_{ser_master} and D_{Rev_Batt} in pull-up path (Figure 3). $V_{SerDiode} = V_{ANODE} - V_{CATHODE}$[f]
Param 22	V_{Shift_BAT}	0	—	11,5 %	V_{BAT}	Battery shift $V_{Shift\_BAT} = V_{BATTERY} - V_{Shift\_GND} - V_{BAT}$[g]
Param 23	V_{Shift_GND}	0	—	11,5 %	V_{BAT}	GND shift $V_{Shift\_GND} = V_{GND\_ECU} - V_{GND\_BATTERY}$[g]
Param 24	$V_{Shift\_Difference}$[h]	0	—	8 %	V_{BAT}	Difference between battery shift and GND shift $V_{Shift\_Difference} = \lvert V_{Shift\_BAT} - V_{Shift\_GND} \rvert$
Param 82	$V_{BUS\_MAX\_RATINGS}$	−27	—	40	V	The part should not suffer any damage.

[a] V_{BAT} denotes the supply voltage at the connector of the control unit and may be different from the internal supply, V_{SUP}, for electronic components (see 5.3.2).

[b] V_{SUP} denotes the supply voltage at the transceiver inside the control unit and may be different from the external supply, V_{BAT}, for control units (see 5.3.2).

[c] I_{BUS}: current flowing into the node.

[d] A transceiver shall be capable to sink at least 40 mA. The maximum current flowing into the node shall not exceed 200 mA under DC conditions to avoid possible damage.

[e] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

[f] V_{ANODE}: voltage at the anode of the diode. $V_{CATHODE}$: voltage at the cathode of the diode.

[g] $V_{BATTERY}$: voltage across the vehicle battery connectors. V_{GND_ECU}: voltage on the local ECU ground connector with respect to vehicle battery ground connector ($V_{GND\_BATTERY}$).

[h] This constraint refers to duty cycle D1 and D2 only.

Table 11 defines the parameters of the pull-up resistors.

Table 11 — Parameters of the pull-up resistors

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
Param 25	R_{MASTER}	900	1 000	1 100	Ω	The serial diode is mandatory (see Figure 3).
Param 26	R_{SLAVE}	20	30	60	kΩ	The serial diode is mandatory.

5.3.4.2 AC parameters

The electrical AC parameters of the LIN electrical physical layer are listed in Tables 12, 13 and 14, with the parameters being defined in Figure 5. The electrical AC characteristics of the bus can be strongly affected by the line characteristics as shown in 5.3.3. The time constant, τ, (and thus the overall capacitance) of the bus (see 5.3.5) shall be selected carefully in order to allow for a correct signal implementation under worst case conditions.

Table 12 specifies the timing parameters for proper operation at 20 kbit/s.

Table 12 — Driver electrical AC parameters of the LIN electrical physical layer of BR_Range_20K 12 V LIN networks

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
LIN driver, bus load conditions (C_{BUS}; R_{BUS}): 1 nF; 1 kΩ/6,8 nF; 660 Ω/10 nF; 500 Ω						
Param 27	D1 (Duty Cycle 1)	0,396	—	—	—	$TH_{Rec(max)} = 0{,}744 \times V_{SUP}$; $TH_{Dom(max)} = 0{,}581 \times V_{SUP}$; V_{SUP} = 7,0 V to 18 V; t_{BIT} = 50 µs; $D1 = t_{Bus\_rec(min)}/(2 \times t_{BIT})$
Param 28	D2 (Duty Cycle 2)	—	—	0,581	—	$TH_{Rec(min)} = 0{,}422 \times V_{SUP}$; $TH_{Dom(min)} = 0{,}284 \times V_{SUP}$; V_{SUP} = 7,6 V to 18 V; t_{BIT} = 50 µs; $D2 = t_{Bus\_rec(max)}/(2 \times t_{BIT})$

For improved EMC performance, exception is granted for speeds of 10 417 kbit/s or below. For details, see Table 13, which specifies the timing parameters for proper operation at 10 417 kbit/s.

Table 13 — Driver electrical AC parameters of the LIN electrical physical layer of BR_Range_10K 12 V LIN networks

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
LIN driver, bus load conditions (C_{BUS}; R_{BUS}): 1 nF; 1 kΩ/6,8 nF; 660 Ω/10 nF; 500 Ω						
Param 29	D3 (Duty Cycle 3)	0,417	—	—	—	$TH_{Rec(max)} = 0{,}778 \times V_{SUP}$; $TH_{Dom(max)} = 0{,}616 \times V_{SUP}$; V_{SUP} = 7,0 V to 18 V; t_{BIT} = 96 µs; $D3 = t_{Bus\_rec(min)}/(2 \times t_{BIT})$
Param 30	D4 (Duty Cycle 4)	—	—	0,590	—	$TH_{Rec(min)} = 0{,}389 \times V_{SUP}$; $TH_{Dom(min)} = 0{,}251 \times V_{SUP}$; V_{SUP} = 7,6 V to 18 V; t_{BIT} = 96 µs; $D4 = t_{Bus\_rec(max)}/(2 \times t_{BIT})$

Application specific implementations (ASICs) shall meet the parameters in Table 12 and/or Table 13. If both sets of parameters are implemented, the proper mode shall be selected based on the bus bit rate.

Table 14 defines the receiver electrical AC parameters of the LIN electrical physical layer.

Table 14 — Receiver electrical AC parameters of the LIN electrical physical layer

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
LIN receiver, RXD load condition (C_{RXD}): 20 pF; (if open drain behaviour: R_{pull_up} = 2,4 kΩ)						
Param 31	trx_pd	—	—	6	µs	propagation delay of receiver
Param 32	trx_sym	−2	—	2	µs	symmetry of receiver propagation delay rising edge with respect to falling edge

The EMC behaviour of the LIN bus depends on the signal shape represented by slew rate and other factors such as di/dt and d^2V/dt^2. The signal shape should be carefully selected in order to reduce emissions and allow for bit rates up to 20 kbit/s.

5.3.5 24 V LIN systems: Electrical parameters

5.3.5.1 DC parameters

The electrical DC parameters of the LIN electrical physical layer and the termination resistors are listed in Tables 15 and 16, respectively. Unless otherwise specified, all voltages are referenced to the local ECU ground and positive currents flow into the ECU.

In case of an integrated resistor/diode network, no parasitic current paths shall be formed between the bus line and the ECU-internal supply (V_{SUP}), for example by ESD elements.

Table 15 defines the electrical DC parameters of the LIN electrical physical layer.

Table 15 — Electrical DC parameters of the LIN electrical physical layer

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
Param 52	$V_{BAT\_BR\_Range\_20K}$[a]	16	—	36	V	ECU operating voltage range in BR_Range_20K 24 V LIN systems
Param 53	$V_{SUP\_BR\_Range\_20K}$[b]	15	—	36	V	supply voltage range in BR_Range_20K 24 V LIN systems
Param 54	$V_{BAT\_BR\_Range\_10K}$[a]	8	—	36	V	operating voltage range in BR_Range_10K 24 V LIN systems
Param 55	$V_{SUP\_BR\_Range\_10K}$[b]	7	—	36	V	supply voltage range in BR_Range_10K 24 V LIN systems
Param 56	$V_{SUP\_NON\_OP}$	−0,3	—	58	V	voltage range within which the device is not destroyed; no guarantee of correct operation
Param 57	I_{BUS_LIM}[c]	75	—	300	mA	current limitation for driver dominant state driver on $V_{BUS} = V_{BAT\_max}$[d]
Param 58	$I_{BUS\_PAS\_dom}$	−2	—	—	mA	input leakage current at the receiver including pull-up resistor as specified in Table 16 Param 71 driver off V_{BUS} = 0 V V_{BAT} = 24 V
Param 59	$I_{BUS\_PAS\_rec}$	—	—	20	µA	driver off 8 V < V_{BAT} < 36 V 8 V < V_{BUS} < 36 V $V_{BUS} \geq V_{BAT}$

[a] V_{BAT} denotes the supply voltage at the connector of the control unit and may be different from the internal supply, V_{SUP}, for electronic components (see 5.3.2).

[b] V_{SUP} denotes the supply voltage at the transceiver inside the control unit and may be different from the external supply V_{BAT} for control units (see 5.3.2).

[c] I_{BUS}: current flowing into the node.

[d] A transceiver shall be capable to sink at least 75 mA. The maximum current flowing into the node shall not exceed 300 mA under DC conditions to avoid possible damage.

[e] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

[f] V_{ANODE}: voltage at the anode of the diode. $V_{CATHODE}$: voltage at the cathode of the diode.

[g] $V_{BATTERY}$: voltage across the vehicle battery connectors. V_{GND_ECU}: voltage on the local ECU ground connector with respect to vehicle battery ground connector ($V_{GND\_BATTERY}$).

[h] This constraint refers to duty cycle D1 and D2 only.

Table 15 *(continued)*

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
Param 60	$I_{BUS\_NO\_GND}$	−2	—	2	mA	control unit disconnected from ground $GND_{Device} = V_{SUP}$ $0\ V < V_{BUS} < 36\ V$ $V_{BAT} = 24\ V$ loss of local ground shall not affect communication in the residual network.
Param 61	$I_{BUS\_NO\_BAT}$	—	—	100	µA	V_{BAT} disconnected $V_{SUP} = GND$ $0 < V_{BUS} < 36\ V$ node shall sustain the current that can flow under this condition. Bus shall remain operational under this condition.
Param 62	V_{BUSdom}	—	—	0,4	V_{SUP}	receiver dominant state
Param 63	V_{BUSrec}	0,6	—	—	V_{SUP}	receiver recessive state
Param 64	V_{BUS_CNT}	0,475	0,5	0,525	V_{SUP}	$V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$[e]
Param 65	V_{HYS}	—	—	0,175	V_{SUP}	$V_{HYS} = V_{th\_rec} - V_{th\_dom}$
Param 66	$V_{SerDiode}$	0,4	0,7	1,0	V	voltage drop at the serial diodes D_{ser_master} and D_{ser_int} in pull-up path (Figure 3). $V_{SerDiode} = V_{ANODE} - V_{CATHODE}$[f]
Param 67	V_{Shift_BAT}	0	—	11,5 %	V_{BAT}	battery-shift $V_{Shift\_BAT} = V_{BATTERY} - V_{Shift\_GND} - V_{BAT}$[g]
Param 68	V_{Shift_GND}	0	—	11,5 %	V_{BAT}	GND-shift $V_{Shift\_GND} = V_{GND\_ECU} - V_{GND\_BATTERY}$[g]
Param 69	$V_{Shift\_Difference}$[h]	0	—	8 %	V_{BAT}	difference between battery-shift and GND-shift $V_{Shift\_Difference} = \lvert V_{Shift\_BAT} - V_{Shift\_GND} \rvert$
Param 83	$V_{BUS\_MAX\_RATINGS}$	−6	—	36	V	The part should not suffer any damage.

[a] V_{BAT} denotes the supply voltage at the connector of the control unit and may be different from the internal supply, V_{SUP}, for electronic components (see 5.3.2).

[b] V_{SUP} denotes the supply voltage at the transceiver inside the control unit and may be different from the external supply V_{BAT} for control units (see 5.3.2).

[c] I_{BUS}: current flowing into the node.

[d] A transceiver shall be capable to sink at least 75 mA. The maximum current flowing into the node shall not exceed 300 mA under DC conditions to avoid possible damage.

[e] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

[f] V_{ANODE}: voltage at the anode of the diode. $V_{CATHODE}$: voltage at the cathode of the diode.

[g] $V_{BATTERY}$: voltage across the vehicle battery connectors. V_{GND_ECU}: voltage on the local ECU ground connector with respect to vehicle battery ground connector ($V_{GND\_BATTERY}$).

[h] This constraint refers to duty cycle D1 and D2 only.

Table 16 defines the parameters of the pull-up resistors.

Table 16 — Parameters of the pull-up resistors

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
Param 70	R_{MASTER}	900	1 000	1 100	Ω	The serial diode is mandatory (see Figure 3).
Param 71	R_{SLAVE}	20	30	60	kΩ	The serial diode is mandatory.

5.3.5.2 AC parameters

The electrical AC parameters of the LIN electrical physical layer are listed in Tables 17, 18 and 19 with the parameters being defined in Figure 5. The electrical AC characteristics of the bus can be strongly affected by the line characteristics as shown in 5.3.3. The time constant τ (and thus the overall capacitance) of the bus (see 5.3.5) shall be selected carefully in order to allow for a correct signal implementation under worst case conditions.

Table 17 specifies the timing parameters for proper operation at 20 kbit/s.

Table 17 — Driver electrical AC parameters of the LIN electrical physical layer of BR_Range_20K 24 V LIN networks

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
LIN driver, bus load conditions (C_{BUS}; R_{BUS}): 1 nF; 1 kΩ/6,8 nF; 660 Ω/10 nF; 500 Ω						
Param 72	D1 (duty cycle 1)	0,330	—	—	—	$TH_{Rec(max)} = 0{,}710 \times V_{SUP}$; $TH_{Dom(max)} = 0{,}554 \times V_{SUP}$; V_{SUP} = 15 V to 36 V; t_{BIT} = 50 µs; $D1 = t_{Bus\_rec(min)}/(2 \times t_{BIT})$
Param 73	D2 (duty cycle 2)	—	—	0,642	—	$TH_{Rec(min)} = 0{,}446 \times V_{SUP}$; $TH_{Dom(min)} = 0{,}302 \times V_{SUP}$; V_{SUP} = 15,6 V to 36 V; t_{BIT} = 50 µs; $D2 = t_{Bus\_rec(max)}/(2 \times t_{BIT})$

BR_Range_10K 24 V LIN systems operate at speeds of approximately 10 417 kbit/s or below. For details, see Table 18, which specifies the timing parameters for proper operation at 10 417 kbit/s.

Table 18 — Driver electrical AC parameters of the LIN electrical physical layer of BR_Range_10K 24 V LIN networks

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
LIN driver, bus load conditions (C_{BUS}; R_{BUS}): 1 nF; 1 kΩ/6,8 nF; 660 Ω/10 nF; 500 Ω						
Param 74	D3 (duty cycle 3)	0,386	—	—	—	$TH_{Rec(max)} = 0{,}744 \times V_{SUP}$; $TH_{Dom(max)} = 0{,}581 \times V_{SUP}$; V_{SUP} = 7,0 V to 36 V; t_{BIT} = 96 µs; $D3 = t_{Bus\_rec(min)}/(2 \times t_{BIT})$
Param 75	D4 (duty cycle 4)	—	—	0,591	—	$TH_{Rec(min)} = 0{,}422 \times V_{SUP}$; $TH_{Dom(min)} = 0{,}284 \times V_{SUP}$; V_{SUP} = 7,6 V to 36 V; t_{BIT} = 96 µs; $D4 = t_{Bus\_rec(max)}/(2 \times t_{BIT})$

Application specific implementations (ASICs) shall meet the parameters in Table 17 and/or Table 18. If both sets of parameters are implemented, the proper mode shall be selected based on the bus bit rate.

Table 19 defines the receiver electrical AC parameters of the LIN electrical physical layer.

Table 19 — Receiver electrical AC parameters of the LIN electrical physical layer

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
LIN receiver, RXD load condition (C_{RXD}): 20 pF; (if open drain behaviour: R_{pull_up} = 2,4 kΩ)						
Param 76	t_{rx_pd}	—	—	6	µs	propagation delay of receiver
Param 77	t_{rx_sym}	−2	—	2	µs	symmetry of receiver propagation delay rising edge with respect to falling edge

The EMC behaviour of the LIN bus depends on the signal shape represented by slew rate and other factors such as di/dt and d^2V/dt^2. The signal shape should be carefully selected in order to reduce emissions and allow for bit rates up to 20 kbit/s.

5.3.6 Line characteristics

The maximum slew rate of rising and falling bus signals are in practice limited by the active slew rate control of typical bus transceivers. The minimum slew rate for the rising signal, however, can be given by the RC time constant, τ. Therefore, the bus capacitance should be kept low in order to keep the waveform asymmetry small. The capacitance of the master module can be chosen higher than in the slave modules, in order to provide a "buffer" in case of network variants with various number of nodes. The total bus capacitance, C_{BUS}, can be calculated by Formula (3):

$$C_{BUS} = C_{MASTER} + n \times C_{SLAVE} + C'_{LINE} \times LEN_{BUS} \quad (3)$$

The RC time constant, τ, is calculated by Formula (4):

$$\tau = C_{BUS} \times R_{BUS} \quad (4)$$

with R_{BUS} in Formula (5):

$$R_{BUS} = R_{MASTER} || R_{SLAVE\_1} || R_{SLAVE\_2} || \text{ to } || R_{SLAVE\_N} \quad (5)$$

Line characteristics and parameters are defined in Table 20.

Table 20 — Line characteristics and parameters

Number	Parameter	Min.	Typ.	Max.	Unit	Comment/condition
Param 33	LEN_{BUS}	—	—	40	m	total length of bus line
Param 34	C_{BUS}	1	4	10	nF	total capacitance of the bus including slave and master capacitances
Param 35	τ	1	—	5	µs	time constant of overall system
Param 36	C_{MASTER}	—	220	—	pF	capacitance of master node
Param 37	C_{SLAVE}	—	220	250	pF	capacitance of slave node
Param 38	C'_{LINE}	—	100	150	pF/m	line capacitance

C_{MASTER} and C_{SLAVE} are defining the total node capacitance at the connector of an ECU including the physical bus driver (transceiver) and all other components applied to the LIN bus pin such as capacitors or protection circuitry. The number of nodes in a LIN cluster should not exceed 16. The network impedance may prohibit a fault-free communication under worst case conditions with more than 16 nodes. Every additional node lowers the network resistance by approximately 3 % (30 kΩ || ~1 kΩ).

5.3.7 12 V LIN systems: performance in non-operation supply voltage range

For V_{BAT} > 18 V or V_{BAT} < 8 V, the ECU may still operate, but communication is not guaranteed. If an ECU is not intending to transmit on the LIN bus (e.g. transmit input of a LIN transceiver is recessive), the LIN driver shall not drive the LIN bus to dominant state. If the LIN bus is in recessive state, the LIN receiver output shall provide a recessive state.

5.3.8 24 V LIN systems: performance in non-operation supply voltage range

For V_{BAT} > 36 V or V_{BAT} < 16 V for a BR_Range_20K system or for V_{BAT} > 36 V or V_{BAT} < 8 V for a BR_Range_10K system, the ECU may still operate, but communication is not guaranteed. If an ECU is not intending to transmit on the LIN bus (e.g. transmit input of a LIN transceiver is recessive), the LIN driver shall not drive the LIN bus to dominant state. If the LIN bus is in recessive state, the LIN receiver output shall provide a recessive state.

5.3.9 Performance during fault modes

5.3.9.1 General

All LIN device state changes on conditional events (e.g. temperature shutdown) shall be specified in the LIN device data sheet.

5.3.9.2 Loss of supply voltage connection or ground connection

ECUs with loss of connection to either supply voltage or ground shall not interfere with normal communication among the remaining LIN participants. Upon return of connection, normal operation shall resume without any intervention on the LIN bus line.

5.3.9.3 12 V LIN systems: LIN systems bus wiring short to battery or ground

The network data communication may be interrupted but there shall be no damage to any ECU when the LIN bus line is shorted to either positive battery with less than 26,5 V or GND. Upon remove of the fault, normal operation shall resume without any intervention on the LIN bus line.

NOTE The 26,5 V is specified to stay within the non-conducting range of the commonly used 27 V zener stacks.

5.3.9.4 24 V LIN systems: LIN systems bus wiring short to battery or ground

The network data communication may be interrupted but there shall be no damage to any ECU when the LIN bus line is shorted to either positive battery with less than 26,5 V or GND. The 26,5 V condition comes from a double battery jump start. Upon remove of the fault, normal operation shall resume without any intervention on the LIN bus line.

5.3.10 ESD/EMI compliance

Semiconductor electrical physical layer devices shall comply with requirements for protection against human body discharge according to IEC 61000-4-2. The minimum discharge voltage level shall be ±2 kV.

The required ESD level for automotive applications may be up to ±25 kV at the connectors of the ECU.

Annex A
(informative)

LIN peripheral interface design considerations

A.1 General

LIN compliancy can only be achieved when specific properties required by the LIN protocol and physical layer specification are supported by the underlying peripheral hardware interface.

This is a collection of requirements and optional features for UART and LIN controller hardware interfaces.

A.2 UART requirements

UART interfaces shall respect the minimum requirements as specified in Table A.1.

Table A.1 — UART minimum requirements

Category	Affected node		Requirement
	Master	Slave	
Byte transmission/ reception	X	X	1 start bit, 8 data bit, 1 (or 2) stop bit, register based configuration
Byte transmission	X	X	— Possibility to cancel transmission at bit or latest byte boundary after detection of disturbance. — Preceding stop bit (from PID) shall not be shortened by new byte transmission request. — Transmit byte register (could be same as Rx byte register).
Tx monitoring	X	X	Optional (Rx monitoring may be used alternatively): — distinguish framing error (start bit and stop bit) and data error; — possible also via Rx monitoring except start bit error detection (acceptable); — separate status register flag for framing error and for data error; — Tx-Interrupt generation after stop bit has been sampled (see 5.2.3); — no disabling of transmitter (and re-enabling in software) but cancelling of ongoing transmission.

Table A.1 *(continued)*

Category	Affected node		Requirement
	Master	Slave	
Byte reception and monitoring	X	X	— Synchronization to falling edge on receive pin. — Sample point according to 5.2.3. — Rx error interrupt or Rx interrupt generation after stop bit has been sampled. — Framing error detection on stop bit (including checksum byte). — Overrun error detection (receive byte was not read out before a new reception is finished). — Status flag for framing error and status flag for register overrun error in status register (flag shall be set in register before interrupt function can check the status). — Receive byte register (could be same as Tx byte register). — Bus loads: long dominant bit, short recessive bit (should be no issue if sampling is implemented correctly).
Wake up transmission	X	X	(UART mode), software shall decide when a wake up shall be transmitted (LIN sleep state).
Wake up detection	X	X	Software decides when a wake up pulse is expected (LIN sleep state, this is different to ECU low power mode). Optional: — low power mode / stop mode IRQ generation; — suppression of short pulses <150 µs (also part of the LIN transceiver requirements); — IRQ generation on rising edges.
Baudrate configuration	X	X	Recommendation: — configuration with small configuration fault <0,5 % (16 bit); — read and write process (update in software, verification of valid baudrate, rejection of invalid break field/sync byte field sequences not matching expected baudrate); — reconfiguration shall be supported while receiving a header at the end of sync byte field
Rx pin	X	X	Recommendation: Connected to timer/input capture peripheral unit for baudrate synchronization algorithm in software (fallback solution)
Break field detection	—	X	Optional (also a UART framing error can be used for start of frame detection): — 11 bit dominant bus threshold; — distinguish from byte with stop bit framing error with data 00_{16} (10 dominant bits) for correct response_error reporting; — only one event should occur.

Table A.1 *(continued)*

Category	Affected node		Requirement
	Master	Slave	
Baudrate synchronization in hardware	—	X	Optional (can be more stable/efficient than software solution): — verification of relation between break field (11 bit to 32 bit) and sync byte field length; — measurement is performed on falling edges of sync byte field (4 times a 2 bit sequence is measured); — verification of maximum deviation of two bit sequences in sync byte field; — stop bit disturbance detection; — 8th data bit disturbance detection; — sync byte field/header interrupt only if all checks are met; — error reporting optional (header error IRQ with separate flag in register); — break delimiter check or total header length <40 %; — bus idle detection necessary if interrupts are generated only in case of successful header or break field and sync byte field; — criteria to stay in LIN operational state: transitions on the bus (recessive - > dominant and dominant - > recessive); — bus idle timeout protocol version dependent: 1,25 s (25 000 T_{BIT} at 20 kbit/s) - 10 s (LIN ≥ 2.1), required length defined in separate register; — interrupt generation in case of bus idle detection (no transitions on the bus longer than the register configured value); — separate status flag in status register; — in LIN sleep mode bus idle is not checked - > en/disable in register configuration by software; — break field and sync byte field detection active at any time when configured active.
Dominant/ Recessive disturbance	X	X	Recommendation: same reporting to the software.
Register design	X	X	Recommendation: Data consistency, clear register, clear on read.
Polling (no interrupt usage)	X	X	Recommendation: Only one register should be necessary to be evaluated to decide if software shall evaluate events (rx, error, tx).
LIN interrupt disable/restore	X	X	— All LIN interrupt sources should be activated, deactivated in just one atomic operation. — Register should not be shared with other peripheral sources. — Separate register for enable and disable.
LIN current status on Rx pin (recessive/ dominant)	X	X	Recommendation: Read Rx pin status while communication is active.
Error detection	—	X	Recommendation: parity error detection (see SAE J2602).
LIN sleep state while shot to GND	X	X	Entering LIN sleep state shall not be prevented by interrupts while LIN is permanent short to GND.
Idle line state	X	X	Idle line shall be (register configurable) recessive.

A.3 LIN frame controller requirements

LIN controller interfaces shall respect the following minimum requirements (see Table A.2).

Table A.2 — LIN controller requirements

Category	Affected node		Requirement
	Master	Slave	
Operational independency	X	—	If multiple LIN channels should be supported, any of them shall operate independently (network status, scheduling, baudrate, frame transmission and reception, register access).
Header detection	—	X	Break field and sync byte field detection shall be active at any time and operate in parallel to normal frame reception and transmission. If a new header is detected also the response shall be received/ transmitted/ignored depending on the PID received.
Error handling	—	X	Error reporting shall allow to distinguish no response from incomplete response (for correct response_error setting) when a new header is received.
Header specification	X	—	Configuration should allow to define the break field in a range of 13 T_{BIT} to 27,6 T_{BIT} (default 13 or 14) and at least 1 bit to 2 bits for break delimiter (default two).
Error handling	X	—	Error reporting shall allow to distinguish for a receive frame no response from incomplete response (for EVT-Support and collision detection) when a new header is scheduled.
Baudrate detection (multiple baudrates supported)	—	X	A header reception shall be rejected if the sync byte field is valid but the break field is too short, e.g. <9,5/11 T_{BIT} or too long, e.g. >27,6 T_{BIT} in relation to a sync byte field bit.
Bus idle detection	X	X	Timeout should be configurable in a range of 4 s to 10 s.
Bus idle detection	—	X	If no valid headers are visible on the LIN bus but transitions of the bus (recessive to dominant and vice versa), the node shall not enter sleep state. If there is no hardware timeout detection implemented, transitions on the bus shall be notified to allow the software to recover the timeout timer. This could be done based on a register flag which is polled and cleared by the driver and set by hardware whenever a transition has been detected.
Baudrate synchronization	—	X	A header reception shall be rejected when two bit sequences of the break field filed have significant different values. Recommendation is 15 % maximum deviation.
Checksum	X	—	The checksum type changes frame by frame and therefore shall be configurable at runtime.
Checksum	—	X	The checksum type is set in a slave node when the PID has been received and may change frame by frame.
Checksum	X	X	Recommendation to allow a mode where the checksum is provided by the driver and not calculated in hardware automatically (fallback solution).
Frame length	—	X	The frame length is set after reception of the PID frame and may change frame by frame.
Baudrate synchronization	—	X	Over all baudrate deviation after the synchronization procedure may be below 1 % for slave to slave communication.
Baudrate synchronization	—	X	The baudrate adjusted shall be visible in registers to allow the driver to confirm or reject a header if the baudrate is not in the expected range due to noise.

Table A.2 *(continued)*

Category	Affected node		Requirement
	Master	Slave	
Error detection	X	X	Data error and framing error shall be detected during transmission to stop transmission latest at the byte boundary of the affected byte. It is recommended to report data error and framing error in different register flags (required for SAE J2602).
Wake up frame transmission	X	X	The wake up pulse length should be configurable in registers. Wake up transmission should also be monitored and confirmed to the application.
Wake up frame reception	X	X	Wake up interrupt should not be generated before the rising edge is seen after a sufficient dominant pulse.
Transition to low power mode	X	X	After reception of a sleep command frame, a wake up frame shall be detected and reported to the software (interrupt) also in the LIN controller because setting the LIN transceiver may take time (SPI communication) and a wake up shall not be missed.
Response transmission	X	X	Response transmission shall not be started before the stop bit of the PID has been completely transmitted.
Response ignored	X	X	Depending on the PID, a frame may be received, transmitted or completely ignored if other nodes are addressed. Ignoring the response of a frame shall not affect header detection/transmission capabilities and also next frame response handling.
Header detection	—	X	The type of a frame (receive, transmit, ignore and also the checksum type and data length) is derived from the header interrupt which is generated after PID reception in a slave node. It shall be ensured that the appropriate register configuration can be performed at least until the end of the response first receive byte. If the decision is expected before the first response byte is received, the frame will be lost if the interrupt is delayed due to other tasks (interrupt disable sections, other interrupts currently serviced). (A response may follow the header without any response space.)

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