BRITISH STANDARD

BS IEC
60747-9:2007

Semiconductor devices — Discrete devices —

Part 9: Insulated-gate bipolar transistors (IGBTs)

ICS 31.080.30

BSI
British Standards

National foreword

This British Standard is the UK implementation of IEC 60747-9:2007. It supersedes BS IEC 60747-9:1998 which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

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Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)

CONTENTS

SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

Part 9: Insulated-gate bipolar transistors (IGBTs)

1 Scope

This part of IEC 60747 gives product specific standards for terminology, letter symbols, essential ratings and characteristics, verification of ratings and methods of measurement for insulated-gate bipolar transistors (IGBTs).

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-2, *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*

IEC 60747-6, *Semiconductor devices – Part 6: Thyristors*

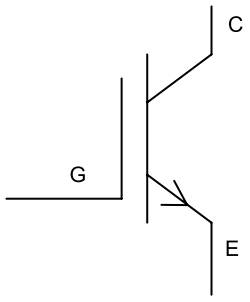
IEC 61340 (all parts), *Electrostatics*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1 Graphical symbol of IGBT

The graphical symbol as shown below is used in this edition of IEC 60747-9.



Graphical symbol

NOTE Only the graphical symbol for N-channel IGBT is used in this standard. It equally applies for the measurement of P-channel devices. In the case of P-channel devices polarity must be adapted.

3.2 General terms

3.2.1
insulated-gate bipolar transistor
IGBT
transistor having a conduction channel and a PN junction. The current flowing through the channel and the junction is controlled by an electric field resulting from a voltage applied between the gate and emitter terminals
See IEV 521-04-05.

NOTE With collector-emitter voltage applied, the PN junction is forward biased.

3.2.2
N-channel IGBT
IGBT that has one or more N-type conduction channels
See IEV 521-05-06.

3.2.3
P-channel IGBT
IGBT that has one or more P-type conduction channels
See IEV 521-04-05.

3.2.4
collector current (of an IGBT)
I_C
direct current that is switched (controlled) by the IGBT

3.2.5
collector terminal, collector (of an IGBT)
C
for an N-channel (a P-channel) IGBT, the terminal to (from) which the collector current flows from (to) the external circuit
See IEV 521-07-05 and IEV 521-05-02.

3.2.6
emitter terminal, emitter (of an IGBT)
E
for an N-channel (a P-channel) IGBT, the terminal from (to) which the collector current flows to (from) the external circuit
See IEV 521-07-04.

3.2.7
gate terminal, gate (of an IGBT)
G
terminal to which a voltage is applied against the emitter terminal in order to control the collector current
See IEV 521-07-09.

3.3 Terms related to ratings and characteristics; voltages and currents

3.3.1
collector-emitter (d.c.) voltage
voltage between collector and emitter

3.3.2
collector-emitter voltage with gate-emitter short-circuited
V_{CES}
collector-emitter voltage at which the collector current has a specified low (absolute) value with gate-emitter short-circuited

3.3.3
collector-emitter sustaining voltage
V_{CE*sus}
collector-emitter breakdown voltage at relatively high values of collector current where the breakdown voltage is relatively insensitive to changes in collector current, for a specified termination between gate and emitter terminals

NOTE 1 The specified termination between gate and emitter terminals is indicated in the letter symbol by the third subscript '*'; see 4.1.2 of IEC 60747-7.

NOTE 2 When necessary, a suitable qualifier is added to the basic term to indicate a specific termination between gate and emitter terminals.

Example: Collector-emitter sustaining voltage with gate and emitter terminals short-circuited V_{CESsus}.

NOTE 3 The basic term may be shortened if the meaning is clear from the letter symbol used.

Example: Collector-emitter sustaining voltage V_{CERsus}.

NOTE 4 This term is important for high-voltage devices, for example more than 4 kV.

3.3.4
collector-emitter breakdown voltage
$V_{(BR)CES}$
voltage between collector and emitter above which the collector current rises steeply, with gate to emitter short-circuited
See IEV 521-05-06.

3.3.5
collector-emitter saturation voltage
V_{CEsat}
collector-emitter voltage under conditions of gate-emitter voltage at which the collector current is essentially independent of the gate-emitter voltage

3.3.6
gate-emitter (d.c.) voltage
voltage between gate and emitter

3.3.7
gate-collector (d.c.) voltage
voltage between gate and collector

3.3.8
gate-emitter threshold voltage
$V_{GE(th)}$
gate-emitter voltage at which the collector current has a specified low (absolute) value

3.3.9
electrostatic discharge voltage
voltage that can be applied to the gate terminal without destruction of the isolation layer
See IEV 521-05-27

3.3.10
collector cut-off current
collector current at a specific collector-emitter voltage below the breakdown region and gate off-state

3.3.11
collector current
current through collector

3.3.12
tail current
I_{CZ}
collector current during the tail time

3.3.13
gate leakage current
I_{GES}
leakage current into the gate terminal at a specified gate-emitter voltage with the collector terminal short-circuited to the emitter terminal

3.3.14
safe operating area
SOA
collector current versus collector emitter voltage where the IGBT is able to turn-on and turn-off without failure

3.3.14.1
forward bias safe operating area
FBSOA
collector current versus collector emitter voltage where the IGBT is able to turn-on and is able to be on-state without failure

3.3.14.2
reverse bias safe operating area
RBSOA
collector current versus collector emitter voltage where the IGBT is able to turn-off without failure

3.3.14.3
short circuit safe operating area
SCSOA
short circuit duration and collector emitter voltage where the IGBT is able to turn-on and turn-off without failure

3.4 Terms related to ratings and characteristics; other characteristics

3.4.1
input capacitance
C_{ies}
capacitance between the gate and emitter terminals with the collector terminal short-circuited to the emitter terminal for a.c.

3.4.2
output capacitance
C_{oes}
capacitance between the collector and emitter terminals with the gate terminal short-circuited to the emitter terminal for a.c.

3.4.3
reverse transfer capacitance
C_{res}
capacitance between the collector and gate terminals

3.4.4
gate charge
Q_G
charge required to raise the gate-emitter voltage from a specified low to a specified high level

3.4.5
internal gate resistance
r_g
internal series resistance

3.4.6
turn-on energy (per pulse)
E_{on}
energy dissipated inside the IGBT during the turn-on of a single collector current pulse

NOTE The corresponding turn-on power dissipation under periodic pulse conditions is obtained by multiplying E_{on} by the pulse frequency.

3.4.7
turn-off energy (per pulse)
E_{off}
energy dissipated inside the IGBT during the turn-off time plus the tail time of a single collector current pulse

NOTE The corresponding turn-off power dissipation under periodic pulse conditions is obtained by multiplying E_{off} by the pulse frequency.

3.4.8
turn-on delay time
$t_{d(on)}$, t_d
time interval between the beginning of a voltage pulse across the input terminals which switches the IGBT from the off-state to the on-state and the beginning of the rise of the collector current

NOTE Usually, the time is measured between points corresponding to 10 % of the input and output pulse amplitudes.

3.4.9
rise time
t_r
time interval between the instants at which the rise of the collector current reaches specified lower and upper limits, respectively, when the IGBT is being switched from the off-state to the on-state

NOTE Usually the lower and upper limits are 10 % and 90 % of the pulse amplitude.

3.4.10
turn-on time
t_{on}
sum of the turn-on delay time and the rise time

3.4.11
turn-off delay time
$t_{d(off)}$, t_s
time interval between the end of the voltage pulse across the input terminals which has held the IGBT in its on-state and the beginning of the fall of the collector current when the IGBT is switched from the on-state to the off-state

NOTE Usually, the time is measured between points corresponding to 90 % of the input and output pulse amplitudes.

3.4.12
fall time
t_f
time interval between the instants at which the fall of the collector current reaches specified upper and lower limits, respectively, when the IGBT is switched from the on-state to the off-state

NOTE Usually, the upper and lower limits are 90 % and 10 % of the pulse amplitude.

3.4.13
turn-off time
t_{off}
sum of the turn-off delay time and the fall time

3.4.14
tail time
t_z
time interval from the end of the turn-off time to the instant at which the collector current has fallen to 2 % or lower specified value

4 Letter symbols

4.1 General

General letter symbols for IGBTs are defined in Clause 4 of IEC 60747-1.

4.2 Additional general subscripts

C,c	collector
E,e	emitter
G,g	gate
sat	saturation
th	threshold
Z,z	tail
S	termination with a short circuit
R	termination with a resistor
X	termination with specified gate emitter voltage
sus	sustaining

4.3 List of letter symbols

Name and designation	Letter symbol
4.3.1 Voltages	
Collector-emitter voltage	V_{CE}
Collector-emitter voltage, gate-emitter short-circuited	V_{CES}
Collector-emitter sustaining voltage	V_{CE*sus}
Collector-emitter breakdown voltage, gate-emitter short-circuited	$V_{(BR)CES}$
Collector-emitter saturation voltage	V_{CEsat}
Gate-emitter voltage	V_{GE}
Gate-emitter voltage, collector-emitter short-circuited	V_{GES}
Gate-emitter threshold voltage	$V_{GE(th)}$
Collector-gate voltage, gate-emitter resistance specified	V_{CGR}
4.3.2 Currents	
Collector current	I_C
Peak collector current	I_{CM}
Repetitive peak collector current	I_{CRM}
Collector-emitter cut-off current, gate-emitter short-circuited	I_{CES}
Tail current	I_{CZ}
Gate current	I_G
Gate leakage current, collector-emitter short-circuited	I_{GES}
4.3.3 Other electrical magnitudes	
Input capacitance	C_{ies}
Output capacitance	C_{oes}
Reverse transfer capacitance	C_{res}
Gate charge	Q_G
Internal gate resistance	r_g
Turn-on power dissipation	P_{on}
Turn-on energy	E_{on}
Turn-off power dissipation	P_{off}
Turn-off energy	E_{off}
Conducting state power dissipation	P_{cond}
Conducting state energy	E_{cond}
Total power dissipation	P_{tot}
4.3.4 Time	
Tail time	t_Z
4.3.5 Thermal magnitudes	
Thermal resistance junction to heatsink	$R_{th(j-c)}$
Transient thermal impedance junction to heatsink	$Z_{th(j-c)}$

5 Essential ratings and characteristics

5.1 Ratings (limiting values)

Ratings shall be valid for the whole range of operating conditions as stated for the particular device, with reference to a curve where appropriate.

5.1.1 Ambient or case or virtual junction operating temperature (T_a or T_c or T_{vj})

Maximum and minimum values.

5.1.2 Storage temperature (T_{stg})

Maximum and minimum values.

5.1.3 Collector-emitter voltage with gate-emitter short-circuited (V_{CES})

Maximum value.

NOTE This rating should not be less than $V_{(BR)CES}$. (See 5.2.1.)

5.1.4 Gate-emitter voltages with collector emitter short circuit (V_{GES})

Maximum positive and negative values.

5.1.5 Continuous collector current (I_C)

Maximum value.

5.1.6 Repetitive peak collector current (I_{CRM})

Maximum value for rectangular pulses with specified pulse duration and duty cycle.

5.1.7 Non-repetitive peak collector current (I_{CSM})

Maximum value for a rectangular pulse with specified pulse duration.

5.1.8 Total power dissipation (P_{tot})

Maximum value with a derating curve where appropriate.

5.1.9 Maximum safe operating area

Diagram showing the maximum rated collector current I_c after turn-on, which may not be exceeded, even under best cooling conditions, as a function of the collector-emitter voltage V_{CE} before and during turn-on for direct current and various pulse durations at 25 °C case temperature.

5.1.10 Maximum reverse biased safe operating area (RBSOA)

Diagram showing the area of collector current I_C and collector-emitter voltage V_{CE} which the IGBTs will sustain simultaneously for a short period of time during turn-off without failure under the specified conditions.

5.1.11 Maximum short circuit safe operating area (SCSOA)

SCSOA is given by a pair of values of short-circuit duration t_{psc} and collector-emitter voltage V_{CE} which may not be exceeded under the load short-circuit conditions. The device may be turned on and turned off again for shorting a voltage source without failure.

5.1.12 Maximum terminal current (I_{tRMS}) (where appropriate)

Maximum r.m.s. value of the current through the main terminal.

5.1.13 Mounting force (*F*)

Maximum and minimum values, where appropriate.

5.1.14 Mounting torque (*M*)

Maximum and minimum values, where appropriate.

5.2 Characteristics

Characteristics shall be given at T_{vj} = 25 °C except where otherwise stated; and at one other specified temperature.

5.2.1 Collector-emitter breakdown voltage ($V_{(BR)CES}$)

Minimum value with gate-emitter short-circuited and at specified collector current.

5.2.2 Collector-emitter sustaining voltage (V_{CE*sus})

Where appropriate, minimum value at specified collector current and gate conditions.

5.2.3 Collector-emitter saturation voltage (V_{CEsat})

Maximum value at specified gate voltage and collector current.

5.2.4 Gate-emitter threshold voltage ($V_{GE(th)}$)

Minimum and maximum values at specified collector-emitter voltage and collector current.

5.2.5 Collector-emitter cut-off current (I_{CE*})

Maximum value at specified high collector-emitter voltage and for a specified termination between gate and emitter terminals.

5.2.6 Gate leakage current (I_{GES})

Maximum value at the maximum rated gate-emitter voltage.

5.2.7 Capacitances

Typical values of the following, at specified collector-emitter voltage and test frequency.

5.2.7.1 Input capacitance (C_{ies})

Typical input capacitance as small-signal value, in common-emitter configuration, under specified bias conditions and at a specified frequency, with the output short-circuited to a.c.

5.2.7.2 Output capacitance (C_{oes})

Typical output capacitance as small-signal value, in common-emitter configuration, under specified bias conditions and at a specified frequency, with the input short-circuited to a.c.

5.2.7.3 Reverse transfer capacitance (C_{res})

Typical reverse transfer capacitance as small-signal value, in common-emitter configuration, under specified bias conditions and at a specified frequency.

5.2.8 Gate charge (Q_G)

Typical value at specified values of gate-emitter voltage, collector-emitter voltage before turn-on and collector current after turn-on.

5.2.9 Internal gate resistance (r_g)

Maximum and/or typical value with collector short circuited to emitter in a.c. at the specified values of gate -emitter voltage, collector -emitter voltage and frequency

5.2.10 Turn-on energy (E_{on})

Maximum value per pulse under the following specified conditions:

- collector-emitter voltage before turn-on;
- collector current after turn-on;
- load conditions;
- gate-emitter voltage;
- resistance in the gate-emitter circuit;
- case or ambient temperature or virtual junction temperature.

5.2.11 Turn-off energy (E_{off})

Maximum value per pulse under the following specified conditions:

- collector current before turn-off;
- collector-emitter voltage after turn-off;
- load conditions;
- gate-emitter voltage;
- resistance in the gate-emitter circuit;
- case or ambient temperature or virtual junction temperature.

5.2.12 Switching times

5.2.12.1 Turn-on delay time ($t_{d(on)}$) and rise time (t_r)

Maximum values under the following specified conditions:

- collector-emitter voltage before turn-on;
- collector current after turn-on,
- load conditions;
- gate-emitter voltage;
- resistance in the gate-emitter circuit.

5.2.12.2 Turn-off delay time ($t_{d(off)}$), fall time (t_f) and tail time (t_z)

Maximum values with a free-wheeling diode connected under the following specified conditions:

- collector-emitter voltage after turn-off;
- collector current before turn-off;
- load conditions;
- gate-emitter voltage;
- resistance in the gate-emitter circuit.

5.2.13 Thermal resistance junction to case ($R_{th(j-c)}$)

Maximum value for case-rated IGBTs.

5.2.14 Thermal resistance junction to ambient ($R_{th(j-a)}$)

Maximum value for ambient-rated IGBTs.

5.2.15 Transient thermal impedance junction to case ($Z_{th(j-c)}$)

For case-rated IGBTs, diagram showing the maximum values against the time elapsed after a step change in power dissipation, or analytical elements.

5.2.16 Transient thermal impedance junction to ambient ($Z_{th(j-a)}$)

For ambient-rated IGBTs, diagram showing the maximum values against the time elapsed after a step change in power dissipation.

6 Measuring methods

6.1 General

The polarities shown in these circuits are applicable to N channel devices. The circuits can be adapted for P channel devices by inverting the polarities of the meters, generators and power supplies. The handling precautions given in IEC 61340 and the measuring method procedures given in 60747-1 apply.

6.2 Verification of ratings (limiting values)

After the following test, confirm the IGBT characteristics specified in Table 1.

Table 1 – Acceptance-defining characteristics

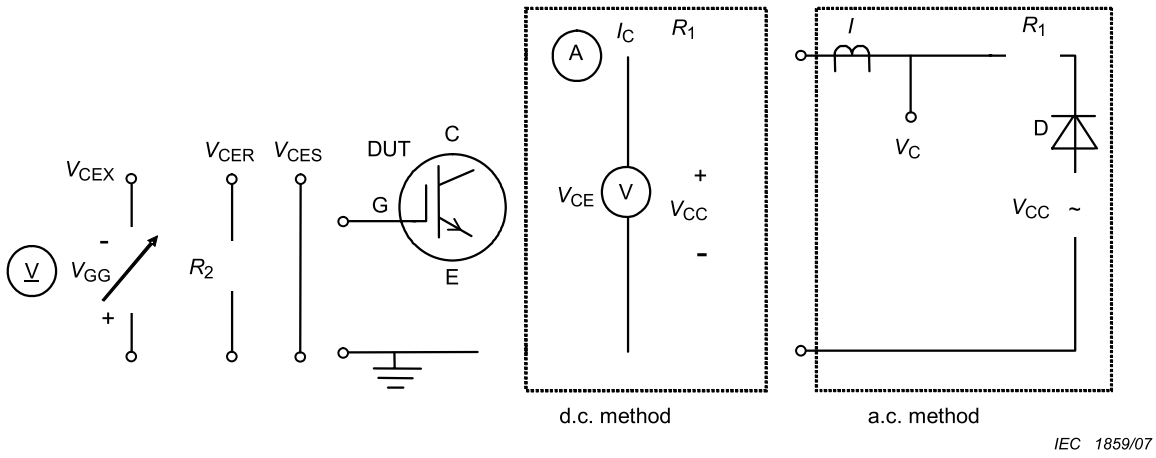
Characteristics	Acceptance criteria
I_{CES}	I_{CES} < USL
I_{GES}	I_{GES} < USL
$V_{CE(sat)}$	$V_{CE(sat)}$ < USL
$V_{GE(th)}$	$V_{GE(th)}$ < USL or > LSL
NOTE USL: upper specification limit LSL: lower specification limit	

6.2.1 Collector-emitter voltages (V_{CES}, V_{CER}, V_{CEX})

6.2.1.1 Purpose

To verify that an IGBT withstands the rated collector-emitter voltages V_{CES}, V_{CER} or V_{CEX} under specified conditions.

6.2.1.2 Circuit diagram (see Figure 1)



DUT (device under test)

Figure 1 – Circuit for measuring the collector-emitter voltages V_{CES}, V_{CER}, V_{CEX}

6.2.1.3 Circuit description

V_{CC} and V_{GG} are the voltage supply. R_1 is a circuit protection resistor.

6.2.1.4 Test procedure

There are two methods, i.e. the d.c. method and the a.c. method, with circuits according to Figure 1.

The specified conditions between gate and emitter shall be applied. The collector-emitter voltage is set to the specified value.

6.2.1.5 Specified conditions

– Collector-emitter voltage V_{CE}
– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}
– V_{CEX}: gate-emitter voltage $-V_{GG}$
– V_{CER}: resistor connected between gate and emitter
– V_{CES}: short circuit between gate and emitter

6.2.2 Gate-emitter voltage with collector emitter short circuit ($\pm V_{GES}$)

6.2.2.1 Purpose

To verify that an IGBT withstands the rated gate emitter voltage $\pm V_{GE}$ under specified conditions.

6.2.2.2 Circuit diagram (see Figure 2)

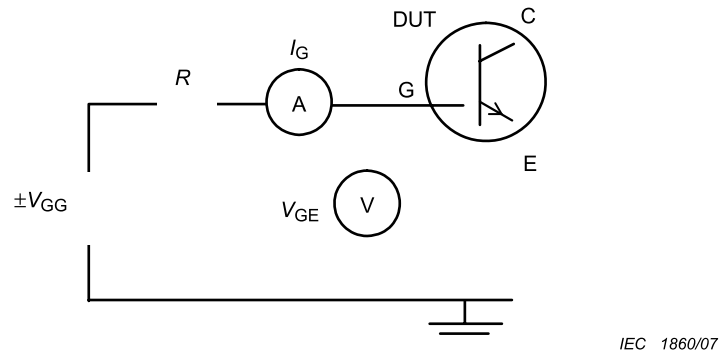


Figure 2 – Circuit for testing the gate-emitter voltage $\pm V_{GES}$

6.2.2.3 Circuit description

V_{GG} is the voltage supply. R is a circuit protection resistor.

6.2.2.4 Test procedure

The gate-emitter voltage V_{GE} is set to the specified value. A small protective resistor R is to be provided.

6.2.2.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}

– Gate-emitter leakage current I_{GES}

– Short circuit between collector and emitter

6.2.3 Maximum collector current (I_C)

6.2.3.1 Purpose

To verify that the collector current capability of an IGBT is not less than the maximum rated value I_C under specified conditions.

6.2.3.2 Circuit diagram (see Figure 3)

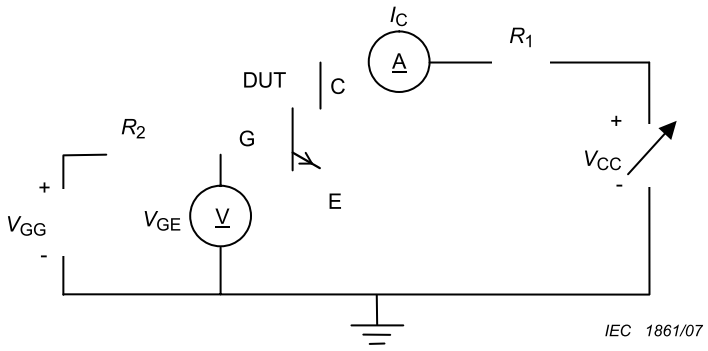


Figure 3 – Circuit for measuring collector current

6.2.3.3 Circuit description

V_{CC} and V_{GG} are the voltage supply. R_1 is a circuit protection resistor.

6.2.3.4 Test procedure

The temperature (T_a or T_c) and the gate-emitter voltage are set and kept to the specified values. The supply voltage (V_{CC}) is increased until I_C reaches the specified value. The thermal equilibrium might be reached.

6.2.3.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c

– Collector current I_C

– Gate-emitter voltage V_{GE}

6.2.4 Maximum peak collector current (I_{CM})

6.2.4.1 Purpose

To verify that the peak collector current capability of an IGBT is not less than the maximum rated value I_{CM} under specified conditions.

6.2.4.2 Circuit diagram (see Figure 4)

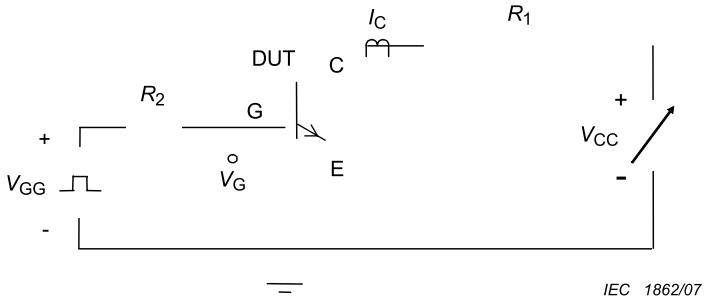


Figure 4 – Circuit for measuring peak collector current

6.2.4.3 Circuit description

V_{CC} is the voltage supply and V_{GG} is the gate pulse generator. R_1 is a circuit protection resistor.

6.2.4.4 Test procedure

The temperature (T_a or T_c or T_{vj}) and the gate-emitter voltage are set and kept at the specified values. The supply voltage (V_{cc}) is increased until I_C reaches the specified value.

6.2.4.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}

– Collector current I_{CM}

– Gate emitter voltage, pulse width and duty cycle

6.2.5 Maximum reverse biased safe operating area (RBSOA)

6.2.5.1 Purpose

To verify that the IGBT operates reliably without failure in RBSOA.

6.2.5.2 Circuit diagram and waveforms (see Figure 5 and Figure 6)

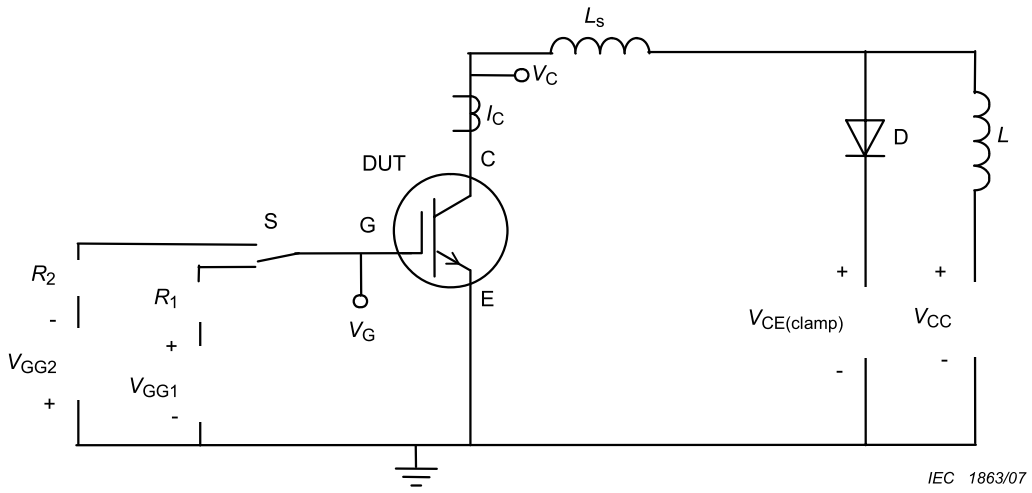


Figure 5 – Test circuit of reverse safe operating area (RBSOA)

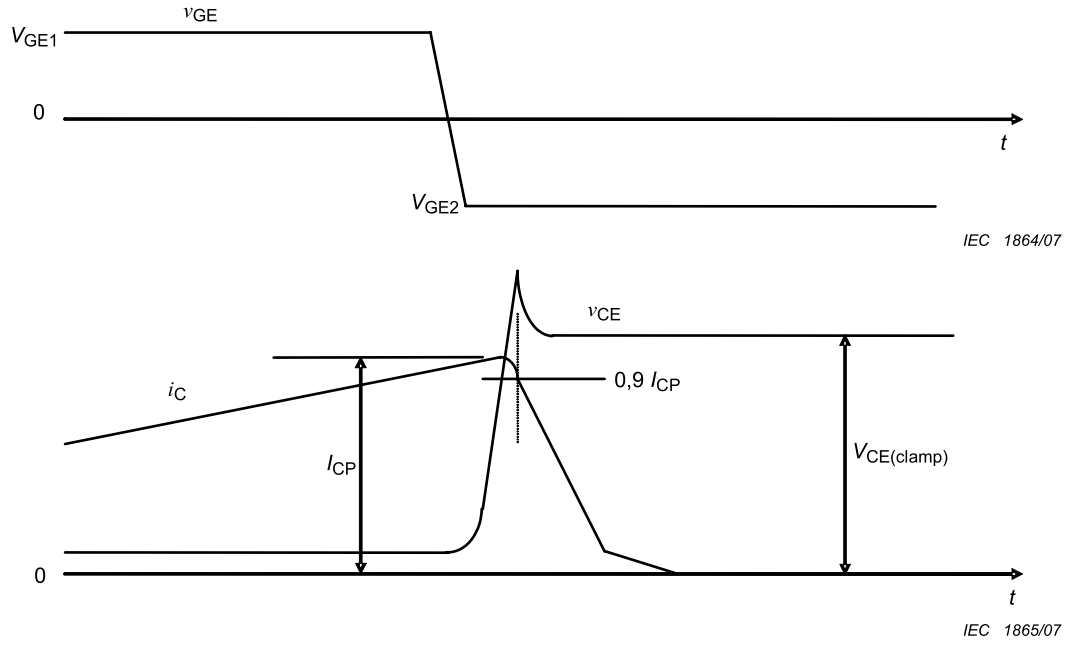


Figure 6 – Waveforms of gate-emitter voltage V_{GE} and collector current I_C during turn-off

6.2.5.3 Circuit description and requirements

The value of load inductance L shall be high enough to maintain the specified I_C and $V_{CE(clamp)}$ to the DUT for least the whole duration of the fall and tail time. V_{CC} is a low voltage to supply the on-state collector current I_C. $V_{CE(clamp)}$ must be capable of carrying a reverse current equal to I_C, while maintaining the specified voltage. Alternatively, a single voltage source capable of supplying the special I_C at the specified V_{CE} and with diode D in parallel with inductor L may be used. R_1 and R_2 are circuit protection resistors. L_s is an inductor representing the maximum permitted unclamped stray inductance.

6.2.5.4 Test procedure

DUT is turned off at specified I_C.

V_{CE} and I_C are monitored. The DUT has to turn off I_C and withstand $V_{CE} = V_{CE(clamp)}$.

NOTE Collector-emitter peak voltage $V_{CEM} < V_{(BR)CE*}$.

6.2.5.5 Specified conditions

– Collector current I_C
– Gate emitter voltage V_{GE1} and V_{GE2}
– Collector-emitter voltage $V_{CE(clamp)}$
– Single-pulse or repetition rate
– Inductance L
– Value of unclamped stray inductance L_s
– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}
– Gate resistor R_1, R_2

6.2.6 Maximum short-circuit safe operating area (SCSOA)

6.2.6.1 Purpose

To verify that the IGBT operates reliably without failure during a load short-circuit condition. Two types of load short circuit can occur. The first one is to switch the IGBT on to an existing load short circuit. Another one is when the IGBT is already in the on-state $V_{CE} = V_{CEsat}$, and then the load short circuit occurs. Both methods must be applied.

6.2.6.2 Maximum short-circuit safe operating area 1 (SCSOA1)

6.2.6.2.1 Circuit diagram and waveforms (see Figure 7 and Figure 8)

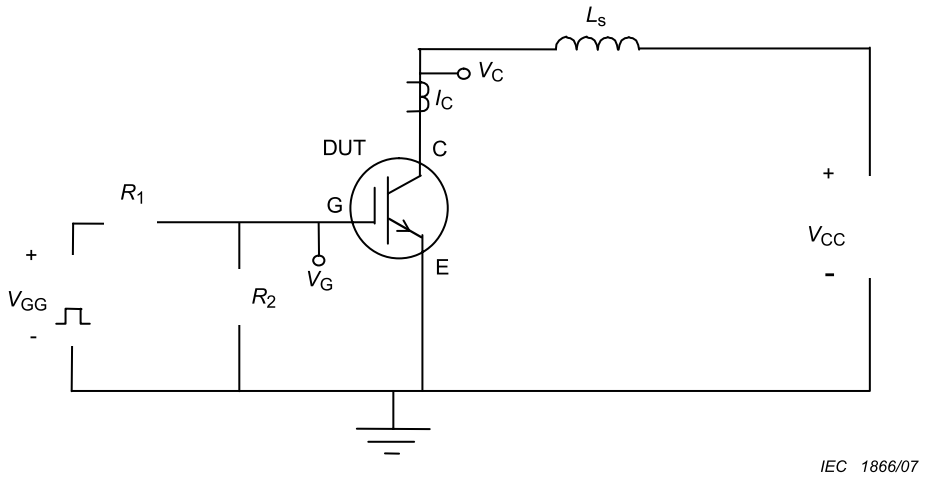


Figure 7 – Circuit for testing safe operating pulse width at load short circuit (SCSOA1)

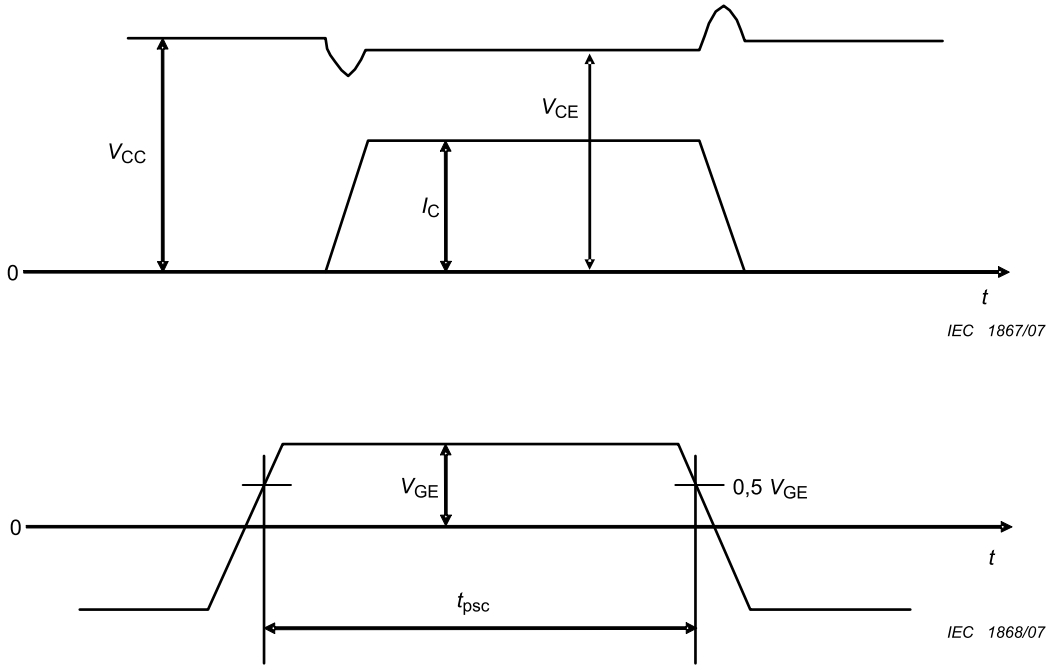


Figure 8 – Waveforms of gate-emitter voltage V_{GE}, collector current I_C and voltage V_{CE} during load short-circuit condition SCSOA1

6.2.6.2.2 Circuit description

L_s represents the maximum permitted stray inductance, it must be low enough to ensure that maximum short-circuit current is reached within the first 25 % of the gate pulse width t_{psc}.

6.2.6.2.3 Test procedure

Set the temperature to the specified value. Apply the specified off-state gate-emitter voltage. Set the collector-emitter voltage to the specified value. Apply the specified gate-emitter on-state pulse. I_C, V_{CE} and V_{GE} are monitored in order to see whether the IGBT turns on and off correctly.

6.2.6.2.4 Specified conditions

– Collector-emitter voltage $V_{CE} = V_{CC}$
– On and off-state gate-emitter voltage V_{GE}
– Gate pulse width t_{psc}
– Gate resistors R_1, R_2
– Value of stray inductance L_s
– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}

6.2.6.3 Maximum short-circuit safe operating area 2 (SCSOA2)

6.2.6.3.1 Features of the operation

The gate voltage increases from the gate-emitter voltage V_{GE} by the dv_{CE}/dt of the collector-emitter voltage V_{CE}. It induces the fast increase of the collector current and high peak energy, as shown in Figure 10.

6.2.6.3.2 Circuit diagram and operating waveforms (see Figure 9 and Figure 10)

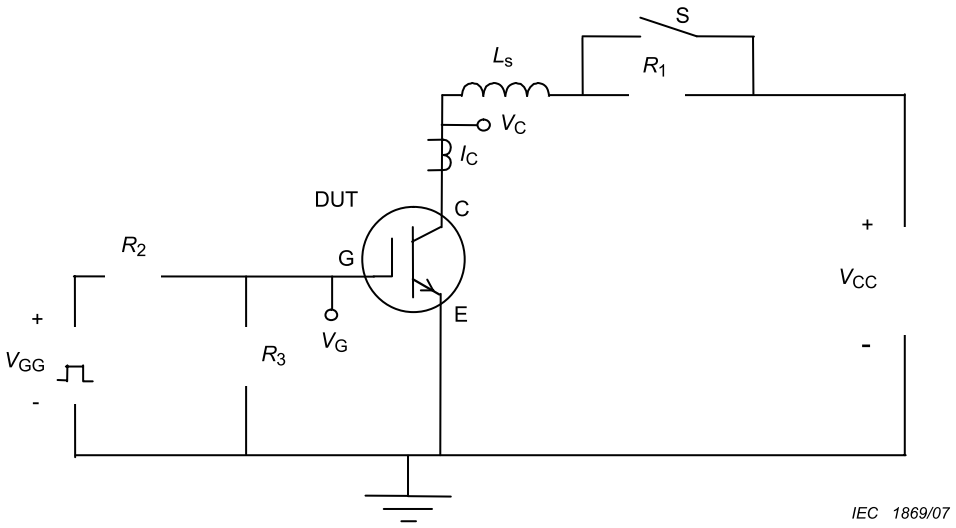


Figure 9 – Short-circuit safe operating area 2 (SCSOA2)

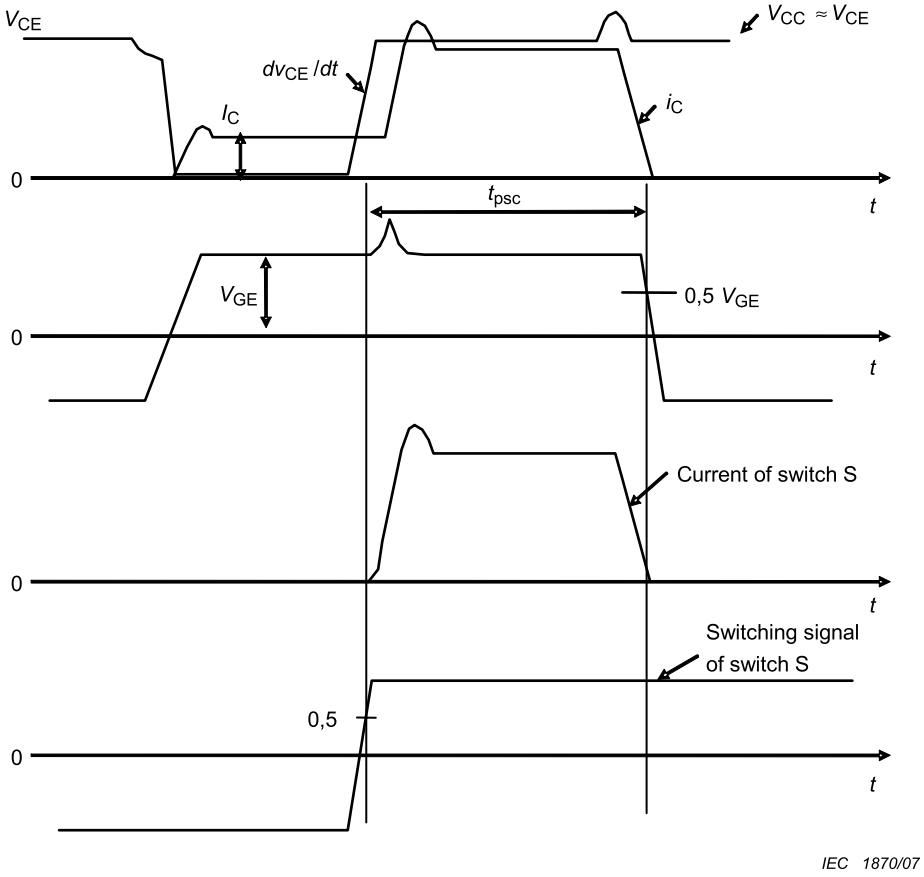


Figure 10 – Waveforms during SCSOA2

6.2.6.3.3 Circuit description

L_S is an inductor representing the maximum permitted unclamped stray inductance. Switch S in the circuit should have much lower impedance compared to the device under test (DUT). The type name or characteristics of switch S should be specified.

6.2.6.3.4 Test procedure

Set the temperature to the specified value. Apply the specified off-state gate-emitter voltage. Set the collector-emitter voltage to the specified value. Apply the specified gate-emitter on-state pulse. The current capability of switch S should be substantially larger than the expected short-circuit current of the DUT. I_C, V_{CE}, V_{GE} and the switching signal of the switch S are monitored in order to see whether the IGBT turns on and off correctly.

6.2.6.3.5 Specified conditions

– Collector current prior to short circuit I_C (= Vcc / R_1)
– Collector-emitter voltage $V_{CE} \approx V_{CC}$
– On and off-state gate-emitter voltage V_{GE}
– Gate pulse width t_{psc}
– Gate resistors R_2, R_3
– Value of unclamped stray inductance L_s
– Type name or characteristics of switch S, if restrictive
– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}

6.3 Methods of measurement

6.3.1 Collector-emitter sustaining voltage (V_{CE*sus})

6.3.1.1 Purpose

The purpose is to ensure that the collector-emitter sustaining voltage of an IGBT is not less than the maximum specified value V_{CE*sus} under specified conditions.

6.3.1.2 Circuit diagram (see Figure 11)

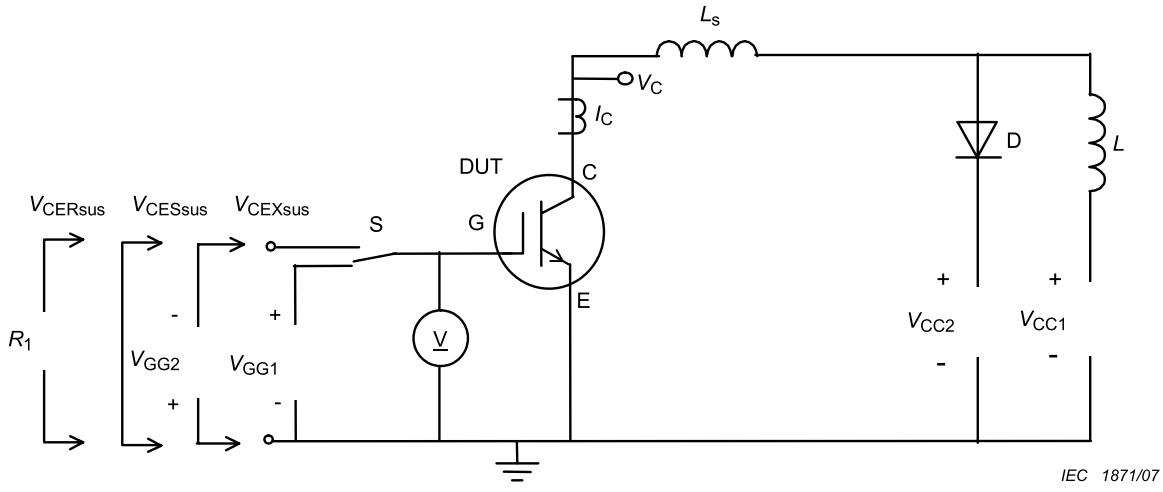


Figure 11 – Circuit for measuring the collector-emitter sustaining voltage V_{CE*sus}

6.3.1.3 Circuit description and requirements

The IGBT is operated in a saturated condition under pulse operation.

Due to the inductance L, switching off the gate voltage causes the IGBT to be swept through a current-voltage cycle.

The voltage source V_{CC1} is adjustable; it enables the collector current to be set to the specified value.

A voltage clamping unit, indicated in Figure 11 as a variable voltage source V_{CC2} in series with a diode, limits the voltage V_{CE}. V_{CC2} is set to the expected value of V_{CE*sus}.

The minimum value of load inductance L may be given in the detail specification; otherwise, it may be calculated from

$$L_{min} = (V_{CC2} - V_{CC1}) * t_{off} / 0{,}1\ I_C$$

This ensures that I_C does not drop by more than 10 % during t_{off}.

6.3.1.4 Test procedure

The clamping unit is adjusted to operate at the specified minimum value V_{CE*sus}. With voltage V_{CC1} set at zero, V_{GE} is adjusted so that the specified current I_C can be reached with a V_{CE} value in the saturated condition (point A in Figure 12).

The value V_{CC1} is progressively increased until the specified current I_C is reached for the expected V_{CE*sus} (point B in Figure 12). As a result, the current at which the cycle starts may reach a value I_0 slightly higher than the specified current I_C (point A′ of Figure 12).

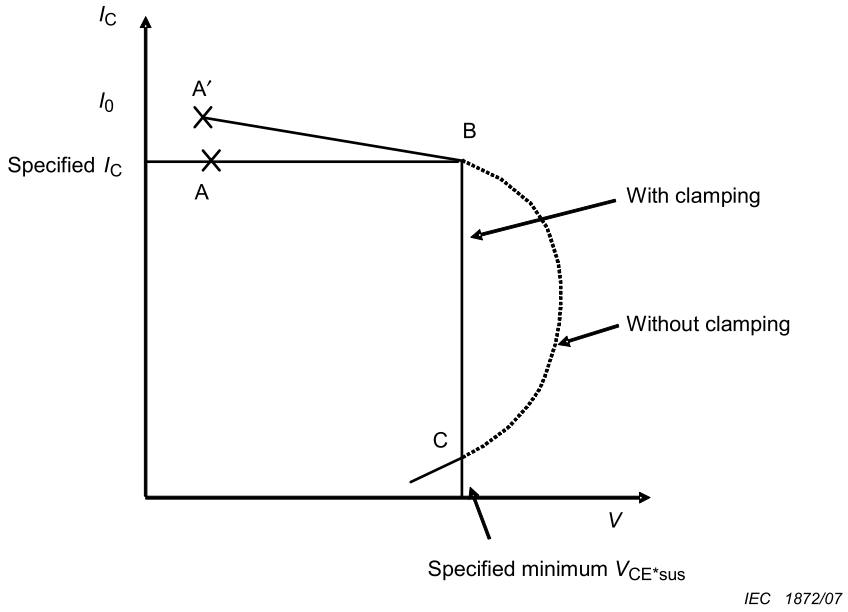


Figure 12 – Operating locus of the collector current

6.3.1.5 Precautions to be observed

In a preliminary test, the action of the clamping unit should be verified by decreasing its adjustable voltage V_2; then the clamping unit should be adjusted to the desired value of V_{CE} that corresponds to the specified current I_C (point B of Figure 12).

6.3.1.6 Requirements

– The IGBT is satisfactory when the trace moving from point B to point C does not pass to the left of the line BC.

– When the clamping unit is not used, the IGBT is satisfactory if the trace effectively turns around point B, as shown in Figure 12.

6.3.1.7 Specified conditions

– Case or ambient or virtual junction temperature T_c or T_a or T_{vj}

– Collector current I_C

– Minimum sustaining voltage V_{CERsus}, V_{CESsus}
– Value of load inductance L, where appropriate
– Value of unclamped stray inductance L_s
– Frequency of the gate voltage pulse generator V_G, if different from 50 Hz
– Gate resistor R_1, R_2, if available
– Gate voltage V_{GG1} and V_{GG2} (shall be specified)

6.3.2 Collector-emitter saturation voltage (V_{CEsat})

6.3.2.1 Purpose

To measure the collector-emitter saturation voltage of an IGBT under specified conditions.

6.3.2.2 Circuit diagram (see Figure 13)

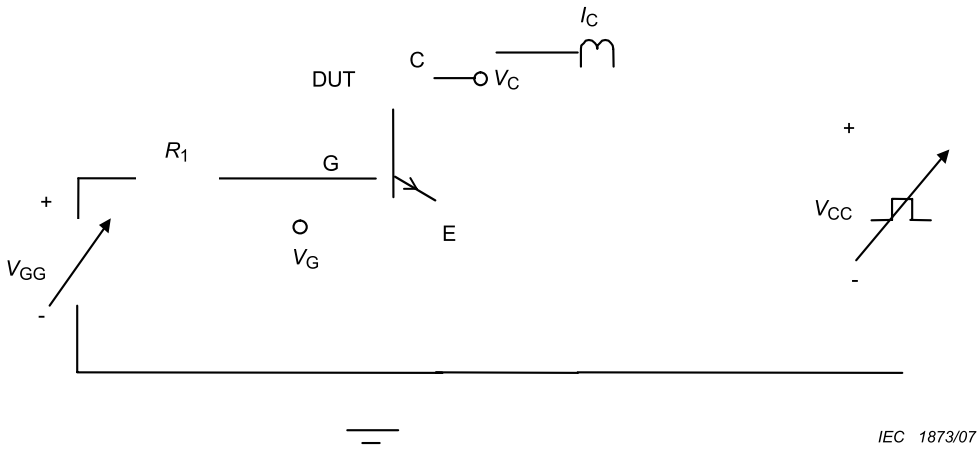


Figure 13 – Circuit for measuring the collector-emitter saturation voltage V_{CEsat}

6.3.2.3 Circuit description

V_{GG} is the voltage supply. The source V_{CC} provides short collector current pulses, without any significant heat specified.

6.3.2.4 Precautions

No significant heat dissipation shall occur in the IGBT during the measurement.

6.3.2.5 Measurement procedure

The temperature is set to the specified value, adapted to the specified values in the gate-emitter voltage and the collector current. The collector-emitter saturation voltage $V_{CE} = V_{CEsat}$ is measured.

6.3.2.6 Specified conditions

– Ambient or case or virtual junction temperature T_{vj}
– Gate-emitter voltage V_{GE}
– Collector current I_C

6.3.3 Gate-emitter threshold voltage ($V_{GE(th)}$)

6.3.3.1 Purpose

To measure the gate-emitter threshold voltage of an IGBT under specified conditions.

6.3.3.2 Circuit diagram (see Figure 14)

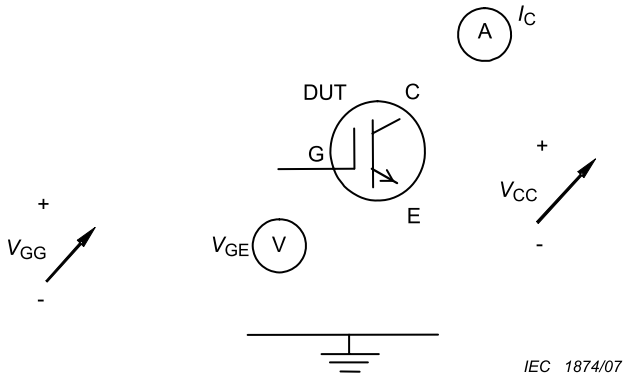


Figure 14 – Basic circuit for measuring the gate-emitter threshold voltage

6.3.3.3 Circuit description

V_{CC} and V_{GG} are the voltage supply.

6.3.3.4 Measurement procedure

The device temperature and the collector-emitter voltage are set to the specified value. The gate-emitter voltage V_{GE} is increased until the specified collector current I_C is reached. The gate-emitter voltage at this current is measured.

6.3.3.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}

– Collector-emitter voltage V_{CE}

– Collector current I_C

6.3.4 Collector cut-off current (I_{CES}, I_{CER}, I_{CEX})

6.3.4.1 Purpose

To measure the collector cut-off current of an IGBT under specified conditions.

6.3.4.2 Circuit diagram (see Figure 15)

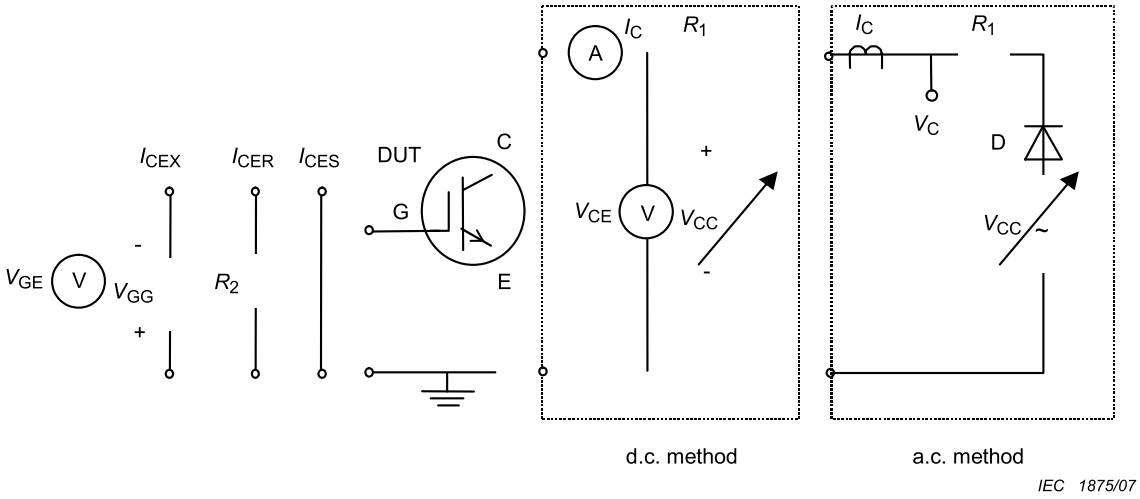


Figure 15 – Circuit for measuring the collector cut-off current

6.3.4.3 Circuit description

V_{CC} and V_{GG} are the voltage supply. R_1 is a circuit protection resistor.

6.3.4.4 Measurement procedure

There are two methods, i.e. the d.c. method and the a.c. method, as shown in Figure 15. The temperature is set to the specified value. The voltage V_{CE} is increased until it reaches the specified value. The cut-off currents I_{CEX}, I_{CER}, I_{CES} are read on the ampere meter or the current probe.

6.3.4.5 Specified conditions

– V_{CC} in a.c. method with a frequency of 50 Hz or 60 Hz unless otherwise specified
– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}
– Collector-emitter voltage V_{CE}
– I_{CER}: resistor R_2 connected between gate and emitter
– I_{CES}: short circuit between gate and emitter
– I_{CEX}: gate emitter voltage

6.3.5 Gate leakage current (I_{GES})

6.3.5.1 Purpose

To measure the gate-emitter leakage current of an IGBT with the collector emitter short circuited.

6.3.5.2 Circuit diagram (see Figure 16)

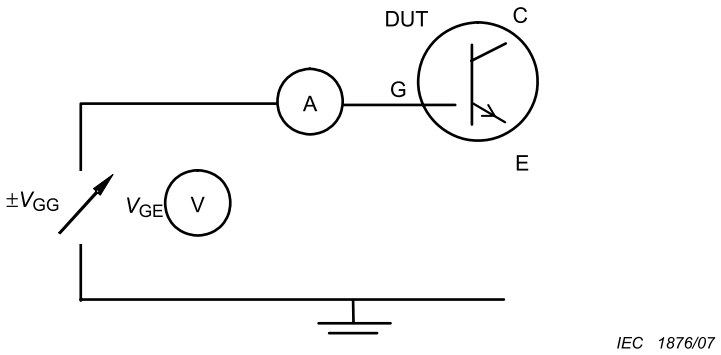


Figure 16 – Circuit for measuring the gate leakage current

6.3.5.3 Circuit description

V_{GG} is the voltage supply.

6.3.5.4 Measurement procedure

Collector and emitter terminals are shorted. The gate-emitter voltage is set to the specified value. The gate-emitter leakage current is measured.

6.3.5.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}

– Gate-emitter voltage V_{GE}

6.3.6 Input capacitance (C_{ies})

6.3.6.1 Purpose

To measure the input capacitance of an IGBT under specified conditions.

6.3.6.2 Circuit diagram (see Figure 17)

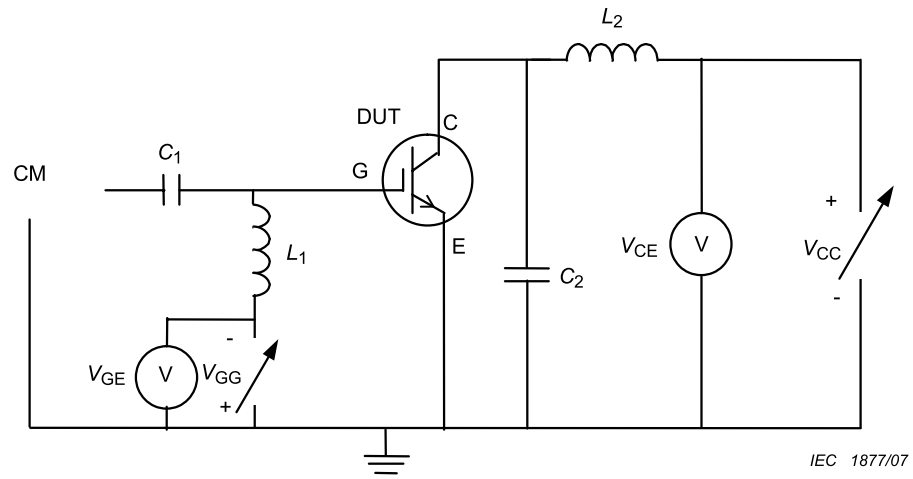


Figure 17 – Circuit for measuring the input capacitance

6.3.6.3 Circuit description and requirements

CM is a capacitance meter. V_{CC} and V_{GG} are adjustable d.c. supplies. Capacitances C_1 and C_2 should present short circuit at the measurement frequency, inductance L_1 and L_2 are to decouple the measurement signal from the d.c. supplies, satisfying the following conditions:

$$1/\omega L_1 \ll |y_{ie}| \text{ and } \omega C_1 \gg |y_{ie}|$$
$$1/\omega L_2 \ll |y_{oe}| \text{ and } \omega C_2 \gg |y_{oe}|$$

6.3.6.4 Measurement procedure

CM is set to the specified frequency without the IGBT. The IGBT is inserted into the test socket. The temperature is set to the specified value. The gate-emitter voltage V_{GE} and the collector-emitter voltage V_{CE} are set to their specified values. Capacitance C_{ies} can be read on CM.

6.3.6.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}

– Collector-emitter voltage V_{CE}

– Gate-emitter voltage V_{GE}

– Measurement frequency

6.3.7 Output capacitance (C_{oes})

6.3.7.1 Purpose

To measure the output capacitance of an IGBT under specified conditions.

6.3.7.2 Circuit diagram (see Figure 18)

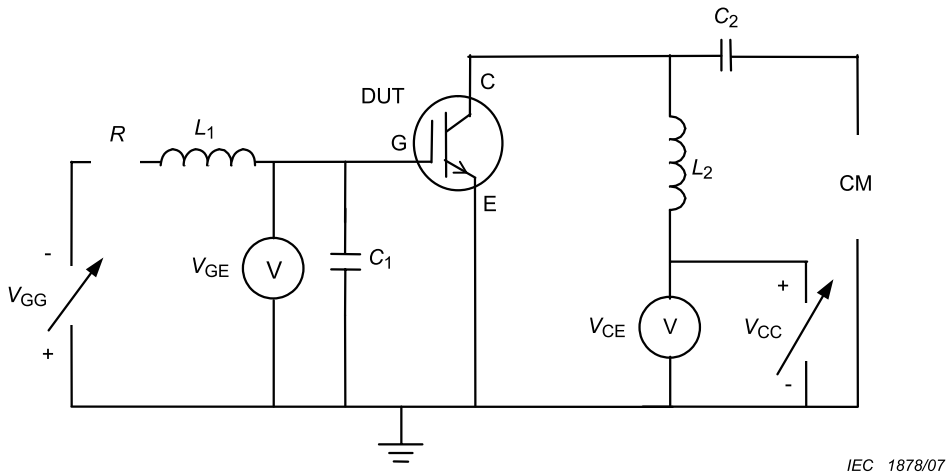


Figure 18 – Circuit for measuring the output capacitance

6.3.7.3 Circuit description and requirement

CM is a capacitance meter. V_{CC} and V_{GG} are adjustable d.c. supplies. Capacitances C_1 and C_2 should present short circuit at the measurement frequency, inductance L_1 and L_2 are to decouple the measurement signal from the d.c. supplies, satisfying the following conditions:

$$1/\omega L_1 \ll |y_{ie}| \quad \text{and} \quad \omega C_1 \gg |y_{ie}|$$
$$1/\omega L_2 \ll |y_{oe}| \quad \text{and} \quad \omega C_2 \gg |y_{oe}|$$

6.3.7.4 Measurement procedure

CM is set to the specified frequency without the IGBT. The IGBT is inserted into the test socket. The temperature is set to the specified value. The gate-emitter voltage V_{GE} and the collector-emitter voltage V_{CE} are set to their specified values respectively. Capacitance C_{oes} can be read on CM.

6.3.7.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}

– Collector-emitter voltage V_{CE}

– Gate-emitter voltage V_{GE}

– Measurement frequency

6.3.8 Reverse transfer capacitance (C_{res})

6.3.8.1 Purpose

To measure the reverse transfer capacitance of an IGBT under specified conditions.

6.3.8.2 Circuit diagram (see Figure 19)

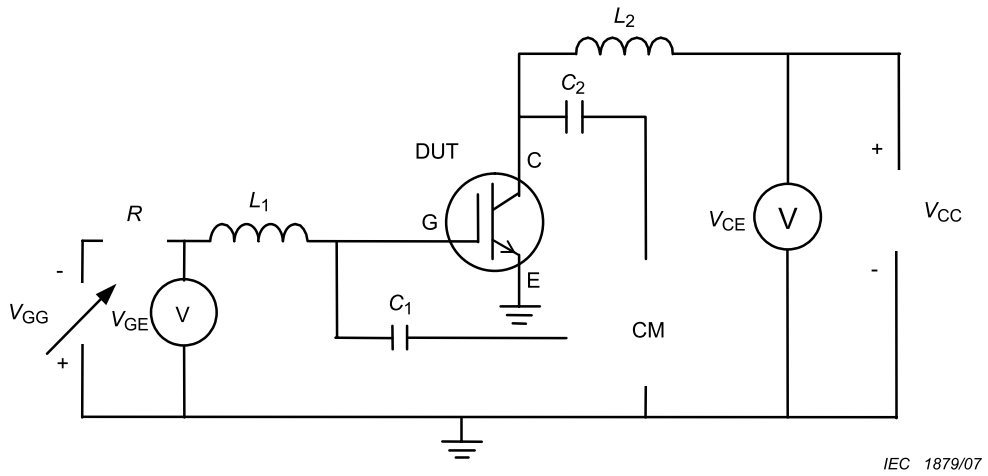


Figure 19 – Circuit for measuring the reverse transfer capacitance

6.3.8.3 Circuit description and requirement

CM is a capacitance meter. Capacitances C_1 and C_2 must form an adequate short circuit for the test frequency. R shall not be too high. Inductance L_1 and L_2 are to decouple the measurement signal from the d.c. supplies. V_{GG} and V_{CC} are adjustable d.c. supplies.

6.3.8.4 Measurement procedure

CM is set to the specified frequency without the IGBT. The IGBT is inserted into the test socket. The temperature is set to the specified value. The gate-emitter voltage V_{GE} and the collector-emitter voltage V_{CE} are set to their specified value. Capacitance C_{res} can be read on CM.

6.3.8.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}

– Collector-emitter voltage V_{CE}

– Gate-emitter voltage V_{GE}

– Measurement frequency

6.3.9 Gate charge (Q_G)

6.3.9.1 Purpose

To measure gate charge of an IGBT under specified conditions.

6.3.9.2 Circuit diagram and waveforms (see Figure 20 and Figure 21)

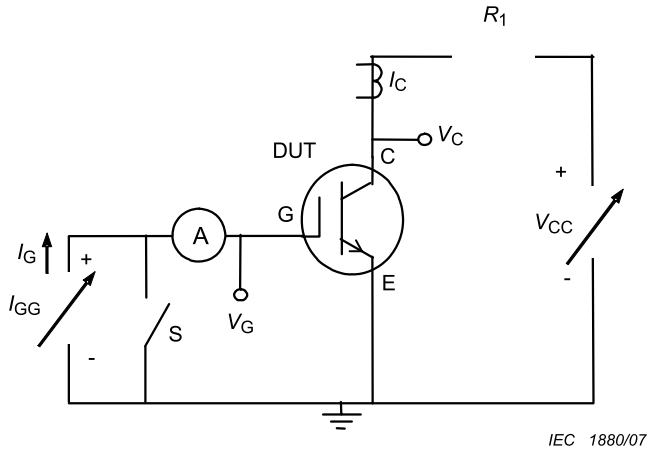


Figure 20 – Circuit for measuring the gate charge

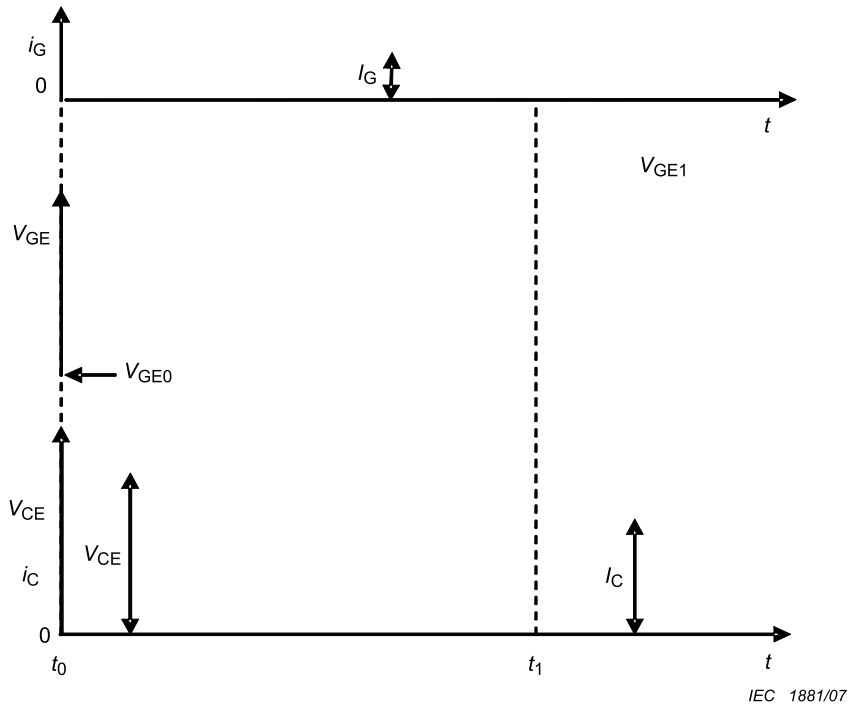


Figure 21 – Basic gate charge waveform

6.3.9.3 Circuit description

V_{CC} is the voltage supply. R_1 is a circuit protection resistor.

6.3.9.4 Test procedure

The gate is fed with a constant current I_{GG} until the specified gate emitter voltage is reached. V_{CE} and V_{GE} are monitored from zero t_0 to t_1. Then, the total gate charge can be calculated as follows:

$$Q_G = \int_{t_0}^{t_1} i_G(t)\, dt = I_G * (t_1 - t_0)$$

6.3.9.5 Specified conditions

– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}

– Collector current I_C

– Collector emitter voltage V_{CE}

– V_{GE0} at t_0 and V_{GE1} at t_1

6.3.10 Internal gate resistance (r_g)

6.3.10.1 Purpose

To measure the internal gate resistance of an IGBT, under specified conditions.

6.3.10.2 Circuit diagram (see Figure 22)

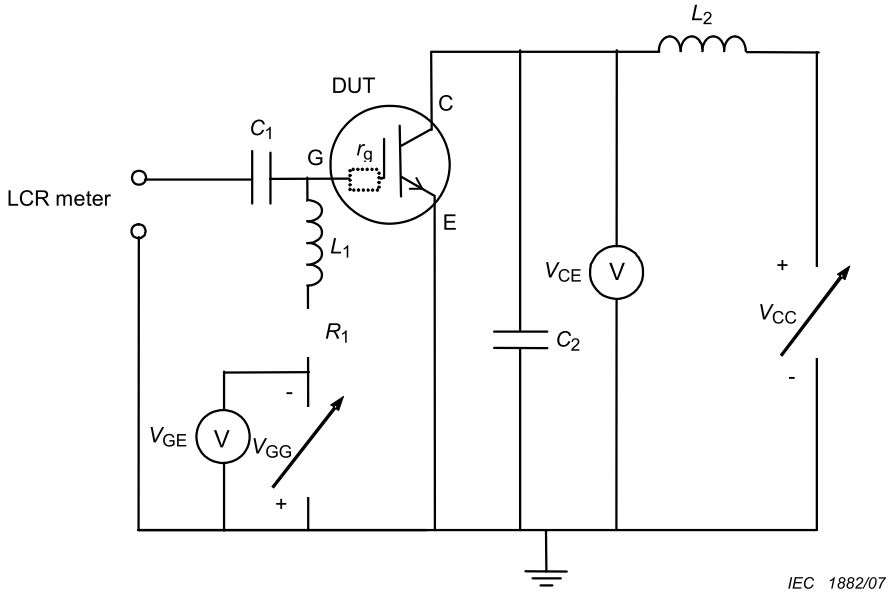


Figure 22 – Circuit for measuring the short-circuit internal gate resistance

6.3.10.3 Circuit description and requirements

A LCR meter is used, thus making it possible to apply a null method. C_2 should be much larger than C_{oes} and ωC_1, much larger than $|y_{ie}|$ at the measurement frequency. The impedance of L_1, L_2 should be sufficiently high, so that it is possible to compensate it by the bridge adjustments.

$$1/\omega L_1 \ll |y_{ie}| \text{ and } |y_{ie}| \gg \omega C_1$$

$$1/\omega L_2 \ll |y_{os}| \text{ and } |y_{os}| \gg \omega C_2$$

6.3.10.4 Measurement procedure

Collector-emitter voltage V_{CE} and gate-emitter voltage V_{GE} of DUT are set to specified values and then internal gate resistance r_g is measured by the LCR meter in series capacitance / resistance mode.

6.3.10.5 Specified conditions

– Collector-emitter voltage V_{CE}

– Gate-emitter voltage V_{GE}

– Measuring frequency f

– Ambient or case or virtual junction temperature T_a or T_c or T_{Vj}

6.3.11 Turn-on times ($t_{d(on)}$, t_r, t_{on}) and turn-on energy (E_{on})

6.3.11.1 Purpose

To measure the turn-on times $t_{d(on)}$, t_r, t_{on} and turn-on energy E_{on} of an IGBT under specified conditions with inductive load.

6.3.11.2 Circuit diagram and waveforms (see Figure 23 and Figure 24)

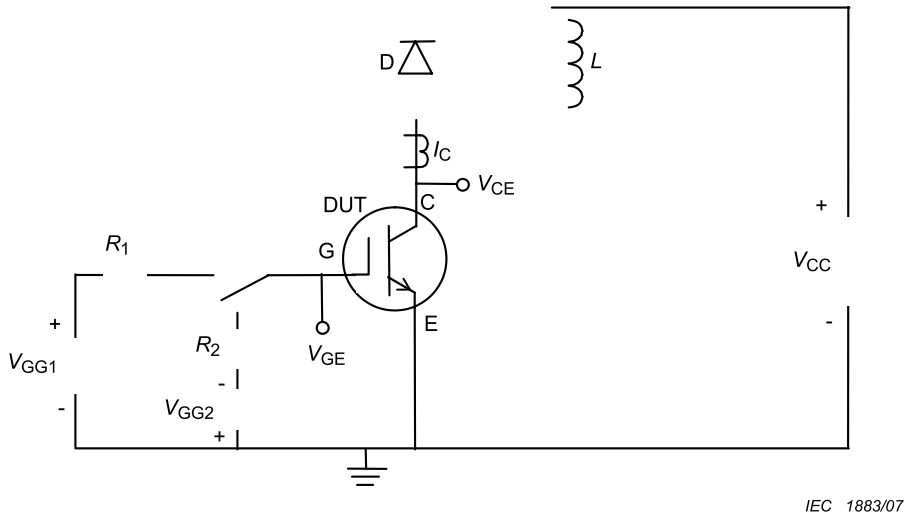


Figure 23 – Circuit for measuring turn-on times and energy

6.3.11.3 Circuit description and requirement

D is a freewheeling diode for the current in the inductance L.

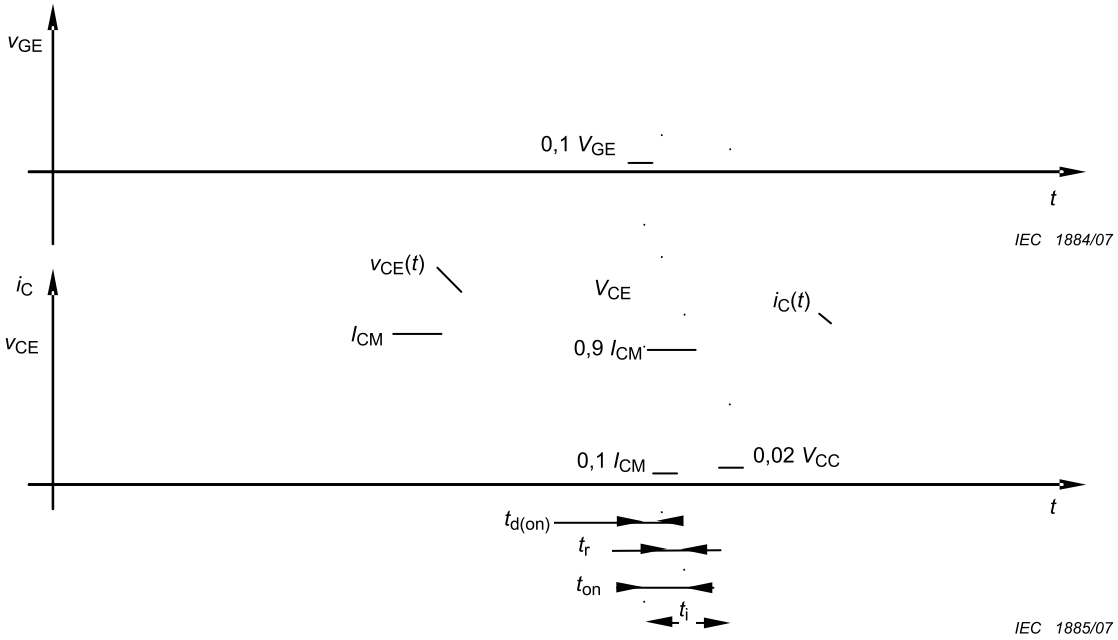


Figure 24 – Waveforms during turn-on times

6.3.11.4 Measurement procedure

The gate voltage level V_{GG1} and V_{GG2} and the supply voltage V_{CC} are set to the specified values. The IGBT is turned on and turned off twice and then the second turn-on is observed. During the first pulse the current is increased to the specified level. The inductance L has to be large enough to keep the current constant during the free wheeling interval. The collector current I_C, the gate voltage V_{GE} and collector-emitter voltage V_{CE} are monitored simultaneously.

E_{on} is the integral of $V_{CE} \times I_C \times dt$. Integral time t_i starts from the 10 % rise point of V_{GE} and ends at the specified low V_{CE} point, the 2 % point of V_{CC}. The turn-on power dissipation is the product of the switching frequency and the turn-on energy per pulse as determined by the integration.

6.3.11.5 Specified conditions

– Case or ambient or virtual junction temperature of the IGBT and the diode
– Voltage of intermediate circuit V_{CC}
– Collector current I_C just before 1st turn-off (I_{CM})
– Gate voltage $-V_{GE}$ before and $+V_{GE}$ after turn-on
– Gate resistor R_1 ($R_{G(on)}$)
– Characteristics of freewheeling diode

NOTE If there is a free wheeling diode in the same package with the IGBT, this type of diode should be used for the measurement.

6.3.12 Turn-off times ($t_{d(off)}$, t_f, t_{off}, t_z) and turn-off energy (E_{off})

6.3.12.1 Purpose

To measure the turn-off times $t_{d(off)}$, t_f, t_{off}, t_z and turn-off energy E_{off} of an IGBT under specified conditions with inductive load.

6.3.12.2 Circuit diagram and waveforms (see Figure 25 and Figure 26)

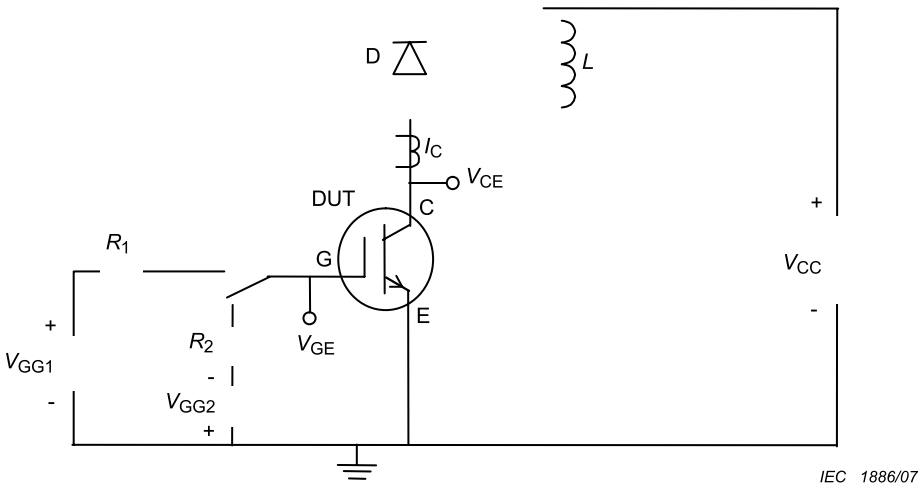


Figure 25 – Circuit for measuring turn-off times and energy

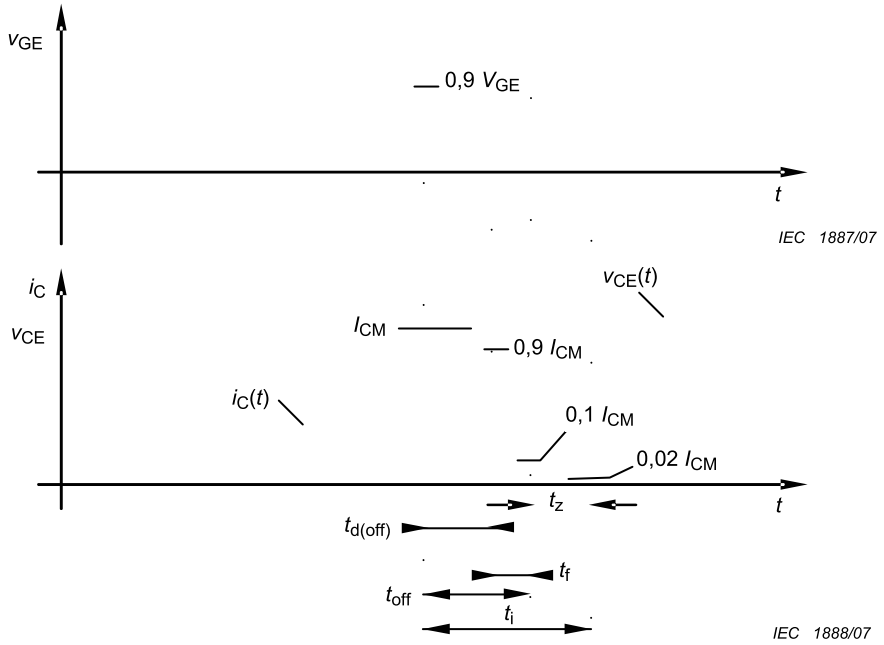


Figure 26 – Waveforms during turn-off times

6.3.12.3 Circuit description and requirement

D is a freewheeling diode for the current in the inductance L.

6.3.12.4 Measurement procedure

The gate voltage level V_{GG1} and V_{GG2} and the supply voltage V_{CC} are set to the specified values. The minimum turn-on pulse duration must ensure a complete saturation of the IGBT. The collector current I_C, the gate emitter voltage V_{GE} and the collector emitter voltage V_{CE} are monitored simultaneously.

E_{off} is the integral of $V_{CE} \times I_C \times dt$. Integral time t_i starts from the 90 % fall point of V_{GE} and ends at the specified low I_C point, the 2 % point of I_C before turn-off. The turn-off power dissipation is the product of the switching frequency and the turn-off energy per pulse as determined by the integration.

6.3.12.5 Specified conditions

– Case or ambient or virtual junction temperature of the IGBT and the diode
– Voltage of intermediate circuit V_{CC}
– Collector current before turn-off (I_{CM})
– Gate voltage $+V_{GE}$ before and $-V_{GE}$ after turn-off
– Gate resistor R_2 ($R_{G(off)}$)

6.3.13 Thermal resistance junction to case ($R_{th(j-c)}$) and transient thermal impedance junction to case ($Z_{th(j-c)}$)

6.3.13.1 Method 1 (using collector emitter voltage at low current as a temperature sensitive parameter)

6.3.13.1.1 Purpose

To measure the thermal resistance junction to case and/or the transient thermal impedance junction to case of an IGBT.

The measurement is made in two steps:

a) determination of the temperature coefficient of the collector-emitter voltage at the low measuring current;
b) measurement of the response of the IGBT to a step change in the internal power dissipation.

6.3.13.1.2 Circuit diagram (see Figure 27)

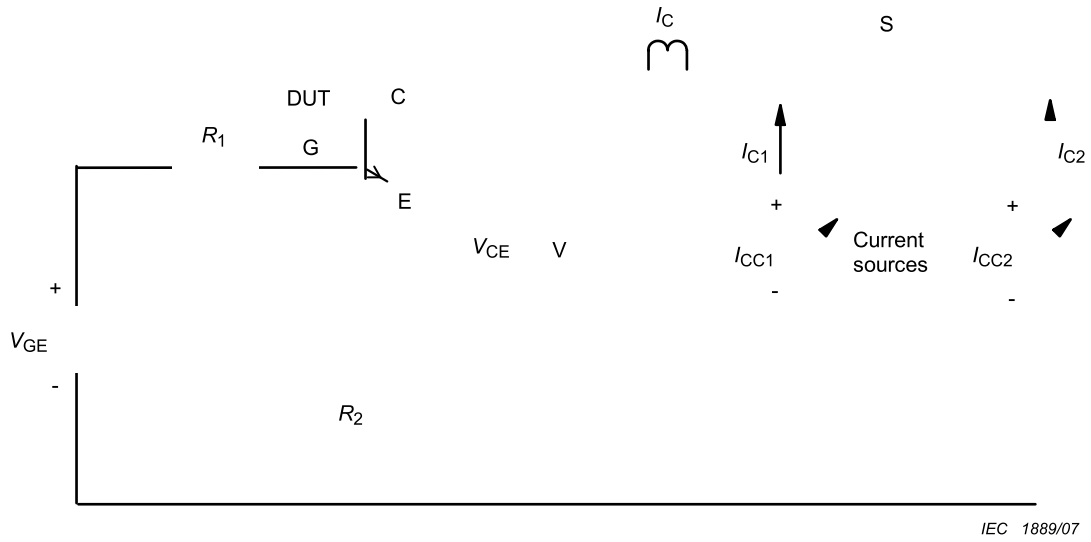


Figure 27 – Circuit for measuring the variation with temperature of the collector-emitter voltage V_{CE} at a low measuring current I_{C1} and for heating up the IGBT by a high current I_{C2}

6.3.13.1.3 Circuit description and requirements

A current source supplies a low continuous direct collector current I_{C1} which is just sufficient to raise the collector-emitter voltage V_{CE} above the saturation value. An electronic power switch S supplies on top of I_{C1} a high collector current I_{C2}. After switching I_{C2} off, the IGBT returns to the I_{C1} conduction. R_2 is a current measuring resistor. In its place, any other appropriate current probe may be used.

6.3.13.1.4 Measurement procedure

a) Determination of the temperature coefficient α_{VCE} of the collector-emitter voltage V_{CE} at the low measuring current I_{C1} (see Figure 28).

The IGBT to be measured is heated subsequently to the temperatures T_1 and T_2 by immersing it in a heated chamber or inert fluid. Thermal equilibrium must be achieved before measurements are taken. At temperature T_1 the collector-emitter voltage at the measuring current I_{C1} is V_{CE1}. At a higher temperature T_2 it is V_{CE2}. Then the temperature coefficient α_{VCE} is:

$$\alpha_{VCE} = \frac{V_{CE1} - V_{CE2}}{T_2 - T_1}$$

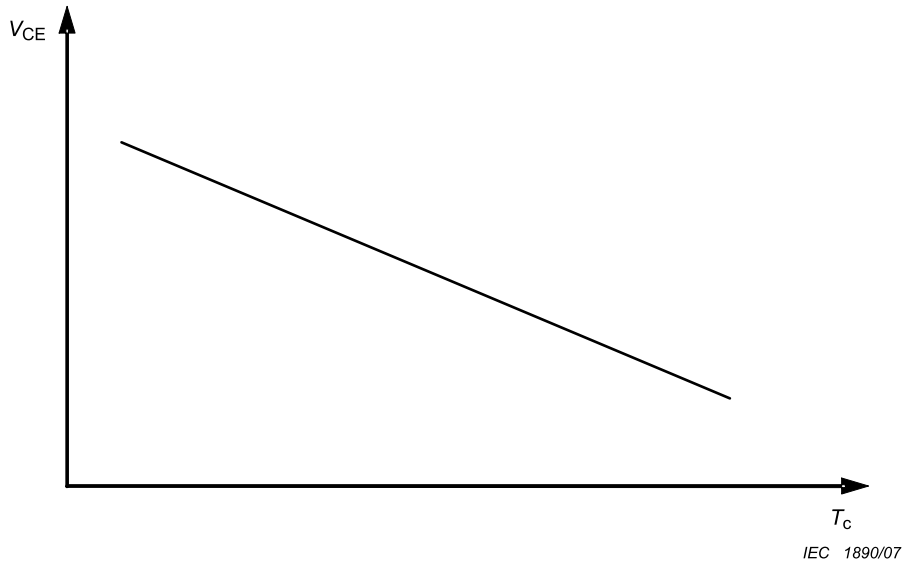


Figure 28 – Typical variation of the collector-emitter voltage V_{CE} at a low measuring current I_{C1} with the case temperature T_c (when heated from outside, i.e. $T_c = T_{vj}$)

b) Measurement of the response to a step change in the internal power dissipation

The IGBT to be measured is fixed on a suitable heatsink. The case temperature T_{c1} is measured. At that temperature, the measuring current produces the collector-emitter voltage V_{CE3}. The power switch S is switched on. The high collector current I_{C2} flows. When thermal equilibrium is established, T_c = const. = T_{c2} and V_{CE} = V_{CE4} are measured. Now I_{C2} is switched off. Immediately after switch-off, the collector-emitter voltage at I_{C1} is measured to be V_{CE5}. Then at that instant

$$T_{vj} = T_{c1} + \frac{V_{CE3} - V_{CE5}}{\alpha_{VCE}}$$

and

$$R_{th(j-c)} = \frac{T_{vj} - T_{c2}}{V_{CE4} * I_{C2}}$$

If the transient thermal impedance $Z_{th(j-c)}$ is to be determined, the variations with time of V_{CE} at I_{C1} and of T_c during the cooling period after switching off I_{C2} are plotted, and the $Z_{th(j-c)}$ values are calculated point by point using the above equations.

6.3.13.1.4.1 Specified conditions

– Reference point for measuring the case temperature

6.3.13.2 Method 2 (using the gate-emitter threshold voltage as a temperature-sensitive parameter)

6.3.13.2.1 Purpose

To measure the thermal resistance junction to case and/or the transient thermal impedance junction to case of an IGBT (method 2)

The measurement is made in two steps:

a) determination of the temperature coefficient of the gate-emitter voltage at the low measuring current ;

b) measurement of the response of the IGBT to a step change in the internal power dissipation.

6.3.13.2.2 Circuit diagram (see Figure 29)

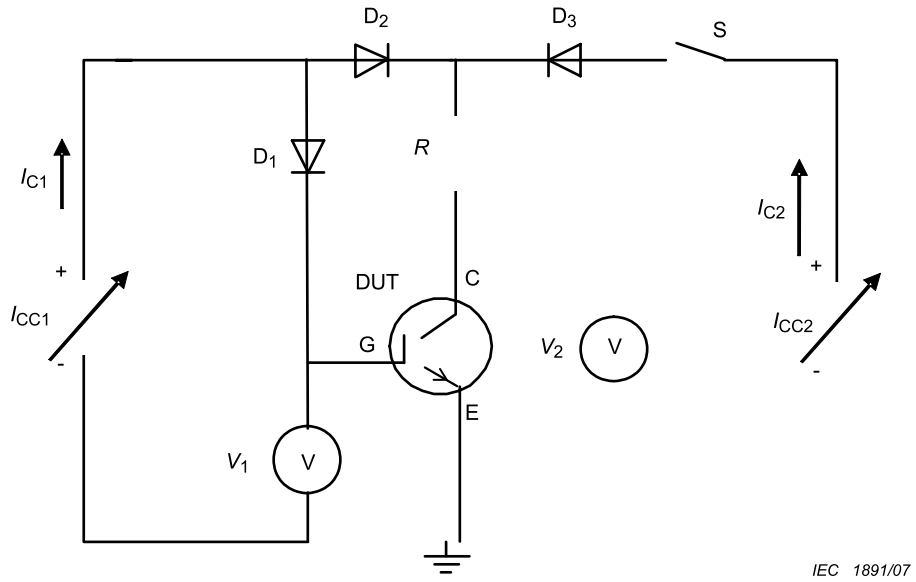


Figure 29 – Circuit for measuring thermal resistance and transient thermal impedance: method 2

6.3.13.2.3 Circuit description and requirements

S is an electronic power switch. I_{CC1} is an adjustable current source which provides a low continuous direct collector current I_{C1} which can make the gate-emitter voltage reach the threshold voltage $V_{GE(th)}$ when switch S is opened. I_{CC2} is an adjustable current source which provides a high collector current I_{C2} when switch S is closed. The I_{C2} current shall be high enough to make I_C (I_{C1} + I_{C2}) reach its rating. D_1, D_2 and D_3 are insulation diodes; V_1 and V_2 are d.c. voltage meters. R is the current-measuring resistor. Any other appropriate current probe may be used.

6.3.13.2.4 Measurement procedure

a) Determination of the temperature coefficient c_T of the gate-emitter voltage $V_{GE(th)}$ at the low measuring current I_{C1} (see Figure 30). The IGBT to be measured is heated subsequently to the temperatures T_1 and T_2 ($T_2 > T_1$) by immersing it in a heated chamber or inert fluid. Thermal equilibrium must be achieved before measurements are taken. At temperature T_1, the gate-emitter threshold voltage at the measuring current I_{C1} is $V_{GE(th)1}$. At temperature T_2, it is $V_{GE(th)2}$. Then the temperature coefficient c_T is

$$c_T = \left| \left(V_{GE(th)1} - V_{GE(th)2}\right) / \left(T_2 - T_1\right) \right| \ (V/K)$$

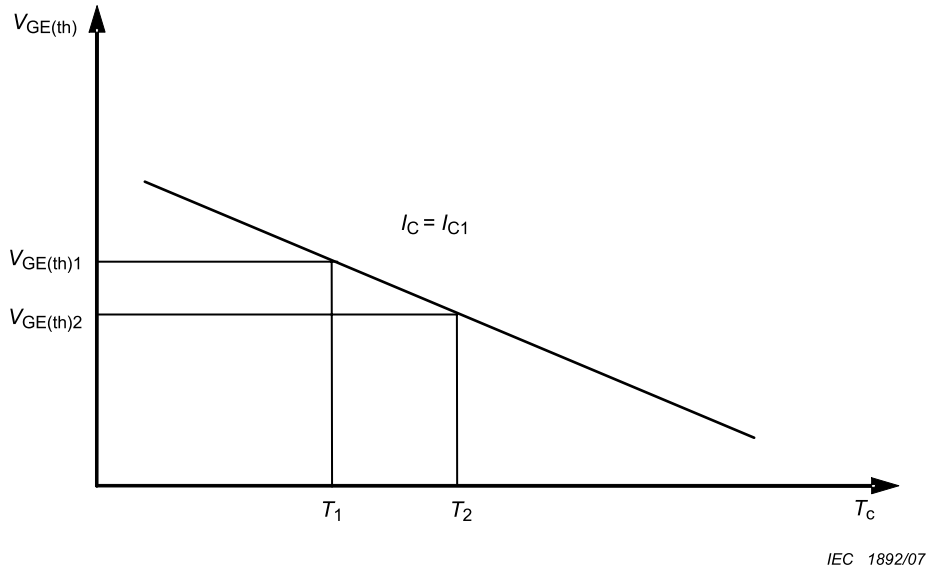


Figure 30 – Typical variation of the gate-emitter threshold voltage $V_{GE(th)}$ at a low measuring current I_{C2} with the case temperature T_c (when heated from the outside, i.e. $T_c = T_{vj}$)

b) Measurement of the response to a step change in the internal power dissipation (see Figure 31)

The IGBT to be measured is fixed on a suitable heat sink. The case temperature T_{c1} is measured. At that temperature, the measuring current I_{C1} produces the gate-emitter threshold voltage $V_{GE(th)3}$. Switch S is switched on, the high collector current I_{C2} flows. When thermal equilibrium is established, T_c = const. = T_{c2} and V_{CE} are measured. I_{C2} is then switched off. Immediately after switch-off, the gate-emitter threshold voltage at I_{C1} is measured to be $V_{GE(th)4}$.

Then,

$$T_{vj} = T_{c1} + (V_{GE(th)3} - V_{GE(th)4}) / cT$$

and

$$R_{th(j\text{-}c)} = (T_{vj} - T_{c2}) / (V_{CE} * I_{C2})$$

If the transient thermal impedance $Z_{th(j\text{-}c)}$ is to be determined, the variations with time of $V_{GE(th)}$ at I_{C1} and of T_c during the cooling period after switching off I_{C2} are plotted, and the $Z_{th(j\text{-}c)}$ values are calculated point by point using the above equations.

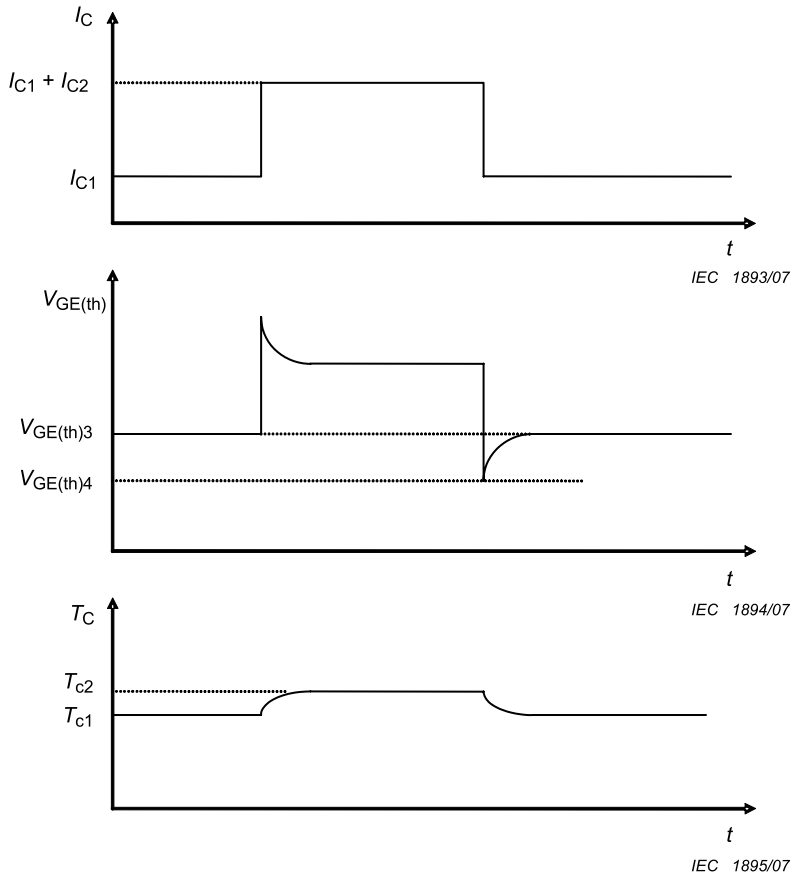


Figure 31 – I_C, V_{GE} and T_c with time

6.3.13.2.5 Specified conditions

– Reference point for measuring the case temperature

7 Acceptance and reliability

7.1 General requirements

Subclause 7.2 of IEC 60747-1 is valid.

The testing times of the endurance tests should be introduced in the data sheet.

7.2 Specific requirements

7.2.1 List of endurance and reliability tests

A choice of endurance tests is given in Figures 32, 33 and 34.

7.2.2 Conditions for endurance and reliability tests

Test conditions and test circuits are described in Figures 32, 33 and 34. The data sheet will state which tests will apply.

7.2.3 Acceptance-defining characteristics and criteria for endurance and reliability tests

Acceptance-defining characteristics, their criteria and measurement conditions are listed in Table 2.

NOTE Characteristics should be measured in the sequence in which they are listed in Table 1, because the changes in characteristics caused by some failure mechanisms may be wholly or partially masked by the influence of other measurements. These characteristics are those given in published data sheets. They may be outside the initial production test limits.

Table 2 – Acceptance-defining characteristics for endurance and reliability tests

Characteristics	Criteria (see note)	Measurement conditions
I_{CES}	< USL	Specified V_{CE}
I_{GES}	< USL	Specified V_{GE}
$V_{GE(th)}$	> LSL < USL	Specified V_{CE} and I_C
V_{CEsat}	< USL	Specified I_C
R_{th}	< USL	Specified I_C
NOTE USL: upper specification limit LSL: lower specification limit		

7.2.4 Procedure in case of a testing error

The results of tests carried out using inaccurate or faulty test equipment shall not be included for the purpose of device assessment.

7.2.5 Endurance and reliability tests and test methods

7.2.5.1 High-temperature blocking (HTRB)

7.2.5.1.1 Operating conditions

– Voltage: preferably 80 % of V_{CESmax} or V_{CEXmax}

– Temperature: preferably maximum virtual junction temperature $T_{vj(max)}$ or $T_c = T_{stg(max)}$ –5 °C as specified

7.2.5.1.2 **Test circuit** (see Figure 32)

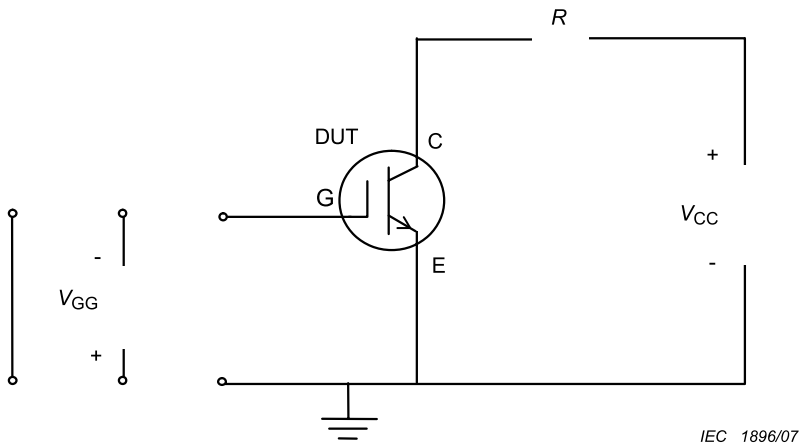


Figure 32 – Circuit for high-temperature blockings

7.2.5.2 High-temperature gate bias

7.2.5.2.1 Operating conditions

– Voltage: preferably 80 % of specified continuous V_{GESmax}

– Temperature: preferably $T_{vj\ (max)}$ or $T_c = T_{stg\ (max)} - 5$ °C

7.2.5.2.2 **Test circuit** (see Figure 33)

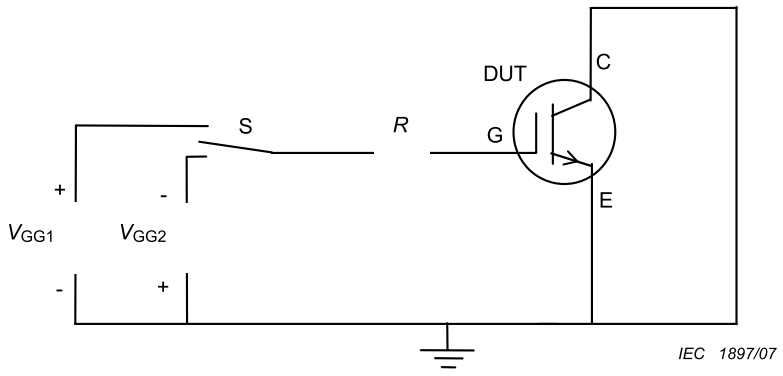


Figure 33 – Circuit for high-temperature gate bias

7.2.5.3 Intermittent operating life (load cycles)

7.2.5.3.1 Operating conditions

– Current: specified value

– Temperature: ΔT_{vj} as specified

– Gate voltage $V_{GE:}$ specified value

– Case temperature

Method 1: T_c = constant

Method 2: T_c = variable with T_{vj}

– On-time t_p and off-time ($t_c - t_p$) specified

NOTE Mechanical stress in the device under test by method 1 concentrates on the wire-bonded emitter portions of dies of the module type devices. Mechanical stress in the device under test by method 2 concentrates mainly on the soldering material portion or the pressure contact portion of dies of the devices.

7.2.5.3.2 **Test circuits** (see Figure 34 and Figure 35)

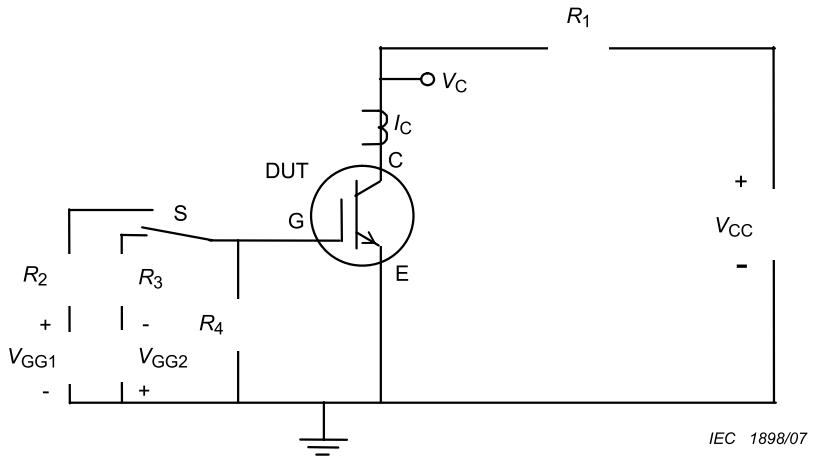


Figure 34 – Circuit for intermittent operating life

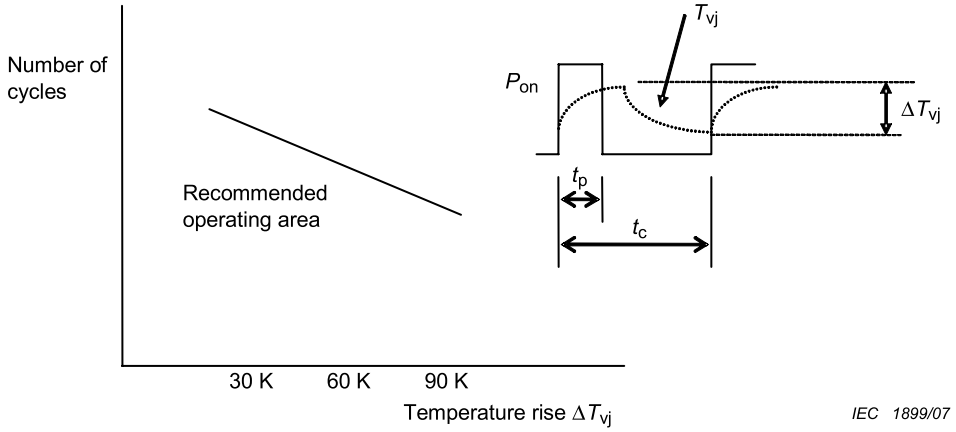


Figure 35 – Expected number of cycles versus temperature rise ΔT_{vj}

7.3 Type tests and routine tests

7.3.1 Type tests

Type tests are carried out on new products on a sample basis, in order to confirm the electrical and thermal ratings (limiting values) and characteristics to be given in the data sheet and to be referenced to the test limits for future routine tests.

Some or all of the type tests may be repeated from time to time on samples drawn from current production or deliveries, so as to confirm that the quality of the product continuously meets the specified requirements.

The minimum items of type tests to be carried out on IGBTs are listed in Table 3. Some of the type tests are destructive.

7.3.2 Routine tests

The routine tests are carried out on the current production or deliveries normally on a 100 % basis, in order to verify that the ratings (limiting values) and characteristics specified in the data sheet are met by each specimen.

Routine tests may comprise distribution of the devices into groups.

The minimum items of routine tests to be carried out on IGBTs are listed in Table 3, unless otherwise agreed between supplier and purchaser.

Table 3 – Minimum type and routine tests for IGBTs when applicable

Subclause	Testing of ratings	Type test	Routine test
6.2.1	Collector-emitter voltages (V_{CES}, V_{CER}, V_{CEX})	X	X
6.2.2	Gate-emitter voltage ($\pm V_{GES}$)	X	
6.2.3	Collector current (I_C)	X	
6.2.4	Peak collector current (I_{CM})	X	
6.2.5	Reverse biased safe operating area (RBSOA)	X	
6.2.6	Short-circuit safe operating area (SCSOA)	X	
Measurement of characteristics			
6.3.1	Collector-emitter sustaining voltage (V_{CE*sus})	X	
6.3.2	Collector-emitter saturation voltage (V_{CEsat})	X	X
6.3.3	Gate-emitter threshold voltage ($V_{GE(th)}$)	X	X
6.3.4	Collector-emitter cut-off current (I_{CES}, I_{CER}, I_{CEX})	X	X
6.3.5	Gate leakage current (I_{GES})	X	X
6.3.6	Input capacitance (C_{ies})	X	
6.3.7	Output capacitance (C_{oes})	X	
6.3.8	Reverse transfer capacitance (C_{res})	X	
6.3.11	Turn-on intervals ($t_{d(on)}$,t_r,t_{on}) and turn-on energy (E_{on})	X	
6.3.12	Turn-off intervals ($t_{d(off)}$, t_f, t_{off}, t_z) and turn-off energy (E_{off})	X	
6.3.13	Thermal resistance junction to case ($R_{th(j-c)}$) and transient thermal impedance junction to case ($Z_{th(j-c)}$)	X	
Endurance and reliability tests			
7.2.5.1	High-temperature blocking (HTRB)	X	
7.2.5.2	High-temperature gate bias	X	
7.2.5.3	Intermittent operating life (load cycles)	X	

Annex A
(normative)

Measuring method for collector-emitter breakdown voltage

A.0 Introduction

The following test or measurement may exceed the specified ratings. IGBTs under test may be changed in characteristics or destroyed. However, to permit evaluation of limiting values, the test or measurement is presented in this annex. When the information is given in the form of data on characteristics, measurements should be made under the specified limit conditions.

A.1 Purpose

To measure the collector-emitter breakdown voltage which is useful to evaluate change or degradation of IGBTs during endurance tests.

A.2 Circuit diagram (see Figure A.1)

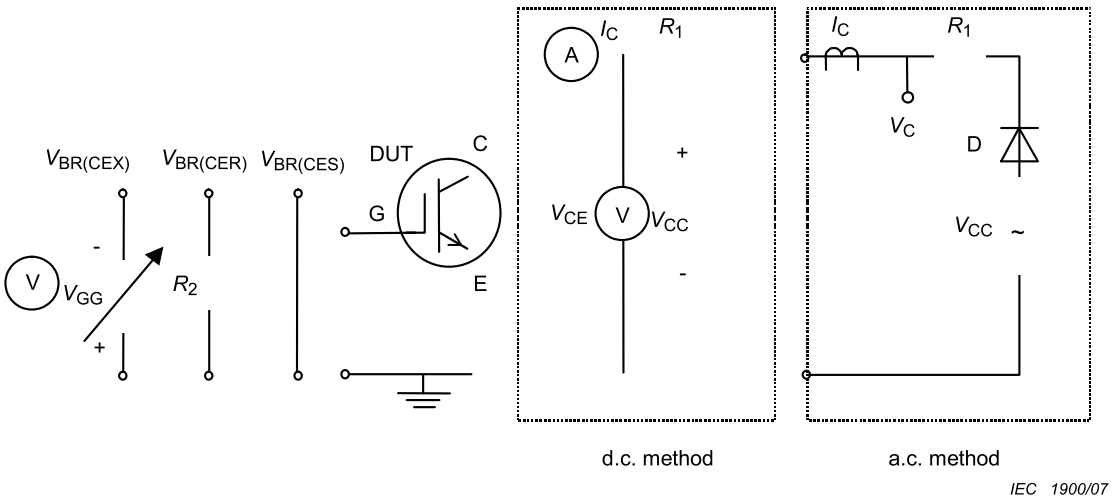


Figure A.1 – Circuit for testing the collector-emitter breakdown voltage

A.3 Measuring procedure

There are two methods, i.e. the d.c. method and the a.c. method, according to the circuit diagrams in Figure A.1. The temperature is set to the specified value. The voltage V_{CE} is increased until the collector current rises steeply with the specified gate-emitter condition and T_a or T_c or T_{vj}. After the above test, confirm the acceptance criteria of the DUT defined in Table 1.

A.4 Specified conditions

– Ambient or case or junction temperature T_a or T_c or T_{vj}
– Gate-emitter bias
– $V_{(BR)CEX}$: gate-emitter voltage V_{GE}
– $V_{(BR)CER}$: resistor R_2 connected between gate and emitter
– $V_{(BR)CES}$: short circuit between gate and emitter

Annex B
(normative)

Measuring method for inductive load turn-off current under specified conditions

B.0 Introduction

The following test or measurement may exceed the specified ratings. IGBTs under test may be changed in characteristics or destroyed. However, to permit evaluation of limiting values, the test or measurement is presented in this annex. When the information is given in the form of data on characteristics, measurements should be made under the specified limit conditions.

B.1 Purpose

To measure the IGBT turn-off current for inductive load under specified conditions.

B.2 Circuit diagram and waveforms (see Figure B.1 and Figure B.2)

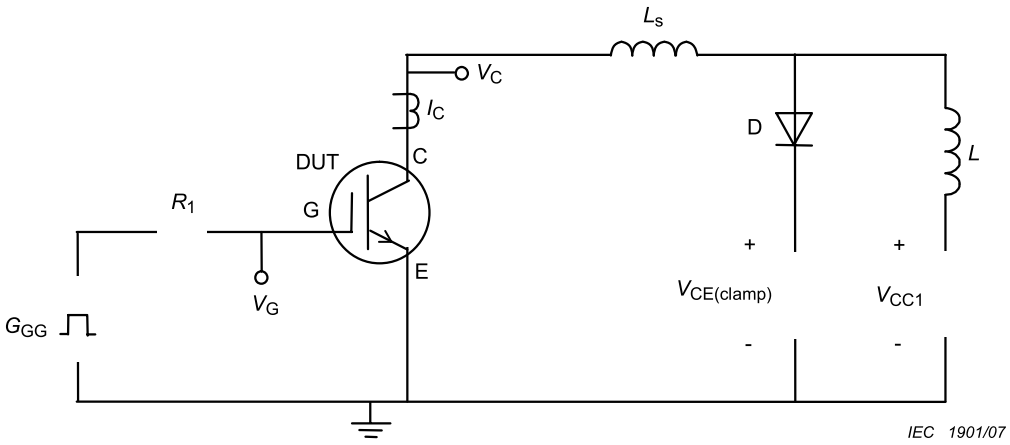


Figure B.1 – Measuring circuit for inductive load turn-off current

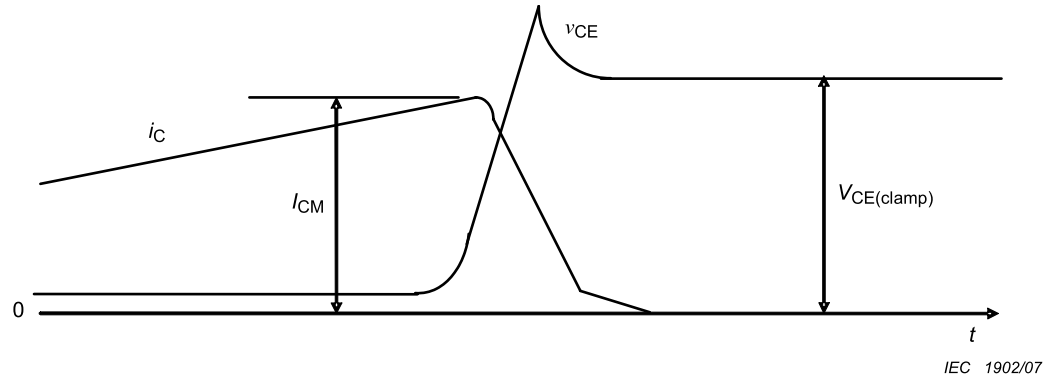


Figure B.2 – Waveforms of collector current I_C and collector voltage V_{CE} during turn-off

B.3 Circuit description and requirements

The value of load inductance L shall be high enough to apply $V_{CE(clamp)}$ to the DUT at least before the beginning of the fall time t_f plus tail time t_z.

B.4 Test procedure

I_C is increased until turn-off failure occurs with the specified V_{CE} value. V_{CE} and I_C are monitored.

B.5 Specified conditions

– Gate reverse voltage $-V_{GE}$
– Collector-emitter voltage $V_{CE(clamp)}$
– Single pulse or repetition rate
– Inductance L
– Ambient or case or junction temperature T_a or T_c or T_{vj}
– Gate resistor R_1
– Value of unclamped stray inductance L_s

NOTE A stray inductance value of the package for big size devices should be taken into consideration.

Annex C
(normative)

Forward biased safe operating area (FBSOA)

C.0 Introduction

The following test or measurement may exceed the specified ratings. IGBTs under test may be changed in characteristics or destroyed. However, to permit evaluation of limiting values, the test or measurement is presented in this annex. When the information is given in the form of data on characteristics, measurements should be made under the specified limit conditions.

C.1 Purpose

FBSOA should only be specified if the device can be used in linear mode. Measure that the IGBT operates reliably without failure in FBSOA for linear applications. There is no requirement of FBSOA for IGBTs in switching applications.

C.2 Method 1

Method 1 is the same as that with bipolar transistors. The FBSOA (for short-pulse operation to d.c. operation) is determined by using the thermal resistance measurement.

C.2.1 Circuit diagram (see Figure C.1)

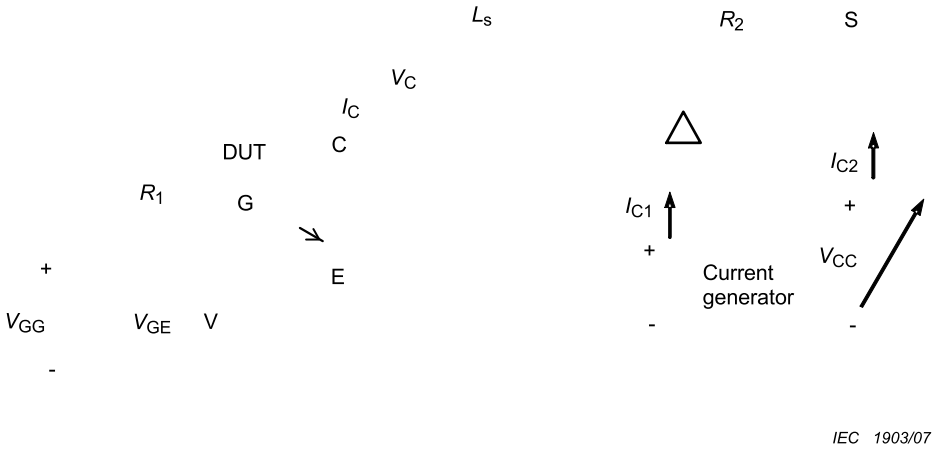


Figure C.1 – Test circuit of forward biased safe operating area (method 1)

C.2.2 Test procedure

The value of the variation of the collector-emitter voltage ΔV_{CE} increases when increasing the collector-emitter voltage V_{CE} for a given I_{C2} and t_p condition. It increases rapidly at a certain value of V_{CE}; this is an indication of the onset of the second breakdown. Further increase may run the IGBT into the second breakdown and may destroy it. These phenomena are shown in Figure C.2. FBSOA is specified at values less than the conditions for the rising point of ΔV_{CE}. After the above test, confirm the acceptance criteria of the DUT defined in Table 1.

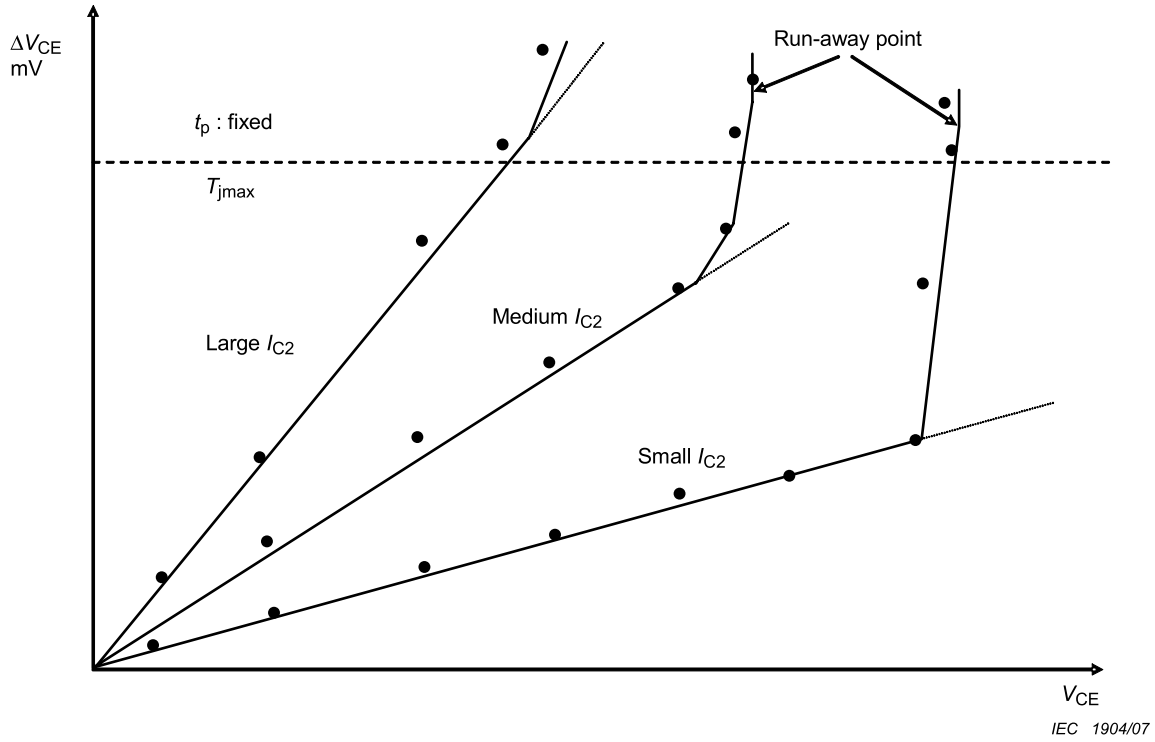


Figure C.2 – Typical ΔV_{CE} versus collector-emitter voltage V_{CE} characteristics

The same result will also be obtained by changing the magnitude of the high current I_{C2} for a fixed V_{CE}.

Figure C.3 shows a typical FBSOA at various t_p within specified maximum values of I_C and V_{CE}.

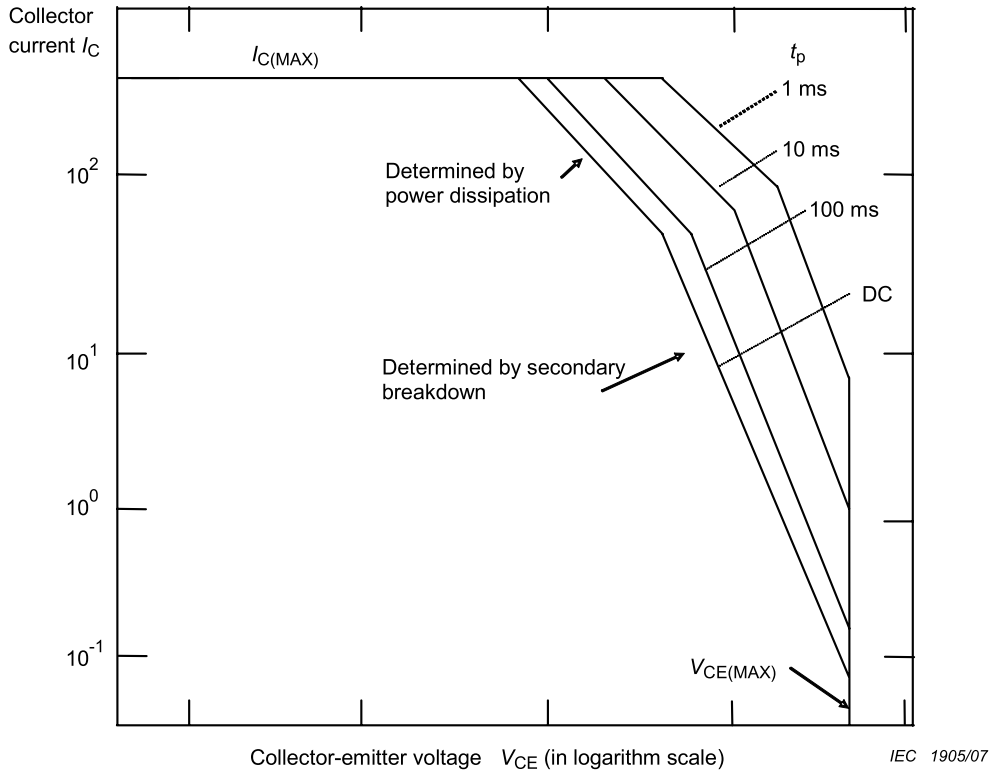


Figure C.3 – Typical forward biased safe operating area

C.2.3 Specified conditions

– Collector current I_C
– Collector-emitter voltage V_{CE}
– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}
– Pulse width t_p
– Single pulse or repetition rate
– Stray inductance L_s

C.3 Method 2

Method 2 is to test the operating point just below the latching mode operation.

C.3.1 Circuit diagram

Figure C.4 shows the circuit description of method 2 of IGBTs.

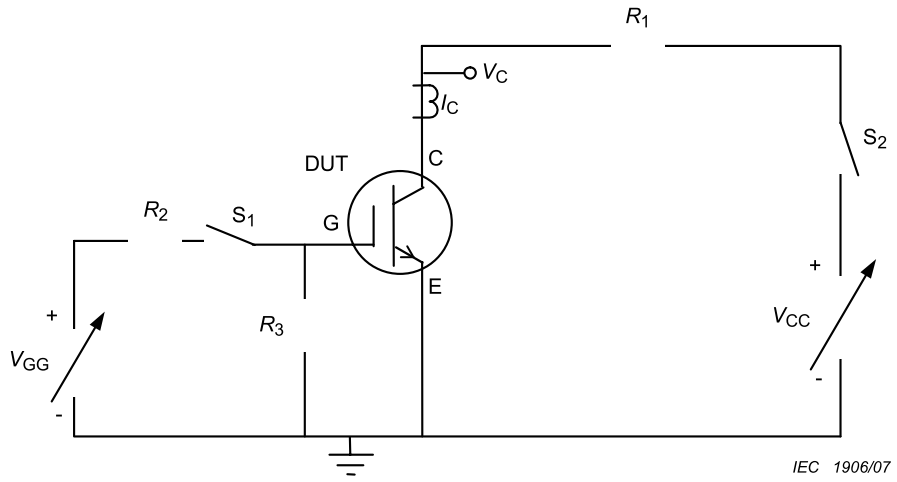


Figure C.4 – Circuit testing forward biased safe operating area (method 2)

C.3.2 Test procedure and precautions to be taken

The value of V_{GG} is increased until the specified collector current is reached. The value of V_{GG} shall be kept within the area where the latching mode does not occur (see Figure C.5). The latching mode is shown in Figure C.6. By increasing the value of V_{CC}, the operating point moves from P_1 to P_m. After P_m, P_s exists and P_s is the starting point of latching. The FBSOA is tested under the specified I_C, V_{CE} and pulse width t_p. IGBTs may be destroyed in the latching mode operation. After the above test, confirm the acceptance criteria of the DUT defined in Table 1.

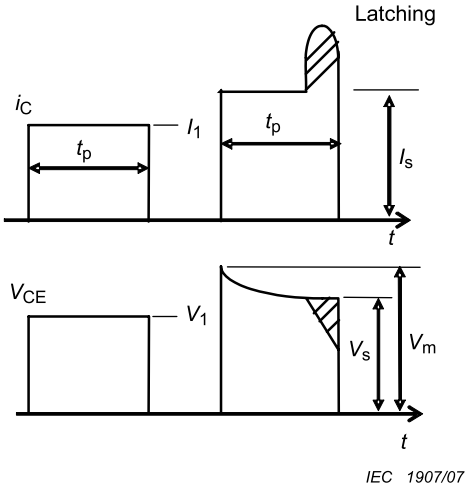


Figure C.5 – Latching mode operation waveforms

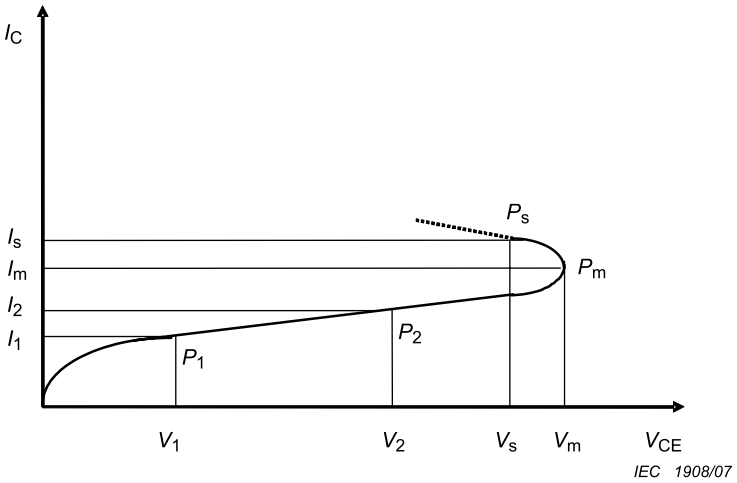


Figure C.6 – Latching mode I-V characteristic

C.3.3 Specified conditions

– Collector current I_C
– Collector-emitter voltage V_{CE}
– Ambient or case or virtual junction temperature T_a or T_c or T_{vj}
– Pulse width t_p
– Single-pulse or repetition rate

Annex D
(normative)

Case non-rupture

D.1 Introduction

The following test or measurement may exceed the specified ratings. IGBTs under test may be changed in characteristics or destroyed. However, to permit evaluation of limiting values, the test or measurement is presented in this annex. When the information is given in the form of data on characteristics, measurements should be made under the specified limit conditions.

IEC 60747-2 and IEC 60747-6 define the case non-rupture current I_{RSMC} for diodes and thyristors.

High currents which are applied to devices having maintained blocking capability or applied to wire-bonded devices lead to the failure mechanisms under consideration.

Bibliography

IEC 60050-521:2002, *International Electrotechnical Vocabulary – Part 521: Semiconductor devices and integrated circuits*

IEC 60747-7: 2000, *Semiconductor discrete devices and integrated circuits – Part 7: Bipolar transistors*

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