BS EN 62878-1-1:2015

BSI Standards Publication

Device embedded substrate

Part 1-1: Generic specification — Test methods

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National foreword

This British Standard is the UK implementation of EN 62878-1-1:2015. It is identical to IEC 62878-1-1:2015.

The UK participation in its preparation was entrusted to Technical Committee EPL/501, Electronic Assembly Technology.

A list of organizations represented on this committee can be obtained on request to its secretary.

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Date	Text affected

EUROPEAN STANDARD

NORME EUROPÉENNE

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EN 62878-1-1

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ICS 31.180; 31.190

English Version

Device embedded substrate - Part 1-1: Generic specification - Test methods (IEC 62878-1-1:2015)

Substrat avec appareil(s) intégré(s) -
Partie 1-1: Spécification générique - Méthodes d'essai
(IEC 62878-1-1:2015)

Trägermaterial mit eingebetteten Bauteilen -
Teil 1-1: Fachgrundspezifikation - Prüfverfahren
(IEC 62878-1-1:2015)

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Comité Européen de Normalisation Electrotechnique
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European foreword

The text of document 91/1248/FDIS, future edition 1 of IEC 62878-1-1, prepared by IEC/TC 91 "Electronics assembly technology" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62878-1-1:2015.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2016-03-24
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2018-06-24

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IEC 60068-1	NOTE	Harmonized as EN 60068-1.
IEC 60068-2-6	NOTE	Harmonized as EN 60068-2-6.
IEC 60068-2-14	NOTE	Harmonized as EN 60068-2-14.
IEC 60068-2-20	NOTE	Harmonized as EN 60068-2-20.
IEC 60068-2-21	NOTE	Harmonized as EN 60068-2-21.
IEC 60068-2-30	NOTE	Harmonized as EN 60068-2-30.
IEC 60068-2-38	NOTE	Harmonized as EN 60068-2-38.
IEC 60068-2-53	NOTE	Harmonized as EN 60068-2-53.
IEC 60068-2-58	NOTE	Harmonized as EN 60068-2-58.
IEC 60068-2-64	NOTE	Harmonized as EN 60068-2-64.
IEC 60068-2-66	NOTE	Harmonized as EN 60068-2-66.
IEC 60068-2-78	NOTE	Harmonized as EN 60068-2-78.
IEC 60068-2-80	NOTE	Harmonized as EN 60068-2-80.
IEC 61189-1	NOTE	Harmonized as EN 61189-1.
IEC 61189-2	NOTE	Harmonized as EN 61189-2.
IEC 61189-11	NOTE	Harmonized as EN 61189-11.
IEC 61190-1-2	NOTE	Harmonized as EN 61190-1-2.
IEC 61190-1-3	NOTE	Harmonized as EN 61190-1-3.
IEC 62137-1-2	NOTE	Harmonized as EN 62137-1-2.
IEC 62137-1-3	NOTE	Harmonized as EN 62137-1-3.
IEC 62421	NOTE	Harmonized as EN 62421.
ISO 291	NOTE	Harmonized as EN ISO 291.

ISO 2409	NOTE	Harmonized as EN ISO 2409.
ISO 3611	NOTE	Harmonized as EN ISO 3611.
ISO 4957	NOTE	Harmonized as EN ISO 4957.
ISO 9445-1	NOTE	Harmonized as EN ISO 9445-1.
ISO 9453	NOTE	Harmonized as EN ISO 9453.
ISO 9455 Series	NOTE	Harmonized as EN ISO 9455 Series.
ISO 15184	NOTE	Harmonized as EN ISO 15184.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu

Publication	Year	Title	EN/HD	Year
IEC 60068-2-1	-	Environmental testing - Part 2-1: Tests - Test A: Cold	EN 60068-2-1	-
IEC 60068-2-2	-	Environmental testing - Part 2-2: Tests - Test B: Dry heat	EN 60068-2-2	-
IEC 60194	-	Printed board design, manufacture and assembly - Terms and definitions	EN 60194	-
IEC 61189-3	-	Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 3: Test methods for interconnection structures (printed boards)	EN 61189-3	-
IEC/TS 62878-2-4	2015	Device embedded substrate - Part 2-4: Guidelines - Test element groups (TEG)	-	-

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DEVICE EMBEDDED SUBSTRATE –

Part 1-1: Generic specification – Test methods

FOREWORD

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International Standard IEC 62878-1-1 has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this standard is based on the following documents:

FDIS	Report on voting
91/1248/FDIS	91/1260/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

A list of all parts in the IEC 62878, published under the general title *Device embedded substrate,* can be found on the IEC website.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
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DEVICE EMBEDDED SUBSTRATE –

Part 1-1: Generic specification – Test methods

1 Scope

This part of IEC 62878 specifies the test methods of passive and active device embedded substrates. The basic test methods of printed wiring substrate materials and substrates themselves are specified in IEC 61189-3.

This part of IEC 62878 is applicable to device embedded substrates fabricated by use of organic base material, which include for example active or passive devices, discrete components formed in the fabrication process of electronic wiring board, and sheet formed components.

The IEC 62878 series neither applies to the re-distribution layer (RDL) nor to the electronic modules defined as an M-type business model in IEC 62421.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-1, *Environmental testing – Part 2-1: Tests – Test A: Cold*

IEC 60068-2-2, *Environmental testing – Part 2-2: Tests – Test B: Dry heat*

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

IEC 61189-3, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 3: Test methods for interconnection structures (printed boards)*

IEC TS 62878-2-4:2015, *Device embedded substrate – Part 2-4 – Guidelines – Test element groups (TEG)*

3 Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 apply.

3.2 Abbreviations

AABUS as agreed between user and supplier

AOI automated optical inspection

LSI large scale integration

4 Test methods

4.1 General

This clause is given for guidance only. The test shall be carried out at the standard air conditions (or simply stated as standard environment):

Temperature	Relative humidity	Atmospheric pressure
15°C to 35°C	25 % to 75 %	86 kPa to 106 kPa

4.2 Visual inspection and micro-sectioning

4.2.1 General

Visual inspection and micro-sectioning of multi-layer printed wiring boards are specified in 4.2.2 and 4.2.3.

4.2.2 Visual inspection

Visual inspection consists of checking the appearance, finish, and pattern of specimens using the naked eye or a magnifying glass in reference to its individual specification. The test result shall be as agreed between user and supplier (hereafter referred as AABUS).

4.2.3 Micro-sectioning

Micro-sectioning is to check the state, appearance, and dimensions according to individual specifications of the plated through hole, the via in the build-up layer, the conductor, the interlayer distance, the conductor distance, and the connections to the embedded device. The specimen is mounted in epoxy or polyester resin and the specimen is cross-sectioned and polished for observation. The evaluation of the results shall be AABUS. The equipment, material, specimen and test are specified in a) to d).

a) Equipment

   An industrial microscope capable of measuring plated film thicknesses with an accuracy of 0,001 mm.

b) Material

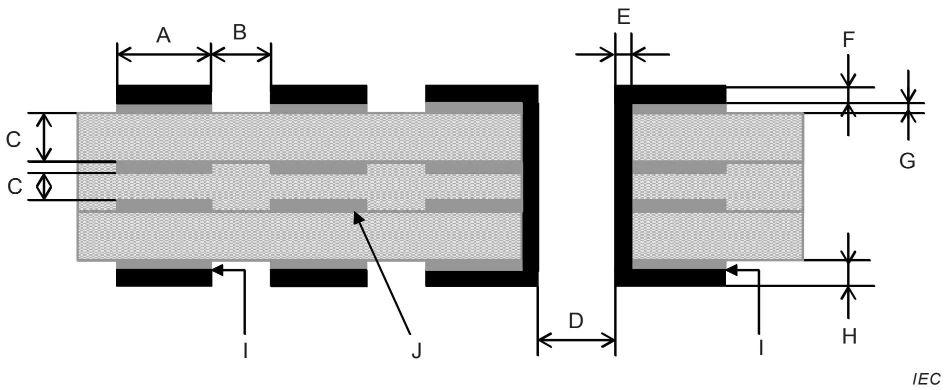
   Materials used in this test are releasing agent, moulding resin, polishing cloth or paper (#180, #400, #1 000, etc.) with the option to use polishing materials (alumina or chromium oxide).

c) Specimen

   A specimen is cut from the product to an appropriate size sufficient for observation and mounted in moulding resin. The cut surface is then polished with polishing cloth/paper starting from coarse to fine using a rotating felt surface and the above mentioned polishing material. The polishing face shall be within an angle of 85° to 95° to the layer to be observed. The diameter of the plated film of the through hole and of the vias in the build-up layer observed by micro-sectioning shall be no less than 90 % of the previously observed hole diameter. Etch the specimen if the boundary of the plating needs to be clarified after polishing.

d) Test

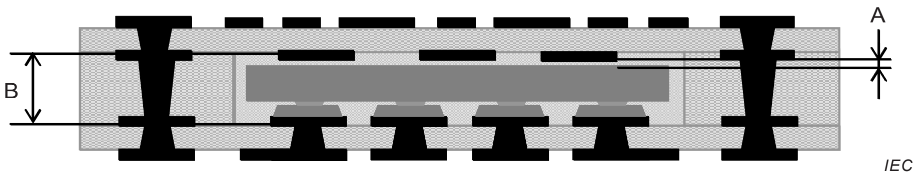
   The test consists of observing the items specified in the individual specifications by means of a microscope of specified magnification. Figure 1 illustrates the test items for the through hole to check the micro-sectioned faces, and Figure 2 for the build-up structure and embedded devices. Table 1 gives the characteristics and observation items of the test.



Key

A	Conductor width	F	Conductor plated film thickness
B	Conductor gap	G	Thickness of copper foil
C	Insulation layer thickness	H	Conductor thickness
D	Hole diameter	I	Boundary of plated film
E	Plated film thickness of through hole	J	Internal circuit

Figure 1 – Measuring items of the micro-sectioned through hole structure



Key

A Distance between conductor and embedded device

B Device embedding layer

Figure 2 – Measuring items of the micro-sectioned device embedded board with build-up structure

Table 1 – Test items, characteristics and observations of micro-sectioned specimens

No	Test item	Characteristics and observation
1	Conductor width (inner layer , outer layer)	– Upper conductor width – Lower conductor width – Etch factor
2	Conductor gap (inner layer, outer layer)	– Minimum conductor gap
3	Insulation layer thickness/conductor gap	– Minimum insulation layer/minimum conductor gap – Delamination – Measling – Crazing
4	Hole diameter and land width	– Hole diameter – Land width

No	Test item	Characteristics and observation
5	Plated film thickness of the through hole	– Plated film thickness of the through hole – Plated film thickness of the via in the build-up layer (conformal via) – Corner crack – Barrel crack – Foil crack
6	Film thickness of the plated conductor	– Film thickness of the plated conductor
7	Copper foil thickness	– Copper foil thickness
8	Conductor thickness	– Total conductor thickness(copper foil and film thickness of the plated conductor)
9	Distance between conductor and embedded device	– Distance between conductor and embedded device
10	Thickness of the device embedding layer	– Thickness of the device embedding layer – Delamination – Measling – Crazing

4.2.4 Lack of conductor and residue of conductor

In order to measure lack and residue of conductor, a) and b) apply:

a) Equipment

   An industrial microscope with an accuracy of at least 0,001 mm.

b) Measurement

   Measure the lack of conductor and residue of the conductor in the vertical and horizontal directions at the insulating area.

4.2.5 Land dimension and land width (annular ring)

4.2.5.1 Component insertion land and through hole land

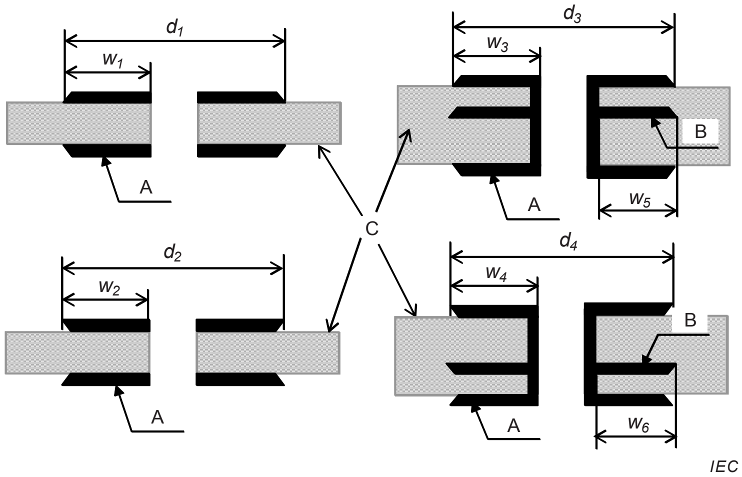
In order to measure component insertion land and through hole land, a) and b) apply:

a) Equipment

   An industrial microscope with an accuracy of at least 0,001 mm.

b) Measurement

   1) Measure the land dimension d_1 to d_4 as illustrated in Figure 3.
   2) Measure the left outer land width w_1 to w_4 as illustrated in Figure 3 by micro-sectioning of the distance between the hall edge and not including the plated film and land edge to better than 0,001 mm.



a) Non-plated hole b) Plated hole

Key

A	Non-plated hole
B	Plated hole
C	Via in the build-up layer with the form of conformal via
d_1 to d_4	Maximum dimension of land
w_1 to w_4	Width of lands in outer layer
w_5, w_6	Width of lands in inter layer

Figure 3 – Measurement of land dimension

4.2.5.2 Via (including interstitial via hole and via in the build-up layer)

In order to measure the via, a) and b) apply:

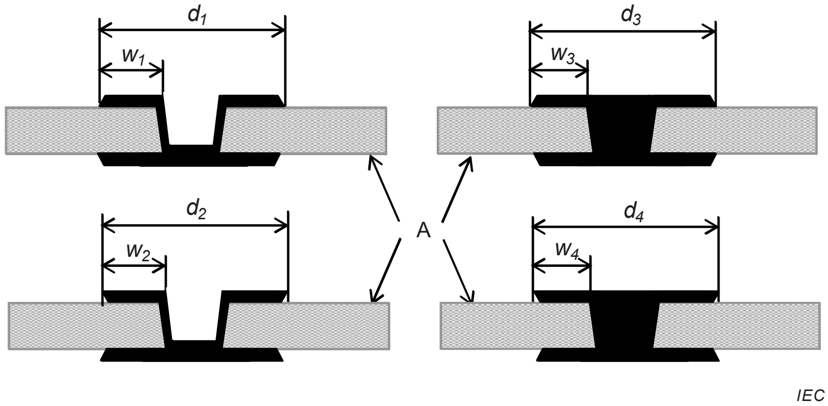
a) Equipment

Industrial microscope with an accuracy of at least 0,001 mm.

b) Measurement

1) Measure the land dimension d_1 to d_4 as illustrated in Figure 4.

2) It is not necessary to measure the land dimension w_1 to w_4 as shown in Figure 4 unless there is a problem with the electrical connection. The measurement can be carried out upon agreement between user and supplier and by means of micro-sectioning to better than 0,001 mm of the maximum dimension.



a) Conformal via b) Filled via

Key

A Insulation layer

d_1 to d_4 Maximum land dimension

w_1 to w_4 Land edge width

Figure 4 – Build-up land measurement

4.2.5.3 Coplanarity

4.2.5.3.1 Bend

In order to measure the bend, a) and b) apply.

a) Equipment

A gap gauge or a height gauge with an accuracy of 0,1 mm or better shall be used.

b) Measurement

Place a device embedded board on a precision plate with the protruded side up and then measure the maximum gap between the base and specimen to an accuracy of 0,1 mm to find the bend.

4.2.5.3.2 Twist

In order to measure the twist, a) and b) apply

a) Equipment

A gap gauge or a height gauge with an accuracy of 0,1 mm or better shall be used.

b) Measurement

Place a device embedded board on a precision plate with the protruded side up with three corners of the specimen touched to the plate and measure the distance between the plate and the untouched corner of the specimen to an accuracy of 0,1 mm.

4.2.5.3.3 Test method

Table 2 gives the test method for coplanarity around the land pattern.

Table 2 – Test method for coplanarity around the land pattern

Item	Criteria	Test method
Effect on embedded device	AABUS	Use TEG in-place of an embedded device A test for terminal connections of embedded devices is under consideration.

4.3 Electrical tests

4.3.1 Conductor resistance

In order to check conductor resistance, a) to d) apply:

a) Equipment

Voltage drop method (four-terminal method) or equivalent. The measuring signal (voltage or current) shall be DC or AC.

b) Specimen

The specimen is the specified section of the test pattern or the complex test pattern of a device embedded board illustrated in IEC TS 62878-2-4:2015, Figures 1 to 27.

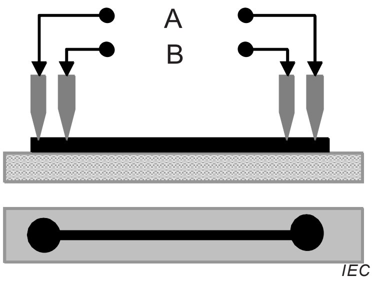
c) Pre-treatment

Pre-treatment shall be either 1) or 2), depending on the individual specifications.

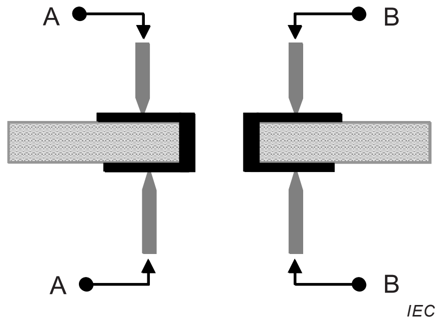
1) Leave a specimen in the standard environment for 24 h ± 4 h.
2) Leave a specimen in a bath of 85 °C ± 2 °C for 4 h and then in the standard environment for 24 h ± 4 h.

d) Test

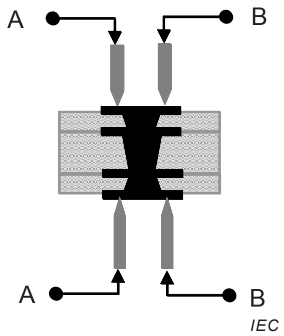
The measurement shall be carried out as illustrated in Figure 5 to an accuracy of ± 5 %. Ensure that effects of probe contacting and heating due to measuring current are avoided. The specimen includes the connection between an embedded device and terminals, a conductor including through hole and a via in the build-up layer.



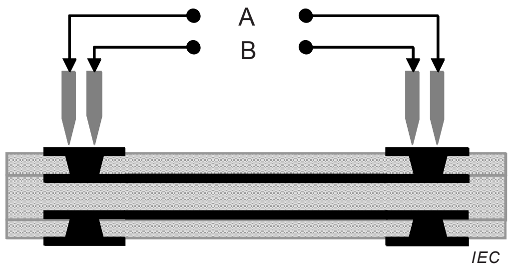
a) Conductor resistance measurement



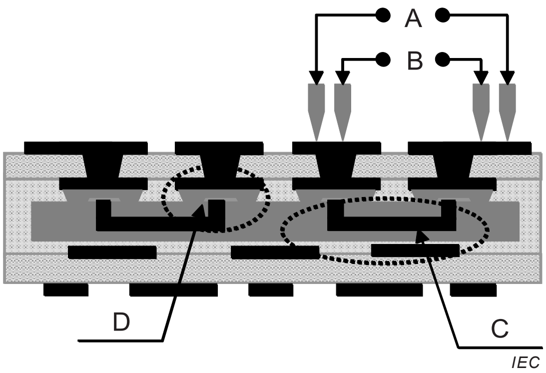
b) Through hole resistance measurement



c) Resistance measurement of via in the build-up layer



d) Resistance measurement of via in the inner conductor layer



e) Resistance measurement for connection of embedded device

Key

A	Current terminal	C	TEG
B	Voltage terminal	D	Connection actually used

Figure 5 – Conductor resistance measurement

4.3.2 Through hole and build-up via

In order to check through hole and build-up via, a) to d) apply:

a) Equipment

The equipment shall be in accordance with 4.3.1 a).

b) Specimen

Specimen is the specified section of the test pattern or of the complex test pattern of a device embedded board illustrated in Figures 1 to 27 of IEC TS 62878-2-4:2015.

c) Pre-treatment

Pre-treatment shall be in accordance with 4.3.1 c).

d) Test

Measurement shall be made as illustrated in Figure 5 to an accuracy of ± 5 % with an effort to avoid effects of probe contacting and heating due to measuring current.

Table 3 gives the characteristics and test method for conductor resistance.

Table 3 – Characteristics and test methods for conductor resistance

Item	Characteristics	Test method
Connection to embedded device/Pad connection/Via connection	AABUS	As indicated in 4.3.2, plated through hole and via in the build-up layer. Use TEG for embedded device.

4.3.3 Withstanding current of embedded device connection

In order to measure withstanding current of embedded device connection, a) to d) apply:

a) Equipment

A DC or AC power supply capable of giving the test current specified in Table 4 and an ammeter. The equipment shall be a DC or AC power supply capable of giving the test current specified in 4.3.2 a) and an ammeter.

b) Specimen

The specimen shall be the terminals of the TEG and the specified part of the complex test pattern (Figures 1 to 28 in IEC TS 62878-2-4:2015). A zero ohm jumper resistor is recommended for the TEG for an embedded device.

c) Pre-treatment

Pre-treatment shall be in accordance with 4.3.1 c).

d) Test

Check any abnormality after supplying a current contact terminal of TEG and pad on the board with a specified current given its individual specification for 30 s. Test current for a given hole diameter is given in Table 5.

Table 4 shows the withstanding current characteristics and test methods.

Table 4 – Withstanding current and test methods

<table>
<tr><th>Item</th><th>Characteristics</th><th>Test method</th></tr>
<tr><td>Conductor</td><td>Withstanding current characteristics shall be AABUS.

The relationship between current and conductor width, conductor thickness and temperature rise is shown in Figure 6.</td><td>As per 4.3.2 withstanding current for through hole and via in the build-up layers.

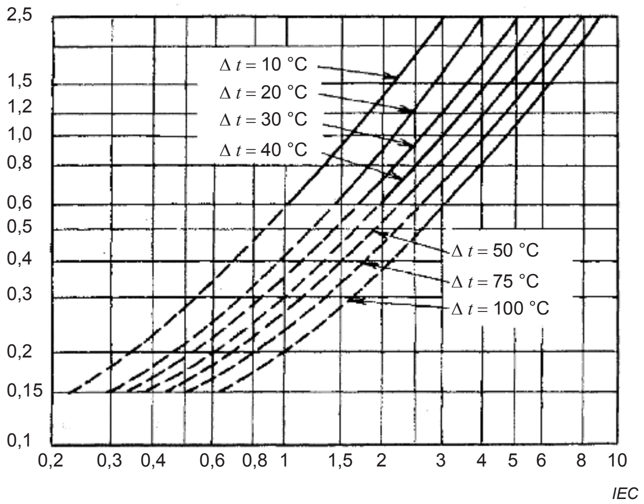
As per 4.3.3 withstanding current of conductor. Shape and dimension of specimen shall be AABUS.</td></tr>
<tr><td>Through hole and via in the build-up layer</td><td></td><td>As per 4.3.3 withstanding current of conductor. Shape and dimension of specimen shall be AABUS.</td></tr>
<tr><td>Embedded device

– Pad connection

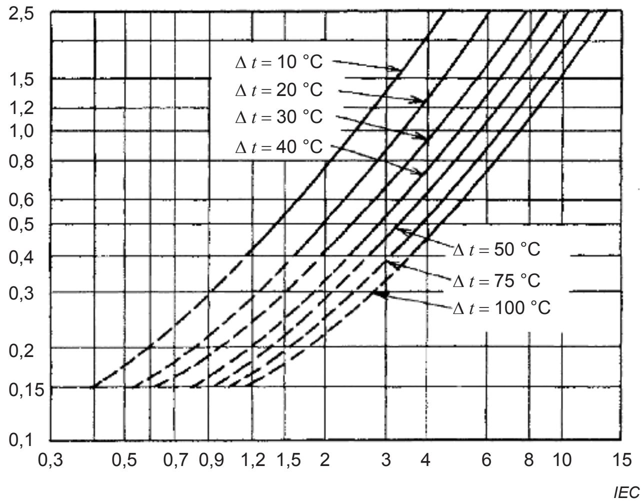
– Via connection</td><td></td><td>As per 4.3.3 withstanding current of embedding device connection. Use the TEG for embedded device. Internal resistance of the TEG shall be less than 50 mΩ. The test current shall not exceed the rated current shown below.

Rated current is for steady state loading of 30 s.

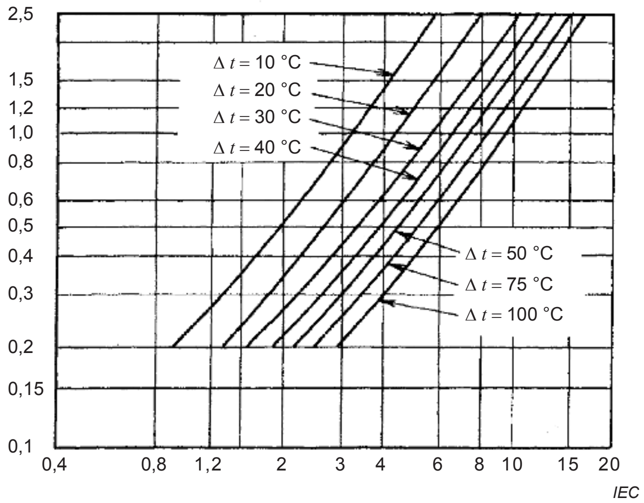
The maximum overload current is defined for 2 s.
<table>
<tr><th>Type</th><th>Rated current
70 °C, A</th><th>Maximum overload current, A</th></tr>
<tr><td>0402</td><td>—</td><td>—</td></tr>
<tr><td>0603</td><td>0,5</td><td>1,0</td></tr>
<tr><td>1005</td><td>1,0</td><td>2,0</td></tr>
<tr><td>1608</td><td>1,0</td><td>2,0</td></tr>
</table>
</td></tr>
</table>



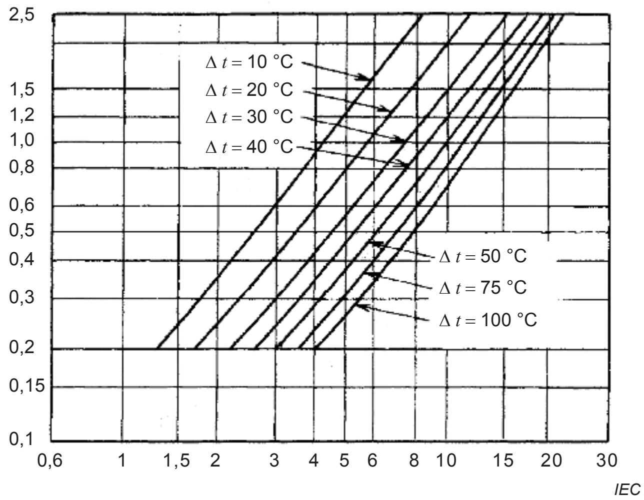
a) Conductor thickness is 18 µm



b) Conductor thickness is 35 µm



c) Conductor thickness is 70 µm



d) Conductor thickness is 105 µm

X current (A)

Y conductor width (mm)

Figure 6 – Relationship between current, conductor width and thickness and temperature rise

4.3.4 Withstanding voltage in embedded boards

4.3.4.1 General

Withstanding voltages of conductor, plated through hole and via in the build-up layers, inner connection and connection to the embedded device shall be measured according to each individual specification. This test shall be made only when the test of withstanding voltage is required.

4.3.4.2 Withstanding voltage of inner layers in embedded boards

In order to measure withstanding voltage of inner layer in embedded boards, a) to d) apply:

a) Equipment

The equipment shall be in accordance with 4.3.2.a).

b) Specimen

The specimen shall be manufactured to fit the connection terminal of the TEG in the device embedding board or the pad of complex test pattern (see Figures 1 to 27 in IEC TS 62878-2-4:2015). A specimen suffering from mechanical damage, flashover, sparkover or breakdown shall not be used in further tests.

c) Pre-treatment

Pre-treatment shall be as described in 4.3.1 c).

d) Test

The test shall be as described in 4.3.1 d).

4.3.4.3 Withstanding voltage of embedded device connection

Items a) to d) apply:

a) Equipment

The equipment shall be in accordance with 4.3.1 a).

b) Specimen

The specimen shall be a specified part of the TEG in a device embedding board or complex test pattern (Figures 1 to 27 of IEC TS 62878-2-4:2015). It is recommended to use a zero ohm jumper resistor for the TEG. A specimen suffering from mechanical damage, flush over, spark over or breakdown shall not be used in further tests.

c) Pre-treatment

Pre-treatment shall be as described in 4.3.1 c).

d) Test

The test shall be as described in 4.3.1 d).

Table 5 shows the test methods for withstanding voltage.

Table 5 – Withstanding voltage and test methods

<table>
<tr><th>Item</th><th>Characteristics</th><th>Test</th></tr>
<tr><td>Interlayer</td><td>There should be no abnormality such as mechanical damage, flush-over or insulation damage.</td><td>As stated in 4.3.4.2, interlayer surge voltage. The test voltage is given below.
<table>
<tr><th>Interlayer distance x
mm</th><th>Test voltage
V</th></tr>
<tr><td>$0,02 \leqq x < 0,05$</td><td>100</td></tr>
<tr><td>$0,05 \leqq x < 0,08$</td><td>250</td></tr>
<tr><td>$0,08 \leqq x < 0,20$</td><td>500</td></tr>
<tr><td>$0,20 \leqq x$</td><td>1 000</td></tr>
</table></td></tr>
<tr><td>Connection to embedded device</td><td>There should be no abnormality such as mechanical damage, flush-over or insulation damage.</td><td>As stated in 4.3.4.3, withstanding voltage for embedded device.
Use the TEG for embedded device.
The internal resistance of the TEG shall be less than 50 mΩ. Test below the isolation voltage of the TEG.
<table>
<tr><th>Type</th><th>Isolation voltage
(effective value of V_{dc} or V_{ac})</th></tr>
<tr><td>0402</td><td>—</td></tr>
<tr><td>0603</td><td>30</td></tr>
<tr><td>1005</td><td>100</td></tr>
<tr><td>1608</td><td>100</td></tr>
</table></td></tr>
</table>

4.3.5 Insulation resistance

4.3.5.1 General

The insulation resistance shall be measured between the terminals of the conductor the embedded device based on individual specifications.

4.3.5.2 Insulation resistance of the inner layer

In order to measure insulation resistance of the inner layer, a) to d) apply:

a) Equipment

   An insulation resistance tester capable of measuring values greater than 10^{10} Ω.

b) Specimen

   The specimen shall be a specified part of a device embedding board, test pattern or complex test pattern (Figures 1 to 27 of IEC TS 62878-2-4:2015) including connection to embedded device.

c) Pre-treatment

   Pre-treatment shall be in accordance with 4.3.4.2 c).

d) Test

   Apply a DC voltage of 10 V ± 1 V, 50 V ± 5 V, 100 V ± 10 V or 500 V ± 50 V depending on the individual specification for 1 min and then measure the insulation resistance while applying the voltage.

4.3.5.3 Insulation resistance between inner layers

In order to measure insulation resistance between inner layers, a) to d) apply:

a) Equipment

   Equipment shall be in accordance with 4.3.1 a).

b) Specimen

   The specimen shall be a specified part of a device embedding board, test pattern or a complex test pattern (Figures 1 to 27 of IEC TS 62878-2-4:2015) including connection to embedded device.

c) Pre-treatment

   Pre-treatment shall be in accordance with 4.3.1 c).

d) Test

   The test shall be in accordance with 4.3.1 d).

4.3.5.4 Insulation resistance between embedded terminals

In order to measure insulation resistance between embedded terminals, a) to d) apply:

a) Equipment

   The equipment shall be in accordance with 4.3.4.3 a).

b) Specimen

   The specimen shall be a specified part of a device embedding board, test pattern or a complex test pattern (Figures 1 to 27 in IEC TS 62878-2-4:2015) including connection to embedded device. It is recommended to use a zero ohm jumper resistor for TEG.

c) Pre-treatment

   Pre-treatment shall be in accordance with 4.3.1 c).

d) Test

The test shall be in accordance with 4.3.1 d).

Table 6 shows evaluation items of insulation resistance, characteristics and test methods.

Table 6 – Criteria and test methods for insulation resistance

<table>
<tr><th colspan="2">Item</th><th>Criteria</th><th>Test</th></tr>
<tr><td>Interlayer</td><td>Normal</td><td>Resistance shall be larger than:
<table>
<tr><th>Minimum insulator thickness x
mm</th><th>Resistance
Ω</th></tr>
<tr><td>0,02 ≦ x < 0,05</td><td>5×10^{9}</td></tr>
<tr><td>0,05 ≦ x < 0,13</td><td>1×10^{10}</td></tr>
<tr><td>0,13 ≦ x</td><td>5×10^{10}</td></tr>
</table></td><td>As per 4.3.5.3 interlayer insulation resistance. Test voltage shall be:
<table>
<tr><th>Minimum insulation layer thickness x
mm</th><th>Test voltage
V</th></tr>
<tr><td>0,03 ≦ x < 0,05</td><td>10</td></tr>
<tr><td>0,05 ≦ x < 0,08</td><td>50</td></tr>
<tr><td>0,08 ≦ x < 0,20</td><td>100</td></tr>
<tr><td>0,20 ≦ x</td><td>500</td></tr>
</table></td></tr>
<tr><td>Between embedded device terminals</td><td>Normal</td><td>Resistance shall be larger than:
<table>
<tr><th>Minimum distance between insulation terminal or pads x
mm</th><th>Resistance
Ω</th></tr>
<tr><td>0,02 ≦ x < 0,05</td><td>5×10^{8}</td></tr>
<tr><td>0,05 ≦ x < 0,13</td><td>1×10^{9}</td></tr>
<tr><td>0,13 ≦ x</td><td>5×10^{9}</td></tr>
</table></td><td>As stated in 4.3.5.4 insulation resistance between terminals of embedded device. Use TEG. Internal resistance of the TEG shall be less than 50 mΩ. When using a resistor, the guaranteed insulation resistance shall be 10^{9} Ω.</td></tr>
</table>

4.3.6 Conduction and insulation of circuit

This test has been developed to verify the insulation of points not electrically connected to a specified conductor pattern and not connected to a device embedding board by the board specification (test data by CAD/CAM and individual specification), and electrical connection to specified connecting positions of the conductor pattern. It is recommended to use this test for the actual device embedding board.

4.4 Mechanical tests

This test has been developed to verify the mechanical strength of a device embedding board by the board specification (test data by CAD/CAM and individual specification) of the conductor, the land of a hole without plating, a plated through hole, pad of land pattern, solder resist and symbol mark by applying a specified mechanical load.

4.4.1 Pulling strength of conductor

a) Equipment

Pulling test machine capable of keeping a cross head speed of 50 mm/min. Accuracy of measurement within the effective measuring range shall be ± 1 % of indication and for the pulling load range of 15 % to 85 %. Use a jig which can keep the pulling direction of 90° to the specimen surface when a conductor film is pulled from the specimen.

b) Specimen

The specimen shall be a board having an appropriate length and conductor with a constant width (Figures 1 to 27 in IEC TS 62878-2-4:2015). Use of a specimen with conductor narrower than 0,8 mm shall be AABUS.

c) Pre-treatment

Pre-treatment shall be in accordance with 4.3.1 c).

d) Test

The test is made under the standard test environment. A specimen with the conductor pulled off about 10 mm from the base is fastened to the holding jig of the equipment. Hold the end of the pulled conductor film and pull the conductor for more than 25 mm with a speed of 50 mm/min.

Table 7 shows the pulling strength of conductor and test method.

Table 7 – Characteristics and test method of pulling strength of conductor

<table>
<tr><th>Item</th><th colspan="2">Characteristics</th><th>Test method</th></tr>
<tr><td rowspan="4">Pulling strength of conductor</td><td colspan="2">Pulling strength of conductor shall be AABUS.
N/mm</td><td rowspan="4">Test method, shape and size shall be AABUS.</td></tr>
<tr><td>Item</td><td>IEC 61249-2-7 (FR-4)
Copper foil thickness: 18 μm
Width of pattern: 0,8 mm</td></tr>
<tr><td>Specification (for reference)</td><td>General: ≧ 0,98 N/mm
Halogen free: ≧ 80 N/mm</td></tr>
<tr><td colspan="2">Note: General material may contain halogen (to be stated as general).</td></tr>
</table>

4.4.2 Pulling strength of un-plated through hole

a) Equipment

Equipment shall be in accordance with 4.4.1 a).

b) Specimen

The specimen is a board pre-soldered for 3 s in a soldering bath for an independent round land shown in Figures 1 to 27 of IEC TS 62878-2-4:2015 and land, hole and lead dimensions as shown in Table 8. Solder to be used shall be AABUS. The use of dimensions other than stated in Table 8 shall also be AABUS.

c) Pre-treatment

Pre-treatment shall be in accordance with 4.3.1 c).

d) Test

Insert a lead wire into a hole of the specimen. Do not bend the end of the wire, but extrude a little to the back of the board and solder in 3 s to 5 s, touching only the wire not the land directly, using a soldering iron with a tip diameter of 5 mm ± 0,1 mm.

The temperature of the tip of the soldering iron is 270 °C ± 10 °C. Leave the specimen for more than 30 min at room temperature to cool. Pull the wire vertically using a pulling test machine at a pulling speed of 50 mm/min and measure the force to pull off the land from the board. Repeat the test if the wire itself is pulled off or broken.

The repeat soldering test may be performed by using a specimen whose soldered wire is removed using a soldering iron as stated in a) and where a new lead wire is soldered to the land. Repeat the unsoldering and soldering of the wire for the number of times given in the individual specification. Cool down the specimen for each soldering for more than 30 min at room temperature.

Pull the wire vertically using a pulling test machine at a pulling speed of 50 mm/min and measure the force necessary to pull the land from the board. Repeat the test if the wire itself is pulled off or broken.

Table 8 – Dimensions of land, hole and conductor

Land (mm)	2,0	4,0
Hole diameter (mm)	0,8	1,3
Lead diameter (mm)	0,6 to 0,7	0,9 to 1,0

4.4.3 Pulling strength of plated through hole

a) Equipment

Equipment shall be in accordance with 4.4.1 a).

b) Specimen

The specimen is an independent pad of land pattern with no lead wire attached to the pad. Size of a pad and lead wire shall be AABUS.

The lead wire shall be soldered to the land within 3 s using the equipment described in 4.4.2 a). Solder to be used shall be AABUS.

c) Pre-treatment

Pre-treatment shall be in accordance with 4.3.1 c).

d) Test

The test shall be in accordance with 4.4.2 d).

Table 9 shows characteristics and test methods of pulling strength of plated through hole.

Table 9 – Characteristics and test methods of pulling strength of plated through hole

Item	Characteristics	Test method
Pulling strength of plated through hole	Pulling strength of plated through hole shall be AABUS N/hole Item: Board grade:IEC 61249-2-7 (FR-4) Board thickness: 1,6 mm Hole diameter: ø1,0 mm Specification Information: General material:≧88,3 N/mm	Test shall be in accordance with 4.4.3 d)

4.4.4 Pulling strength of pad of land pattern

a) Equipment

Equipment shall be in accordance with 4.4.1 a).

b) Specimen

The specimen is an independent pad of land pattern with no lead wire attached to the pad. Size of a pad and lead wire shall be AABUS. The lead wire shall be soldered to the land within 3 s using the equipment described in 4.4.1 a). Solder to be used shall be AABUS.

c) Pre-treatment

Pre-treatment shall be in accordance with 4.3.1 c).

d) Test

The test shall be in accordance with 4.4.2 d).

Table 10 shows specification and test method of pad pulling strength of land pattern.

Table 10 – Specification and test method of pad pulling strength of land pattern

<table>
<tr><th>Item</th><th>Characteristics</th><th>Test method</th></tr>
<tr><td>Pad pulling strength of land pattern</td><td>Pad pulling strength of land pattern shall be AABUS
N/mm²
<table>
<tr><td>Item</td><td>Glass epoxy resin, copper laminater
Board grade: IEC 61249-2-7 (FR-4)
Copper foil (conductor thickness): 18 μm
Pad: 1,0 mm × 1,0 mm</td></tr>
<tr><td>Specification information</td><td>General material: ≦39,2 N/mm²
(Halogen free material: ≦32,0 N/mm²)</td></tr>
</table></td><td>Test shall be in accordance with 4.4.4 d)</td></tr>
</table>

4.4.5 Adhesivity of plated foil

a) Material

The material used in this test shall be transparent adhesive tape of 12 mm width and adhesive power of more than 1,8 N/cm.

b) Specimen

The specimen shall be a completed product or a board with the complex conductor pattern shown in Figures 1 to 27 of IEC TS 62878-2-4:2015.

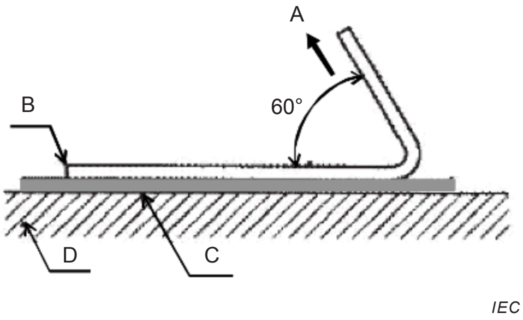
c) Pre-treatment

Pre-treatment shall be in accordance with 4.3.1 c).

d) Test

Clean the surface of a specimen and adhere the adhesive tape more than 50 mm on the specimen surface by finger pressing or other appropriate method so as not to leave any bubble between the tape and the specimen. Leave as is for about 10 s and then pull off quickly within 5 min as shown in Figure 7 at an angle of about 60°.

The area for testing shall be larger than 100 mm^2. With the naked eye or a magnifying glass, check delamination or a fragment detached from the plated film which is stuck to the adhesive tape. The fragment from the overhang of plated film is not used as the test subject.



Key

A	Direction of pulling	C	Plated foil
B	Tape	D	Device embedding board

Figure 7 – Adhesivity of plated film

4.4.6 Adhesivity of solder resist and symbol mark

4.4.6.1 Adhesivity of paint (total surface method)

a) Material

The material used in this test shall be transparent adhesive tape of 12 mm width and adhesive power of more than 1,8 N/cm.

b) Specimen

The specimen shall be a device embedded board with solder resist and a symbol mark.

c) Pre-treatment

Pre-treatment shall be in accordance with 4.3.1 c).

d) Test

Clean the surface of a specimen and adhere adhesive tape more than 50 mm on the specimen by finger pressing or other appropriate method so as not to leave any bubble between the tape and specimen. Leave as is for about 10 s and then pull off quickly the pre-treatment within 5 min at an angle of about 60° and peel off the entire tape in 0,5 s to 1,0 s. With the naked eye or a magnifying glass, check delamination or a piece of solder resist or symbol mark attached to the adhesive tape.

4.4.6.2 Adhesivity of paint (cross-cut method)

a) Material to be used in the test

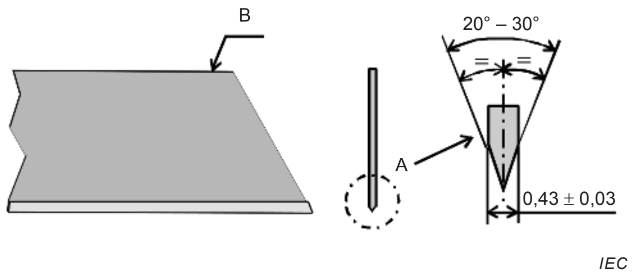
Material to be used in the test shall be in accordance with 4.4.6.1 a).

b) Equipment and tool

The equipment and tool used in this test shall be one or both of the following:

1) a single cutting tool with a cutting edge of 20° to 30° as illustrated in Figure 8, or a cutter knife as illustrated in Figure 9;
2) a multiple cutting edge tool with 6 or 11 cutting edges with a gap of 1 mm as illustrated in Figure 10.

Dimensions in millimetres

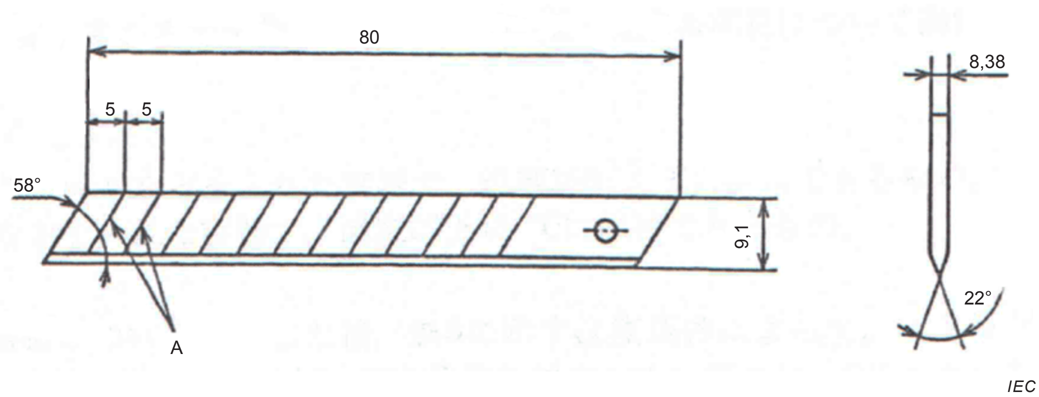


Key

A	Specification of cutter	B	Single cutter

Figure 8 – Single cutting tool

Dimensions in millimetres

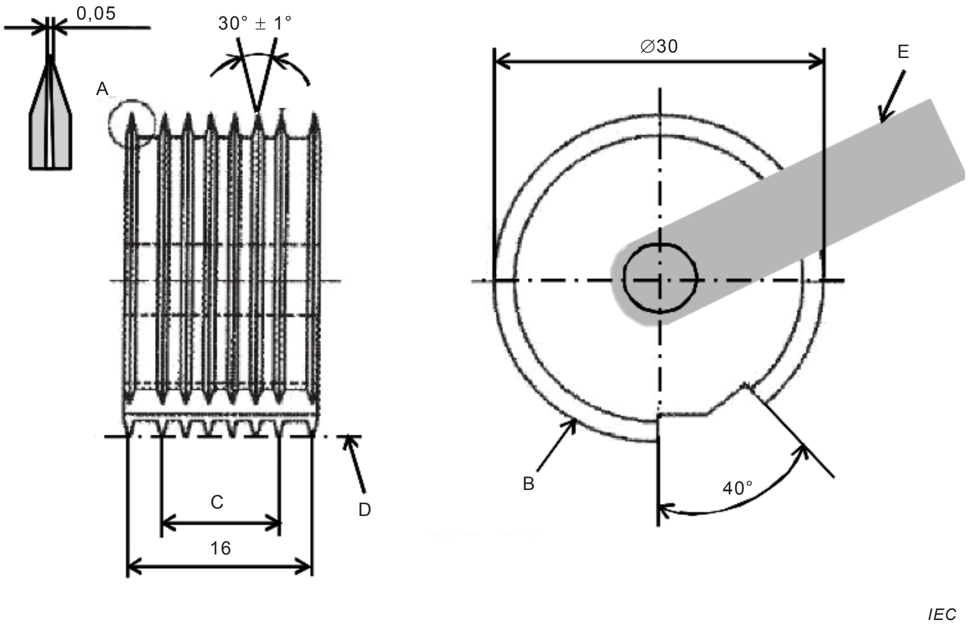


Key

A Breaking line

Figure 9 – Cutter knife

Dimensions in millimetres



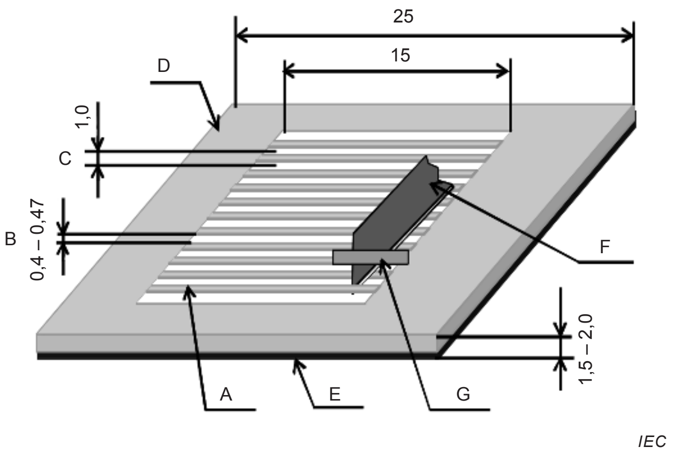
Key

A	Edge dimension (sharpen edge if the edge is worn).	D	Blades have the same diameter. Diameter is AABUS.
B	Cutting edge	E	Handle
C	5 mm or 10 mm		

Figure 10 – Multiple blade cutter

An equal-distance spacer illustrated in Figure 11 shall be used as a single cutting tool.

Dimensions in millimetres



Key

A	Single cutting edge guide	E	Rubber sheet (to prevent slippage)
B	Guide width (of single blade)	F	Cutting tool
C	Cross cut dimension (same)	G	Cutting tool guide
D	Board, e.g. stainless steel		

Figure 11 – Equal-distance spacer with guide

An electric powered single edge cutter shall also be AABUS.

NOTE Use of a single edge cutting tool and a cutter knife is simple and desirable for all the paint types used in an adhesivity test.

A multiple cutting edge tool is good for a thick board test but not suitable for thin board and soft paint. Care should be taken in using a single cutting edge tool as deviation in the cutting space and depth may occur in a test. Use of an equal-distance spacer with guide is recommended to reduce deviation of cutting.

c) Specimen

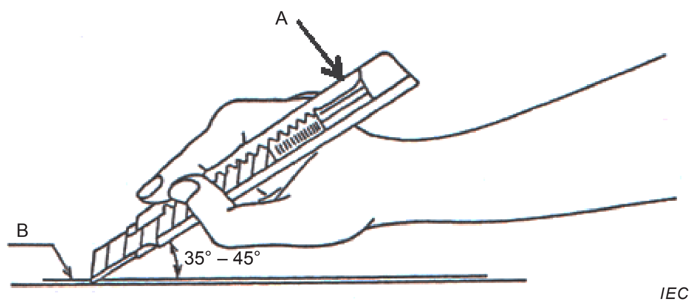
   The specimen shall be in accordance with 4.4.6.1 b).

d) Pre-treatment

   Pre-treatment shall be in accordance with 4.3.1 c).

e) Test

   Cut the surface of a specimen at a speed of about 0,5 s for each cut in case of cutting using a single blade cutting tool or a cutter knife at an angle of about 35° to 45° penetrating the paint film as illustrated in Figure 12.

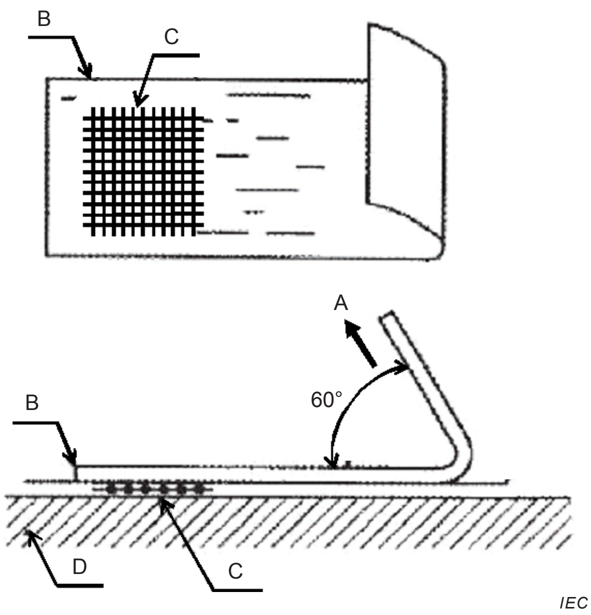


Key

A Single cutting tool B Coated surface

Figure 12 – Cutting using a single cutting tool or a cutting knife

Figure 13 shows the cross-cut test. 11 or 6 parallel cuts are made on the paint film 1 mm apart to form 100 squares in an area of 100 mm^2 or 25 squares in an area of 25 mm^2.



Key

A	Tape peeling direction	C	Cross-cut coating surface
B	Tape	D	Device embedding board

Figure 13 – Cross-cut test

Clean the surface using a soft brush to remove cutting dust and put the adhesive tape at the centre of cross cut as illustrated in Figure 12. Check the adhesivity of 100 or 25 1 mm × 1 mm dies by the test method described in 4.4.6.1 d).

4.4.7 Hardness of painted film (solder resist and symbol mark)

a) Material

The tool to be used in the test is the pencil specified in ISO 9180. The types of pencils are 9H, 8H, 7H, 6H, 5H, 4H, 3H, 2H, H, F, B, 2B, 3B, 4B, 5B and 6B.

The pencils shall be produced by the same manufacturer. The wood part of one end of a pencil shall be cut to expose about 5 mm to 6 mm of the lead. The end of the lead shall be turned on a polishing paper of # 400 specified by ISO 21948 so that it is flat and has a sharp edge.

The thread shall be sharpened each time. The hardness standard here is the degree of scratching when the surface is scratched by an obstacle, expressed by Morse hardness. A pencil is used for scratching as it is easy to obtain with a reliable reproducibility of hardness.

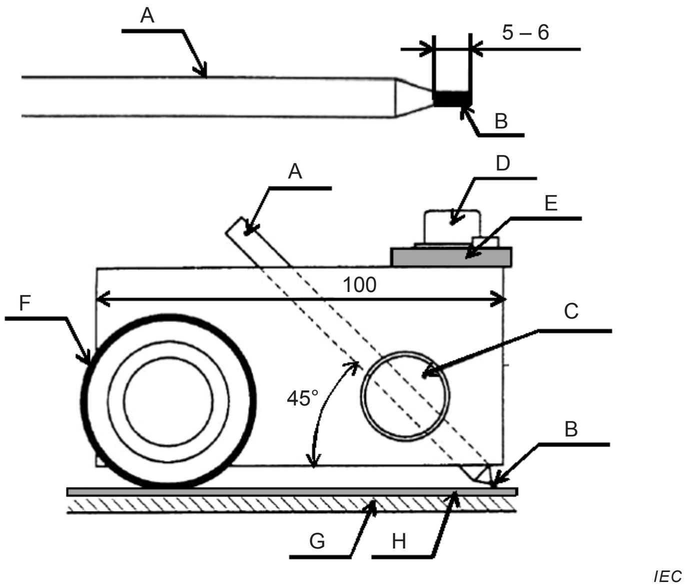
b) Equipment

The test shall be made using the equipment illustrated in Figure 14.

This equipment is made of metal with two wheels at one end and a holder to hold a pencil at an angle of 45° ± 1°.

It is desirable to install a level so as to keep the face of the wheels and the extruding pencil horizontal. Adjust the weight so that the load at the end of the pencil lead is 750 g ± 10 g. The wheels shall be made of rubber so as to avoid any flaw in the specimen surface.

Dimensions in millimetres



Key

A	Pencil	E	Weight
B	Pencil lead	F	Wheel (rubber)
C	Pencil holder	G	Device embedding board
D	Level	H	Solder resist film

Figure 14 – Coated film hardness test

c) Specimen

The specimen is a device embedded board with solder resist and symbol mark. The specimen shall be in accordance with 4.4.6.1 b).

d) Pre-treatment

Pre-treatment shall be in accordance with 4.3.1 c). The pre-treatment of a specimen for this test after use in another test shall be AABUS.

e) Test

Hold the specimen firmly in a horizontal position. Place the pencil with the hardest lead in the holder as illustrated in Figure 14 and move the holder in the testing direction. Draw a line on the painted surface to scratch the face, then change the pencil to the next hardest one until a pencil does not scratch the film in order to find the softest pencil lead to make a cut on the film.

4.5 Environmental tests

4.5.1 General

The environmental test of device embedded boards is a test to estimate the life of a product under overload of high and low temperatures and humidity by estimating the environmental load in use conditions for a device embedded board. Test methods may be selected from the methods stated in Table 11.

Table 11 – High and low temperature characteristics and tests

Item		Characteristics	Test
Connection to embedded device	High and low temperatures	Rate of change of conduction resistance including plated through hole, via connection shall be AABUS.	As stated in IEC 60068-2-2 for high temperature and IEC 60068-2-1 for low temperature in this test. Use the TEG for embedded device. Internal resistance of the TEG shall be less than 50 mΩ.

4.5.2 Vapour phase thermal shock

Table 12 shows characteristics and test methods for vapour phase thermal shock.

Table 12 – Thermal shock characteristics and test methods

Item	Characteristics	Test method
Embedded device	The rate of change of conduction resistance including plated through hole, via connection shall be AABUS.	As stated in IEC 61189-3, 3N01 to 3N05, low temperature cycle test. Use the TEG for embedded device. The internal resistance of the TEG shall be less than 50 mΩ.

4.5.3 High temperature immersion tests

In order to perform high temperature immersion tests, a) to e) apply:

a) Purpose

The vapour phase high temperature immersion test is to estimate the life of a product under overload by immersing a specimen in high temperature oil with a specified environmental condition.

b) Equipment

Equipment shall satisfy the following conditions:

1) a container large enough to contain a sufficient volume of silicone oil and able to maintain a temperature of 260 °C;
2) a container large enough to contain a sufficient volume of organic solvent and able to maintain a temperature of 20 °C ± 15 °C.

c) Specimen

The specimen shall be a completed product or a board with the complex conductor pattern shown in Figures 1 to 28.

d) Test

Measure characteristics of the specimen for the items specified in its individual specification and select the temperature condition from Table 13 and change the temperature condition from step 1 to step 4 as one cycle. Repeat the change for the specified cycles according to the individual specification. The number of cycles is 5 when not specified in the individual specification. Then measure its characteristics for the specified items in the standard condition specified below.

Table 13 – Thermal shock (high temperature immersion test)

Step		Temperature °C	Time s	Liquid to immerse
1 cycle	1	260	3 to 5	Silicone oil
	2	20 ± 15	< 15	Transport
	3	20 ± 15	20	Organic solvent
	4	20 ± 15	< 15	Transport

e) Measuring environment

Test environment adopted in the tests described in this part of IEC 62878. Tests are performed unless otherwise specified in the standard atmospheric pressure of 86 kPa to 106 kPa and air flow of smaller than 1 m/s. In cases where it is difficult to test a specimen in the standard condition, a test may be made in a different condition if there is no question in evaluating test results. The test shall be made with the conditions shown in Table 14 when there is any question about the test result or when specifically requested.

Table 14 – Measuring environment

<table>
<tr><th colspan="3">Classification</th><th>Temperature
°C</th><th>Humidity
%</th><th>Pressure
kPa</th><th>Remarks</th></tr>
<tr><td rowspan="5">Standard condition</td><td colspan="2">Common</td><td>15 to 35</td><td>25 to 75</td><td>86 to 106</td><td rowspan="3">Standard condition if not specified otherwise</td></tr>
<tr><td rowspan="2">23/50</td><td>Class 1</td><td>23 ± 1</td><td>50 ± 5</td><td rowspan="2">86 to 106</td></tr>
<tr><td>Class 2</td><td>23 ± 2</td><td>50 ± 10</td></tr>
<tr><td rowspan="2">27/65</td><td>Class 1</td><td>27 ± 1</td><td>65 ± 5</td><td rowspan="2">86 to 106</td><td rowspan="2">AABUS
e.g. in a tropical area</td></tr>
<tr><td>Class 2</td><td>27 ± 1</td><td>65 ± 5</td></tr>
<tr><td>Evaluation</td><td colspan="2">Common</td><td>20 ± 2</td><td>60 to 70</td><td>86 to 106</td><td></td></tr>
</table>

Table 15 shows specification and test methods for thermal shock (high temperature immersion tests).

Table 15 – Thermal shock (high temperature immersion tests)

Item	Characteristics	Test method
Embedded device	The rate of change of conduction resistance, including plated through holes and via connections shall be AABUS.	As stated in IEC 60068-2-2, high temperature cycle test. Use the TEG for the embedded device. Internal resistance of the TEG shall be less than 50 mΩ.

4.5.4 Resistance to humidity

In order to check resistance to humidity, a) to d) apply:

a) Equipment

Equipment shall satisfy the following conditions.

1) The bath shall be able to maintain the temperature and humidity cycle shown in Figure 15.
2) The resistivity of water shall be greater than 500 Ωm; if necessary, humidify the bath by injecting water directly.
3) Water drops condensed on the roof or wall of the bath shall not drop on or near the specimen.

b) Specimen

The specimen shall be a specified part of a device embedding board, test pattern or complex test pattern (see Figures 1 to 27 of IEC TS 62878-2-4:2015) including connection to the embedded device. It is recommended to use a zero ohm jumper resistor for TEG.

c) Pre-treatment

Pre-treatment shall be either 1) or 2) depending on individual specification.

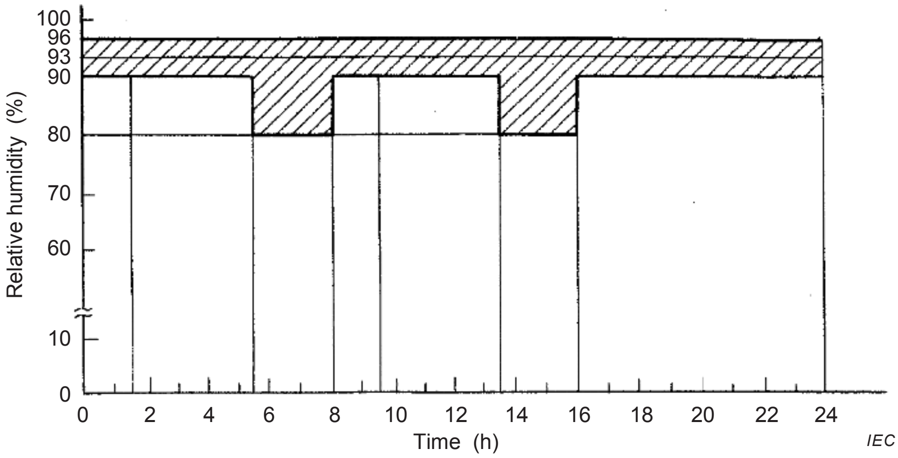
1) Leave a specimen in the standard environment for 24 h ± 4 h.

2) Leave a specimen in a bath of 85 °C ± 2 °C for 4 h and then in the standard environment for 24 h ± 4 h.

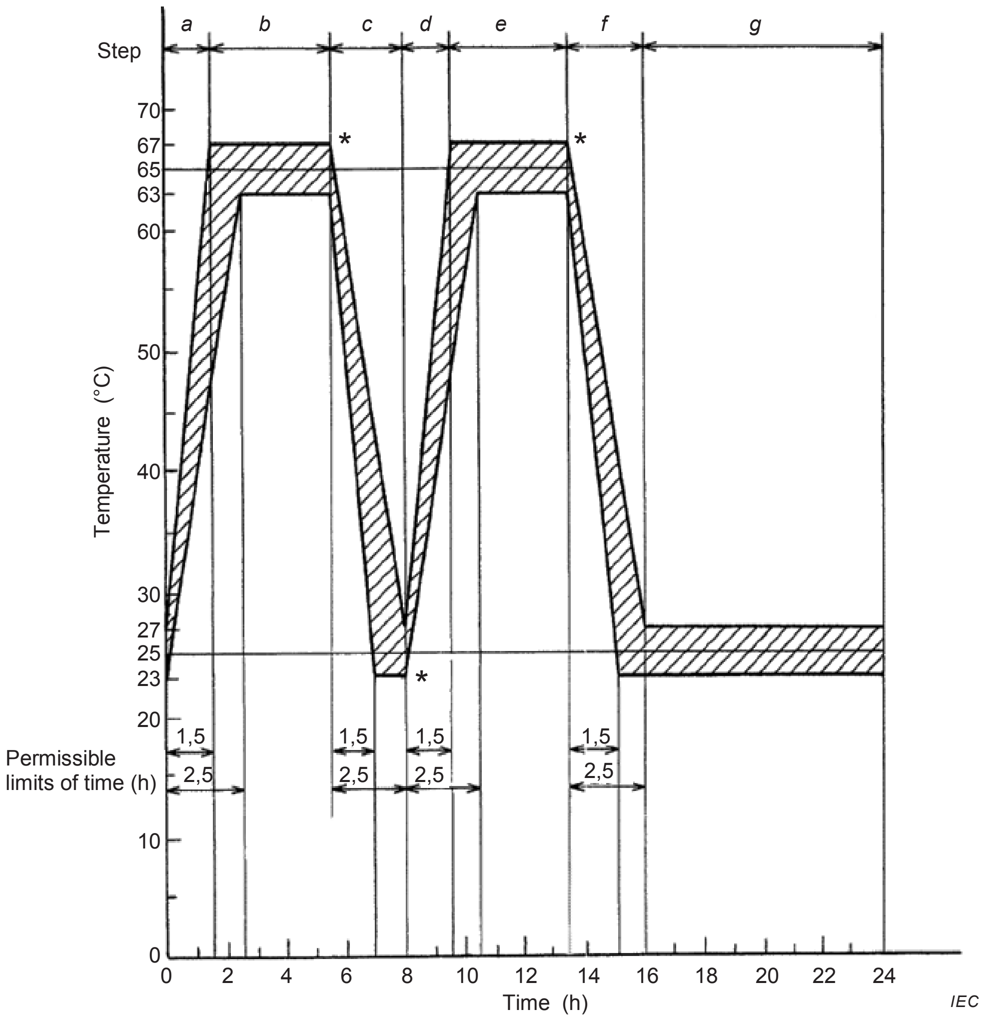
d) Test

A specimen shall be measured for its individual specification and then held in a bath with temperature of 40 °C ± 2 °C and relative humidity of 90 % to 95 %. It is recommended to pre-heat the specimen beforehand so that water drops do not appear on the surface of the specimen. Leave the specimen in the bath for a specified time or 240 h when the time is not specified. Wipe the specimen surface if there is a water drop on the specimen surface and then measure the items specified in its individual specification. A specimen damaged in this test (e.g. mechanical damage, flush over, spark over or breakdown) shall not be used in other tests.

Apply a DC voltage of 10 V ± 1 V, 50 V ± 5 V, 100 V ± 10 V or 500 V ± 50 V depending on individual specification for 1 min and then measure the insulation resistance while applying the voltage.



a) Humidity cycle



b) Temperature cycle

* The permissible limits at this time point are ± 5 min.

Figure 15 – Temperature and humidity cycles

Table 16 – Resistance to humidity characteristics and test methods

<table>
<tr><th colspan="2">Item</th><th>Characteristics</th><th>Test method</th></tr>
<tr><td>Between embedded device terminals</td><td>Resistance to humidity (temperature and humidity cycle)</td><td>Resistance shall be larger than the following values:
<table>
<tr><th>Minimum conductor thickness or insulation gap
x
mm</th><th>Insulation resistance

Ω</th></tr>
<tr><td>0,02 ≦ x < 0,05</td><td>5×10^7</td></tr>
<tr><td>0,05 ≦ x < 0,13</td><td>1×10^8</td></tr>
<tr><td>0,13 ≦ x</td><td>5×10^8</td></tr>
</table></td><td>Refer to 4.5.4</td></tr>
</table>

4.6 Mechanical environmental test – Resistance to migration

4.6.1 General

The resistance to migration test enables to measure the insulation resistance decrease after applying a potential between conductor layers in a board at a certain temperature and humidity environment in order to induce metal ion resolution into an insulation layer to reduce the insulation resistance. Table 17 shows the resistance to migration characteristics and test methods.

In order to check resistance to migration, the following are recommended:

4.6.2 Equipment

a) Structure of test equipment

- The chamber shall be able to keep an air velocity at the air blowing outlet of 2,5 m/s.
- It shall be possible to check temperature and humidity of the chamber using a detector installed in the chamber.
- The temperature and humidity deviation in the effective area of the chamber shall be ± 2 °C and ± 3 % RH, respectively.
- The material of the chamber shall not affect the specimen and humidifying water.

b) Conditions for the test equipment

- It shall be possible to control temperature and humidity in the chamber within a specified range.
- The chamber shall be able to monitor temperature and humidity.
- The chamber shall have a system to supply humidifying water continuously into the chamber.
- The chamber structure shall be such that water does not drip onto the specimen.
- Impurity or any residue of previous tests shall not be left in the chamber to affect the following test.

c) Performance of the test equipment

The chamber shall be able to change periodically from 25 °C ± 3 °C to the specified high temperature. Relative humidity in the chamber shall be checked using test equipment which has a specified accuracy.

d) Insulation resistance measurement equipment

- The instrument shall be able to measure resistance of over 10^{10} Ω. It should have its own power supply and able to supply the desired test voltage or measurement voltage.
- The insulation resistance meter shall be able to change its range automatically. Insulation resistance shall be measured after applying for 1 min a measuring voltage of one of the specified values: 10 V ± 1 V, 50 V ± 5 V, 100 V ± 10 V, and 500 V ± 50 V.

e) Insulation resistance tester

The insulation resistance tester shall be able to measure resistance of over 10^{10} Ω.

f) Power supply

The power supply shall have an appropriate power capacity and shall be able to supply an arbitrary measuring voltage.

g) Materials, jig, tool to be used in the measurement

Wiring materials and specimen fixing jigs shall be clean and low in thermal conductivity and thermal capacity, and thermally isolated from each other. They shall be selected from materials not affecting the measurement considering electrical insulation characteristics, contact resistance, or contamination of specimen such as by generation of corrosive gas. Cables used in the test equipment shall be durable for long-term use in various temperature, humidity or pressure conditions.

4.6.3 Specimen

The specimen shall be a complete product or a specimen with the complex test pattern shown in Figures 1 to 27 of IEC TS 62878-2-4:2015. The specimen board shall be handled using a glove so as not to contaminate by touching with a bare hand. The number of specimens shall be either of the following but the agreement between user and supplier shall have priority.

- The number at the stage of test production shall be $n \geqq 5$ for the product AABUS.
- The number at the stage of volume production shall be $n \geqq 10$ for the product AABUS.

4.6.4 Test condition

Test condition should be as follows:

a) Standard condition

Measurement shall be made at a temperature of 15 °C to 35 °C, relative humidity of 25 % to 75 % and atmospheric pressure of 86 kPa to 106 kPa unless otherwise specified in the individual specification. The measuring environment given in 4.6.4 b) shall be used if there is any question about the result using the above standard condition, or if specifically required. It is possible to measure in a condition other than the standard condition if realization of the standard condition is difficult, or AABUS.

b) Evaluation condition

Evaluation condition shall be made at a temperature of 20 °C ± 2 °C, relative humidity of 60 % to 70 % and atmospheric pressure of 86 kPa to 106 kPa.

c) Measurement outside of the bath

The condition given in 4.6.4 a) and b) is applicable.

Table 17 – Resistance to migration characteristics and test methods

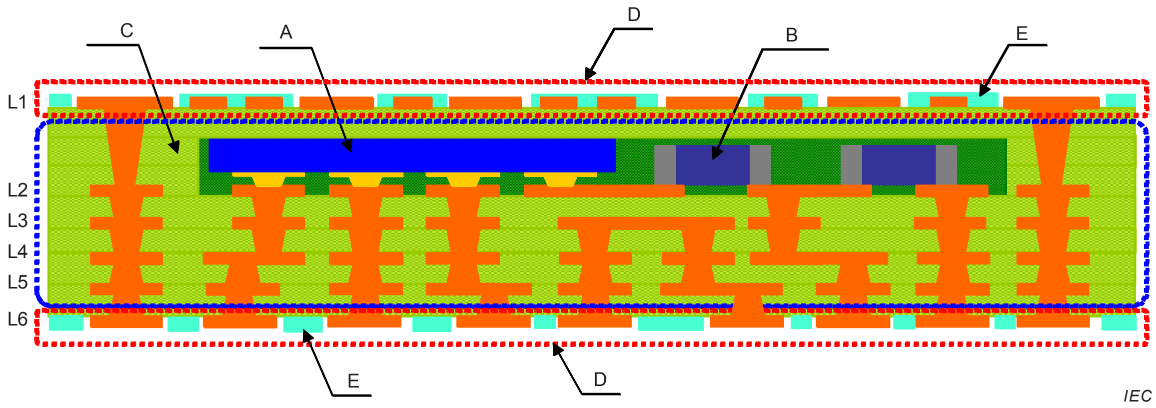
<table>
<tr><th>Item</th><th>Characteristics</th><th>Test</th></tr>
<tr><td>Embedded device and pattern.</td><td>The following value shall be attained.
<table><tr><th>Item</th><th>Specification</th></tr><tr><td>Anti-migration</td><td>≧ 1 × 10⁸ Ω</td></tr></table>Measurement shall be made after leaving the specimen for 1 h.</td><td>Refer to 4.6.1.3</td></tr>
</table>

5 Shipping inspection

5.1 General

Shipping inspection consists of checking the quality of all the products based on this standard. It is desirable to test all the products. However, sampled specimens may be tested AABUS for sampling and details of tests. The test items at shipping are specified below for device embedded boards, as illustrated in Figure 16.

The detailed items are expressed in Table 18.



Key

A Embedded active component

B Embedded passive component

C Inner layer

D Surface layer

E Solder resist

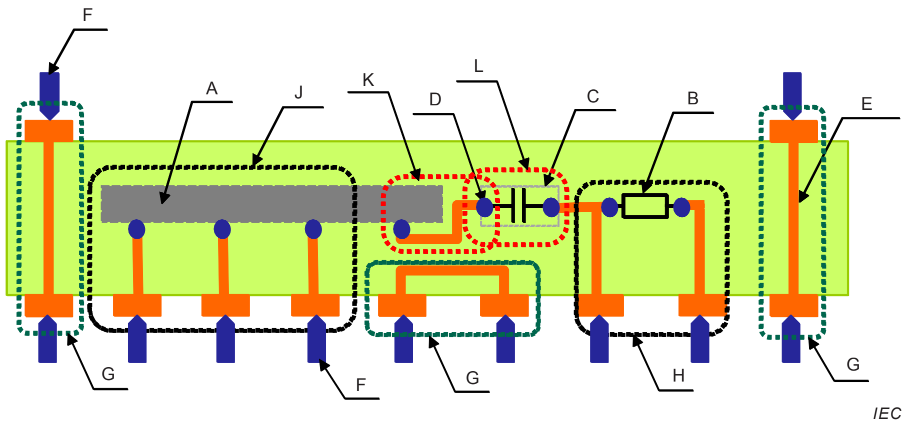
Figure 16 – Device embedded board for shipping inspection

A representative circuit construction of an electrical test is given in Figure 17. Test methods are divided into three types, a), b), and c), i.e. conduction, opening and short-circuit.

a) Test of conductor pattern not connected to embedded component (Figure 17, G).

b) Test of connection of embedded component terminals connected to the conductor pattern (Figure 17, H, J).

c) Test of connection of embedded component whose terminals are not connected to surface conductors (Figure17, K, L).



Key

A	Passive component	F	Test probe point
B	Resistor	G	Conductor not connected to embedded component
C	Capacitor	H	Conductor connected to passive component
D	Connection to embedded component	J	Conductor connected to active component
E	Conductor pattern	K, L	Conductor and embedded component not soldered to surface

Figure 17 – Typical circuit construction of device embedded board

Table 18 – Applicable items of shipping inspection

Class	Testing item		Testing range		
			Conductor pattern (Conduction/open/ short-circuit)	**Conductor pattern connected to passive component**	**Conductor pattern connected to active component**
1	Electrical test	a) Embedded component terminals are not connected to circuit.	As indicated in 5.2.2	—	—
		b) Embedded component terminals are connected to surface circuit.	—	As indicated in 5.2.3.2, 5.2.3.3, and 5.2.3.4	As indicated in 5.2.4.2, 5.2.4.3
		c) Embedded component terminals are not connected to the surface circuit.	—	As indicated in 5.2.6	
2	Visual inspection (AOI)		As indicated in 5.4		
3	Internal observation (X-ray test)		As indicated in 5.3		
4	Electrical test		NA	As indicated in 5.2	NA
5	Functional test		NA	NA	NA

5.2 Electrical test

5.2.1 General

Tests of conduction and the opening of the conductor pattern not connected to embedded components are similar to the general electrical test of the circuit board. Electrical tests for embedded passive component terminals and conductor pattern electrical tests are made by conduction, opening and short-circuit tests of the circuit including passive component terminals. Tests for the construction having embedded active components shall be carried out after the completion of the circuit. Electrical tests are classified into the following as shown in Figure 18.

- Test of conduction, opening and short-circuiting of the conductor pattern that is not connected to an embedded component.
- Test of conduction, opening and short-circuiting of the conductor pattern which can be reached from a surface layer.
- Test of conduction, opening and short-circuiting of conductor pattern of connection terminals of embedded active devices: IC (integrated circuit), LSI (large scale integration), transistor, diode.

5.2.2 Test of conductor pattern not connected to an embedded component

Tests of conductor patterns not connected to an embedded component, as shown in Figure 19, are carried out like electrical tests for the general electronic circuits.

In order to perform the test of conductor pattern not connected to an embedded component, a) to c) apply:

a) Equipment

The equipment used in the test is similar to the one stated below and includes electrical connection jigs to obtain electrical connection to the specified part of the conductor pattern.

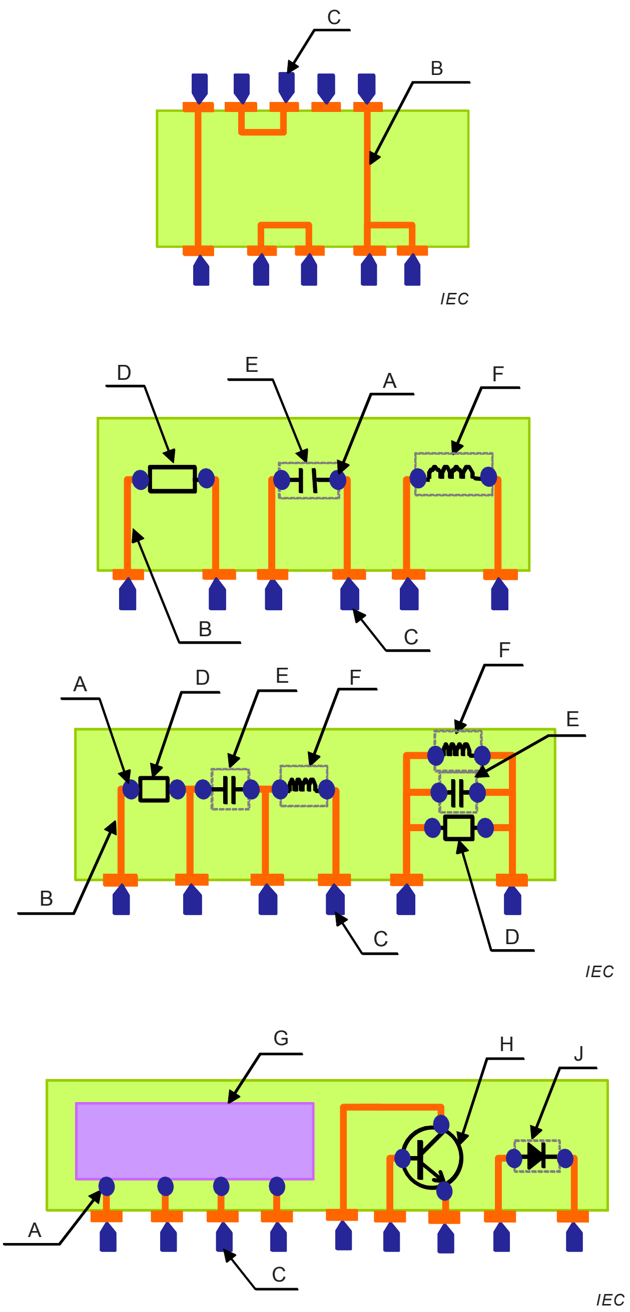
- The equipment shall be able to test the conductor pattern and via resistance by the voltage drop method. In case good measurement accuracy is required in the measurement of the very small resistor, the four-terminal method equipment may be used AABUS.
- The test signal (voltage or current) shall be a DC signal or an AC signal of less than 1 MHz.
- The test range shall be 1 mΩ to 100 MΩ. The values shall be AABUS.
- The test equipment shall be calibrated before the tests.

b) Pre-treatment

It is recommended to wash and clean, and to remove rust and other foreign materials on the testing probe points of the conductor circuit or pattern as the contact resistance may result in erroneous measurements.

c) Inspection and evaluation

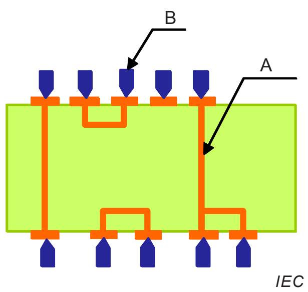
The conductivity of the circuit is considered acceptable if the measured resistance is within the stated values when a specified voltage and/or current is applied to the specified part of the conductor pattern. No short-circuit occurs when the measured resistance between different networks exceeds the specified minimum resistance. The applied voltage, the applied current, the signal application time, the specified resistance and the minimum allowable resistance are to be AABUS.



Key

A	Connection to embedded component
B	Conductor pattern
C	Testing probe point
D	Resistor
E	Capacitor
F	Inductor
G	Integrated circuit, large scale integration
H	Transistor
J	Diode

Figure 18 – Examples of evaluation levels of electrical test



Key

A	Conductor pattern
B	Testing probe point

Figure 19 – Circuit construction not connected to embedded component

5.2.3 Test on the pattern having a passive component and a conductor pattern

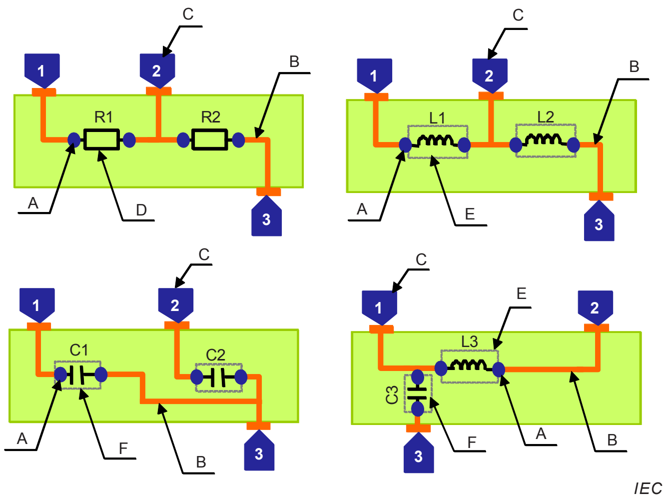
5.2.3.1 General

Tests of conduction for embedded passive components vary depending on whether the connections to the embedded component are connected to the surface conductor pattern or not. Test methods are specified in this standard for typical circuit cases as stated below. Inspection shall be carried out by measuring the component resistance of the circuit impedance using a DC signal or an AC signal of less than 1 MHz frequency. No test for an embedded component shall be carried out during this inspection.

- Test for conductivity including testable terminals of an embedded passive component and a conductor pattern on surface.
- Test for conductivity including testable parallel connected terminals of an embedded passive component and a conductor pattern on surface.
- Test for conductivity including series connected terminals that cannot be tested as embedded passive components and the surface conductor pattern.

5.2.3.2 Test of a circuit having both individual passive component(s) and a conductor pattern

This is a test to confirm conductance, in open and short-circuit of a component embedded board as shown in Figure 20, which has connections from embedded component terminal(s) and individual or common connections to the surface pattern. This test consists of measuring the resistance, inductance or capacitance using a DC or an AC signal of less than 1 MHz frequency. The performance characteristics of resistance, inductance or capacitance of embedded component(s) are not verified by this test. The testing current and voltage are within the rated values of the embedded components.



Key

A Connection to an embedded component

B Conductor pattern

C Testing probe point

D Resistor

E Inductor

F Capacitor

EXAMPLE

Measurement between 1 and 2
Measurement between 1 and 3
Measurement between 2 and 3

Figure 20 – Circuit construction which is capable of independent check

In order to perform test of a circuit having both individual passive component(s) and a conductor pattern, a) to c) apply:

a) Equipment

The equipment shall consist of components equivalent to the ones described below and including testing jigs to obtain electrical connections to the specimen.

- The equipment shall be able to measure resistance and impedance.
- The testing signal (voltage or current) shall be a DC or an AC signal of less than 1 MHz frequency.
- The measuring range of resistance is 1 mΩ to 100 MΩ. However, the values agreed upon between user and supplier take priority.
- The test equipment shall be calibrated before the tests.

b) Pre-treatment

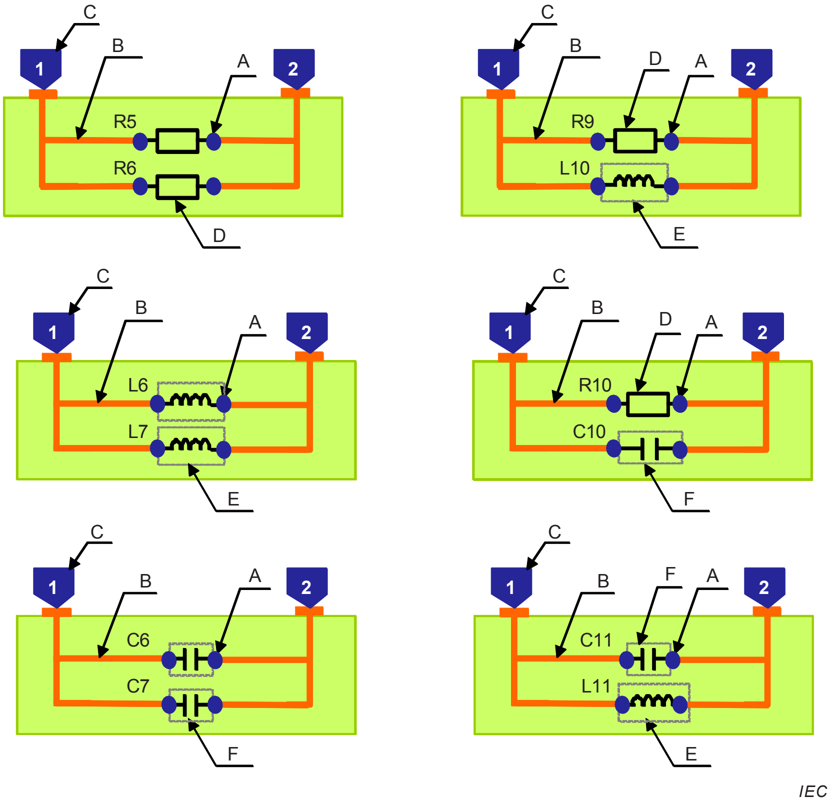
Pre-treatment shall comply with 5.2.3.2 b).

c) Inspection and evaluation

The conductivity of the circuit is considered acceptable if the measured resistance is within the stated values when the specified voltage and/or current is applied to the specified part of the conductor pattern. No short-circuit occurs when the measured resistance between different networks exceeds the specified minimum resistance. The applied voltage, the current, the signal application time, the specified resistance and the minimum allowable resistance are to be AABUS.

5.2.3.3 Test of a circuit having both passive component(s) and a conductor pattern in parallel connections

The circuit whose terminal connections of embedded passive components are connected in parallel to the surface pattern as shown in Figure 21 cannot check the individual component and conductor pattern. Conduction, the opening and short-circuiting of the circuit shall be confirmed by measuring the composite resistance or composite impedance of a composite circuit of resistors, inductors and capacitors of the circuit by applying a DC or an AC signal of less than 1 MHz. The applied signal for the test shall be within the rated value of embedded components.



Passive components of a similar type **Passive components of a different type**

Key

A	Connection to embedded component	D	Resistor
B	Conductor pattern	E	Inductor
C	Measuring probe	F	Capacitor

EXAMPLE

Measurement between 1 and 2

Figure 21 – Circuit construction for parallel connection of passive components

In order to test a circuit having both passive component(s) and a conductor pattern in parallel connections, a) to c) apply:

a) Equipment

The equipment shall consist of a component equivalent to the ones described below and including testing jigs to obtain electrical connections to the specimen.

- The equipment shall be able to measure composite resistance and impedance.
- The testing signal (voltage or current) shall be a DC or an AC signal of less than 1 MHz frequency.
- The measuring range of resistance is 1 mΩ to 100 MΩ. However, the values agreed upon between user and supplier take priority.
- The test equipment shall be calibrated before tests.

b) Pre-treatment

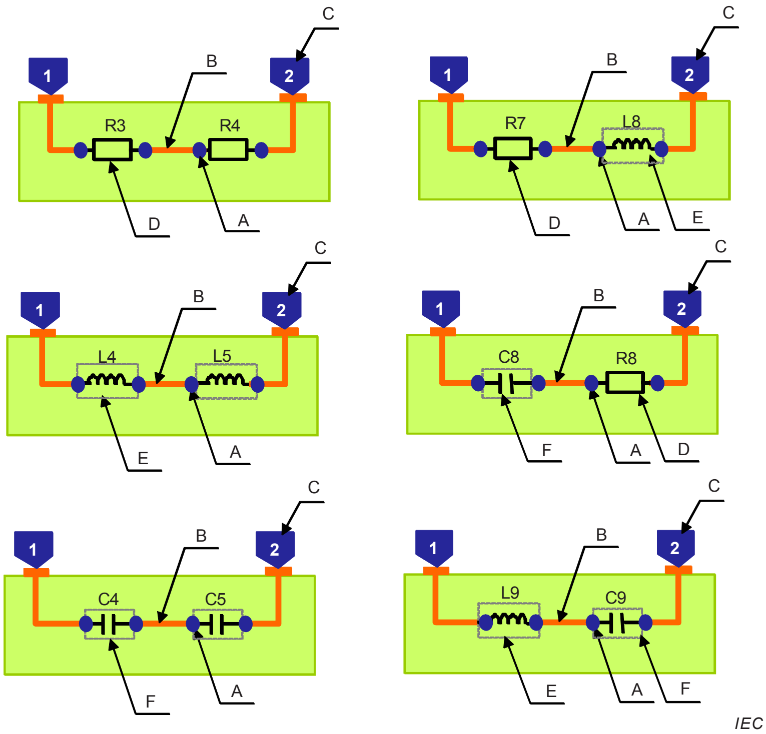
Pre-treatment shall comply with 5.2.2 b).

c) Inspection and evaluation

The conductivity of the circuit is considered acceptable if the measured composite impedance of the circuit including resistor(s), inductor(s) and capacitor(s) is within the stated values when the specified voltage and/or current is applied to the specified part of the conductor pattern. No short-circuit occurs when the measured resistance between different networks exceeds the specified minimum resistance. The applied voltage, the current, the signal application time, the specified resistance and the minimum allowable resistance are to be AABUS.

5.2.3.4 Test of a circuit having both in series connected passive component(s) and a conductor pattern

In the circuit whose terminal connections of embedded passive components are connected in series to the surface pattern, as shown in Figure 22, the individual component and conductor pattern cannot be checked. Conduction, opening and short-circuiting of the circuit shall be confirmed by measuring the composite resistance or composite impedance of a composite circuit of resistors, inductors and capacitors of the circuit by applying a DC or an AC signal of less than 1 MHz. The applied signal for the test shall be within the rated value of embedded components.



Passive component of the same type **Passive component of a different type**

Key

A Connection to embedded component
B Conductor pattern
C Measuring probe
D Resistor
E Inductor
F Capacitor

EXAMPLE

Measurement between 1 and 2

Figure 22 – Circuit construction for series connection of passive components

5.2.4 Test of a circuit having both active component(s) and a conductor pattern

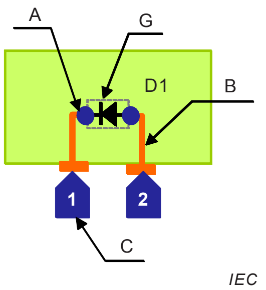
5.2.4.1 General

It is difficult to standardize a test method of a circuit composed of various types of active components and a circuit consisting of various types of passive components and conductor patterns. A test method is presented in this standard for an embedded diode as a guide. This test is given as an example because it can be carried out rather simply in production for the test of conduction, opening or short-circuiting of a circuit having terminal connections of an embedded active component and conductor pattern.

5.2.4.2 Test of a circuit having both individual active component(s) and a conductor pattern

The test of an individual embedded active device such as a diode or a transistor which has a terminal connection connected to a surface conductor pattern, as illustrated in Figures 23 and 24, can be carried out for conduction, opening and short-circuiting of embedded components and conductor patterns by measuring the voltage by applying a DC current.

Characteristics of the embedded diode or the transistor are not measured. The signal applied for the test shall be within the rated value of the embedded components.



Key

A Terminal connection of embedded component

B Conductor pattern

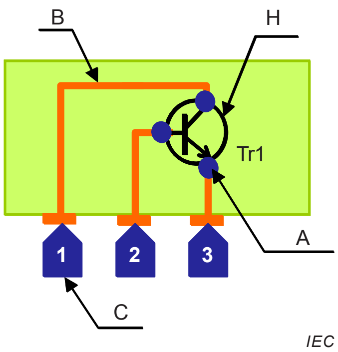
C Testing probe point

G Diode

EXAMPLE

Measurement between 2 and 1

Figure 23 – Circuit construction of embedded diode



Key

A Connection of embedded component

B Conductor pattern

C Testing probe point

H Transistor

EXAMPLE

Measurement between 2 and 1
Measurement between 2 and 3

Figure 24 – Circuit construction of transistor circuit

In order to perform test of a circuit having both individual active component(s) and a conductor pattern, a) to c) apply:

a) Equipment

The equipment shall consist of a component equivalent to the ones described below and that include testing jigs to obtain electrical connections to the specimen.

- The equipment shall be able to supply a constant current and to measure the voltage.
- The testing signal (voltage or current) shall be DC and 0 to 1 V.
- The measuring range of the resistance is 0 to 1 V. However, the values agreed upon between user and supplier take priority.
- The test equipment shall be calibrated before tests.

b) Pre-treatment

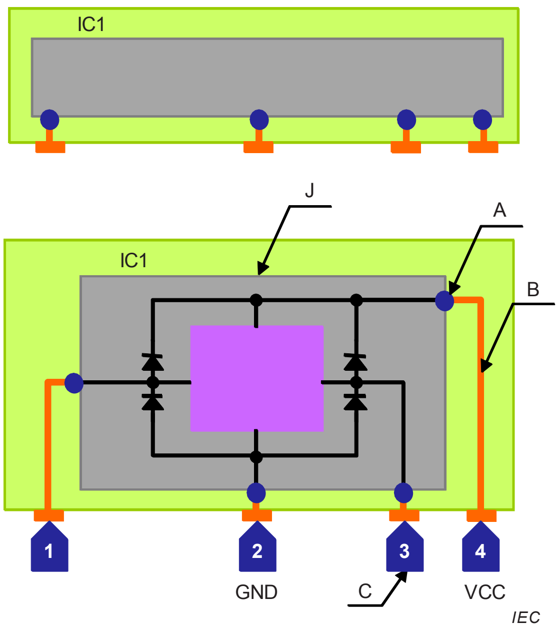
Pre-treatment shall comply with 5.2.2 b).

c) Inspection and evaluation

The conductivity of the circuit is considered acceptable if the measured voltage is within the stated values when the specified voltage and/or current is applied to the specified part of a diode or a transistor and a conductor pattern. No short-circuit occurs when the measured resistance between different networks exceeds the specified minimum resistance. The applied voltage, the applied current, the signal application time, the specified resistance and the minimum allowable resistance are to be AABUS.

5.2.4.3 Test of a circuit having IC, LSI and a conductor pattern

The test of an individual embedded active device such as an IC or LSI which has a terminal connection and is connected to a surface conductor pattern, as illustrated in Figure 25, can be carried out for conduction, opening and short-circuiting of the embedded component and conductor pattern by measuring the voltage at the component applying a DC current to the embedded diode. The characteristics of an embedded IC or LSI are not measured. The applied signal for the test shall be within the rated value of embedded components.



Key

A Connection of embedded component

B Conductor pattern

C Testing probe point

J Integrated circuit (IC), large scale integration

EXAMPLE

Measurement between 1 and 4
Measurement between 2 and 3
Measurement between 3 and 4

Figure 25 – Circuit construction of a conductor pattern with embedded IC and LSI

In order to perform test of a circuit having IC, LSI and a conductor pattern, a) to c) apply:

a) Equipment

The equipment shall comply with 5.2.4.2 a).

b) Pre-treatment

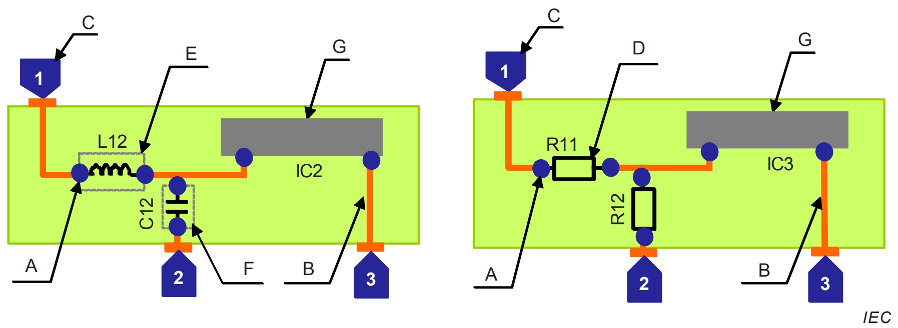
Pre-treatment shall comply with 5.2.2 b).

c) Inspection and evaluation

The conductivity of the circuit containing embedded IC and LSI is considered acceptable if the measured voltage is within the stated values when specified current is applied to the specified part of the conductor pattern. No short-circuit occurs when the measured resistance between different networks exceeds the specified minimum resistance. The applied voltage, the applied current, the signal application time, the specified resistance and the minimum allowable resistance are to be AABUS.

5.2.5 Test of a circuit having connections of both individual passive component(s) and conductor pattern

The test of an individual embedded active device such as an IC or LSI which has a terminal connection connected to the surface conductor pattern via a passive component, as illustrated in Figure 26, can be carried out for conduction, opening and short-circuiting of an embedded component and conductor pattern by measuring the voltage at the component by applying a DC current or an AC signal of a frequency of less 1 MHz to the embedded IC or LSI. The characteristics of the embedded IC or LSI are not measured. The applied signal for the test shall be within the rated value of the embedded components.



Key

A	Connection of embedded component	E	Inductor
B	Conductor pattern	F	Capacitor
C	Testing probe point	G	Integrated circuit (IC), large scale integration
D	Resistor		

EXAMPLE

Measurement between 1 and 2
Measurement between 1 and 3
Measurement between 2 and 3

Figure 26 – Circuit construction composed of a passive component and an active component

In order to test a circuit having connections of both individual passive component(s) and conductor pattern, a) to c) apply.

a) Equipment

The equipment shall comply with 5.2.4.2 a).

b) Pre-treatment

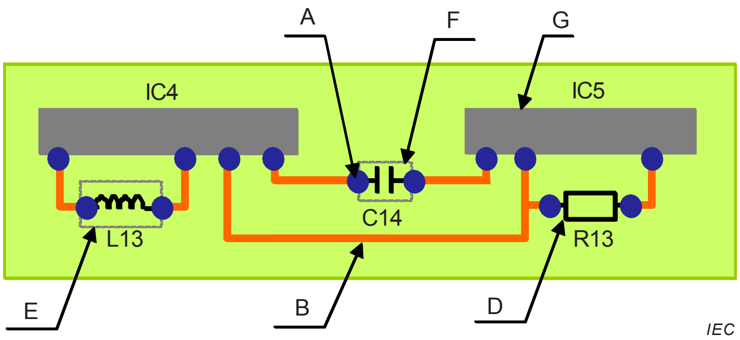
Pre-treatment shall comply with 5.2.2 b).

c) Inspection and evaluation

The conductivity of the circuit containing embedded IC and LSI is considered acceptable if the measured voltage is within the stated values when the specified current is applied to the specified part of the conductor pattern. No short-circuit occurs when the measured resistance between different networks exceeds the specified minimum resistance. The applied voltage, the applied current, the signal application time, the specified resistance and the minimum allowable resistance are to be AABUS.

5.2.6 Test of a circuit having an embedded component which cannot be checked from the surface and a conductor pattern

The quality guarantee of an embedded structure which cannot be tested from the surface as illustrated in Figure 27 shall be AABUS.



Key

A Connection of embedded component

B Conductor pattern

D Resistor

E Inductor

F Capacitor

G IC, LSI

Figure 27 – Circuit construction of embedded components having no connection terminal on the surface

5.3 Internal transparent test

A device embedded board contains embedded components inside the board and cannot be observed from outside. The status of an embedded component may be checked using X-ray which can check the inside of a board. The X–ray test demands appreciable work. Use of an X-ray inspection shall be as AABUS. The X-ray inspection may be used as one of the product reliability tests.

In order to perform the internal transparent test, a) to c) apply:

a) Equipment

The equipment shall be X-ray inspection equipment which can inspect the inside of a specimen by means of X-rays.

b) Pre-treatment

Pre-treatment shall comply with 5.2.2 b).

c) Inspection and evaluation

The test equipment and test method shall be AABUS. The evaluation of the test result shall be in accordance with the individual specification.

5.4 Visual test

The appearance of a device embedded board seems exactly the same as that of an ordinary electric circuit board as embedded components are embedded within the board and cannot be observed from outside. The visual test of a device embedded board is like the visual test of an ordinary electric circuit board. The visual test method shall be AABUS. The method described here is a guideline and not to be used as a standard.

In order to perform visual test, a) to c) apply:

a) Equipment

The equipment should correspond to one of the following two descriptions:

- observation by the naked eye using a magnifying glass or a microscope;
- AOI (automatic optical inspection).

b) Pre-treatment

The surface treatment shall be carried out according to the individual specification.

c) Inspection and evaluation

The equipment for the test and the test method shall be AABUS. The evaluation of the test result shall be in accordance with the individual specification.

Annex A
(informative)

Related test methods

Table A.1 lists related test method standards.

Table A.1 – Related test methods

Test	Name of test and equipment	IEC	ISO and others
	Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 2: Test methods for materials for interconnection structures	IEC 61189-2	
	Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 3:Test methods for interconnection structures (printed boards)	IEC 61189-3	
Environmental tests	Environmental testing – Part 1 General and guidance	IEC 60068-1	
	Test methods for electrical materials, interconnection structures and assemblies – Part 1: General test methods and methodology	IEC 61189-1	
	Testing condition and environment for plastics		ISO 291
Visual test and micro-sectioning	IEC 61198-3		
Dimensions	IEC 61189-3		
	Venire gauge		ISO 6906 ISO 3599
	Micrometer		ISO 3611
	Height gauge	—	—
	Precision plate		ISO 8512-1 ISO 8512-2
	Gap gauge	—	—
Electrical tests	IEC 61189-3		
Conductor resistance	IEC 61189-3	3E12	
Withstand current	IEC 61189-3	3E15	
Withstand voltage	IEC 61189-3	3E09, 3E10	
AC voltage	IEC 61189-3	3E09, 3E10	
DC voltage	IEC 61189-3	3E09, 3E10	
Insulation resistance	IEC 61189-3	3E03, surface layer 3E05, between layers	
Circuit isolation and conductivity	IEC 61189-3	3E01, isolation 3E02, continuity	
Mechanical tests	IEC 61189-3		
Peel strength	IEC 61189-3	3M01, standard atmosphere	

Test	Name of test and equipment	IEC	ISO and others
Peeling strength of land without plated land hole	IEC 61189-3	3M07	
Pulling strength of plated through hole for component mounting	IEC 61189-3	3M03	
Pulling strength of land pattern pad	IEC 61189-3	3M07	
Adhesivity of plating	IEC 61189-3	3M01	
Cellophane adhesive tape		3M01	—
Adhesive tape and sheet		—	ISO 29862 ISO 29863 ISO 29864
Adhesivity of solder resist and symbol marks	IEC 61189-3	3M01	
Cross cut test	IEC 61189-3	IEC 61189-3	ISO 2409
Cellophane adhesive tape		IEC 61189-3	—
Adhesive tape and sheet		—	ISO 29862 ISO 29863 ISO 29864
Carbon steel cutter knife			ISO 4957
Coated film hardness (solder resist and symbol marks)	IEC 61189-3	3M01	
	Paint test, general (scratch hardness)		ISO 15184
	Pencil, pencil colour and lead used		ISO 9180
	Polishing paper		ISO 3366 ISO 21948
Environmental tests	IEC 61189-3		
High temperature	Environmental testing – IEC 60068-2-2: Test B: Dry heat	IEC 60068-2-2	
Low temperature	IEC 60068-2-1: Test A: Cold	IEC 60068-2-1	
Thermal shock (high and low temperatures)	IEC 61189-3	3N01 to 3N05	
	IEC 60068-2-14: Test N: Change of temperature	IEC 60068-2-14	
	IEC 60068-2-30: Test Db: Dump heat, cyclic (12 h + 12 h cycle)	IEC 60068-2-30	
	IEC 60068-2-38: Test Z/AD: Composite temperature/humidity cycle test	IEC 60068-2-38	
Resistance to humidity	IEC 61189-3	3N06	
	IEC 60068-2-78: Test Cab: Damp heat, steady state	IEC 60068-2-78	
Migration	IEC TR 62866	3E20	—
	IEC 60068-2-66: Test Cx: Damp heat, steady state (unsaturated pressurized vapour)	IEC 60068-2-66	
	Flux for soldering		ISO 9455
Vibration	IEC 60068-2-53: Test and guidance – combined climatic (temperature/humidity	IEC 60068-2-53	
	IEC 60068-2-6: Test Fc: Vibration (sinusoidal)	IEC 60068-2-6	

Test	Name of test and equipment	IEC	ISO and others
	IEC 60068-2-64: Test Fh: Vibration, broadband random and guidance	IEC 60068-2-64	
	IEC 60068-2-80: Test Fi: Vibration-mixed mode	IEC 60068-2-80	
Drop shock	IEC 62137-1-3: Surface mounting technology – Environmental and endurance test methods for surface mount solder joint – Part 1-3: Cyclic drop test	IEC 62137-1-3	JASO D 0143
Bending	IEC 62137-1-4: Surface mounting technology – Environmental and endurance test methods for surface mount solder joint – Part 1-4: Cyclic bending test	IEC 62137-1-4	—
Screwing	IEC 60068-2-21: Test U: Robustness of terminations and integral mounting devices	IEC 60068-2-21	—
Chemical tests	IEC 61189-3		
Flammability	IEC 61189-3	3C03 (to be revised)	
Resistance to chemicals	IEC 61189-3	3C04	
Solderability	IEC 60068-2-58: Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices	IEC 60068-2-58	
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	Rosin	—	—
	Propanol		ISO 6353-3
	Ethanol		ISO 6353-2
Resistance to soldering heat	IEC 60068-2-20: Test T: Test methods for solderability and resistance to soldering heat of devices with leads IEC 60068-2-58: Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices	IEC 60068-2-20 IEC 60068-2-58	
	IEC 60068-2-20: Test T: Test methods for solderability and resistance to soldering heat of devices with leads	IEC 60068-2-20	
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