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BSI Standards Publication

Thyristor valves for thyristor controlled series capacitors (TCSC) — Electrical testing

National foreword

This British Standard is the UK implementation of EN 62823:2015. It is identical to IEC 62823:2015.

The UK participation in its preparation was entrusted to Technical Committee PEL/22, Power electronics.

A list of organizations represented on this committee can be obtained on request to its secretary.

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English Version

Thyristor valves for thyristor controlled series capacitors (TCSC) - Electrical testing (IEC 62823:2015)

Valves à thyristors pour condensateurs série commandés par thyristors (CSCT) - Essai électrique (IEC 62823:2015)

Thyristorventile für thyristorgesteuerte Reihenkondensatoren (TCSC) - Elektrische Prüfung (IEC 62823:2015)

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Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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European foreword

The text of document 22F/342/CDV, future edition 1 of IEC 62823, prepared by SC 22F "Power electronics for electrical transmission and distribution systems", of IEC/TC 22 "Power electronic systems and equipment" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62823:2015.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2016-06-24
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2018-09-24

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In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60068-1	NOTE	Harmonized as EN 60068-1.
IEC 60143-1	NOTE	Harmonized as EN 60143-1.
IEC 60721-1	NOTE	Harmonized as EN 60721-1.
IEC 61000-6-5	NOTE	Harmonized as EN 61000-6-5.
IEC 61954	NOTE	Harmonized as EN 61954.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

Publication	Year	Title	EN/HD	Year
IEC 60060-1	2010	High-voltage test techniques - Part 1: General definitions and test requirements	EN 60060-1	2010
IEC 60071-1	-	Insulation co-ordination - Part 1: Definitions, principles and rules	EN 60071-1	-
IEC 60071-2	-	Insulation co-ordination - Part 2: Application guide	EN 60071-2	-
IEC 60270	-	High-voltage test techniques - Partial discharge measurements	EN 60270	-

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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THYRISTOR VALVES FOR THYRISTOR CONTROLLED SERIES CAPACITORS (TCSC) – ELECTRICAL TESTING

FOREWORD

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International Standard IEC 62823 has been prepared by subcommittee 22F: Power electronics for electrical transmission and distribution systems, of IEC technical committee 22: Power electronic systems and equipment.

The text of this standard is based on the following documents:

CDV	Report on voting
22F/342/CDV	22F/354A/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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THYRISTOR VALVES FOR THYRISTOR CONTROLLED SERIES CAPACITORS (TCSC) – ELECTRICAL TESTING

1 Scope

This International Standard defines routine and type tests on thyristor valves used in thyristor controlled series capacitor (TCSC) installations for AC power transmission.

The tests specified in this International Standard are based on air insulated valves operating in capacitive boost mode or bypass mode. For other types of valve and for a valve operating in inductive boost mode, the test requirements and acceptance criteria are agreed between purchaser and supplier.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60060-1:2010, *High-voltage test techniques – Part 1: General definitions and test requirements*

IEC 60071-1, *Insulation co-ordination – Part 1: Definitions, principles and rules*

IEC 60071-2, *Insulation co-ordination – Part 2: Application guide*

IEC 60270, *High-voltage test techniques – Partial discharge measurements*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
thyristor valve
electrically and mechanically combined assembly of thyristor levels, complete with all connections, auxiliary components and mechanical structures, which can be connected in series with each phase of the reactor of a TCSC

3.2
valve section
electrical assembly, comprising a number of thyristors and other components, which exhibits prorated electrical properties of a complete valve

Note 1 to entry: This term is mainly used to define a test object for valve testing purposes.

3.3
thyristor level
<of a valve> part of a valve comprising an anti-parallel connected pair of thyristors together with their immediate auxiliaries, and reactor, if any

3.4
redundant thyristor levels, pl
maximum number of thyristor levels in the thyristor valve that may be short-circuited, externally or internally, during service without affecting the safe operation of the thyristor valve as demonstrated by type tests and which, if and when exceeded, would require either the shutdown of the thyristor valve to replace the failed thyristors or the acceptance of increased risk of failures

3.5
valve arrester
arrester connected across a valve

3.6
valve electronics
VE
electronic circuits at valve potential(s) that perform control functions

Note 1 to entry: This note applies to the French language only.

3.7
valve interface electronics unit
electronic unit which provides an interface between the control equipment, at earth potential, and the valve electronics or valve devices

Note 1 to entry: Valve interface electronics units, if used, are typically located at earth potential close to the valve(s).

Note 2 to entry: The term "valve base electronics" (VBE) is also used to designate this unit.

3.8
thyristor-controlled series capacitor bank
TCSC bank
assembly of thyristor valves, reactor(s), capacitors, and associated auxiliaries, such as structures, support insulators, switches, and protective devices, with control equipment required for a complete operating installation

3.9
TCSC reactor
one or more reactors connected in series with the thyristor valve

SEE: Figure 1, item 4.

3.10
valve enclosure
platform-mounted enclosure containing thyristor valve(s) with associated valve cooling and electronic hardware

3.11
temporary overload
short-term overload capability of the TCSC at rated frequency and ambient temperature range

SEE: Figure 5.

Note 1 to entry: Temporary overload is typically of several seconds duration, less than 10 s.

3.12
valve protective firing
means of protecting the thyristors from excessive voltage by firing them at a predetermined voltage

3.13
line current
i_L
power frequency line current

SEE: Figure 2.

3.14
rated current
I_N
RMS line current (I_L) at which the TCSC should be capable of continuous operation with rated reactance (X_N) and rated voltage (U_N)

3.15
valve current
i_V
current through the thyristor valve

SEE: Figure 2.

3.16
bypass current
current flowing through the thyristor valve in parallel with the series capacitor, when the series capacitor is bypassed

3.17
capacitor voltage
U_C
voltage across the TCSC

SEE: Figure 2.

3.18
nominal reactance
X_N
nominal power frequency reactance for each phase of the TCSC with nominal boost factor

3.19
rated TCSC voltage
U_N
power frequency voltage across each phase of the TCSC that can be continuously controlled at nominal reactance (X_N), rated current (I_N), nominal power frequency, and ambient temperature range

3.20
apparent reactance
$X(\alpha)$
TCSC apparent power frequency reactance as a function of thyristor control angle (α)

SEE: Figure 3, Figure A.1 and Formula A.1.

3.21
rated capacitance
C_N
capacitance value for which the TCSC capacitor has been designed

3.22
physical reactance
X_C
power frequency reactance for each phase of the TCSC bank with thyristors blocked and a capacitor internal dielectric temperature of 20 °C

$$X_C = 1/(\omega_N \cdot C_N)$$

3.23
boost factor
k_B
the ratio of apparent reactance $X(\alpha)$ divided by physical reactance X_C

$$k_B = X(\alpha) / X_C$$

3.24
conduction interval
σ
part of a half of a power frequency cycle during which a thyristor valve is in the conducting state

$$\sigma = 2\beta$$

SEE: Figure 3**.**

3.25
control angle
α
time expressed in electrical angular measure from the capacitor voltage (U_C) zero crossing to the starting of current conduction through the thyristor valve

SEE: Figure 3.

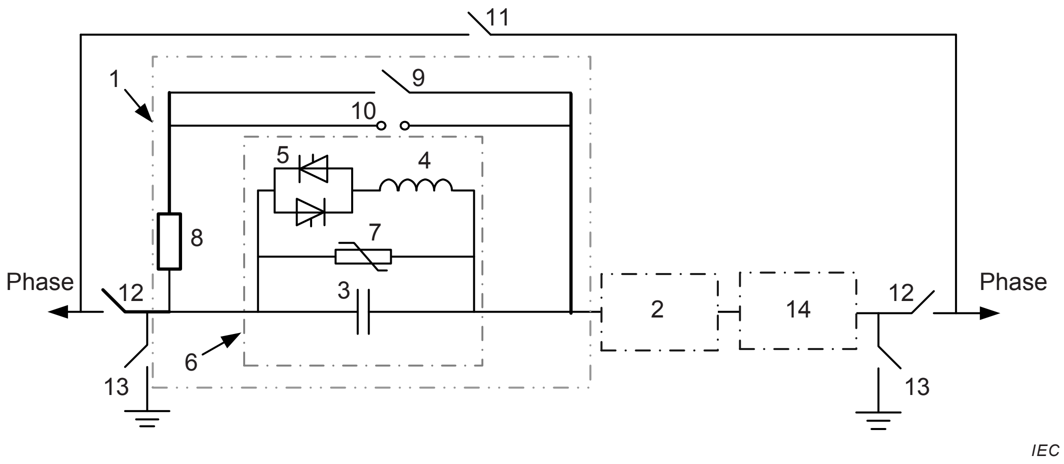
3.26
internal fault
line fault occurring within the protected line section containing the series TCSC subsegment

3.27
external fault
line fault occurring outside the protected line section containing the series TCSC subsegment

4 TCSC valve and valve operation in general

4.1 TCSC installation and TCSC valve

Transmission line series reactance can be compensated by combinations of fixed series capacitors (FSC) and TCSC based controllable segments, as shown in Figure 1. A TCSC subsegment uses a thyristor-controlled reactor (TCR) in parallel with a capacitor bank with the rated capacitance C_N, as shown in Figure 2. The thyristor valve used in this TCSC subsegment is a TCSC valve (See Figure 1, item 5).



Key

1	TCSC unit	8	Discharge current limiter, if applicable
2	Additional TCSC unit when required	9	Bypass switch
3	TCSC capacitor	10	Bypass gap
4	TCSC reactor	11	External bypass disconnector
5	TCSC thyristor valve	12	External isolating switch
6	TCSC subsegment	13	External earth switch
7	Capacitor arrester	14	Additional FSC unit when required

Figure 1 – Typical connection and nomenclature of a TCSC installation

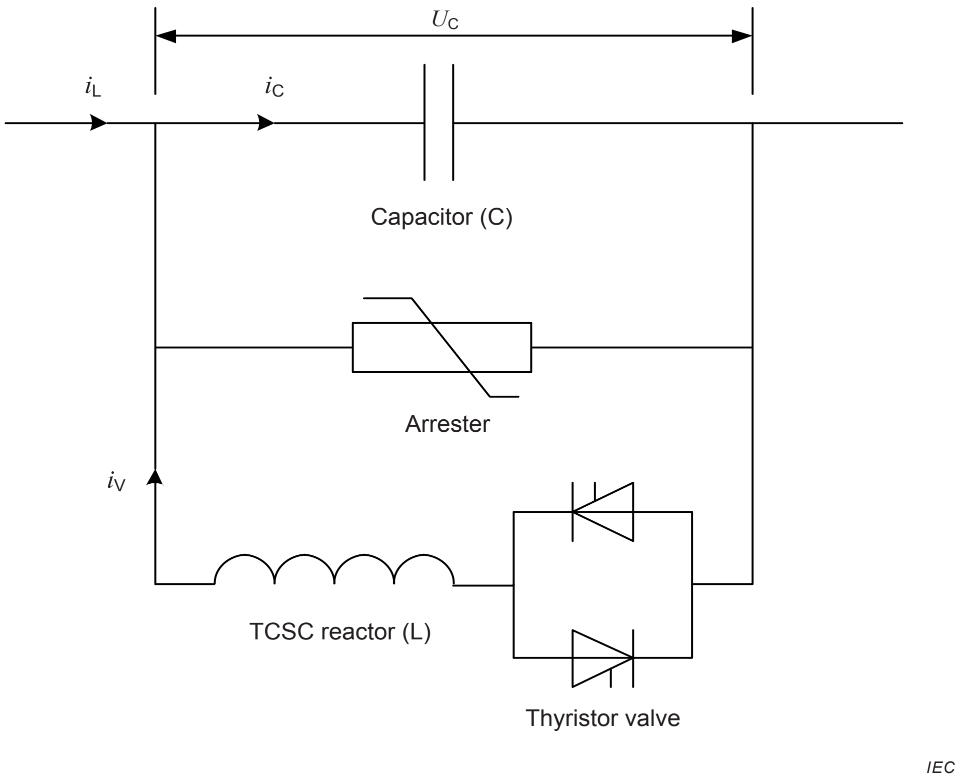


Figure 2 – TCSC subsegment

4.2 TCSC valve current and voltage at capacitive boost operation

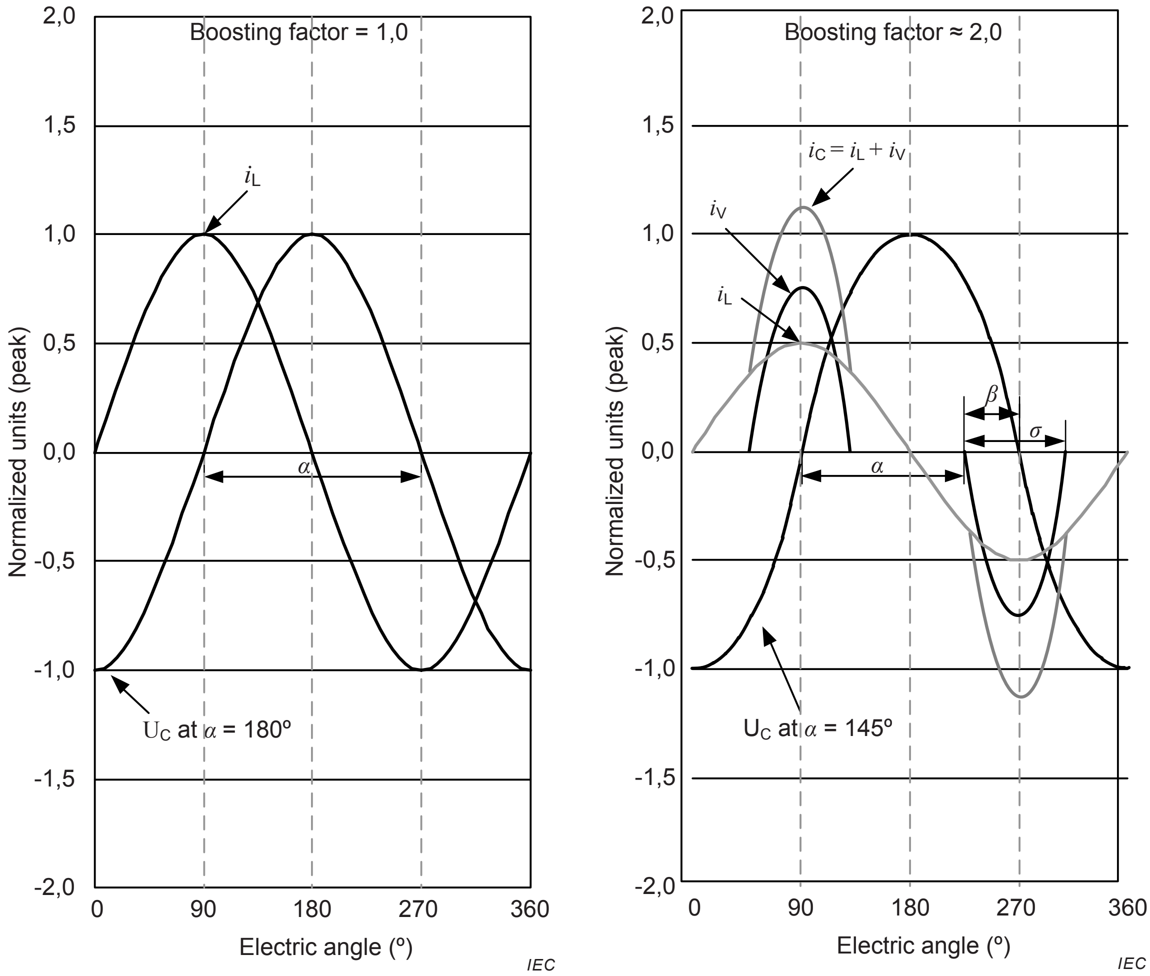
4.2.1 General

Even if a TCSC valve can be, theoretically, operated in an inductive boost mode, this operation is not used in practice in a TCSC installation due to the system compensation need and other limitations. Capacitive boost operation mode is a used operation mode of a TCSC valve.

4.2.2 Waveshapes of valve current and voltage in capacitive boost operation

At a sinusoidal line current and voltage (see Figure 3 a)), the capacitive boost operating of a TCSC valve leads to a deformed sinusoidal current flow through the capacitor bank, C, and TCSC valve (see Figure 3 b)). This current boosts the fundamental frequency voltage drop across the TCSC subsegment.

The waveform of the thyristor valve voltage in a TCSC is shown in Figure 4.



a) Capacitor bank voltage U_C and current i_L at α = 180°

b) Capacitor bank voltage U_C and current i_C at α = 145°

Figure 3 – TCSC steady state waveforms for control angle α and conduction interval σ

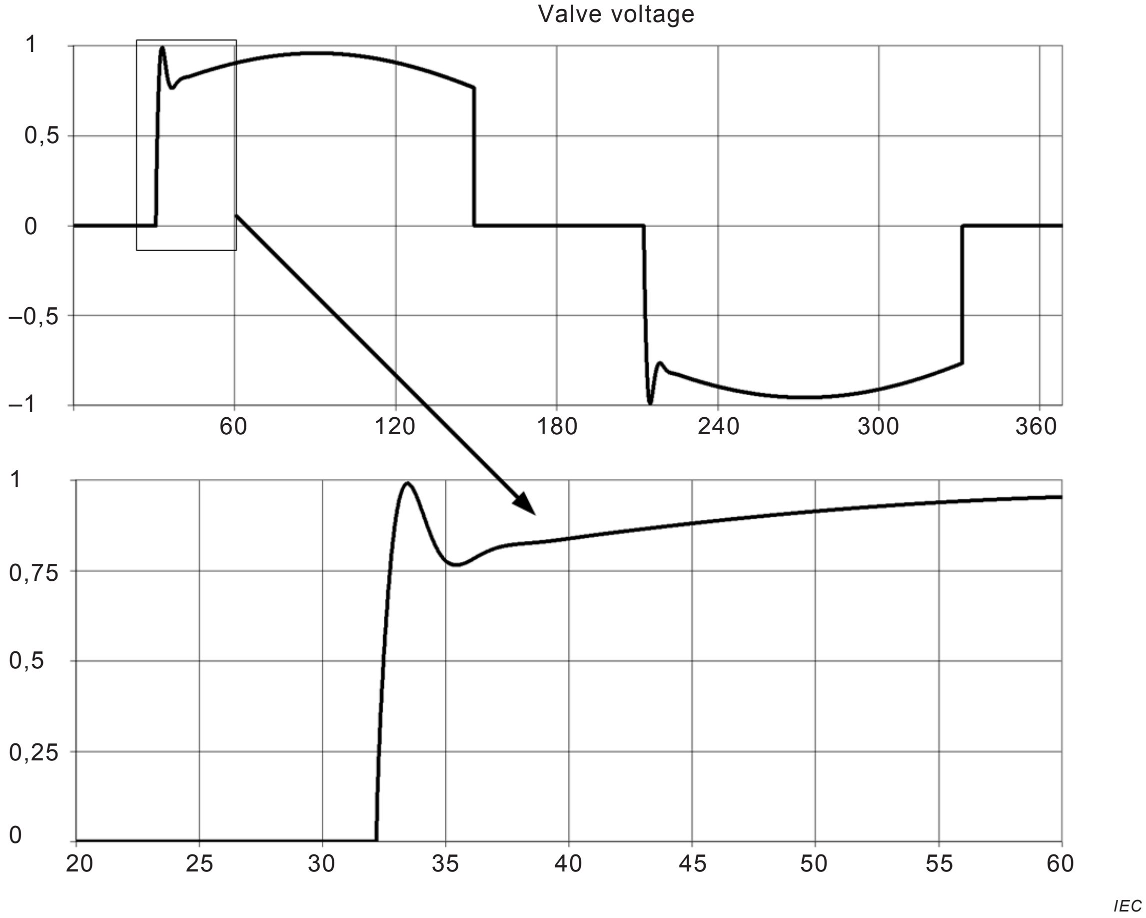


Figure 4 – Thyristor valve voltage in a TCSC

4.2.3 Formulas for TCSC valve current and voltage stresses calculation

4.2.3.1 Capacitive boost operation mode

In TCSC capacitive boost operation mode, the TCSC valve current follows the formulation below:

$$i_V = (-1)^n \cdot \frac{\lambda^2 \cdot i_L}{\lambda^2 - 1} \cdot \left(\cos \omega_N \cdot t - \frac{\cos \beta}{\cos \lambda \cdot \beta} \cdot \cos \lambda \cdot \omega_N \cdot t \right), \qquad n \cdot \pi - \beta \leq \omega_N \cdot t \leq n \cdot \pi + \beta$$

$$i_V = 0 \qquad n \cdot \pi + \beta < \omega_N \cdot t < (n + 1) \cdot \pi - \beta$$

$$n = 0, 1, 2, 3, \ldots$$

where

λ is the ratio of TCSC subsegment LC branch natural frequency and AC system power frequency, $\lambda = \frac{1}{\omega_N \cdot \sqrt{L \cdot C}}$;

i_L is the AC system line current;

ω_N nominal angle frequency of AC system;

β is half of the maximum conduction angle of TCSC valves in one direction for capacitive boost at i_L.

The rate of current change, di/dt, at thyristor turn-on and turn-off derives as follows:

$$\left.\frac{\mathrm{d}i_V}{\mathrm{d}t}\right|_{\omega_N \cdot t=\frac{\pi}{2}+\beta} = \frac{\lambda^2 \cdot i_L}{\lambda^2 - 1} \cdot \left[\omega_N \cdot \sin\beta - \omega_N \cdot \frac{\cos\beta}{\cos(\lambda \cdot \beta)} \cdot \sin(\lambda \cdot \beta)\right]$$

The peak current through the TCSC valve is equal to:

$$i_{V\_peak} = \frac{\lambda^2 \cdot i_L}{\lambda^2 - 1} \cdot \left[1 - \frac{\cos\beta}{\cos(\lambda \cdot \beta)}\right]$$

The capacitor voltage, U_{C_N}, at thyristor turn-on and turn-off instants is equal to:

$$U_{C\_N} = \frac{\lambda \cdot i_L}{\lambda^2 - 1} \cdot X_0 \cdot [\sin\beta - \lambda \cdot \cos\beta \cdot \tan(\lambda \cdot \beta)]$$

where

X_0 is the TCSC subsegment LC branch impedance:

$$X_0 = \sqrt{\frac{L}{C}} ,$$

where

L is the inductance of TCSC subsegment LC branch (Figure 2);

C is the capacitance of TCSC subsegment LC branch (Figure 2).

The capacitor voltage peak, appearing on the TCSC valve, is equal to:

$$U_P = \lambda \cdot i_L \cdot X_0 \cdot \left[1 + \frac{\lambda \cdot (\cos\beta \cdot \tan(\lambda \cdot \beta) - \lambda \cdot \sin\beta)}{\lambda^2 - 1}\right]$$

The capacitive boost factor of the TCSC subsegment is equal to:

$$k_B = 1 + \frac{2}{\pi} \cdot \frac{\lambda^2}{\lambda^2 - 1} \cdot \left\{\frac{2 \cdot \cos^2\beta}{\lambda^2 - 1} \cdot [\lambda \cdot \tan(\lambda \cdot \beta) - \tan\beta] - \beta - \frac{\sin(2 \cdot \beta)}{\beta}\right\}$$

4.2.3.2 Bypass operation mode

In TCSC bypass operation mode the TCSC valve is full conduction and the valve conducts a power frequency sinusoidal waveform bypass current equal to:

$$i_{bypass} = \frac{1}{1 - \omega_N^{\,2} \cdot L \cdot C} \cdot i_L$$

The capacitor voltage at bypass operation follows the formula below:

$$U_C = \frac{-i_L}{(\lambda^2 - 1) \cdot \omega_N \cdot C}$$

4.3 Typical operating pattern of TCSC installation

See Figure 5.

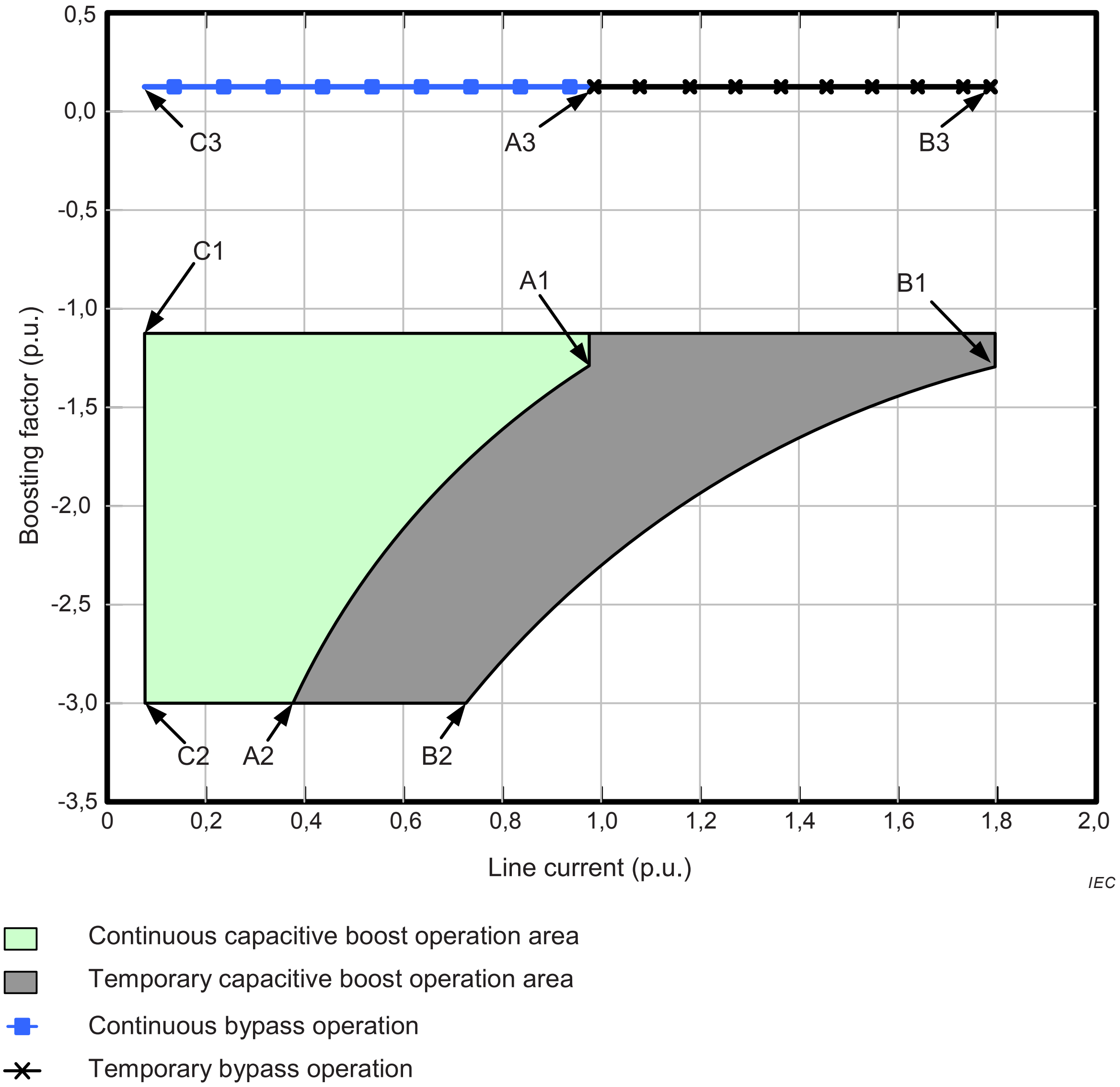


Figure 5 – Example of operating range diagram for TCSC

5 General requirements

5.1 Guidelines for the performance of type tests

5.1.1 Evidence in lieu

5.1.1.1 General

Each design of valve shall be subjected to the type tests specified in this International Standard. If the valve is demonstrably similar to the one previously tested, the supplier may, in lieu of performing a type test, submit a test report of a previous type test for consideration by the purchaser.

5.1.1.2 Test object

The tests described apply to the valve (or valve sections), the valve structure and those parts of the coolant distribution system and firing and monitoring circuits which are contained within the valve structure or connected between the valve structure and platform. Other equipment, such as valve control and protection and valve interface electronics units may be essential for demonstrating the correct function of the valve during the tests but are not in themselves the subject of the valve tests.

Certain type tests may be performed either on a complete valve or on valve sections, as indicated in Table 2. For those type tests on valve sections, the total number of valve sections tested shall be at least as many as the number in a complete valve.

The same valve sections shall be used for all type tests unless otherwise stated.

5.1.2 Sequence of tests

Prior to commencement of type tests, the valve, valve sections and/or the components of them should be demonstrated to have withstood the routine tests to ensure proper manufacture.

The type tests specified can be carried out in any order.

5.1.3 Ambient temperature for testing

The tests shall be performed at the prevailing ambient temperature of the test facility, unless otherwise specified.

5.1.4 Frequency for testing

AC dielectric tests can be performed at either 50 Hz or 60 Hz. For operational tests, specific requirements regarding the frequency for testing are given in 5.3.1.

5.1.5 Test reports

At the completion of the type tests, the supplier shall provide type test reports in accordance with Clause 14.

5.2 Test conditions for dielectric tests

5.2.1 General

Dielectric tests shall be performed on a completely assembled valve.

The valve shall be assembled with all auxiliary components except for the valve arrester, if used. Unless otherwise specified, the valve electronics shall be energized. The cooling and insulating fluids in particular shall be in a condition that represents service conditions such as conductivity, except for the flow rate and anti-freezing media content, which can be reduced. If any object or device external to the structure is necessary for proper representation of the stresses during the test, it shall also be present or simulated in the test. Metallic parts of the valve structure which are not part of the test shall be shorted together and connected to enclosure earth in a manner appropriate to the test in question.

5.2.2 Treatment of redundancy in dielectric tests

All dielectric tests on a complete valve shall be carried out with redundant thyristor levels short-circuited, except where otherwise indicated.

5.2.3 Atmospheric correction factor

When specified in the relevant clause, atmospheric correction shall be applied to the test voltages in accordance with IEC 60060-1. The reference conditions to which correction shall be made are the following.

– Pressure:

  If the insulation coordination of the tested part of the thyristor valve is based on standard rated withstand voltages according to IEC 60071-1, correction factors are only applied for site altitudes a_s exceeding 1 000 m. Hence, if the altitude of the site at which the equipment will be installed is less than 1 000 m, then the standard atmospheric air pressure (b_0 = 101,3 kPa) shall be used with no correction for altitude. If $a_s > 1\,000$ m, then the standard procedure according to IEC 60060-1 is used except that the reference atmospheric pressure b_0 is replaced by the atmospheric pressure corresponding to an altitude of 1 000 m ($b_{1\,000\text{m}}$).

  If the insulation coordination of the tested part of the thyristor valve is not based on standard rated withstand voltages according to IEC 60071-1, then the standard procedure according to IEC 60060-1 is used with the reference atmospheric pressure b_0 (b_0 = 101,3 kPa).

– Temperature:

  design maximum valve hall air temperature (°C).

– Humidity:

  design minimum valve hall absolute humidity (g/m^3).

The values to be used shall be specified by the supplier.

5.3 Test conditions for operational tests

5.3.1 General

Where possible, a complete thyristor valve should be tested. Otherwise the tests may be performed on thyristor valve sections. The choice depends mainly upon the thyristor valve design and the test facilities available. Where tests on the thyristor valve sections are proposed, the tests specified in this International Standard are valid for thyristor valve sections containing five or more series-connected thyristor levels. If tests on thyristor valve sections with fewer than five thyristor levels are proposed, additional test safety factors shall be agreed upon. Under no circumstances shall the number of series-connected thyristor levels in a thyristor valve section be less than three.

Operational tests may be performed at a power frequency different from the service frequency, e.g. 50 Hz instead of 60 Hz or vice versa. Some operational stresses such as switching losses or I^2t of short-circuit current are affected by the actual power frequency during tests. When this situation occurs, the test conditions shall be reviewed and appropriate changes made to ensure that the valve stresses are at least as severe as they would be if the tests were performed at the service frequency.

The coolant shall be in a condition representative of service conditions. Flow and temperature, in particular, shall be set to the most unfavourable values appropriate to the test in question. Anti-freezing media content should, preferably, be equivalent to the service condition; however, where this is not practicable, a correction factor agreed between the supplier and the purchaser shall be applied. Unless otherwise specified, the thyristor junction temperature during operational tests shall not be less than the temperature in service.

5.3.2 Treatment of redundancy in operational tests

For operational tests, redundant valve levels shall not be short-circuited. The test voltages used shall be adjusted by means of a scaling factor k_n:

$$k_n = \frac{N_{tut}}{N_t - N_r}$$

where

N_{tut} is the number of series thyristor levels in the test object;

N_t is the total number of series thyristor levels in the valve;

N_r is the total number of redundant series thyristor levels in the valve.

5.4 Criteria for successful type testing

5.4.1 General

Experience in industry shows that, even with the most careful design of valves, it is not possible to avoid occasional random failures of thyristor level components during service operation. Even though these failures may be stress-related, they are considered random to the extent that the cause of failure or the relationship between failure rate and stress cannot be predicted or is not amenable to precise quantitative definition. Type tests subject valves or valve sections, within a short time, to multiple stresses that generally correspond to the worst stresses that can be experienced by the equipment not more than a few times during the life of the valve. Considering the above, the criteria for successful type testing set out below therefore permit a small number of thyristor levels to fail during type testing, providing that the failures are rare and do not show any pattern that is indicative of inadequate design.

5.4.2 Criteria applicable to valve levels

The following criteria are applicable to valve levels.

a) If, following a type test as listed in Clause 6, the number of failed thyristor levels is greater than the value specified in column 2 of Table 1, then the valve shall be deemed to have failed the type tests.

b) If, following a type test, one thyristor level (or more if still within the limit in column 2 of Table 1) has become short-circuited, then the failed level(s) shall be restored and this type test repeated.

c) If the cumulative number of short-circuited thyristor levels during all type tests exceeds the number given in column 3 of Table 1, then the valve shall be deemed to have failed the type test programme.

d) When type tests are performed on valve sections, the criteria for acceptance above also apply since the number of valve sections tested shall be not less than the number of sections in a complete valve (see 5.1.1.2).

e) The valve or valve sections shall be checked after each type test to determine whether or not any thyristor levels have become short-circuited. Failed thyristors or auxiliary components found during or at the end of a type test may be replaced before further testing.

f) At the completion of the test programme, the valve or valve sections shall undergo a series of check tests, which shall include the following checks as a minimum:
   - check for voltage withstand of thyristor levels in both forward and reverse directions;
   - check of the gating circuits, where applicable;
   - check of the monitoring circuits;
   - check of the thyristor level protection circuits by application of transient voltages above and below the protection setting(s), where applicable;
   - check of the voltage grading circuits.

g) Thyristor level short circuits occurring during the check tests shall be counted as part of the criteria for acceptance defined above. In addition to short-circuited levels, the total number of thyristor levels exhibiting faults which do not result in thyristor level short circuit, which are discovered during the type test programme and the subsequent check tests, shall not exceed the number given in column 4 of Table 1. If the total number of such levels exceeds the number given in column 4 of Table 1, then the nature of the faults and their cause shall be reviewed and additional action, if any, agreed between purchaser and supplier.

h) When applying the percentage criteria to determine the permitted maximum number of short-circuited thyristor levels and the permitted maximum number of levels with faults which have not resulted in a thyristor level becoming short-circuited, it is usual practice to round off all fractions to the next highest integer, as illustrated in Table 1.

Table 1 – Valve level faults permitted during type tests

Number of thyristor levels in a completed valve minus the number of redundant levels	Number of thyristor levels permitted to become short-circuited in any one type test	Total number of thyristor levels permitted to become short-circuited in all type tests	Additional number of thyristor levels, in all type tests, which have experienced a fault but have not become short-circuited
Up to 33	1	2	2
34 to 67	2	3	3
> 67	2	4	4

The distribution of short-circuited levels and of other thyristor level faults at the end of all type tests shall be essentially random and not show any pattern that may be indicative of inadequate design.

5.4.3 Criteria applicable to the valve as a whole

No breakdown of or external flashover across common electrical equipment associated with more than one thyristor level of the valve shall occur. There shall be no disruptive discharge in dielectric material forming part of the valve structure, cooling ducts, light guides or other insulating parts of the pulse transmission and distribution system.

Component and conductor surface temperatures, together with associated current-carrying joints and connections, and the temperature of adjacent mounting surfaces shall at all times remain within limits permitted by the design.

6 Summary of tests

Table 2 lists the tests given in this International Standard.

Table 2 – List of tests

Test	Subclause	Test object
Dielectric tests between valve terminals and valve enclosure earth (type tests)		
AC test	7.2	valve
Lightning impulse test	7.3	valve
Dielectric tests between valve terminals (type tests)		
AC test	8.2	valve
Switching impulse test	8.3	valve
Operational tests (type tests)		
Maximum continuous capacitive boost test	9.3.2	valve or valve section
Maximum temporary capacitive boost test	9.3.3	valve or valve section
Minimum capacitive boost test	9.3.4	valve or valve section
Operation at maximum temporary line current bypass mode	9.3.5.1	valve or valve section
Operation at minimum temporary line current bypass mode	9.3.5.2	valve or valve section
Fault current without subsequent blocking	10.3.1	valve or valve section
Fault current with subsequent blocking	10.3.2	valve or valve section
Test for valve insensitivity to electromagnetic disturbance		
Switching impulse test	11.3	valve
Routine tests		
Visual inspection	13.2	each thyristor level [a]
Connection check	13.3	each thyristor level [a]
Voltage grading circuit check	13.4	each thyristor level [a]
Voltage withstand check	13.5	each thyristor level [a]
Partial discharge test	13.6	each thyristor level [a]
Check of auxiliaries	13.7	each thyristor level [a], and complete valve or valve section
Firing check	13.8	each thyristor level [a]
Cooling system pressure test	13.9	valve or valve section
[a] Where tests are specified to be performed on each thyristor level individually, the tests shall be performed with the thyristor levels integrated into the complete valve or valve module such that all interconnections between the adjacent thyristors are adequately tested.		

7 Dielectric tests between valve terminals and valve enclosure

7.1 Purpose of tests

The principal objectives of these tests are to verify that

- sufficient clearances have been provided to prevent flashovers;
- there is no disruptive discharge in the insulation of the valve structure, cooling ducts, light guides and other insulation parts of the pulse transmission and distribution systems;
- partial discharge inception and extinction voltages are above the maximum steady-state operating voltage appearing on the valve structure.

These tests are not applicable for designs in which one terminal of the valve (designated as the low-voltage terminal) is at the same potential as the valve enclosure and the valve support, cooling ducts and light guides are connected to the low-voltage of the valve. In this case, air clearance between the high-voltage terminal of valve and the valve enclosure shall comply with IEC 60071-2 or be agreed between purchaser and supplier.

7.2 Test object

The test object is the valve support which is connected to the high-voltage terminal of the valve. This valve support may be a separate object representing the adjacent parts of the valve. It shall be assembled with all ancillary components in place. The coolant shall be in a condition representative of the most onerous service condition for the purpose of the test.

When a complete valve is presented for testing, attention has to be paid to the proper termination of the low-voltage terminal of the valve during the tests.

7.3 Test requirements

7.3.1 AC test

7.3.1.1 Test values and waveshapes

The following test values and waveshapes shall be used for the AC test:

a) Test voltage U_{ts1}, 1 min

The test is performed with a 1 min test voltage U_{ts1} and a 10 min test voltage U_{ts2} that have sinusoidal waveshapes with a frequency of 50 Hz or 60 Hz, depending on the test facilities. The test voltage, U_{ts1}, shall be calculated according to

$$U_{ts1} = \frac{U_{s1}}{\sqrt{2}} \cdot k_1 \cdot k_t$$

where

U_{s1} is the peak value of the maximum temporary repetitive operating voltage, including extinction overshoot, across the valve support (typically derived from operation with maximum temporary overload in capacitive boost mode operating point B2 in Figure 5);

U_{ts1} is the 1 min test voltage;

k_1 is a test safety factor, k_1 = 1,30;

k_t is the atmospheric correction factor according to 5.2.3.

b) Test voltage U_{ts2}, 10 min

$$U_{ts2} = \frac{U_{s2}}{\sqrt{2}} \cdot k_2$$

where

U_{s2} is the peak value of the maximum continuous operating voltage, including extinction overshoot, across the valve support (typically derived from operation with maximum continuous capacitive boost mode operating point A2 in Figure 5);

k_2 is a test safety factor (k_2 = 1,20 for the 10 min test);

7.3.1.2 Test procedures

The test consists in applying the specified test voltages U_{ts1} and U_{ts2} for the specified duration between the high-voltage terminal of the valve and the valve enclosure.

a) Raise the voltage from 50 % to 100 % of U_{ts1} in approximately 10 s.

b) Maintain U_{ts1} for 1 min.

c) Reduce the voltage to U_{ts2}.

d) Maintain U_{ts2} for 10 min, record the partial discharge level and then reduce the voltage to zero.

e) The peak value of the periodic partial discharge recorded during the last minute of step d) shall be less than 200 pC, provided that the components which are sensitive to partial discharge in the valve have been separately tested, or alternatively 50 pC if they have not.

f) The measurement of inception and extinction voltage shall be performed in accordance with IEC 60270.

7.3.2 Lightning impulse test

A standard 1,2/50 lightning impulse voltage waveshape in accordance with 7.2.1 of IEC 60060-1:2010 shall be used.

The rated TCSC voltage, U_N, is the base voltage to define the lightning impulse voltage and the peak value of the test voltage shall be the standard lightning impulse withstand voltage according to IEC 60071-1.

The test shall comprise three applications of positive polarity and three applications of negative polarity lightning impulse voltages between the high-voltage terminal of valve and valve enclosure.

8 Dielectric tests between valve terminals

8.1 Purpose of tests

The purpose of these tests is to verify the design of the valve with respect to its capability to withstand overvoltages between its terminals. The tests shall demonstrate that

– sufficient internal insulation has been provided to enable the valve to withstand specified voltages;

– partial discharge inception and extinction voltages are above the maximum steady-state operating voltage appearing on the valve;

– the protective overvoltage firing system (if provided) works as intended;

– the thyristors have adequate dv/dt capability for in-service conditions (in most cases the specified tests are sufficient; however in some exceptional cases, additional tests may be required).

8.2 Test object

The test object shall be a complete valve which shall be assembled with all auxiliary components except for the valve surge arrester, if any. The coolant shall be in a condition that represents service conditions, except for flow rate which can be reduced. If any object external to the structure is necessary for proper representation of the stresses during tests, it shall be included or simulated in the test.

The test object used for the valve dielectric tests will normally not permit the application of atmospheric correction to the specified test voltages without overstressing the thyristors or other internal components. For this reason, no atmospheric correction factor is applied to any of the dielectric tests between valve terminals. The supplier shall demonstrate that the effects of atmospheric conditions on the valve internal withstand have been allowed for adequately.

8.3 Test requirements

8.3.1 AC test

8.3.1.1 Test values and waveshapes

The test is performed with a 1 min test voltage U_{tv1} and a 10 min test voltage U_{tv2} that have sinusoidal waveshapes with a frequency of 50 Hz or 60 Hz, depending on the test facilities.

$$U_{tv1} = \frac{U_{v1}}{\sqrt{2}} \cdot k_3$$

where

U_{v1} is the peak value of the maximum temporary repetitive operating voltage, including extinction overshoot, across the valve (typically derived from operation with maximum temporary overload in capacitive boost mode operating point B2 in Figure 5 or the series capacitor protective level);

k_3 is a test safety factor, k_3 = 1,10.

The prescribed test may thermally overstress some valve components unrealistically. Where this is the case, subject to agreement between purchaser and supplier, the 1 min AC voltage withstand test may be replaced by several shorter tests whose minimum duration is determined from the maximum possible duration of the specified overvoltage condition multiplied by 2, but with a total duration of not less than 1 min.

$$U_{tv2} = \frac{U_{v2}}{\sqrt{2}} \cdot k_{tv2}$$

where

U_{v2} is the peak value of the maximum continuous operating voltage, including extinction overshoot, across the valve (typically derived from operation with maximum continuous capacitive boost mode operating point A2 in Figure 5);

k_3 is a test safety factor (k_3 = 1,10).

8.3.1.2 Test procedures

The test procedure consists in applying the specified test voltages, for the specified duration, between the two valve terminals with one terminal earthed.

a) Raise the voltage from 50 % to 100 % U_{tv1} in approximately 10 s.
b) Maintain U_{tv1} for 1 min.
c) Reduce the voltage to U_{tv2}.
d) Maintain U_{tv2} for 10 min, record the partial discharge level and reduce the voltage to zero.
e) The peak value of the periodic partial discharge recorded during the last minute of step d) shall be less than 200 pC, provided that the components which are sensitive to partial discharge have been separately tested, or alternatively 50 pC if they have not been separately tested.
f) The measurement of inception and extinction voltage shall be performed in accordance with IEC 60270.

If valve protective firing is provided, it shall not operate during this test.

8.3.2 Switching impulse test

8.3.2.1 Test values and waveshapes

A standard 250/2 500 switching impulse voltage waveshape in accordance with 8.2.1 of IEC 60060-1:2010 shall be used.

a) For valve with valve arrester protection the valve switching impulse test voltage, U_{tsv}, shall be determined in accordance with the following:

$$U_{\text{tsv}} = SIPL_{\text{v}} \cdot k_4$$

where

$SIPL_{\text{v}}$ is the the switching impulse protective level of the valve arrester;

k_4 is a test safety factor, k_4 = 1,10.

b) For valve without valve arrester, the valve switching impulse test voltage, U_{tsv}, shall be determined in accordance with the following:

$$U_{\text{tsv}} = U_{\text{valve}} \cdot k_5$$

where

U_{valve} is the maximum prospective switching impulse voltage across valve terminals according to system insulation coordination studies;

k_5 is a test safety factor, k_5 = 1,15.

If the valve incorporates protective firing against overvoltages, which operates during the test, five additional applications of switching impulses of an agreed amplitude, so that the valve does not fire, shall be made. For the additional tests, the valve electronics shall be energized.

8.3.2.2 Test procedures

For any of these tests, three applications of switching impulse voltages of each polarity shall be applied between the valve terminals, with one terminal earthed. Instead of reversing the polarity of the surge generator, the test may be performed with one polarity of the surge generator and reversing the valve terminals.

9 Periodic firing and extinction tests

9.1 Purpose of tests

The principal objectives of the periodic firing and extinction tests are as follows:

– to check the adequacy of the thyristor levels and associated electrical circuits in a valve with regard to current, voltage and temperature stresses at turn-on and turn-off under the worst repetitive stress conditions;
– to demonstrate correct performance of the valve at minimum capacitive boost operation mode under minimum line current, coincident with minimum firing angle.

9.2 Test object

The test object shall be either a complete valve or valve sections, see 5.3.1. The valve or valve sections under test shall be assembled with auxiliary components which are necessary for the proper operation of the valve under test.

The coolant shall be in a condition representative of service conditions. Flow and temperature, in particular, shall be set to the most unfavourable values appropriate to the test in question.

9.3 Test requirements

9.3.1 General

To use an AC current source as test circuit is pertinent but generally infeasible in practice. Alternative suitable test circuits, such as an appropriate synthetic test circuit, shall generate stresses equivalent to the appropriate service conditions.

The valve or valve sections shall be subjected to current and voltage waveshapes as close as possible to those experienced by the valve during firing and extinction, for the most critical operating conditions specified below. The time interval of principal interest for firing is the first 10 μs – 20 μs while, for extinction, the interval of interest is between 0,2 ms before and 1,0 ms after current zero.

In particular, the following conditions shall be no less severe than in service:

- voltage magnitudes at turn-on and turn-off;
- voltage peaks in recovery periods;
- the $\mathrm{d}i/\mathrm{d}t$ at turn-on and at least for 0,2 ms before current zero;
- the thyristor junction temperature.

The following factors shall also be considered:

- the representation of stray capacitance between valve terminals;
- sufficient magnitude and duration of the load current to achieve full area conduction of the thyristor junction.

9.3.2 Maximum continuous capacitive boost test

9.3.2.1 Test values and waveshapes

The test current and test voltage shall be derived from the maximum continuous capacitive boost operation current at maximum capacitive boost factor, operating point A2 in Figure 5, and maximum ambient temperature.

The test current shall incorporate a test safety factor of 1,05.

The test voltage (voltage at thyristor turn-on instant and turn-off instant without overshoot), U_{test}, shall be determined as follows:

$$U_{\text{test}} = U_{\text{C\_N}} \cdot k_n \cdot k_6$$

where

$U_{\text{C\_N}}$ the capacitor voltage at TCSC valve thyristor turn-on or turn-off instant at maximum continuous capacitive boost operation according to 4.2.3.1 and operating point A2 in Figure 5;

k_{n} is a test scaling factor according to 5.3.2;

k_6 is a test safety factor, k_6 = 1,05.

The duration of the test shall be not less than 30 min.

9.3.2.2 Test procedures

The tests shall be performed using suitable test circuits, such as an appropriate synthetic test circuit, giving turn-on and turn-off stresses equivalent to the appropriate service conditions.

Ideally, the test would be performed by reproducing the specified time-dependent source current. For practical reasons, a modified test procedure may be adopted as follows:

a) establish maximum steady-state capacitive boost condition as defined in 9.3.2.1;
b) maintain operation for at least 30 min starting from the time that thermal equilibrium is reached.

9.3.3 Maximum temporary capacitive boost test

9.3.3.1 Test values and waveshapes

The test current and test voltage shall be based on the temporary overload, see point B2 in Figure 5.

The test current shall incorporate a test safety factor of 1,05.

The test voltage (voltage at thyristor turn-on instant and turn-off instant without overshoot), U_{test_max}, shall be determined as follows:

$$U_{test\_max} = U_{C\_max} \cdot k_n \cdot k_7$$

where

U_{C_max} the capacitor voltage at TCSC valve thyristor turn-on or turn-off instant at maximum temporary capacitive boost operation according to 4.2.3.1 and operating point B2 in Figure 5;

k_n is a test scaling factor according to 5.3.2;

k_7 is a test safety factor, k_7 = 1,05.

The test duration shall be 1,1 times the specified temporary overload duration.

9.3.3.2 Test procedures

The tests shall be performed using suitable test circuits, such as an appropriate synthetic test circuit, giving turn-on and turn-off stresses equivalent to the appropriate service conditions.

Ideally, the test would be performed by reproducing the specified time-dependent source current. For practical reasons, a modified test procedure may be adopted as follows:

a) establish maximum steady-state capacitive boost condition as defined in 9.3.2.1 and maintain it until thermal equilibrium is reached;
b) raise the source current to the test value. Maintain operation for 1,1 times the specified temporary overload duration.

9.3.4 Minimum capacitive boost test

9.3.4.1 General

The purpose of this test is to verify proper operation of the firing system in the TCSC valve at the specified minimum line current and specified minimum capacitive boost operating conditions.

9.3.4.2 Test values and waveshapes

The test current shall be based on the specified minimum continuous line current permissible with capacitive boost operation, point C1 in Figure 5.

The test current shall incorporate a test safety factor of 0,95.

The test voltage (voltage at thyristor turn-on instant and turn-off instant without overshoot), U_{test_min}, shall be determined as follows:

$$U_{test\_min} = U_{C\_min} \cdot \frac{N_{tut}}{N_t} \cdot k_8$$

where

U_{C_min} the capacitor voltage at TCSC valve thyristor turn-on or turn-off instant at minimum continuous capacitive boost operation according to 4.2.3.1 and operating point C1 in Figure 5;

N_{tut} is the number of series thyristor levels in the test object;

N_t is the total number of series thyristor levels in the valve;

k_8 is a test safety factor, k_8 = 0,95.

The test duration shall be 10 min.

For valve electronics energized from AC system, the peak of test voltage shall be controlled too. The voltage peak in test is determined according to 4.2.3.1 with the same principle above.

9.3.4.3 Test procedures

The tests shall be performed using suitable test circuits, such as an appropriate synthetic test circuit, giving turn-on and turn-off stresses equivalent to the test conditions defined in 9.3.4.2.

Ideally, the test would be performed by reproducing the specified time-dependent source current. For practical reasons, a modified test procedure may be adopted as follows:

a) establish minimum capacitive boost condition for current and voltage as defined in 9.3.4.2;
b) maintain the operation for 10 min starting from the time that thermal equilibrium is reached.

9.3.5 Operation at bypass

9.3.5.1 Operation at maximum temporary current bypass mode

9.3.5.1.1 General

If calculations indicate that the thyristor losses in bypass mode are greater than the thyristor losses in capacitive boost mode, the following bypass test shall be done to verify the thermal capability of the valve. Otherwise, the bypass test is not necessary since the verification of valve thermal capability has been covered by the maximum capacitive boost tests.

9.3.5.1.2 Test values and waveshapes

The test current and test voltage shall be derived from the maximum temporary bypass operation current according to 4.2.3.2 at operating point B3 in Figure 5 and, maximum ambient temperature.

The test current shall incorporate a test safety factor of 1,05.

The test duration shall be 2 times the specified temporary overload duration or maximum 2 min after the return coolant temperature has stabilized.

9.3.5.1.3 Test procedures

The tests shall be performed using suitable test circuits. All the auxiliary systems which may influence the behaviour of the valve in the operating conditions specified below shall be in operation:

a) establish maximum continuous conditions for line current and maintain them until thermal equilibrium is reached;
b) maintain operation for the specified test duration.

9.3.5.2 Operation at minimum temporary line current bypass mode

9.3.5.2.1 General

This test is not applicable if the valve is not designed to operate at minimum line current bypass operating point C3 in Figure 5.

Subject to the agreement of the purchaser, this test may be omitted in the case where the valve electronics is not energized from the AC system and the thyristor monitoring function at low voltage is demonstrated by other tests.

Depending on the choice of operating point C3 in Figure 5, the valve operation capability at minimum temporary line current bypass mode may be verified by 9.3.4.

9.3.5.2.2 Test values and waveshapes

The test current and test voltage shall be derived from the minimum bypass operation current according to 4.2.3.2 at operating point C3 in Figure 5.

The test current shall incorporate a test safety factor of 0,95.

The test voltage, $U_{\text{test-by\_min}}$, shall be determined as follows:

$$U_{\text{test-by\_min}} = U_{\text{by\_min}} \cdot \frac{N_{\text{tut}}}{N_{\text{t}}} \cdot k_9$$

where

$U_{\text{by\_min}}$	is the capacitor peak voltage at minimum line current and TCSC valve bypass operation according to 4.2.3.2 and operating point C3 in Figure 5;
N_{tut}	is the number of series thyristor levels in the test object;
N_{t}	is the total number of series thyristor levels in the valve;
k_9	is a test safety factor, k_9 = 0,95.

The test duration shall be 2 times the specified minimum temporary line current duration or maximum 2 min after the return coolant temperature has stabilized.

9.3.5.2.3 Test procedures

The tests shall be performed using suitable test circuits. All the auxiliary systems which may influence the behaviour of the valve in the operating conditions specified below shall be in operation:

a) establish minimum line current at bypass operation as defined in 9.3.5.2.2;
b) maintain operation for the specified test duration.

10 Fault current tests

10.1 Purpose of tests

The principal objective of the fault current tests is to demonstrate proper design of the valve to withstand the maximum current, voltage and temperature stresses arising from short-circuit currents.

The tests shall demonstrate that the valve is capable of:

- conducting the maximum fault current through the valve without subsequent blocking at an internal fault at the transmission line section;
- conducting the maximum fault current through the valve with subsequent blocking at an external fault at the transmission line section.

10.2 Test object

See 9.2.

10.3 Test requirements

10.3.1 Fault current without subsequent blocking

10.3.1.1 Test values and waveshapes

When an internal fault occurs, the fault current is high and the line circuit breakers will be tripped to interrupt the fault current and isolate the healthy part of network from the faulted point. Depending on the fault handling procedure, the TCSC protection may order bypass of the series capacitor via both the thyristor valve and the bypass switch. No subsequent blocking voltage appears on the TCSC valve after fault current conduction.

The peak value and conduction duration of the fault current shall be determined from system studies using the maximum AC system short-circuit power.

The waveshape of test current does not need to be identical to the fault current that could occur in service. The current shall have a peak value at least equal to the highest value of overcurrent and also it shall give the thyristor temperature at least equal to the highest value that could occur in service conditions considering the closing time of the bypass switch.

10.3.1.2 Test procedures

The tests shall be performed using suitable test circuits. All the auxiliary systems which may influence the behaviour of the valve in the operating conditions specified below shall be in operation:

a) establish thyristor junction temperature (in any suitable way) corresponding to the maximum steady state condition as defined in 9.3.2.1;
b) apply the test current for the specified time.

10.3.2 Fault current with subsequent blocking

10.3.2.1 Test values and waveshapes

This test is applicable if the TCSC is operated in such way that the valve is exposed to fault current followed by a blocking voltage.

The fault current and fault conduction duration as well as subsequent blocking voltage shall be determined from system studies using the worst external fault cases.

The test current and voltage shall influence the TCSC valve/valve section at least as severely as would occur in service. A test safety factor of 1,05 shall be applied to the subsequent blocking voltage. The current shall have a peak value at least equal to the highest value of overcurrent and also it shall give the thyristor temperature at least equal to the highest value at the instant when the voltage is re-applied.

10.3.2.2 Test procedures

The tests shall be performed using suitable test circuits. All the auxiliary systems which may influence the behaviour of the valve in the operating conditions specified below shall be in operation:

a) establish thyristor junction temperature (in any suitable way) corresponding to the maximum steady state condition as defined in 9.3.2.1;
b) apply the test current for the specified time;
c) apply the test voltage.

11 Test for valve insensitivity to electromagnetic disturbance

11.1 Purpose of tests

The principal objective is to demonstrate the insensitivity of the valve to electromagnetic interference (electromagnetic disturbance) arising from voltage and current transients generated within the valve or imposed on it from the outside. The sensitive elements of the valve are generally electronic circuits used for triggering, protection and monitoring of the thyristor levels.

The tests shall demonstrate that:

- spurious triggering of thyristors does not occur;
- false indication of thyristor level faults or erroneous signals sent to the converter control and protection systems by the valve electronics do not occur.

The valve insensitivity to electromagnetic disturbance shall be checked by monitoring the valve during the valve impulse test (8.3.2).

11.2 Test object

Generally, the test object is the valve or valve sections as used for other tests.

11.3 Test requirements

Insensitivity to electromagnetic interference is verified by monitoring the valve during the switching impulse test between terminals. The electronics of the valve under test shall be pre-energized unless otherwise specified. Those parts of the valve interface electronics units that are necessary for the proper exchange of information with the test valve shall be included. The criteria for test acceptance are that no spurious valve firing or false indication from the valve to control or protection system occurs.

12 Testing of special features

12.1 Purpose of tests

These tests are intended to verify the design and performance of any special features of the valve. Special features may include, but are not limited to, those in the following two categories:

– circuits provided to facilitate the proper control, protection and monitoring of the valve;

– features included in the valve to provide fault tolerance (see Annex B).

Generally, those features in the first category can be demonstrated as part of other tests.

Features in the second category may require special tests. Such tests shall be agreed between the purchaser and supplier on a case-by-case basis.

12.2 Test object

Tests may be performed on a complete valve, valve section or relevant parts of either.

12.3 Test requirements

The test procedures and acceptance criteria shall be chosen having regard to the actual design of the valve. It shall be demonstrated that the components or circuits involved behave as intended.

13 Routine tests

13.1 General

The specified tests define the minimum testing required. The supplier shall provide a detailed description of the test procedures to meet the test objectives.

13.2 Visual inspection

The objectives of the test are:

- to check that all materials and components are undamaged and correctly installed;
- to check data of components installed;
- to check air clearances and creepage distances within the valve.

13.3 Connection check

Test objective:

- to check that all the main current-carrying connections have been made correctly;
- to check the clamping force of thyristors;
- to check the point to point wiring.

13.4 Voltage grading circuit check

Test objective: check the grading circuit parameters (resistance and capacitance) and thereby ensure that voltage sharing between series-connected thyristors will be correct.

13.5 Voltage withstand check

Test objective: check that the thyristor levels can withstand the voltage corresponding to the maximum value specified for the valve.

13.6 Partial discharge tests

To demonstrate correct manufacture, the purchaser and supplier shall agree which components and subassemblies are critical to the design, and appropriate partial discharge tests shall be performed.

13.7 Check of auxiliaries

Test objective: check that the auxiliaries (such as monitoring and protection circuits) at each thyristor level and those common to the complete valve (or valve section) function correctly.

13.8 Firing check

Test objective: check that the thyristors in each thyristor level turn on correctly in response to firing signals.

13.9 Cooling system pressure test

Test objective:

– check that there are no leaks;
– check for adequate flow, both in the valve as a whole and in all subcircuits;
– check the differential pressure.

14 Presentation of type test results

The test report is issued in accordance with the general guidelines as given in ISO/IEC 17025. It shall include the following information:

- name and address of the laboratory and location where the tests were carried out;
- name and address of the purchaser;
- unambiguous identification of the test object, including type and ratings, serial number and any other information necessary to identify the test object;
- dates of performance of the tests;
- description of the test circuits and test procedures used for the performance of the tests;
- reference to the normative documents and clear description of deviations, if any, from procedures stated in the normative documents;
- description of measuring equipment and statement of the measuring uncertainty;
- test results in the form of tables, graphs, oscillograms, and photographs as appropriate;
- description of equipment or component failure, if applicable.

Annex A
(informative)

TCSC valve operating and rating considerations

A.1 Overview

Transmission line series reactance can be compensated by combinations of fixed series capacitors and TCSC banks (see Figure 1 in Clause 4). TCSC banks use one or more controllable modules to achieve the range of performance requirements specified by the purchaser. Annex A discusses requirements of TCSC operating and rating considerations.

The TCSC circuit configuration discussed in Figure 1 has three basic operating modes:

- TCSC valve at blocked operation with thyristors blocked (no current through the thyristor valve);
- TCSC valve at bypass operation with continuous current flow through the valve;
- TCSC valve at capacitive boost operation with reactor being controlled by thyristors.

The definition of control angle (α) with reference to voltage zero crossing is selected to be consistent with other power electronic devices such as the Thyristor Controlled Reactor (TCR). However, it should be noticed that many TCSC control systems use the line current wave form as an important control reference.

When a TCSC is operating in capacitive boost mode, the current in the thyristor valve branch can modify the voltage across the capacitor, resulting in a capacitor apparent reactance larger than the capacitor physical reactance. In a TCSC application, the increased capacitor apparent reactance can result in an increase in line current. The current pulses through the thyristor valve distort the capacitor voltage (U_C). The distorted waveform (see Figure 3 in 4.2.2), means that the capacitor voltage includes non-power frequency components and that the relationship between total RMS and total peak voltage is not √2 as in the case for a pure sinusoidal waveform. Table A.1 shows the typical peak and RMS voltage relationship of a TCSC.

Table A.1 – Peak and RMS voltage relationships

Capacitive boost factor (k_B)	Ratio of LC branch natural frequency and power frequency (λ)	Power frequency RMS voltage	Power frequency peak voltage	Total RMS voltage	Total peak voltage
1,0	2,5	1,0	1,41	1,00	1,41
2,0	2,5	2,0	2,83	2,02	2,55
3,0	2,5	3,0	4,24	3,05	3,70
1,0	3,5	1,0	1,41	1,00	1,41
2,0	3,5	2,0	2,83	2,03	2,54
3,0	3,5	3,0	4,24	3,07	3,67

A.2 TCSC characteristics

TCSC characteristics are determined from the series capacitor (C) and reactor (L) circuit parameters shown in Figure 2 in Clause 4. The steady state TCSC power frequency apparent reactance $X(\alpha)$ as a function of thyristor control angle (α) can be calculated from Formula A.1. Typical reactance characteristics are illustrated in Figure A.1.

$$X(\alpha) = \frac{1}{\omega_N \cdot C}\left[1 - \frac{\lambda^2}{(\lambda^2 - 1)} \cdot \frac{2\cdot\beta + \sin(2\cdot\beta)}{\pi} + \frac{4\lambda^2}{(\lambda^2-1)^2} \cdot \cos^2(\beta) \cdot \frac{\lambda\cdot\tan(\lambda\cdot\beta) - \tan(\beta)}{\pi}\right] \quad \text{(A.1)}$$

where

β is half of the conduction angle of TCSC valve at capacitive boost mode in one current direction ($\beta = \pi - \alpha$);

α is control angle counting from capacitor voltage zero;

λ is the ratio of TCSC subsegment LC branch natural frequency and AC system power frequency:

$$\lambda = \frac{1}{\omega_N \cdot \sqrt{L \cdot C}},$$

where

C is the series capacitor capacitance;

L is the TCSC reactor inductance.

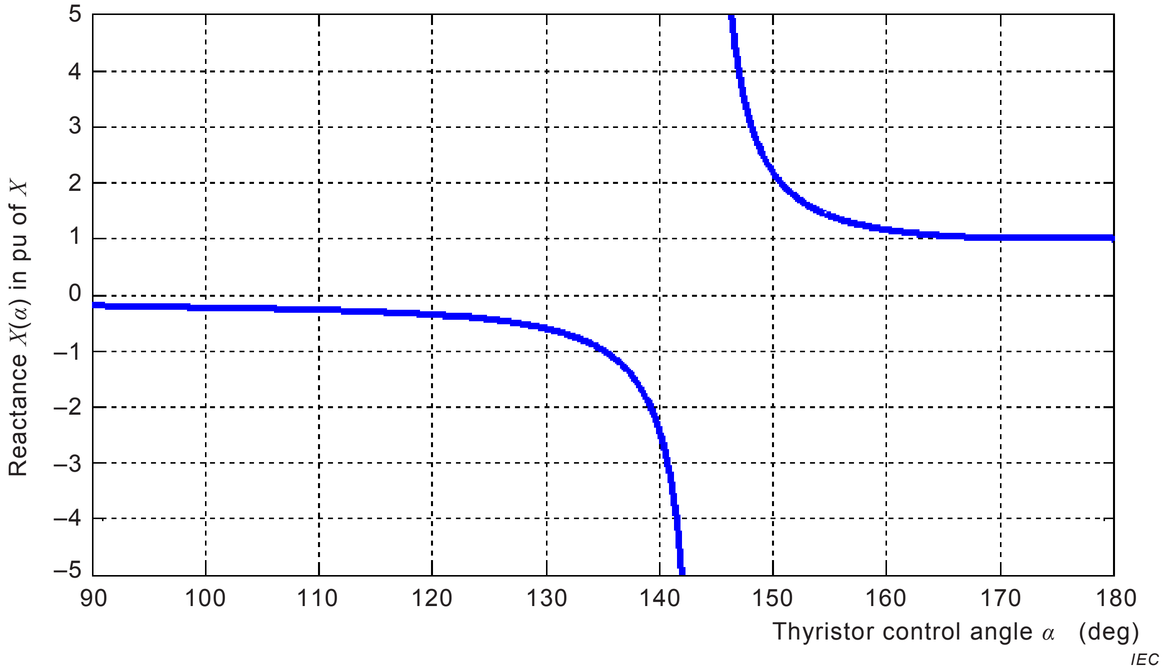


Figure A.1 – TCSC power frequency steady state apparent reactance characteristics according to Formula (A.1) with λ = 2,5

A.3 Operating range

The operating range is one of the most important factors for rating of a TCSC. It has a major impact on the main circuit components stresses and should therefore be clearly specified by the purchaser. The TCSC shall be designed to withstand operation with the different reactance and line currents within the specified operating range. The required operating range shall be defined by system studies performed by the purchaser and be clearly stated in the specification with a set of curves of the fundamental frequency TCSC apparent reactance or boost factor (k_B) versus the line current as indicated in Figure 5 in 4.3. The required operating range depends on the purpose of the TCSC. Generally a TCSC for power oscillation damping (POD) requires a larger operating range than a TCSC for subsynchronous resonance (SSR) mitigation.

A minimum line current should be considered because steady-state firing of a thyristor valve is not possible at very low thyristor valve voltages and currents. All thyristors and associated firing and monitoring electronics have a minimum voltage below which firing and condition monitoring cannot be guaranteed. In addition, some thyristor valves have power supplies for the firing circuits that may place additional constraints on the firing of the thyristor valve when the line current is low. This results in a minimum line current and boost factor (k_B) below which operation in capacitive boost mode is not feasible. This can have implications on the application and operation of the TCSC. The impact of series compensation is of limited value at low line currents. If SSR is a concern, the TCSC should be bypassed at line current levels below which operation in capacitive boost mode cannot be maintained.

A.4 Reactive power rating

When a TCSC is operating in capacitive boost mode, the reactive power seen by the power system differs from the reactive power of the capacitors. The reactive power output of a TCSC and the reactive power of the capacitors are given by

$$Q_{TCSC} = 3 \cdot \frac{k_B}{\omega \cdot C} \cdot I_L^2 \tag{A.2}$$

$$Q_{CAP} = 3 \cdot \frac{k_B^2}{\omega \cdot C} \cdot I_L^2 \tag{A.3}$$

The nominal reactive power rating of the TCSC shall be defined as the reactive power output given by Q_{TCSC} in Formula (A.2) with nominal boost and nominal line current.

A.5 Power oscillation damping (POD)

Power oscillation damping (POD) is a specialized subset of closed loop reactance control which can be realized by modulating the TCSC reactance in response to transmission system conditions to dampen power system oscillations.

A TCSC for POD applications should typically fulfil the following fundamental requirements.

- The POD controller should be able to handle system disturbances that result in power oscillations through zero and be insensitive to the direction of the average power flow.
- The POD controller should be able to handle large system disturbances. This means that the structure of the POD controller should be such that the desired phase shift between the input signal and output signal of the TCSC is maintained independently of the magnitude of the power oscillation.
- The TCSC control system should be able to handle mode switching from capacitive boost mode to bypass mode and bypass to capacitive boost mode during power oscillation damping.

A.6 SSR mitigation

When properly designed and applied, TCSC can provide a degree of SSR mitigation when operated with a boost factor greater than one. The TCSC can help mitigate the resonant SSR series combination that results from fixed series capacitors.

If it is required that SSR concerns be addressed, studies should be performed involving detailed models of the power system, the nearby turbine generators and the TCSC. This recommendation is evident in situations when the power system includes a combination of fixed series capacitors and TCSC and the combined series compensation exceeds 50 %. If the studies indicate that fixed series capacitors with the desired level of compensation will result in an SSR problem, the SSR studies should have the active involvement of the TCSC supplier.

A TCSC can only provide SSR mitigation if the valves are firing on a continuous basis. As a result, in order that the TCSC meets the SSR mitigation objectives, its operating region should be constrained to a boost factor equal to or greater than the minimum value at which it provides the desired SSR mitigation. The degree of mitigation can be a function of the control angle but it is desirable that the TCSC control system be able to provide a subsynchronous impedance that depends as little as possible on the boost factor.

In an application where SSR mitigation is critical, the operation of the TCSC under low line current condition should be reviewed, see A.3.

A.7 Harmonics

A TCSC operating in capacitive boost mode will produce harmonics. The magnitude of the harmonics depends on the operating point in terms of line current and boost factor.

In an application where TCSC is used for SSR mitigation or power oscillation damping purposes, the TCSC normally operates with the nominal boost factor and only temporarily during system disturbances with a higher boost factor. Therefore harmonic requirements on such a TCSC installation should be given for nominal operation i.e. rated line current and nominal boost factor.

Harmonic requirements for a TCSC should be given in terms of maximum allowed voltage distortion caused by the TCSC at the buses connecting the series compensated line segment. Harmonic studies for a TCSC installation require detailed transmission line data of the series compensated line together with harmonic network equivalents for the line ends to be supplied by the purchaser.

A.8 Control interactions between TCSCs in parallel lines

In a situation where two TCSCs are located on parallel lines, there is a risk of control interactions between the TCSCs during system disturbances. To reduce the risk of harmful interactions between parallel connected TCSCs the following is recommended.

- The POD controllers should use the same input signals, i.e. the sum of the power flow on the parallel circuits.
- The POD controllers should have similar dynamics.
- The reactance controllers should have similar dynamics and respond in similar ways when hitting limits.
- The degree of compensation of a line segment at maximum boost factor should be well below 100 %.

A.9 Operating range, overvoltages and duty cycles

A.9.1 Operating range

The operating range is generally specified by the purchaser.

A.9.2 Transient overvoltages

The TCSC should be suitable for repeated operations at transient overvoltages caused by power system faults, with the highest possible value U_{PL} that is expected to occur across the

TCSC terminals. The transient overvoltage is normally limited by an arrester overvoltage protection.

A.9.3 Duty cycles

The TCSC equipment should be designed to withstand the required sequences of faults, temporary overload, and continuous currents as specified by the purchaser. These sequences form the duty cycles that all of the components of the TCSC shall be designed to withstand. The duty cycle should be consistent with the manner in which the surrounding power system will be operated for both internal and external faults at the line. The purchaser should define duty cycles for faults of normal and extended duration and for faults of different types (three-phase and single phase). Phase-to-phase faults should be considered if specifically defined by the purchaser.

The purchaser should specify a power system equivalent to be used in the studies of external and internal faults at the transmission line for equipment rating.

Although the focus of A.9.3 is duty cycles involving power system faults, the TCSC should be designed to operate for other events such as insertion and reinsertion under the conditions specified by the purchaser.

Annex B
(informative)

Valve component fault tolerance

Fault tolerance capability may be defined as the ability of a TCSC thyristor valve to perform its intended function, until a scheduled shutdown, with faulted components or subsystems or overloaded components, and not lead to any unacceptable failure of other components, or extension of the damage due to the faulted condition. Special features may be required in the design to ensure fault tolerance. Examples of faults for which fault tolerance may be required include, but are not limited to, those given below.

a) Short circuit of a thyristor

Even though a short-circuited thyristor will shunt the other components at the thyristor level, in some designs there may be a danger of overloading gate pulse transformers (if any), of overloading current connections (where parallel thyristors are used), or of changing the clamping load.

b) Continuous operation of protective firing at one thyristor level due to loss of normal firing pulses to that level.

Continuous operation of protective firing can lead to overload of the damping resistor and other components at the affected level.

c) Insulation failure of a damping capacitor, damping resistor, voltage divider or grading capacitor (if any)

Insulation failure of any component in parallel with the thyristors can attract load current into it, leading to a hazardous condition.

d) Leakage of small quantities of valve coolant

If the valve is liquid cooled, small leaks may not be easily detected. Escaped coolant can contaminate sensitive components, leading to malfunction, and can increase the probability of insulation failure.

The purchaser should review the proposed design with the supplier to determine the probability and likely consequences of certain failures. Where appropriate, consideration should be given in the type test programme to the performance of special tests to verify critical aspects of the fault tolerance capability of the valve. Such tests should be agreed between the purchaser and supplier on a case-by-case basis.

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