BS EN 62751-2:2014

BSI Standards Publication

Power losses in voltage sourced converter (VSC) valves for high voltage direct current (HVDC) systems

Part 2: Modular multilevel converters

bsi.

...making excellence a habit.™

National foreword

This British Standard is the UK implementation of EN 62751-2:2014. It is identical to IEC 62751-2:2014.

The UK participation in its preparation was entrusted to Technical Committee PEL/22, Power electronics.

A list of organizations represented on this committee can be obtained on request to its secretary.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

Published by BSI Standards Limited 2014

ISBN 978 0 580 76760 9

ICS 29.200; 29.240

Compliance with a British Standard cannot confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 30 November 2014.

Amendments/corrigenda issued since publication

Date	Text affected

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 62751-2

October 2014

ICS 29.200; 29.240

English Version

Power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems - Part 2: Modular multilevel converters (IEC 62751-2:2014)

Pertes de puissance dans les valves à convertisseur de source de tension (VSC) des systèmes en courant continu à haute tension (CCHT) - Partie 2: Convertisseurs multiniveaux modulaires (CEI 62751-2:2014)

Bestimmung der Leistungsverluste in Spannungszwischenkreis-Stromrichtern (VSC) für Hochspannungsgleichstrom(HGÜ)-Systeme - Teil 2: Modulare Mehrstufen-Stromrichter (IEC 62751-2:2014)

This European Standard was approved by CENELEC on 2014-10-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Avenue Marnix 17, B-1000 Brussels

Ref. No. EN 62751-2:2014 E

Foreword

The text of document 22F/303/CDV, future edition 1 of IEC 62751-2, prepared by SC 22F "Power electronics for electrical transmission and distribution systems", of IEC/TC 22 "Power electronic systems and equipment" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62751-2:2014.

The following dates are fixed:

– latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2015-07-01
– latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2017-10-01

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 62751-2:2014 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following note has to be added for the standard indicated:

IEC 61803:1999	NOTE	Harmonised as EN 61803:1999.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

Publication	Year	Title	EN/HD	Year
IEC 60633	-	Terminology for high-voltage direct current (HVDC) transmission	EN 60633	-
IEC 62747	-	Terminology for voltage-sourced converters (VSC) for high-voltage direct current (HVDC) systems	EN 62747	-
IEC 62751-1	2014	Determination of power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems -- Part 1: General requirements	EN 62751-1	2014
ISO/IEC Guide 98-3	-	Uncertainty of measurement -- Part-3: Guide to the expression of uncertainty in measurement (GUM:1995)	-	-

CONTENTS

POWER LOSSES IN VOLTAGE SOURCED CONVERTER (VSC) VALVES FOR HIGH-VOLTAGE DIRECT CURRENT (HVDC) SYSTEMS –

Part 2: Modular multilevel converters

1 Scope

This part of IEC 62751 gives the detailed method to be adopted for calculating the power losses in the valves for an HVDC system based on the “modular multi-level converter”, where each valve in the converter consists of a number of self-contained, two-terminal controllable voltage sources connected in series. It is applicable both for the cases where each modular cell uses only a single turn-off semiconductor device in each switch position, and the case where each switch position consists of a number of turn-off semiconductor devices in series (topology also referred to as “cascaded two-level converter”). The main formulae are given for the two-level “half-bridge” configuration but guidance is also given in Annex A as to how to extend the results to certain other types of MMC building block configuration.

The standard is written mainly for insulated gate bipolar transistors (IGBTs) but may also be used for guidance in the event that other types of turn-off semiconductor devices are used.

Power losses in other items of equipment in the HVDC station, apart from the converter valves, are excluded from the scope of this standard.

This standard does not apply to converter valves for line-commutated converter HVDC systems.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60633, *Terminology for high-voltage direct-current (HVDC) transmission*

IEC 62747, *Terminology for voltage-sourced converters (VSC) for high-voltage direct current (HVDC) systems*

IEC 62751-1:2014, *Power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems – Part 1: General* requirements

ISO/IEC Guide 98-3, *Uncertainty of measurement – Part 3: Guide to the expression of uncertainty in measurement (GUM:1995)*

3 Terms, definitions, symbols and abbreviated terms

For the purposes of this document, the terms and definitions given in IEC 60633, IEC 62747, IEC 62751-1, as well as the following apply.

3.1 Terms and definitions

3.1.1
modular multi-level converter
MMC
multi-level converter in which each VSC valve consists of a number of MMC building blocks connected in series

Note 1 to entry: This note applies to the French language only.

3.1.2
MMC building block
self-contained, two-terminal controllable voltage source together with d.c. capacitor(s) and immediate auxiliaries, forming part of a MMC

3.1.3
IGBT-diode pair
arrangement of IGBT and free-wheeling diode connected in inverse parallel

3.1.4
switch position
semiconductor function which behaves as a single, indivisible switch

Note 1 to entry: A switch position may consist of a single IGBT-diode pair or, in the case of the cascaded two level converter, a series connection of multiple IGBT-diode pairs.

3.1.5
cascaded two-level converter
CTL
modular multi-level converter in which each switch position consists of more than one IGBT-diode pair connected in series

Note 1 to entry: This note applies to the French language only.

3.1.6
submodule
MMC building block where each switch position consists of only one IGBT-diode pair

3.1.7
cell
MMC building block where each switch position consists of more than one IGBT-diode pair connected in series

3.1.8
turn-off semiconductor device
controllable semiconductor device which may be turned on and off by a control signal, for example an IGBT

3.1.9
insulated gate bipolar transistor
IGBT
turn-off semiconductor device with three terminals: a gate terminal (G) and two load terminals emitter (E) and collector (C)

Note 1 to entry: This note applies to the French language only.

3.1.10
operating state
condition in which the HVDC substation is energized and the converters are de-blocked

Note 1 to entry: Unlike line-commutated converter, VSC can operate with zero active/reactive power output.

3.1.11
no-load operating state
condition in which the HVDC substation is energized but the IGBTs are blocked and all necessary substation service loads and auxiliary equipment are connected

3.1.12
idling operating state
condition in which the HVDC substation is energized and the IGBTs are de-blocked but with no active or reactive power output at the point of common connection to the a.c. network

Note 1 to entry: The “idling operating” and “no-load” conditions are similar but from the no-load state, several seconds may be needed before power can be transmitted, while from the idling operating state, power transmission may be commenced almost immediately (less than 3 power frequency cycles).

Note 2 to entry: In the idling operating state, the converter is capable of actively controlling the d.c. voltage, in contrast to the no-load state where the behavior of the converter is essentially “passive”.

Note 3 to entry: Losses will generally be slightly lower in the no-load state than in the idling operating state, therefore this operating mode is preferred where the arrangement of the VSC system permits it.

3.1.13
modulation index of PWM converters
M
ratio of the peak line to ground a.c. converter voltage, to half of the converter d.c. terminal to terminal voltage

$$M = \frac{\sqrt{2} \cdot U_{c1}}{\sqrt{3} \cdot \frac{U_{dc}}{2}}$$

where

U_{c1} is the r.m.s value of the fundamental frequency component of the line-to-line voltage U_c;

U_c is the output voltage of one VSC phase unit at its a.c. terminal;

U_{dc} is the output voltage of one VSC phase unit at its d.c. terminals.

Note 1 to entry: Some sources define modulation index in a different way such that a modulation index of 1 refers to a square-wave output, which means that the modulation index can never exceed 1. The modulation index according to that definition is given simply by $M \cdot (\pi/4)$. However, that definition is relevant mainly to two-level converters using PWM.

3.2 Symbols and abbreviated terms

3.2.1 Valve and simulation data

N_{tc} number of MMC building blocks per valve

N_c number of series-connected semiconductor devices per switch position

N_{sr} total number of series resistive elements contributing to conduction losses in the valve, other than in the IGBTs and diodes

N_{cv} number of d.c. capacitors in the valve

N_s number of switching cycles (on or off) experienced by each VSC valve level during the integration time t_i

N_{pr} total number of parallel resistive elements contributing to d.c. voltage dependent losses in the valve

N_{sn} number of snubber circuits per valve

t_i integration time used in the simulation

3.2.2 Semiconductor device characteristics

V_{0T} average IGBT threshold voltage for the relevant operating conditions

R_{0T} average IGBT slope resistance for the relevant operating conditions, valid at the device terminals

V_{0D} average diode threshold voltage for the relevant operating conditions

R_{0D} average diode slope resistance for the relevant operating condition, valid at the device terminals

E_{on} average turn-on energy dissipated in the IGBT for the relevant operating conditions

E_{off} average turn-off energy dissipated in the IGBT(s) for the relevant operating conditions

$E_{on,T1\_j,k}$ turn-on energy dissipated in IGBT T1 in the j^{th} MMC building block for the k^{th} turn-on event for the relevant operating conditions (voltage, current and junction temperature)

$E_{on,T2\_j,k}$ turn-on energy dissipated in IGBT T2 in the j^{th} MMC building block for the k^{th} turn-on event for the relevant operating conditions (voltage, current and junction temperature)

$E_{off,T1\_j,k}$ turn-off energy dissipated in IGBT T1 in the j^{th} MMC building block for the k^{th} turn-off event for the relevant operating conditions (voltage, current and junction temperature)

$E_{off,T2\_j,k}$ turn-off energy dissipated in IGBT T2 in the j^{th} MMC building block for the k^{th} turn-off event for the relevant operating conditions (voltage, current and junction temperature)

$E_{rec,D1\_j,k}$ diode recovery energy dissipated in diode D1 in the j^{th} MMC building block for the k^{th} diode turn-off event for the relevant operating conditions (voltage, current and junction temperature)

$E_{rec,D2\_j,k}$ diode recovery energy dissipated in diode D2 in the j^{th} MMC building block for the k^{th} diode turn-off event for the relevant operating conditions (voltage, current and junction temperature)

3.2.3 Other component characteristics

R_{s_k} total resistance of the k^{th} series resistive elements in the valve contributing to other conduction losses

R_{dc_k} resistance of the k^{th} parallel resistive component in the valve

R_{ESR_j} average equivalent series resistance of the j^{th} d.c. capacitor

$E_{sn,on\_j,k}$ energy dissipated in the snubber resistor of the j^{th} snubber circuit for the k^{th} turn-on event for the relevant operating conditions (voltage, and current where relevant to the design of the snubber)

$E_{sn,off\_j,k}$ energy dissipated in the snubber resistor of the j^{th} snubber circuit for the k^{th} turn-off event for the relevant operating conditions (voltage, and current where relevant to the design of the snubber)

3.2.4 Operating parameters

I_{T1av_j} mean current of IGBT T1 in the j^{th} MMC building block, averaged over an integration time t_i

I_{T2av_j} mean current of IGBT T2 in the j^{th} MMC building block, averaged over an integration time t_i

I_{T1rms_j} rms current of IGBT T1 in the j^{th} MMC building block, averaged over an integration time t_i

I_{T2rms_j} rms current of IGBT T2 in the j^{th} MMC building block, averaged over an integration time t_i

I_{D1av_j} mean current of diode D1 in the j^{th} MMC building block, averaged over an integration time t_i

I_{D2av_j} mean current of diode D2 in the j^{th} MMC building block, averaged over an integration time t_i

I_{D1rms_j} rms current of diode D1 in the j^{th} MMC building block, averaged over an integration time t_i

I_{D2rms_j} rms current of diode D2 in the j^{th} MMC building block, averaged over an integration time t_i

I_{rms_k} rms current flowing in the k^{th} series resistive element for the relevant operating conditions

U_{rms_k} rms value (including d.c. component) of the voltage across the k^{th} parallel resistive component in the valve

I_{crms_j} rms current flowing in the j^{th} d.c. capacitor of the valve

$P_{GU\_j,k}$ average power input to the power supply of k^{th} IGBT in j^{th} MMC building block

$p_{GU\_j,k}(t)$ instantaneous power input to the power supply of k^{th} IGBT in j^{th} MMC building block

$u_{GU\_j,k}(t)$ instantaneous voltage input to the power supply of k^{th} IGBT in j^{th} MMC building block

$i_{GU\_j,k}(t)$ instantaneous current input to the power supply of k^{th} IGBT in j^{th} MMC building block

P_{GU_j} average power input to the power supply in j^{th} MMC building block

$p_{GU\_j}(t)$ instantaneous power input to the power supply in j^{th} MMC building block

$u_{GU\_j}(t)$ instantaneous voltage input to the power supply in j^{th} MMC building block

$i_{GU\_j}(t)$ instantaneous current input to the power supply in j^{th} MMC building block

3.2.5 Loss parameters

P_{V1} IGBT conduction losses

P_{V2} diode conduction losses

P_{V3} other valve conduction losses

P_{V4} d.c. voltage-dependent losses

P_{V5} d.c. capacitor losses

P_{V6} IGBT switching losses

P_{V7} diode turn-off losses

P_{V8} snubber losses

P_{V9} valve electronics power consumption

P_{Vt} total valve losses

4 General conditions

4.1 General

Modular multi-level converters (MMC) are a family of converters in which each valve forms a controllable voltage source. The converter a.c. voltage is synthesized by switching large numbers of relatively small, self-contained, two-terminal controllable voltage sources at different times, thereby obtaining a high-quality converter waveform with low switching losses and therefore a high overall efficiency. The MMC building blocks from which the overall converter is built up may use multiple IGBT-diode pairs connected in series (in which case the converter is referred to as the “Cascaded two level converter”, CTLC) or only a single IGBT-diode pair per switch position. A detailed description of these types of converter is beyond the scope of this standard; however, Annex A includes a general description of the operation of the MMC (see also IEC TR 62543).

4.2 Principles for loss determination

Theoretically, the losses of a converter station can be determined either by direct measurements of the input and output powers or by means of component characteristics, using suitable mathematical models of the individual components of a converter. The selection of the principle under which the losses are to be determined shall take into consideration the uncertainties.

The overall uncertainty of the value of losses is an important parameter for a converter and for a converter station since it is used to compare investment cost to capitalised cost over the life-time of the converter station. To ensure that estimates are undisputed, adherence to the provisions of this standard and the provisions of ISO/IEC Guide 98-3 is indispensable. All measurements shall furthermore be traceable to national and/or international standards of measurement.

As mentioned above, a determination of the losses of a converter station could in principle be performed by making a direct measurement a.c. and d.c. side power. The difference between these two power values is however small, and a good accuracy will be very difficult to reach. In practice this measurement would require the use of state-of-the-art measurement equipment that rivals the best equipment available at national metrology institutes, equipment that is not intended for on-site use. While not impossible, this method is unlikely to be used.

In rare cases, where there are two converters in a substation, there may be an opportunity to connect the two converters in a temporary back-to-back configuration and circulate d.c. power between them, with their total loss being supplied by the a.c. grid. This loss can be measured, using standard energy meters and voltage transformers, but with special current transformers that have a rated current that is on the order of 5 % to 10 % of the normal operating current of the converters in order to reach sufficient accuracy at the power levels to be measured. In order to enable back-to-back measurements, additional equipment and/or control and protection enhancements could be needed, which will increase the investment cost of the converter station.

For most cases, however, the losses have to be estimated from component characteristics, using suitable mathematical models of the converters, as discussed in this standard. It is however important that all such estimates have a base in actual measurements having sufficiently low uncertainty. Care should also be taken to show the propagation of uncertainties from measurements and how they interact with the model. Estimates of the uncertainty contributions from imperfections in the models themselves should also be considered.

4.3 Categories of valve losses

The various components of valve losses are subdivided into terms referred to as P_{V1} to P_{V9}:

P_{V1} IGBT conduction losses

P_{V2} diode conduction losses

P_{V3} other valve conduction losses

P_{V4} d.c. voltage-dependent losses

P_{V5} d.c. capacitor losses

P_{V6} IGBT switching losses

P_{V7} diode turn-off losses

P_{V8} snubber losses

P_{V9} valve electronics power consumption

For the MMC topology, because the switching frequency is usually low (less than 200 Hz) the largest contributors to the valve losses are usually the IGBT and diode conduction losses P_{V1} and P_{V2}. With half-bridge converters, P_{V1} is dominant in inverter mode and P_{V2} is dominant in

rectifier mode, while with full-bridge converters there is no major difference between rectifier and inverter modes. IGBT switching losses P_{V6} and diode turn-off losses P_{V7} are also a significant (although not dominant) contribution. The other components of valve losses are generally minor.

4.4 Loss calculation method

The proposed method for determining valve losses is based on analytical formulae for the operating conditions. However, some of the necessary input parameters are difficult to obtain by purely analytical means. Numerical solutions using real-time or non-real-time simulations shall be applied, to derive such input parameters, for example valve currents and switching energies. For that, the input parameters described in 4.5 are required.

Important requirement for such simulations is an accurate modelling of the system under investigation. Multi-level converters offer a high degree of freedom in terms of control strategies. Therefore the resulting valve currents strongly depend on the realization and the algorithms of the control itself.

In alignment with the statement presented in 4.2, uncertainties of numerical simulations shall be clearly stated and justified by the manufacturer.

4.5 Input parameters

4.5.1 General

This subclause describes the input parameters necessary for the calculation of power losses in the valves of an MMC to take place. These input parameters refer to the data needed for the performance of numerical simulations as well as the converter and component data needed for calculation of losses. At the same time, converter and component data is divided into two categories: converter station data such as the number of MMC building blocks per valve and the on-state characteristics of the IGBT and free-wheeling diode, and operating parameters such as the converter a.c. and d.c. currents, converter voltage (amplitude and waveshape, including 3rd harmonic injection where applicable), a.c. system frequency and mean MMC building block switching frequency.

4.5.2 Input data for numerical simulations

For numerical simulations, the following requirements shall be considered.

– The simulation model shall include a control block which represents the real control behaviour and realistic behaviour regarding measurements, dead and transfer times, interlocking times, etc.

– The calculations shall be performed for a period of time with stable conditions in terms of active and reactive power transfer on the a.c. side and active power on the d.c. side.

– After the simulation has settled to steady-state conditions, a minimum integration time t_i of 1 s shall be used for operating state losses, but a longer time may be required for standby and no-load operating states, depending on the switching strategies used.

– The simulation models shall represent real conditions of the converter station in terms of number of MMC building blocks, main components, parasitic elements, original control algorithms, voltage and current sensors. For the calculation of valve losses, all redundant VSC levels shall be assumed to be in operation.

– A simplification of the simulation model with a reduced number of MMC building blocks is possible if it can be demonstrated that the resulting valve currents are not influenced by the simplification.

– The simulation shall also consider the junction temperature dependent semiconductor properties, such as on-state voltages, switching and recovery losses. These properties are based on the characterisation testing as described in IEC 62751-1:2014, 4.4.2. The steady-state junction temperatures of the semiconductors are calculated iteratively for the relevant operating point to derive the semiconductor losses. Further outputs of the

simulation are converter valve currents and MMC building block capacitor currents, which are the basis for the calculation of corresponding losses.

4.5.3 Input data coming from numerical simulations

From the numerical simulations the currents through the devices of the valve that are needed as input for calculation of losses are determined. The list of parameters to be derived includes:

– mean and rms current through diodes,
– mean and rms current through IGBTs,
– rms currents though series resistive elements,
– rms currents though parallel resistive elements,
– rms currents flowing in the d.c. capacitors of the valve,
– switching energies in IGBTs and diodes.

Additionally, from numerical simulations, a selection of a suitable integration time can be derived.

4.5.4 Converter station data

The following converter station data are necessary for calculation of losses:

– interface transformer turns ratio and leakage reactance;
– filter configuration;
– phase reactor inductance;
– valve reactor(s) inductance;
– number of MMC building blocks per converter arm;
– number of VSC levels per cell;
– capacitance per MMC building block;
– coolant inlet temperature; where several heat sinks are connected in series, the effect of the bulk water temperature rise shall be taken into account;
– average IGBT threshold voltage $V_{0\mathrm{T}}$ for each type of IGBT used;
– average IGBT slope resistance $R_{0\mathrm{T}}$ for each type of IGBT used;
– average IGBT turn-on energy per turn-on process E_{on} for each type of IGBT used;
– average IGBT turn-off energy per turn-off process E_{off} for each type of IGBT used;
– average diode threshold voltage $V_{0\mathrm{D}}$ for each type of diode used;
– average diode slope resistance $R_{0\mathrm{D}}$ for each type of diode used;
– average-corrected diode recovery energy per turn-off process E_{rec} for each type of diode used;
– equivalent thermal model representing relevant thermal resistances from average junction temperature of IGBTs and diodes to local coolant inlet temperature;

NOTE The average junction temperature of the IGBT or diode represents both a spatial and a temporal average, to remove effects such as lateral temperature variations and cyclic temperature ripple.

– snubber circuit parameters, if any, such as snubber capacitor, snubber resistor and inductance; for the case that the energy dissipated in the snubber resistor is determined by measurements (characterisation testing), the values of the energies have also to be provided;
– resistance R_{s_k} of series resistive elements in the valve;
– resistance R_{dc_k} of parallel resistive elements in the valve;
– equivalent series resistance R_{ESR_j} of d.c. capacitors.

4.5.5 Operating conditions

The following data concerning operation conditions are needed for calculation:

– active power at a defined point,
– reactive power at a defined point,
– a.c. line voltage,
– tap changer position, if applicable,
– d.c. voltage.

In the report of determination of losses to be provided by the converter manufacturer, the input data above described shall be presented.

5 Conduction losses

5.1 General

Each MMC building block of the MMC contains a half-bridge configuration and a d.c. capacitor. Basically the design of the MMC building block is of one of the two following versions shown in Figure 1:

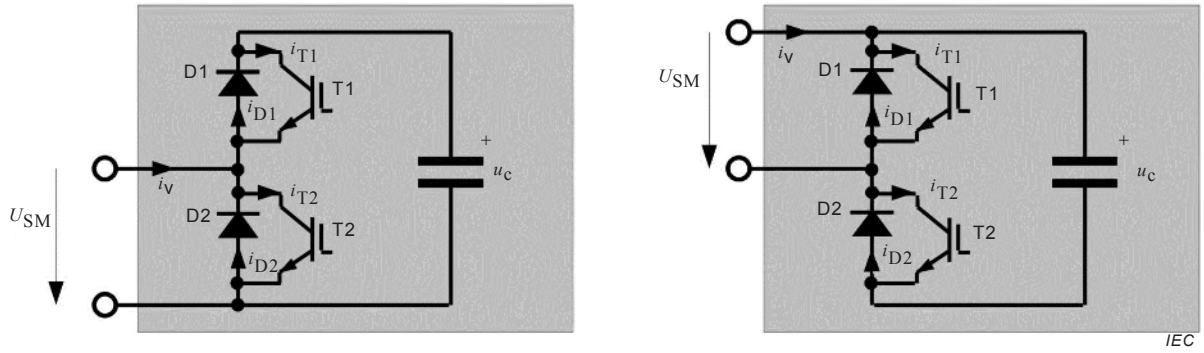


Figure 1 – Two basic versions of MMC building block designs

The designations D1, D2, T1 and T2 of the FWDs and IGBTs are defined so that the devices T1 and D1 are connected to the positive terminal of the capacitor, and T2, D2 are connected to the negative terminal.

In case of CTL converters, T1, T2, D1 and D2, respectively, represent a series connection of N_c IGBTs or diodes.

Dependent on the current direction and on the voltage at the terminals, the conducting paths shown in Figure 2, are possible during steady state operation.

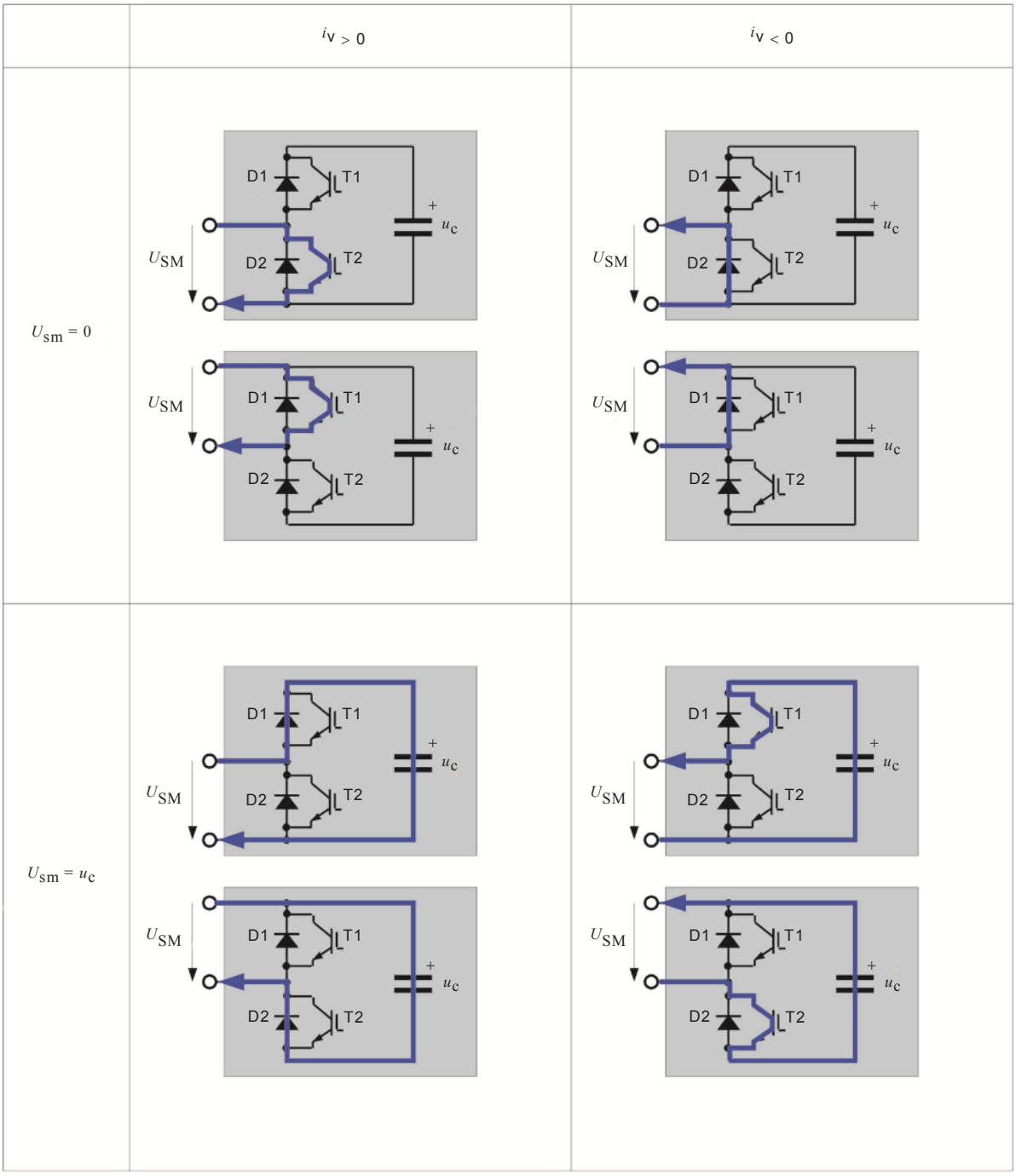


Figure 2 – Conduction paths in MMC building blocks

5.2 IGBT conduction losses

The total IGBT conduction losses per valve may be calculated by summing the conduction losses of all IGBTs per valve:

$$P_{V1} = N_c \cdot \sum_{j=1}^{N_{tc}} (V_{0T} \cdot I_{T1av\_j} + R_{0T} \cdot I_{T1rms\_j}{}^2 + V_{0T} \cdot I_{T2av\_j} + R_{0T} \cdot I_{T2rms\_j}{}^2) \quad (1)$$

where

N_{tc} is the number of MMC building blocks per valve;

N_c is the number of series-connected semiconductor devices per switch position;

V_{0T} is the average IGBT threshold voltage for the relevant operating conditions;

R_{0T} is the average IGBT slope resistance for the relevant operating conditions, valid at the device terminals;

I_{T1av_j} is the mean current of IGBT T1 in the j^{th} MMC building block, averaged over an integration time t_i;

I_{T2av_j} is the mean current of IGBT T2 in the j^{th} MMC building block, averaged over an integration time t_i;

I_{T1rms_j} is the rms current of IGBT T1 in the j^{th} MMC building block, averaged over an integration time t_i;

I_{T2rms_j} is the rms current of IGBT T2 in the j^{th} MMC building block, averaged over an integration time t_i.

By means of numerical simulation, the currents have to be calculated for the IGBTs T1 and T2 for each MMC building block, respectively:

$$I_{T1av} = \frac{1}{t_i} \cdot \int_0^{t_i} i_{T1}(t) \cdot \mathrm{d}(t) \tag{2}$$

$$I_{T2av} = \frac{1}{t_i} \cdot \int_0^{t_i} i_{T2}(t) \cdot \mathrm{d}(t) \tag{3}$$

$$I_{T1rms} = \sqrt{\frac{1}{t_i} \cdot \int_0^{t_i} i_{T1}(t)^2 \cdot \mathrm{d}(t)} \tag{4}$$

$$I_{T2rms} = \sqrt{\frac{1}{t_i} \cdot \int_0^{t_i} i_{T2}(t)^2 \cdot \mathrm{d}(t)} \tag{5}$$

where

t_i is the integration time used in the simulation;

t_i shall not be less than 1 s.

If different IGBT types are used for T1 and T2 the values for threshold voltages and slope resistances have to be used accordingly.

5.3 Diode conduction losses

The total diode conduction losses per valve may be calculated by summing the conduction losses of all diodes per valve:

$$P_{V2} = N_c \cdot \sum_{j=1}^{N_{tc}} (V_{0D} \cdot I_{D1av\_j} + R_{0D} \cdot I_{D1rms\_j}{}^2 + V_{0D} \cdot I_{D2av\_j} + R_{0D} \cdot I_{D2rms\_j}{}^2) \tag{6}$$

where

N_{tc} is the number of MMC building blocks per valve;

N_c is the number of series-connected semiconductor devices per switch position;

V_{0D} is the average diode threshold voltage for the relevant operating conditions;

R_{0D} is the average diode slope resistance for the relevant operating condition, valid at the device terminals;

I_{D1av_j} is the mean current of diode D1 in the j^{th} MMC building block, averaged over an integration time t_i;

I_{D2av_j} is the mean current of diode D2 in the j^{th} MMC building block, averaged over an integration time t_i;

I_{D1rms_j} is the rms current of diode D1 in the j^{th} MMC building block, averaged over an integration time t_i;

I_{D2rms_j} is the rms current of diode D2 in the j^{th} MMC building block, averaged over an integration time t_i.

By means of numerical simulation the currents have to be calculated for the diodes D1 and D2 for each MMC building block, respectively:

$$I_{D1av} = \frac{1}{t_i} \cdot \int_0^{t_i} i_{D1}(t) \cdot \mathrm{d}(t) \tag{7}$$

$$I_{D2av} = \frac{1}{t_i} \cdot \int_0^{t_i} i_{D2}(t) \cdot \mathrm{d}(t) \tag{8}$$

$$I_{D1rms} = \sqrt{\frac{1}{t_i} \cdot \int_0^{t_i} i_{D1}(t)^2 \cdot \mathrm{d}(t)} \tag{9}$$

$$I_{D2rms} = \sqrt{\frac{1}{t_i} \cdot \int_0^{t_i} i_{D2}(t)^2 \cdot \mathrm{d}(t)} \tag{10}$$

where

t_i is the integration time used in the simulation;

t_i shall not be less than 1 s.

NOTE If different diode types are used for D1 and D2 the values for threshold voltages and slope resistances have to be used accordingly.

5.4 Other conduction losses

This subclause covers the power losses due to conduction in components other than IGBTs and diodes. For modular multi-level converters this mainly includes the valve reactors and interconnecting busbars.

Calculation of such losses is relatively straightforward and depends only on the resistance of each conducting element and the rms current that flows through it. The relevant rms currents within the MMC building blocks can be derived from the simulations of the current stresses according to 5.2 and 5.3. Also the rms currents through reactors and between the MMC building blocks respectively can be derived accordingly.

The value of these losses per valve is given by:

$$P_{V3} = \sum_{k=1}^{N_{sr}} {I_{rms\_k}}^2 \cdot R_{s\_k} \quad (11)$$

where

N_{sr} is the total number of series resistive elements contributing to conduction losses in the valve, other than in the IGBTs and diodes;

I_{rms_k} is the rms current flowing in the k^{th} series resistive element for the relevant operating conditions;

R_{s_k} is the total resistance of the k^{th} series resistive elements in the valve contributing to other conduction losses.

6 DC voltage-dependent losses

The d.c. voltage-dependent losses of the valve are simply the U^2/R losses in resistive components connected in parallel with the valve or with parts of the valve.

In principle, the total d.c. voltage-dependent losses in the valve can be found by calculating the power dissipation in each resistive component connected in parallel with part or all of the valve and summing them.

$$P_{V4} = \sum_{k=1}^{N_{pr}} \frac{{U_{rms\_k}}^2}{R_{dc\_k}} \quad (12)$$

where

N_{pr} is the total number of parallel resistive elements contributing to d.c. voltage dependent losses in the valve;

U_{rms_k} is the rms value (including d.c. component) of the voltage across the k^{th} parallel resistive component in the valve;

R_{dc_k} is the resistance of the k^{th} parallel resistive component in the valve.

In an MMC valve these resistive components fall into two main categories: those that are connected in parallel with the d.c. capacitor of each MMC building block (such as capacitor discharge resistors) and those that are connected in parallel with the complete valve or large parts of the valve (for example water cooling pipes).

NOTE The power supply circuit for the valve electronics is equivalent to a parallel resistive load across part of the valve, but these circuits are not included in the assessment of d.c. voltage-dependent losses because they are separately accounted for under “valve electronics power consumption”, 9.2.

7 Losses in d.c. capacitors of the valve

Power losses in the MMC d.c. capacitors of the valve cannot be neglected. They represent $I^2 \cdot R$ losses in the metallic components within the capacitor, chiefly the film metallisation and internal leads, and dielectric losses within the dielectric material.

The total d.c. capacitor losses per valve are then calculated as follows:

$$P_{V5} = \sum_{j=1}^{N_{cv}} {I_{crms\_j}}^2 \cdot R_{ESR\_j} \quad (13)$$

where

N_{cv} is the number of d.c. capacitors in the valve;

I_{crms_j} is the rms current flowing in the j^{th} d.c. capacitor of the valve;

R_{ESR_j} is the average equivalent series resistance of the j^{th} d.c. capacitor.

The rms current in the d.c. capacitor can be derived by the calculations of 5.2 and 5.3.

NOTE 1 The MMC building block capacitor can be a series connection of individual capacitor units. The equivalent series resistance of that series connection has to be considered for the calculations.

NOTE 2 Dielectric losses are normally most significant in a.c. applications where the capacitor voltage polarity reverses twice per cycle. For d.c. capacitors the voltage is usually non-reversing and dielectric losses are therefore small, but depending on the capacitor technology used, they can be non-negligible.

NOTE 3 There can also be a third component of loss caused by the finite insulation resistance of the dielectric material, but this is normally very small. It is covered by d.c. voltage-dependent losses as described in the preceding subclause.

NOTE 4 Losses in balancing resistors in parallel with capacitor units connected in series are covered by d.c. voltage-dependent losses as described in the preceding subclause.

8 Switching losses

8.1 General

The devices in the MMC building block will be stressed with current and voltage during switching events. How the event will occur is dependent on the operational mode of the system. Because of the cyclic charging and discharging of the capacitor, each switching event occurs at a different voltage. The instances for switching can vary much dependent on control principles and a general formula to be applied at any type of converter valve is not feasible.

The integration time shall be at least one second in order to ensure reliable results also for control strategies where the switching pattern varies from one fundamental period to the next.

As input data from device characterisation, typical values representative for the whole population shall be used for E_{on}, E_{off} and E_{rec}.

8.2 IGBT switching losses

The total IGBT switching losses per valve are calculated by summing all the turn-on energies E_{on} and the turn-off energies E_{off} for all of the VSC valve levels in the valve, and for both T1 and T2 over an integration time t_i.

$$P_{V6} = \frac{1}{t_i} \cdot N_c \cdot \sum_{j=1}^{N_{tc}} \sum_{k=1}^{N_s} [E_{on,T1\_j,k} + E_{on,T2\_j,k} + E_{off,T1\_j,k} + E_{off,T2\_j,k}] \quad (14)$$

where

N_{tc} is the number of MMC building blocks per valve;

N_c is the number of series-connected semiconductor devices per switch position;

N_s is the number of switching cycles (on or off) experienced by each VSC valve level during the integration time t_i;

$E_{on,T1\_j,k}$ is the turn-on energy dissipated in IGBT T1 in the j^{th} MMC building block for the k^{th} turn-on event for the relevant operating conditions (voltage, current and junction temperature);

$E_{on,T2\_j,k}$ is the turn-on energy dissipated in IGBT T2 in the j^{th} MMC building block for the k^{th} turn-on event for the relevant operating conditions (voltage, current and junction temperature);

$E_{\text{off,T1\_}j,k}$ is the turn-off energy dissipated in IGBT T1 in the j^{th} MMC building block for the k^{th} turn-off event for the relevant operating conditions (voltage, current and junction temperature);

$E_{\text{off,T2\_}j,k}$ is the turn-off energy dissipated in IGBT T2 in the j^{th} MMC building block for the k^{th} turn-off event for the relevant operating conditions (voltage, current and junction temperature);

t_{i} is the integration time used in the simulation;

t_{i} shall not be less than 1 s.

8.3 Diode switching losses

The total diode switching losses per valve are then calculated by summing all the recovery energies E_{rec} for all of the valve levels in the valve, and for both D1 and D2, over a defined integration time t_{i}.

$$P_{\text{V7}} = \frac{1}{t_{\text{i}}} \cdot N_{\text{c}} \cdot \sum_{j=1}^{N_{\text{tc}}} \sum_{k=1}^{N_{\text{s}}} (E_{\text{rec,D1\_}j,k} + E_{\text{rec,D2\_}j,k}) \tag{15}$$

where

N_{tc} is the number of MMC building blocks per valve;

N_{c} is the number of series-connected semiconductor devices per switch position;

N_{s} is the number of switching cycles (on or off) experienced by each VSC valve level during the integration time t_{i};

$E_{\text{rec,D1\_}j,k}$ is the diode recovery energy dissipated in diode D1 in the j^{th} MMC building block for the k^{th} diode turn-off event for the relevant operating conditions (voltage, current and junction temperature);

$E_{\text{rec,D2\_}j,k}$ is the diode recovery energy dissipated in diode D2 in the j^{th} MMC building block for the k^{th} diode turn-off event for the relevant operating conditions (voltage, current and junction temperature);

t_{i} is the integration time used in the simulation.

t_{i} shall not be less than 1 s.

9 Other losses

9.1 Snubber circuit losses

Valves for modular multi-level converters are frequently not provided with snubber circuits; however this clause will provide general guidance to the method to be used to calculate the losses in snubber circuits where these are provided.

In case of using RC snubbers or other kind of snubbers (RCD and so on) in a design for Modular Multi-level Converters the losses in the resistor shall be included in the calculation.

The losses can be calculated as the energy in the snubber capacitor multiplied by the number of charge/discharging events that happen during the integration time. This is however very conservative for snubbers with very short time constant, since in this case part of the snubber capacitor energy will appear as additional switching energy in the IGBT.

NOTE Including a snubber parallel to a VSC valve level influences the turn-on/turn-off behaviour of the IGBT/diode which means that the snubber circuits are correctly represented during the characterisation tests on the semiconductor devices.

To get a more realistic value, it is needed to do a simulation of the real snubber and evaluate it together with the switching times of the circuit and the switching energies.

$$P_{V8} = \frac{1}{t_i} \cdot \sum_{j=1}^{N_{sn}} \sum_{k=1}^{N_s} (E_{sn\_on\_j,k} + E_{sn\_off\_j,k}) \quad (16)$$

where

N_{sn} is the number of snubber circuits per valve;

N_s is the number of switching cycles (on or off) experienced by each VSC valve level during the integration time t_i;

$E_{sn,on\_j,k}$ is the energy dissipated in the snubber resistor of the j^{th} snubber circuit for the k^{th} turn-on event for the relevant operating conditions (voltage, and current where relevant to the design of the snubber);

$E_{sn,off\_j,k}$ is the energy dissipated in the snubber resistor of the j^{th} snubber circuit for the k^{th} turn-off event for the relevant operating conditions (voltage, and current where relevant to the design of the snubber);

t_i is the integration time used in the simulation.

t_i shall not be less than 1 s.

$E_{sn,on\_j,k}$ and $E_{sn,off\_j,k}$ may be derived either by calculation based on the design of the snubber circuit or by measurement as part of the IGBT and diode characterisation testing.

9.2 Valve electronics power consumption

9.2.1 General

The valve electronics consist of local IGBT gate drive units together with their associated auxiliary circuits for power supply, measurement, monitoring etc. In most cases, the power supply takes the power from the main circuit and feeds the valve electronics. Then, the power consumption of the valve electronics is given by measuring the power input to the power supply.

The gate circuit applies positive and negative voltages to the gate terminal of the IGBT for turn-on and turn-off respectively. At the instant of gate voltage application, some charge or discharge current flows in the gate capacitance and small amount of energy is consumed. The amount of the gate current is affected by the current flowing through the IGBT. Since the power is defined as energy per second, then, the gate power is also affected by the switching frequency of the IGBT.

NOTE Power consumption of valve electronics is generally small when IGBTs are used, but in the event that other types of semiconductor devices are used, such as gate turn-off thyristors (GTOs) or integrated gate-commutated thyristors (IGCTs), the power consumption can be significantly greater because of the much larger turn on and turn off energy required for the gate circuit.

Since the IGBTs in the modular multi-level converter are controlled individually, the instantaneous valve level power consumption varies from IGBT to IGBT, similar to the conduction loss or the switching loss already described in Clauses 5 and 8. Then, the averaging process is again required to evaluate the valve electronics power consumption.

The power consumption of each valve electronics unit should be determined by direct measurement on a real valve electronics unit under representative switching conditions (voltage, current, switching frequency etc). As noted above, the measurement should be averaged over a period of at least one second, in order to smooth out the variations which take place from cycle to cycle. The measurement may be performed either with the valve electronics connected to a real IGBT or to a dummy capacitive load representing the gate capacitance of a worst-case IGBT.

The total valve electronics power consumption per valve is calculated by summing up the valve electronics power consumption per valve level.

Two basic methods exist for deriving the power supply for the valve electronics:

– type A: from the off-state voltage across each IGBT;
– type B: from the MMC building block d.c. capacitor.

9.2.2 Power supply from off-state voltage across each IGBT

In case that the power is derived from the off-state voltage across each IGBT, the total power consumption of the valve electronics is calculated by the following equation.

$$P_{V9} = \sum_{j=1}^{N_{tc}} \sum_{k=1}^{N_c} P_{GU\_j,k} \tag{17}$$

where

N_{tc} number of MMC building blocks per valve;

N_c number of series-connected semiconductor devices per switch position;

$P_{GU\_j,k}$ is the average power input to the power supply of k^{th} IGBT in j^{th} MMC building block.

The average power input to the power supply is calculated by the following equation.

$$P_{GU\_j,k} = \frac{1}{t_i} \cdot \int_0^{t_i} p_{GU\_j,k}(t) dt \tag{18}$$

where

$p_{GU\_j,k}(t) = u_{GU\_j,k}(t) \cdot i_{GU\_j,k}(t)$, and

$p_{GU\_j,k}(t)$ is the instantaneous power input to the power supply of k^{th} IGBT in j^{th} MMC building block;

$u_{GU\_j,k}(t)$ is the instantaneous voltage input to the power supply of k^{th} IGBT in j^{th} MMC building block;

$i_{GU\_j,k}(t)$ is the instantaneous current input to the power supply of k^{th} IGBT in j^{th} MMC building block;

t_i is the integration time used in the simulation.

t_i shall not be less than 1 s.

NOTE Where the valve electronics derives its power from a passive snubber circuit, the power consumption of the valve electronics can already be counted in the losses of the snubber circuit as described in the previous subclause.

9.2.3 Power supply from the d.c. capacitor

In case that the power is derived from d.c. capacitor terminals in the MMC building block, the total power consumption of the valve electronics is calculated by the following equation.

$$P_{V9} = \sum_{j=1}^{N_{tc}} P_{GU\_j} \tag{19}$$

where

N_{tc} is the number of MMC building blocks per valve;

P_{GU_j} is the average power input to the power supply in j^{th} MMC building block.

The average power input to the power supply is calculated by the following equation.

$$P_{GU\_j} = \frac{1}{t_i} \cdot \int_0^{t_i} p_{GU\_j}(t)\, dt \tag{20}$$

where

$p_{GU\_j}(t) = u_{GU\_j}(t) \cdot i_{GU\_j}(t)$ and

$p_{GU\_j}(t)$ is the instantaneous power input to the power supply in j^{th} MMC building block;

$u_{GU\_j}(t)$ is the instantaneous voltage input to the power supply in j^{th} MMC building block;

$i_{GU\_j}(t)$ is the instantaneous current input to the power supply in j^{th} MMC building block;

t_i is the integration time used in the simulation.

t_i shall not be less than 1 s.

10 Total valve losses per HVDC substation

The total losses per valve are calculated by summing the contributions P_{V1} to P_{V9}:

$$P_{VT} = \sum_{i=1}^{9} P_{Vi} \tag{21}$$

The total VSC valve losses per converter substation are equal to the losses per valve, P_{VT} multiplied by the number of valves in the converter substation.

Not all contributions to the valve losses are present in every operational mode. They may also need to be calculated with different input data dependent on operation mode. Table 1 below shows which loss contributions to apply in each state.

The total losses in the operating state include the losses appearing in no-load and/or standby states. It is not correct to add the no-load or standby losses to the operating state losses, since this would imply that the no-load or standby losses are counted twice.

Table 1 – Contributions to valve losses in different operating modes

		Operating state losses (deblocked valve with load)	Idling operating state losses (deblocked valve without load)	No-load operating state losses (blocked valve)
P_{V1}	IGBT conduction losses	X	X [a]	[b]
P_{V2}	diode conduction losses P_{V2}	X	X [a]	[b]
P_{V3}	other valve conduction losses	X	X [a]	[b]
P_{V4}	d.c. voltage-dependent losses	X	X	X
P_{V5}	d.c. capacitor losses	X	X	X
P_{V6}	IGBT switching losses	X	X [a]	[b]
P_{V7}	diode turn-off losses	X	X [a]	[b]
P_{V8}	snubber losses	X	X [a]	X[b]
P_{V9}	valve electronics power consumption	X	X	X
P_{Vt}	total valve losses	Total losses in operating state	Total losses in idling operating state	Total losses in no-load operating state

[a] Idling state is defined as deblocked valve. Here some current and switching can occur. The losses will depend very much on the control strategy, how the switching occur and at what current level. It may be at a different switching frequency and with a different harmonic content than at operating load. The fundamental current is only required to balance the reactive power generated by the filters, if any.

[b] At no-load state in principle no switching shall occur as the valve is blocked. However in some designs it may be necessary to make occasional switching operations to balance voltages between different parts of the converter. Here some losses may occur and need to be accounted for.

Annex A
(informative)

Description of power loss mechanisms in MMC valves

A.1 Introduction to MMC Converter topology

Modular multi-level converters (MMC), including the cascaded two level converter (CTL) are a family of converters whereby each valve is a controllable voltage source. They use a large number of relatively small, two-terminal controllable voltage sources connected in series in each valve. Two series-connected valves form a “Phase Unit” and are used to connect each a.c. phase to the d.c. terminals of the converter. Each phase unit can synthesise a stepped voltage waveform that can be controlled in amplitude and phase independently of the other phase units in the converter.

The CTL converter is distinguished from other types of MMC by using two or more IGBTs connected in series in each switch position. Figure A.1 and Figure A.2 show the main differences between the MMC with submodules (without series-connection of IGBTs), and MMC with CTL, illustrated for the most common variant of each type, the “half-bridge” configuration.

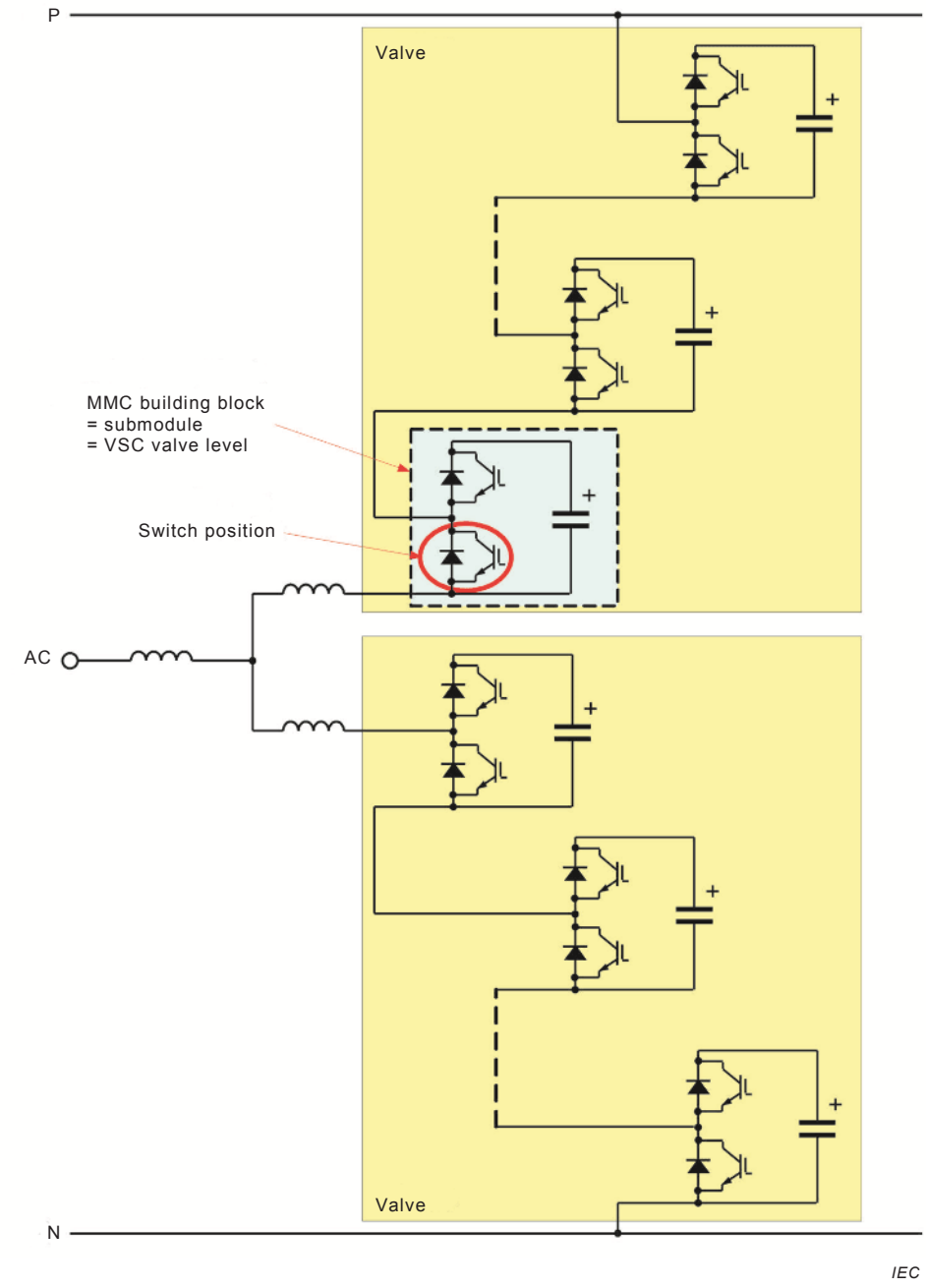


Figure A.1 – Phase unit of the modular multi-level converter (MMC) in basic half-bridge, two-level arrangement, with submodules

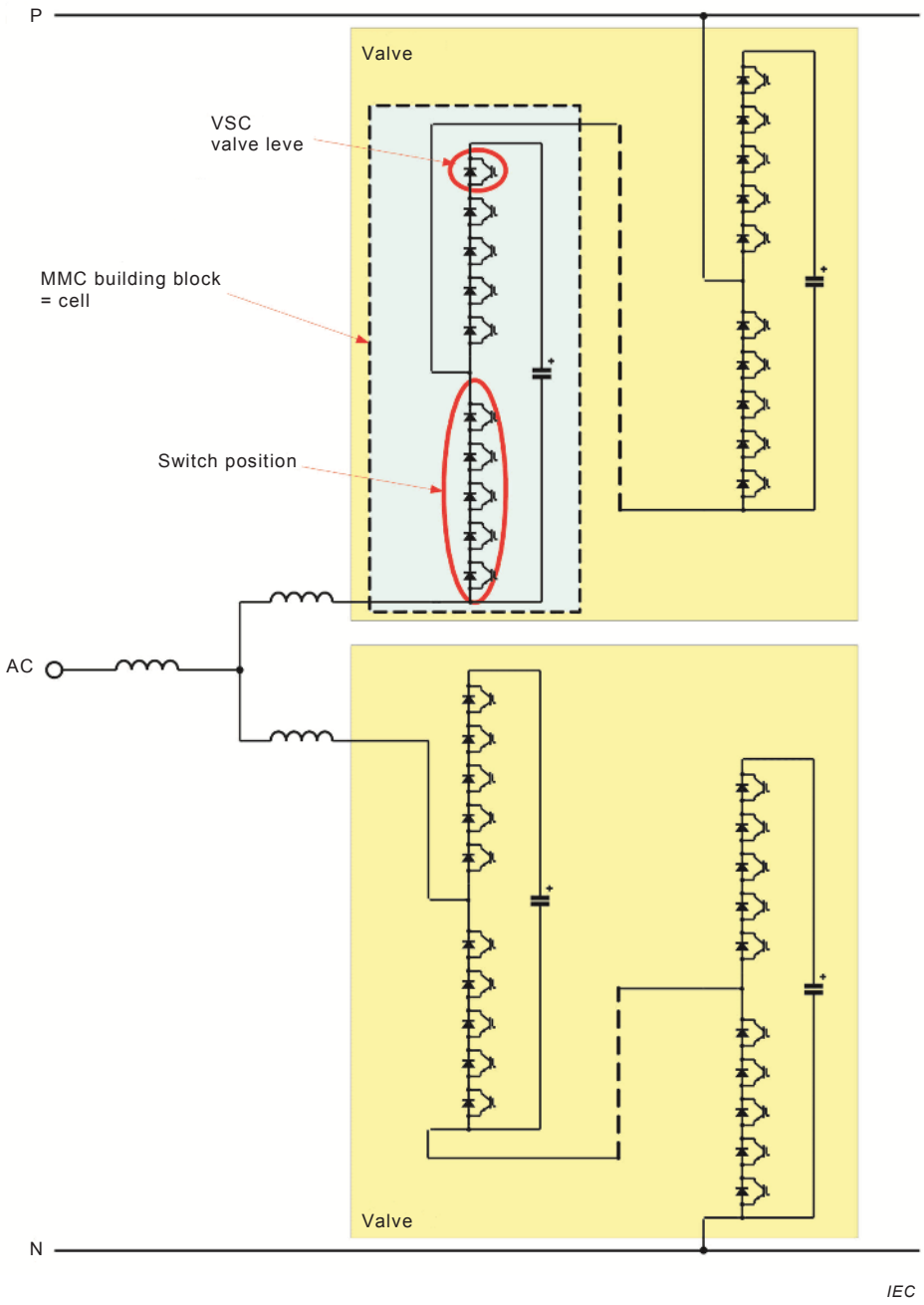


Figure A.2 – Phase unit of the cascaded two-level converter (CTL) in half-bridge form

The output voltage produced by each valve is an offset sinusoidal voltage with a mean value equal to half the d.c. line to line voltage, and the two valves in each phase unit are controlled such that the a.c. components of their output voltages are 180° out of phase (Figure A.3). In this way, the sum of the two valve voltages is almost a pure d.c. voltage (equal to the d.c. line to line voltage of the converter), and the difference between the two valve voltages is an almost pure a.c. voltage representing the a.c. output voltage of the converter.

The sum of the two valve voltages in each phase needs to be controlled accurately, in real time, to be equal to the converter d.c. voltage. However, since the complete converter consists of three phase units connected in parallel to a common d.c. bus, “valve reactors” need to be connected in series with each valve in order to prevent excessive circulating currents between phases caused by the inevitable slight errors in controlling the d.c. voltages of the three phase arms.

The operation of the converter, in so far as it affects the power losses in the valves, is described in the following Clauses A.2 to A.5 for the most commonly used variant of this family of converters, the MMC topology using “half-bridge”, two-level submodules, without series-connection of IGBTs. Other variants are possible, and their main differences are discussed, along with the CTL topology, in Clause A.6.

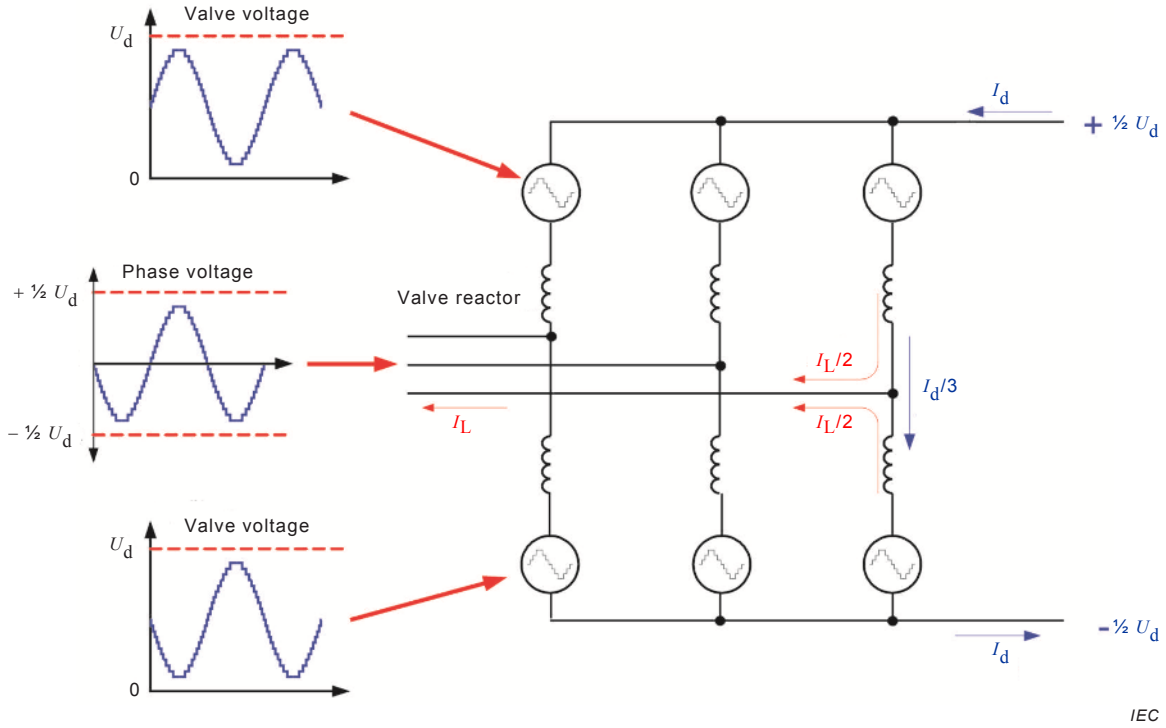


Figure A.3 – Basic operation of the MMC converters

A.2 Valve voltage and current stresses

A.2.1 Simplified analysis with voltage and current in phase

In contrast to converter topologies of the “controllable switch” type, such as the 2-level converter, or the classic “Grätz” bridge used in line-commutated converter HVDC systems, the MMC topology has the unusual feature that all six valves in the converter conduct current all the time.

Figure A.3 shows that the current flowing from each a.c. terminal of the converter splits into two equal parts – one flowing through the upper valve of that phase unit; the other flowing through the lower valve of the phase unit. Similarly the d.c. current splits into three equal branches flowing through each of the phase units. As a result, each valve carries a current equal to one third of the d.c. current plus half of the a.c. current of its associated phase, giving an offset sinusoidal current with a mean value of $I_d/3$.

Figure A.4 shows the typical waveforms of valve voltage and current. The condition shown on Figure A.4 applies when the converter a.c. output voltage and a.c. current are in phase, which means that the valve voltage and valve current are 180° out of phase. Hence, when the valve voltage is at its minimum, valve current is at its peak. This is approximately true when the converter is being used for transmitting active power only, without reactive power generation or absorption. However, even when the converter is not generating or absorbing reactive power, the valve voltage and current will generally not be exactly 180° out of phase, because of the phase shift across the interface transformer and valve reactors. Nevertheless the 180° phase shift shown on Figure A.4 is a useful simplifying assumption in order to aid the understanding of the circuit.

It will also be noted from Figure A.4 that the valve voltage varies cyclically from just above zero to just below the d.c. line to line voltage. When “half-bridge” MMC building blocks are used, the valve voltage can never exceed U_d, nor fall below zero, otherwise the free-wheeling diodes in parallel with each IGBT will conduct. This is an important limitation of the half-bridge design.

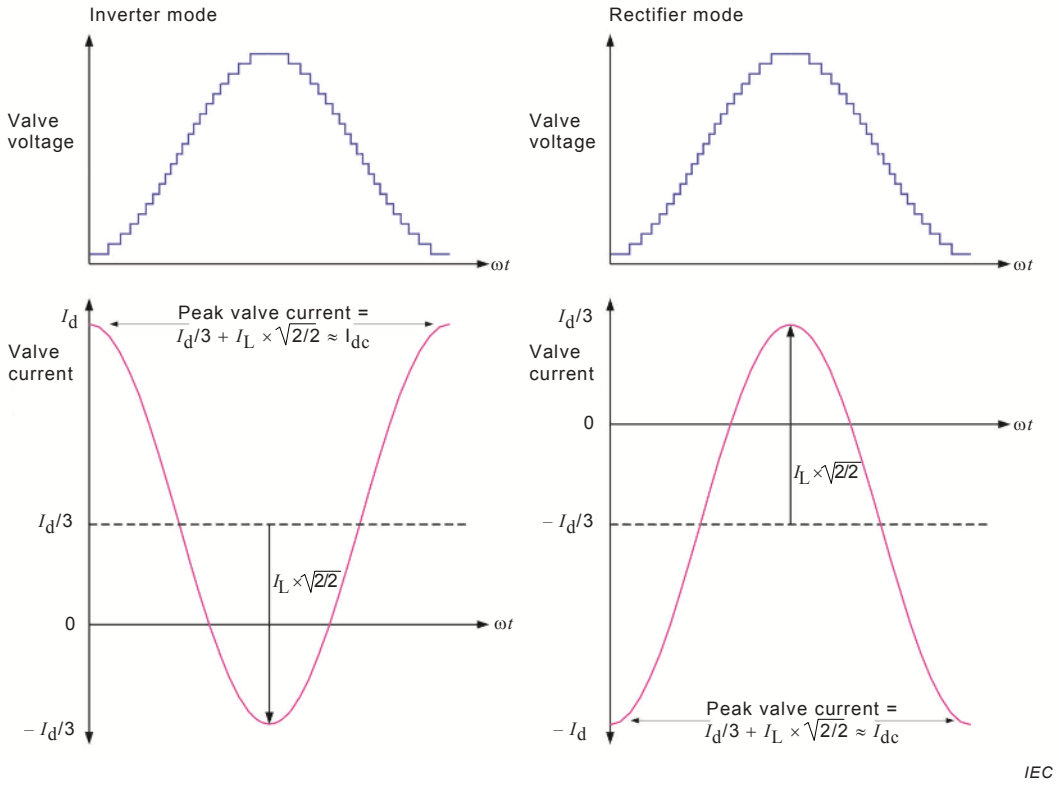


Figure A.4 – MMC converters showing composition of valve current

Optimum efficiency is obtained when the peak converter voltage is equal to ½ U_d. Operating with a peak converter voltage lower than ½ U_d implies that the a.c. current has to be increased to reach the desired value of power; therefore, when “half-bridge” MMC building blocks are used, the controller usually attempts to keep the peak valve voltage just below U_d, so as to minimise the a.c. current (and hence the losses) required for a given amount of active power.

When the d.c. current is flowing into the positive d.c. terminal of the converter, as shown on Figure A.3, the converter is importing power to the a.c. network from the d.c. network and is therefore operating as an inverter. In rectifier operation, d.c. current flows out of the positive d.c. terminal and into the negative d.c. terminal.

In the remainder of this annex, the sign convention adopted is that the valve current is positive when it is flowing towards the negative d.c. terminal of the converter. This means that the valve current is mainly negative at a rectifier and mainly positive at an inverter.

A.2.2 Generalised analysis with voltage and current out of phase

In general, the converter a.c. voltage and a.c. current will not be exactly in phase, because of two effects:

– reactive power demand at the point of common connection with the a.c. system;
– the phase shift between the a.c. system voltage and the converter a.c. voltage.

A major advantage of VSC technology over LCC technology in HVDC is that the converter is inherently capable of generating or absorbing significant amounts of reactive power. Similarly to an electrical machine, the converter has various constraints which may limit the amount of reactive power available at a given operating point, such as an overall MVA limit, a (valve) current limit, a converter voltage limit (where "half-bridge" MMC building blocks are used), etc. Typically, purchasers of HVDC systems specify that the converter should be able to operate at full rated active power with a power factor ($\cos \varphi$) in the range 0,925 lagging to 0,925 leading, which equates to a phase shift of 22° and the generation or absorption of up to ±0,4 p.u. reactive power at rated active power. At lower values of active power, more reactive power is generally available and when the active power is zero, the converter can operate with a power factor of 0, becoming a STATCOM.

The phase shift between the a.c. system voltage and the converter a.c. voltage is equal to the phase shift across the interface transformer and valve reactors (the two valve reactors for a given phase are considered to be in parallel in this case). It is well known from a.c. power system theory that, under sinusoidal conditions, the active power flow through an inductance is related to the phase shift δ across the inductance, by the equation:

$$P = \frac{U_{\mathrm{L}} \cdot U_{\mathrm{C}} \cdot \sin \delta}{X_{\mathrm{L}}} \tag{A.1}$$

where U_{L} and U_{C} are the rms line to line voltages either side of the inductance and X_{L} is the inductive reactance.

At maximum rated power, sin δ becomes approximately equal to the per-unit impedance of the interface transformer and valve reactors. Hence with a typical impedance of 0,15 p.u., the phase shift δ at rated power is typically in the range 8° to 9°.

The relationship between a.c. system voltage, converter a.c. voltage and converter current is best presented by a phasor diagram as in Figure A.5.

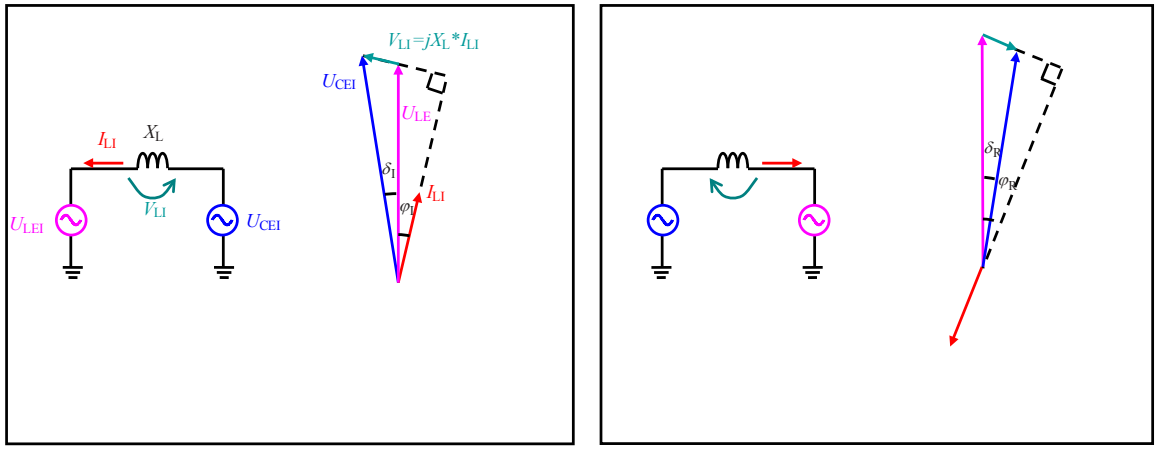


Figure A.5 – Phasor diagram showing a.c. system voltage, converter a.c. voltage and converter a.c. current

A.2.3 Effects of third harmonic injection

The description above is based on the premise that the converter a.c. voltage is sinusoidal, or as close to sinusoidal as possible with the number of MMC building blocks available. However, a commonly used technique in many power electronic converters involves deliberately adding a proportion of third harmonic to the converter voltage. Actually, other odd multiples of 3rd harmonic can also be used, as for example 9th or 15th harmonics.

The advantage of this technique is that it can allow the peak of the fundamental component of the converter voltage to be higher than the peak of the actual converter voltage. This means that the peak of the fundamental component of the converter voltage can exceed the d.c. line to line voltage and allows a lower a.c. current to be used than would otherwise be possible, reducing the conduction losses of the converter. With 3rd harmonic, the maximum benefit is obtained when amplitude of the injected 3rd harmonic is 1/6 of the fundamental component. Because the injected harmonics are multiples of three, they cancel in the line-to-line voltage at the a.c. terminals of the converter; hence if the converter transformer has a delta secondary, the injected harmonics do not transfer to the connected power system.

Figure A.6 illustrates this technique, which is now becoming widespread in VSC HVDC converters because the significant reduction of a.c. current (of the order of 15 %) that it permits leads in turn to substantial reduction of conduction losses.

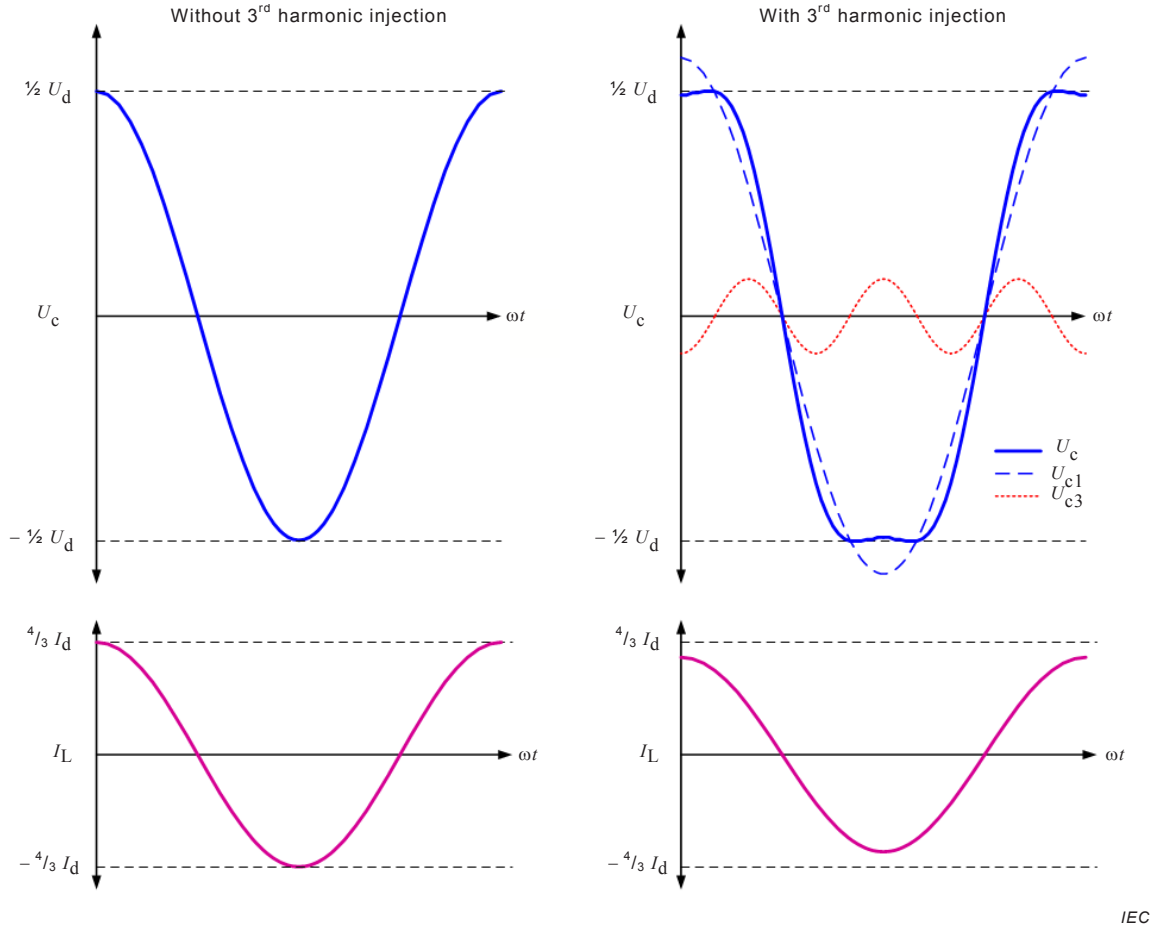
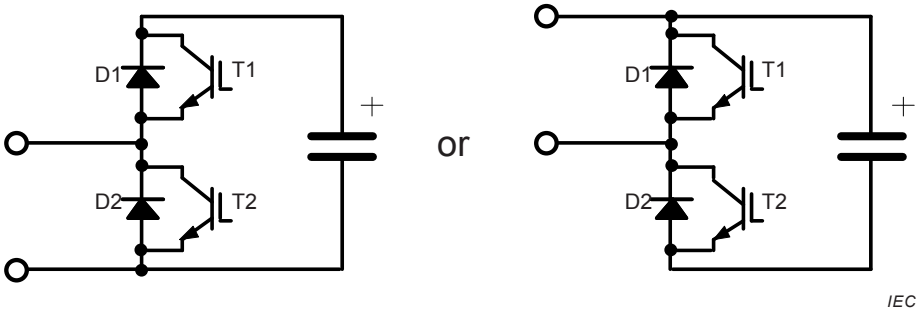


Figure A.6 – Effect of 3rd harmonic injection on converter voltage and current

A.3 Conduction losses in MMC building blocks

A.3.1 Description of conduction paths

Figure A.7 shows an MMC building block of a basic “half-bridge” MMC valve using a two-level converter arrangement. It will be seen that the MMC building block contains four main semiconductor devices: two IGBTs, T1 and T2, and two diodes D1 and D2.



a) b)

Figure A.7 – Two functionally equivalent variants of a "half-bridge", two-level MMC building block

NOTE 1 Usually the IGBT and its anti-parallel diode are supplied as a single, integrated package.

NOTE 2 An additional bypass thyristor can also be included for protection against fault currents, but this is usually arranged not to conduct current in steady-state operation and therefore contributes nothing to the losses of the converter.

Figure A.7 shows two variants of a half-bridge, two-level MMC building block which are functionally equivalent to each other. In both cases, the MMC building block has two possible operating states: bypassed and active. In Figure A.7 a), the bypassed mode is obtained by turning on IGBT T2 and active mode is obtained by turning on IGBT T1. In Figure A.7 b) the roles are reversed.

For the remainder of this annex, descriptions are based around the circuit shown in Figure A.7 a).

Since the valve carries current in both directions at different times, there are a total of four possible conducting states per MMC building block, listed below and shown on Figure A.8:

– negative current, bypassed: D2 conducting;
– negative current, active: T1 conducting;
– positive current, bypassed: T2 conducting;
– positive current, active: D1 conducting.

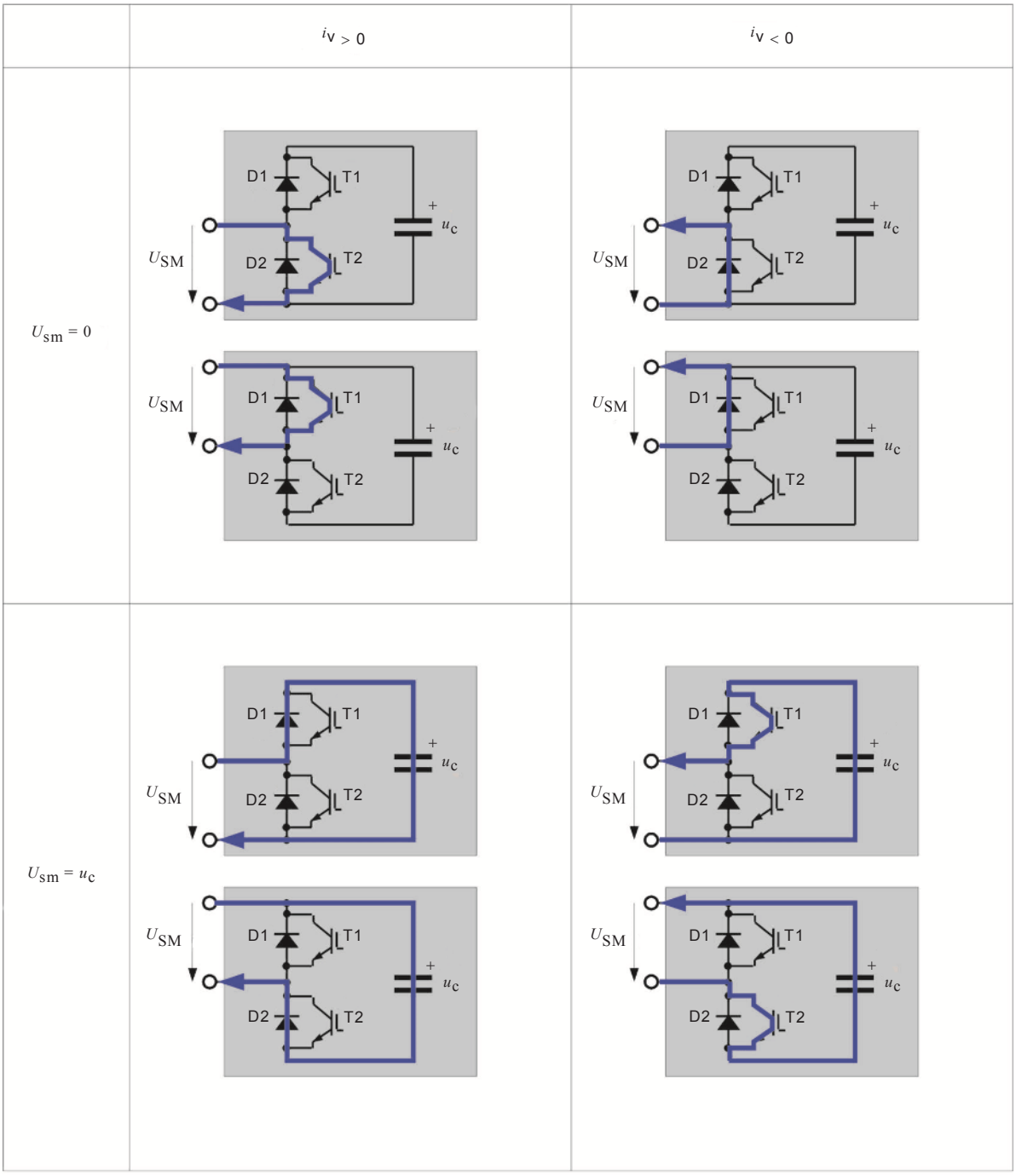


Figure A.8 – Conducting states in “half-bridge”, two-level MMC building block

Figure A.9 illustrates how the patterns of conduction differ between rectifier and inverter operation.

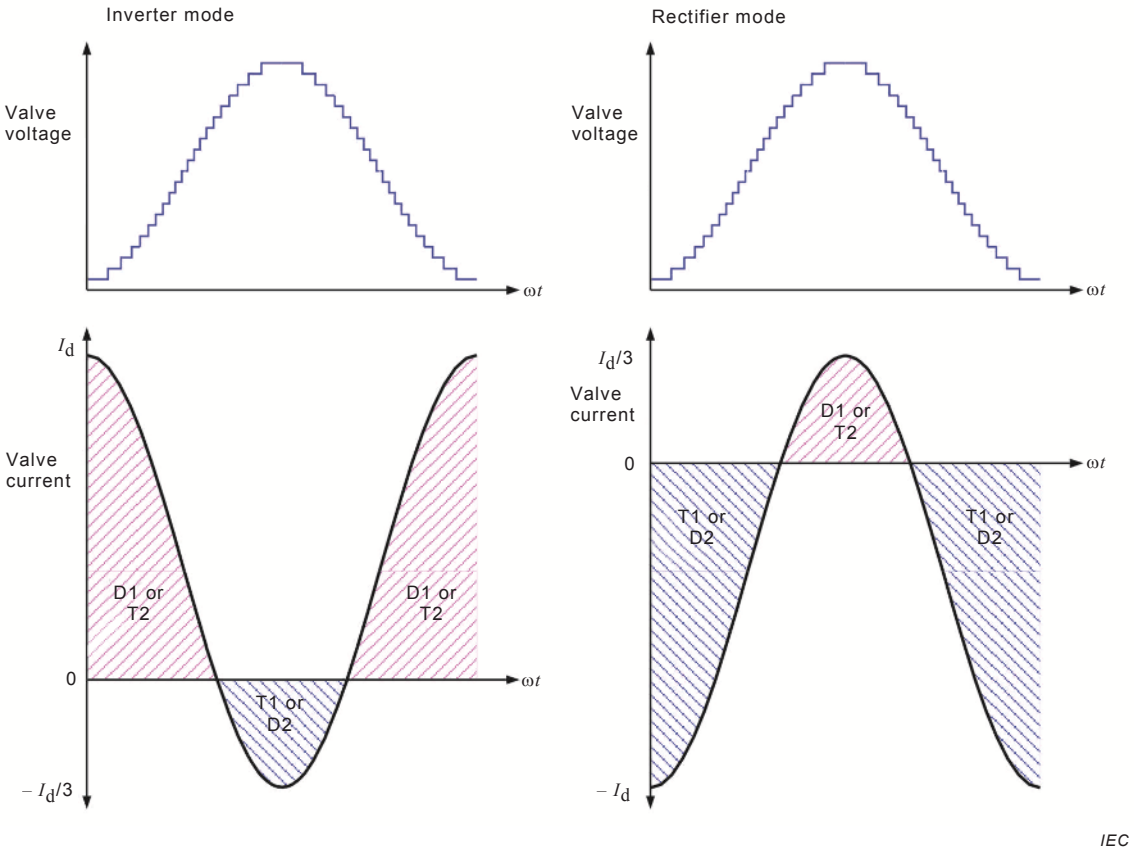


Figure A.9 – Typical patterns of conduction for inverter operation (left) and rectifier operation (right)

An example of a converter with, for illustrative purposes, only one MMC building block per valve, is shown in Figure A.10 below.

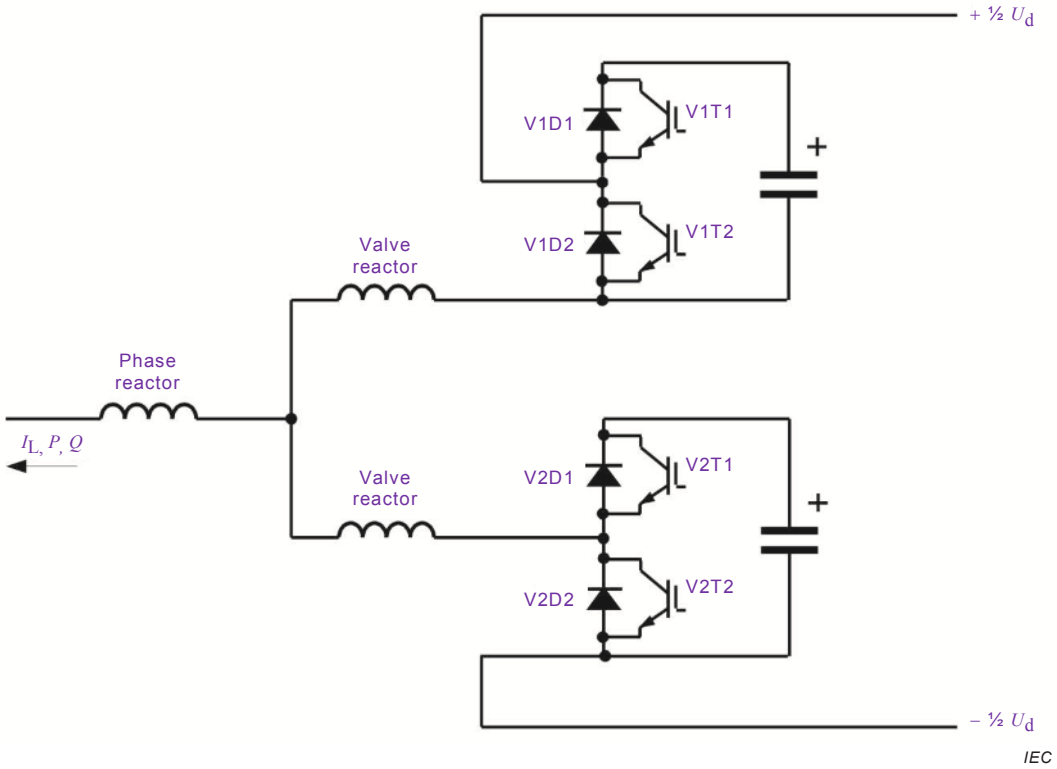


Figure A.10 – Example of converter with only one MMC building block per valve to illustrate switching behaviour

Inverter operation of this converter in a typical case is shown in an example in Figure A.11 and in rectifier operation in Figure A.12.

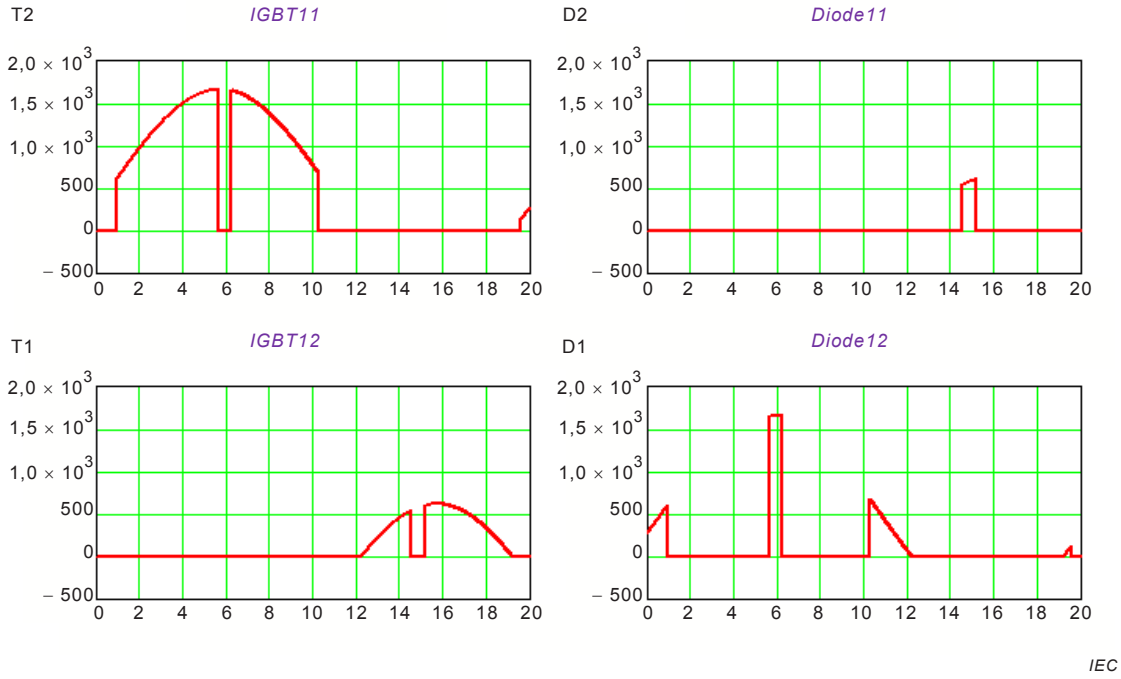


Figure A.11 – Inverter operation example of switching events

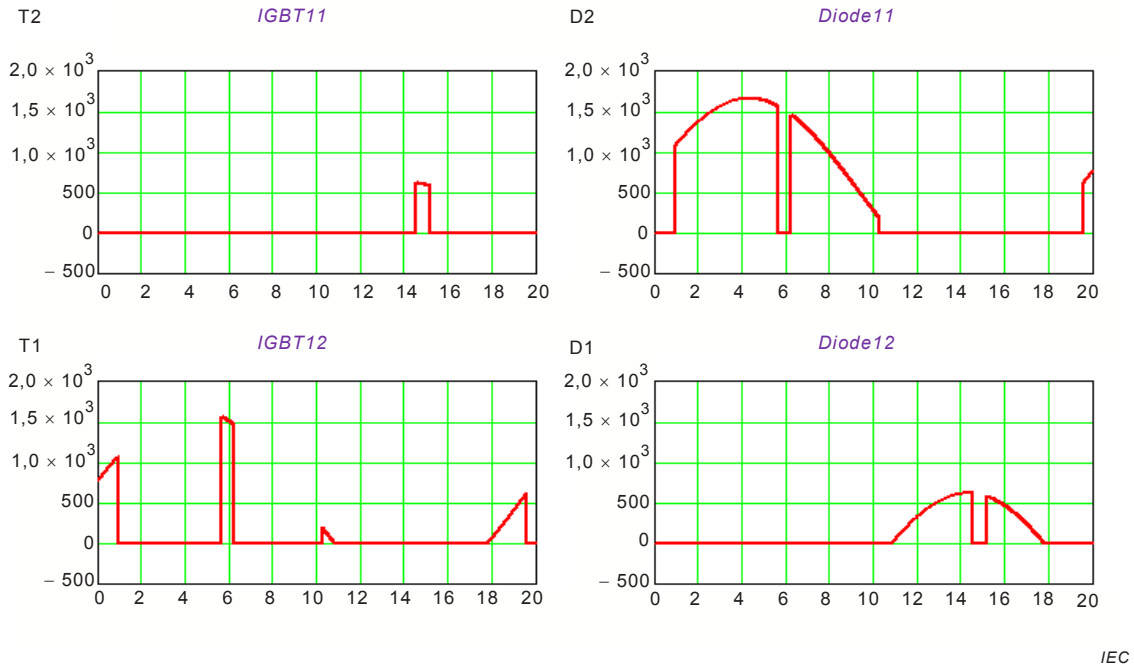


Figure A.12 – Rectifier operation example of switching events

As the two switches in each valve (S1 and S2 with its respective devices here denoted T1, D1 and T2, D2) are stressed with different current and switching events, they need to be calculated separately.

The time of the switching events and the amplitude of the current are dependent on the operational condition of the converter:

– a.c. voltage;
– d.c. voltage;
– active power;
– reactive power;
– modulation strategy.

All series connected MMC building blocks will be stressed with the same switching events, but at different occasions. Thus the same average and rms currents are valid for all MMC building blocks.

The upper valve arm and lower valve arms are also stressed in a similar way.

In rectifier mode, it can be seen that the highest currents flow in either T1 or D2. However, at the time when the current is highest, the valve voltage is near zero, so most MMC building blocks are bypassed and current flows predominantly in D2. D2 therefore has the highest conduction loss in rectifier mode, with only modest conduction losses in T1 and D1, and very low conduction losses in T2.

Conversely, in inverter mode, T2 experiences the highest conduction losses with only modest conduction losses in T1 and D1, and very low conduction losses in D2.

In Figure A.9 it can be seen that the peak valve current is approximately equal to the d.c. current; however this is in general not exactly the case, as the peak valve current may be higher or lower than the d.c. current, depending on the modulation strategy, amount of reactive power and transformer tapchanger position (if appropriate).

A.3.2 Conduction losses in semiconductors

A.3.2.1 Approximate analytical solution

It will be noted from Figure A.8 that at any time there is always one, and only one, current path conducting in each MMC building block.

If the on-state voltage characteristics of the four switch positions in the MMC building block were identical, calculation of the semiconductor device conduction losses would be straightforward, since there would be no need to know the operating state of the MMC building block at any time. The total semiconductor conduction loss per MMC building block would then simply be given by:

$$P_{\text{cond}} = N_c \left(V_0 \cdot I_{\text{vav}} + R_0 \cdot I_{\text{vrms}}{}^2 \right) \tag{A.2}$$

where

N_{c} is the number of series-connected semiconductor devices per switch position;

V_0, R_0 are the threshold voltage and slope resistance of the device;

I_{vav} is the mean value of the rectified current in the valve, averaged over one power-frequency cycle (Figure A.13).

$$I_{\text{vav}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} \left| i_{\text{v}}(\omega t) \right| \cdot \mathrm{d}(\omega t) \tag{A.3}$$

I_{vav} is not the same as the mean valve current, which is simply $I_{\text{d}}/3$. For these purposes, the rectified current is needed because current will only flow in those semiconductor device(s) which are forward biased.

I_{vrms} is the rms current in the valve, averaged over one power-frequency cycle.

$$I_{\text{vrms}} = \sqrt{\frac{1}{2\pi} \cdot \int_0^{2\pi} i_{\text{v}}(\omega t)^2 \cdot \mathrm{d}(\omega t)} \tag{A.4}$$

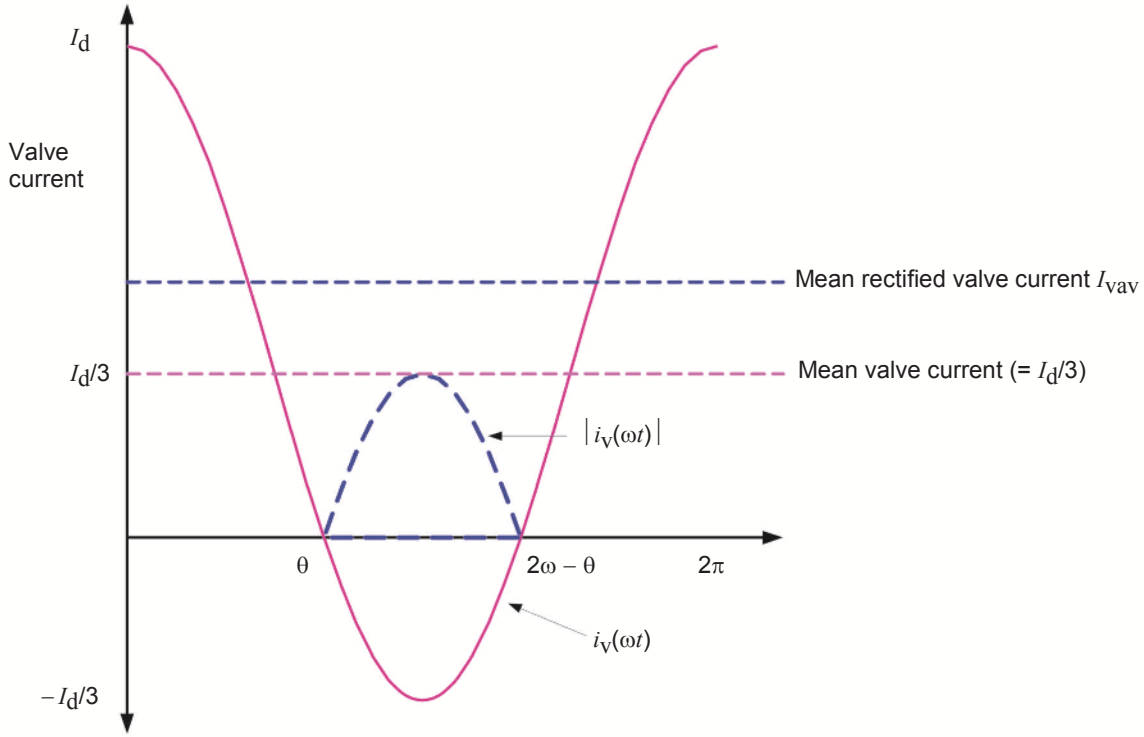


Figure A.13 – Valve current and mean rectified valve current

Knowing that the valve current can be expressed as:

$$i_v(\omega t) = \frac{I_d}{3} + \frac{I_L \cdot \sqrt{2}}{2} \times \sin(\omega t) \tag{A.5}$$

An analytical solution can easily be found:

$$I_{vav} = \frac{1}{\pi} \cdot \left[\frac{I_d}{3} \cdot (2\theta - \pi) + I_L \cdot \sqrt{2} \cdot \sin\theta \right] \tag{A.6}$$

$$I_{vrms} = \sqrt{\frac{I_d^2}{9} + \frac{I_L^2}{4}} \tag{A.7}$$

where

$$\theta = \cos^{-1}\left[\frac{-I_d \cdot \sqrt{2}}{3 \cdot I_L} \right] \tag{A.8}$$

The angle θ corresponds to the point where valve current crosses zero.

Since the current flows mainly in diodes in rectifier mode, and mainly in IGBTs in inverter mode, a reasonable approximation to the conduction losses per MMC building block may be obtained from Equations (A.2), (A.6) and (A.7) as follows:

Rectifier mode:

$$P_{\text{cond\_rec}} = V_{0\_\text{Diode}} \cdot I_{\text{vav}} + R_{0\_\text{Diode}} \cdot I_{\text{vrms}}{}^2 \quad \text{(A.9)}$$

Inverter mode:

$$P_{\text{cond\_inv}} = V_{0\_\text{IGBT}} \cdot I_{\text{vav}} + R_{0\_\text{IGBT}} \cdot I_{\text{vrms}}{}^2 \quad \text{(A.10)}$$

A.3.2.2 Exact analytical solution

The approximate analytical solution presented in the previous subclause assumes that V_0 and R_0 are the same for all the IGBTs and diodes in the MMC building block. Generally this is not true: the IGBTs normally have different values of V_0 and R_0 to the diodes (generally, V_0 and R_0 are higher for the IGBT than the diode) and it is possible for different types of IGBT and diode to be used in the upper and lower switch positions in the MMC building block. In addition, this approach neglects the circulating currents which may occur between phases, depending on the design of controller.

In many cases these assumptions could introduce an unacceptably large error into the calculation process.

A more exact process involves separately calculating the values of I_{av} and I_{rms} for each of the four switch positions in the MMC building block and thus calculating the conduction loss separately for each device.

As noted in the previous subclause, the location of the one switch position that is carrying current at a given time depends on the direction of the current and the switching state of the MMC building block (bypassed or active state). Since the switching state may change several times per fundamental-frequency cycle, it is not practical to calculate the instantaneous conduction loss in each switch position, but neither is it necessary. What is needed is to calculate the conduction loss in each switch position averaged over a period of some few cycles or seconds. However, this is also not straightforward to calculate, since it depends in a complex way on the control strategy for the converter.

For some operating points, for example when the valve current and valve voltage are exactly 180° out of phase, an exact (though complex) analytical solution is possible. Such solutions rely on a statistical approach to the operating state (active or bypassed) of the MMC building block. Although it is not possible to know the exact operating state of an MMC building block at any given time, it is possible to calculate the probability that the MMC building block will be in a given state at that time, since the probability that the MMC building block is in the active state is directly proportional to the valve voltage. It is therefore possible to construct a mathematical equation linking the valve current to the valve voltage, both of which can be described mathematically.

The statistical probability that a given MMC building block will be in the active state can be expressed by the term $p_{\text{c}}(\omega t)$:

$$p_{\text{c}}(\omega t) = \frac{u_{\text{v}}(\omega t)}{N_{\text{tc}} \cdot u_{\text{c\_av}}(\omega t)} \quad \text{(A.11)}$$

where

N_{tc} is the number of MMC building blocks per valve;

$u_{\text{v}}(\omega t)$ is the valve voltage as a function of time;

$u_{\text{c\_av}}(\omega t)$ is the mean MMC building block d.c. capacitor voltage as a function of time.

The probability that a given MMC building block is in the bypassed state is then simply $(1 - p_c(\omega t))$.

T1 and D1 only conduct when the link is in the active state. So the average and rms currents are found by integrating the product of valve current and $p_c(\omega t)$ over the conduction period appropriate to each semiconductor.

$$I_{av} = \frac{1}{2\pi} \cdot \int_{\omega t_1}^{\omega t_2} i_v(\omega t) \cdot p_c(\omega t) \cdot \mathrm{d}(\omega t) \tag{A.12}$$

$$I_{rms} = \sqrt{\frac{1}{2\pi} \cdot \int_{\omega t_1}^{\omega t_2} i_v^{\,2}(\omega t) \cdot p_c(\omega t) \cdot \mathrm{d}(\omega t)} \tag{A.13}$$

where

ωt_1 and ωt_2 are the points at which the valve current changes sign.

T1 only conducts when current is negative. Hence for evaluation of the current in T1, ωt_1 is taken to be where current changes from positive to negative and ωt_2 is taken to be where current changes from negative to positive.

D1 only conducts when current is positive. Hence for evaluation of the current in D1, ωt_1 is taken to be where current changes from negative to positive and ωt_2 is taken to be where current changes from positive to negative.

T2 and D2 only conduct when the link is in the bypassed state. So the average and rms currents are found by integrating the product of valve current and $(1 - p_c(\omega t))$ over the conduction period appropriate to each semiconductor:

$$I_{av} = \frac{1}{2\pi} \cdot \int_{\omega t_1}^{\omega t_2} i_v(\omega t) \cdot (1 - p_c(\omega t)) \cdot \mathrm{d}(\omega t) \tag{A.14}$$

$$I_{rms} = \sqrt{\frac{1}{2\pi} \cdot \int_{\omega t_1}^{\omega t_2} i_v^{\,2}(\omega t) \cdot (1 - p_c(\omega t)) \cdot \mathrm{d}(\omega t)} \tag{A.15}$$

T2 only conducts when current is positive. Hence for evaluation of the current in T2, ωt_1 is taken to be where current changes from negative to positive and ωt_2 is taken to be where current changes from positive to negative.

D2 only conducts when current is negative. Hence for evaluation of the current in D2, ωt_1 is taken to be where current changes from positive to negative and ωt_2 is taken to be where current changes from negative to positive.

Even when it is possible to represent i_v and p_c mathematically, and even for the simplified case where the valve current and valve voltage are exactly 180° out of phase, the analytical solution to these equations is complex. At the time of publication, no exact analytical solution has been found for the general case where valve current and valve voltage are not exactly 180° out of phase.

A.3.3 MMC building block d.c. capacitor losses

To calculate the MMC building block d.c. capacitor losses, it is necessary only to know the rms current in the capacitor, I_{crms}. The mean current in the capacitor is zero in steady-state

$$I_{\mathrm{D1\_av}} + I_{\mathrm{T1\_av}} = 0 \tag{A.16}$$

Once the rms current has been determined for each of the four semiconductor devices, according to the preceding subclause, the rms capacitor current can be found easily from the vectorial sum of the rms currents in T1 and D1:

$$I_{\mathrm{crms}} = \sqrt{{I_{\mathrm{D1\_rms}}}^2 + {I_{\mathrm{T1\_rms}}}^2} \tag{A.17}$$

A.3.4 Other conduction losses

Other conduction losses in the valve are dominated by the resistive (I^2R) losses in busbars from each MMC building block to its neighbours. Here, only the rms valve current I_{vrms}, as given in Equation (A.7), is required.

A.4 Switching losses

A.4.1 Description of state changes

A.4.1.1 General

Every time an MMC building block changes state from bypassed to active state or vice versa, or the direction of current reverses, one switch position in the MMC building block turns off and another turns on. The turn-on of an IGBT is always accompanied by the turn-off of a diode, and vice-versa.

Switching events may be categorised as “soft” or “hard”. Transitions which occur as a result of the reversal of valve current that occurs twice per cycle are referred to as “soft”, while those that occur as a result of state changes from bypassed to active state or vice versa, are referred to as “hard”. Only the hard switching events are of significance in the calculation of losses, because the rate of change of current (di/dt) is several orders of magnitude higher than for soft-switching events.

A.4.1.2 Hard switching events

Table A.1 summarises the effects of the four possible hard switching events in the MMC building block.

Table A.1 – Hard switching events

Current direction	MMC building block state change	Effects	Total switching energy
Negative	Bypassed to active	T1 turns on; D2 turns off	$E_{\mathrm{on\_T1}} + E_{\mathrm{rec\_D2}}$
Negative	Active to bypassed	T1 turns off; D2 turns on	$E_{\mathrm{off\_T1}}$
Positive	Bypassed to active	T2 turns off; D1 turns on	$E_{\mathrm{off\_T2}}$
Positive	Active to bypassed	T2 turns on; D1 turns off	$E_{\mathrm{on\_T2}} + E_{\mathrm{rec\_D1}}$

Since diodes are not controllable, hard switching events are always initiated by the switching of an IGBT. The transition from IGBT to diode is initiated by turning off the IGBT while current is flowing in it. The current, which is flowing through a substantial external inductance, then

has nowhere else to flow except into the diode in the other switch position of the MMC building block. Current then commutates from the IGBT to the diode at a rate determined by the inductance of the loop formed by the IGBT, diode and capacitor. The IGBT experiences a voltage overshoot as a result of this event.

The transition from diode to IGBT is initiated by turning on the IGBT while the diode in the other switch position of the MMC building block is conducting. This temporarily creates a short circuit with the d.c. capacitor connected in series with the diode and the IGBT that has just turned on. The current in the diode falls very rapidly at a rate given by the capacitor voltage divided by the inductance of the loop formed by the IGBT, diode and capacitor. After the current in the diode passes through zero, the diode experiences a short period of reverse current and then finally turns off, incurring a “recovery energy”.

Each hard switching event results in a switching energy dissipation in the IGBT (E_{on} or E_{off}) and those events that involve the turn-off of a diode also result in a recovery energy E_{rec} (diodes have negligible turn-on loss). E_{on}, E_{off} and E_{rec} depend on the instantaneous device current at the time of switching, the d.c. capacitor voltage and the junction temperature. The dependence on current is illustrated on Figure A.14. Switching and recovery energies also increase with voltage (almost linearly) and with temperature.

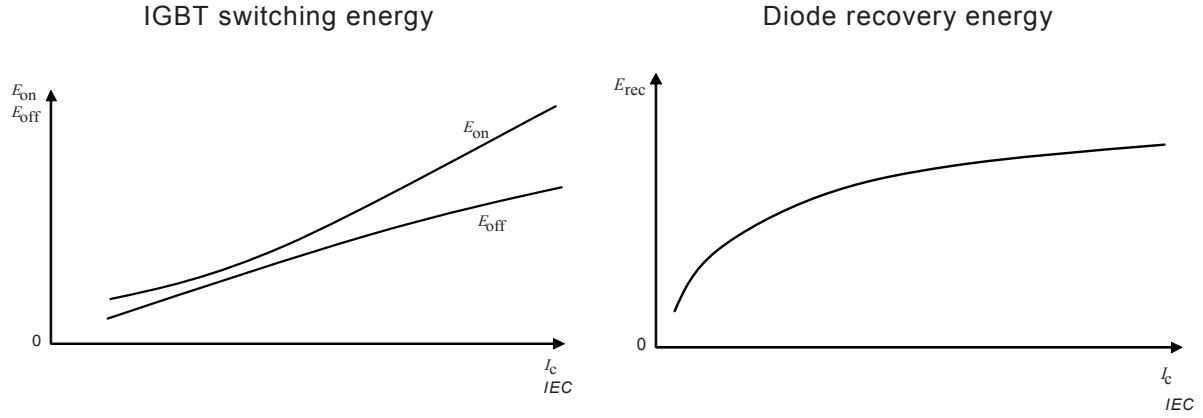


Figure A.14 – IGBT and diode switching energy as a function of collector current

In order to be able to calculate the switching losses for any operating condition, the IGBT and diode used should be characterised thoroughly to define E_{on}, E_{off} and E_{rec} as functions of voltage, current and temperature. The characterisation results may be presented graphically or in a look-up table but a mathematical model is preferred, since it permits the subsequent calculation process to be more easily automated.

A.4.1.3 Soft switching events

Table A.2 summarises the effects of the four possible soft switching events in the MMC building block.

The soft switching events are mentioned only for the sake of completeness, since they do not directly result in switching energy dissipation in the semiconductors. However, the changes of current direction may indirectly provoke some hard switching events, as the capacitor voltage balancing algorithm may cause some MMC building blocks to change from active to bypassed and some others to change from bypassed to active.

Table A.2 – Soft switching events

Change of current direction	MMC building block state	Effects
Negative to positive	Bypassed	D2 turns off; T2 turns on
Negative to positive	Active	T1 turns off; D1 turns on
Positive to negative	Bypassed	T2 turns off; D2 turns on
Positive to negative	Active	D1 turns off; T1 turns on

A.4.2 Analysis of state changes during cycle

In principle, calculation of the total switching losses in the MMC building block requires only that the instantaneous voltage and current is known for each of the various switching events during a cycle. The switching energy per event can then be calculated from knowledge of how E_{on}, E_{off} and E_{rec} vary with voltage and current for the applicable junction temperature, and the switching losses in the complete cycle are obtained by summing each individual event.

However, unlike a 2-level converter, where the d.c. capacitor voltage is fixed and the switching pattern is deterministic and easily analysed, calculating the switching conditions for every switching event in a modular multi-level converter is very complex. There are two principal reasons leading to this complexity:

– the timings of the switching events with respect to the valve current waveform are somewhat unpredictable, since they are governed by the algorithms used for monitoring and balancing the MMC building block d.c. capacitor voltages;
– because the valve current flows through the MMC building block d.c. capacitor for part of each cycle, the capacitor experiences a very large ripple voltage (typically ±20 % of nominal). Moreover, every MMC building block d.c. capacitor in the valve will have a different capacitor voltage at any instant.

For these reasons the only practical way of determining the average switching losses in the IGBTs and diodes is by means of a very detailed numerical simulation. The simulation model should represent the valve in as much detail as possible, including a mathematical model representing the switching energies of the semiconductor devices, along with a representation of at least those parts of the control system that are responsible for producing the valve voltage order and for balancing the MMC building block d.c. capacitors.

A.4.3 Worked example of switching losses

To illustrate the typical switching behaviour of an MMC valve, this subclause describes a simple simulation performed on a hypothetical MMC valve consisting of 5 submodules in series, each with a nominal submodule d.c. capacitor voltage of 2 kV. The valve is assigned a sinusoidal voltage order equal to 5 kV – 5 kV×cos (ωt) and carries a sinusoidal current equal to (333 A + 667 A × cos (ωt)).

Submodules are switched only at 1 ms intervals, according to a simple set of rules:

– if the current through the valve is positive (i.e. in the direction which charges up the submodules that are in active mode), then the submodule with the lowest voltage is switched into circuit first, then the one with the second lowest voltage, and so on until the target voltage is met as closely as possible;
– if the current through the valve is negative (i.e. in the direction which discharges the submodules that are in active mode), then the submodule with the highest voltage is switched into circuit first, then the one with the second highest voltage, and so on until the target voltage is met as closely as possible.

The results of a simulation in which the five submodules initially have voltages of 1 800 V, 1 900 V, 2 000 V, 2 100 V and 2 200 V are shown graphically on Figure A.15.

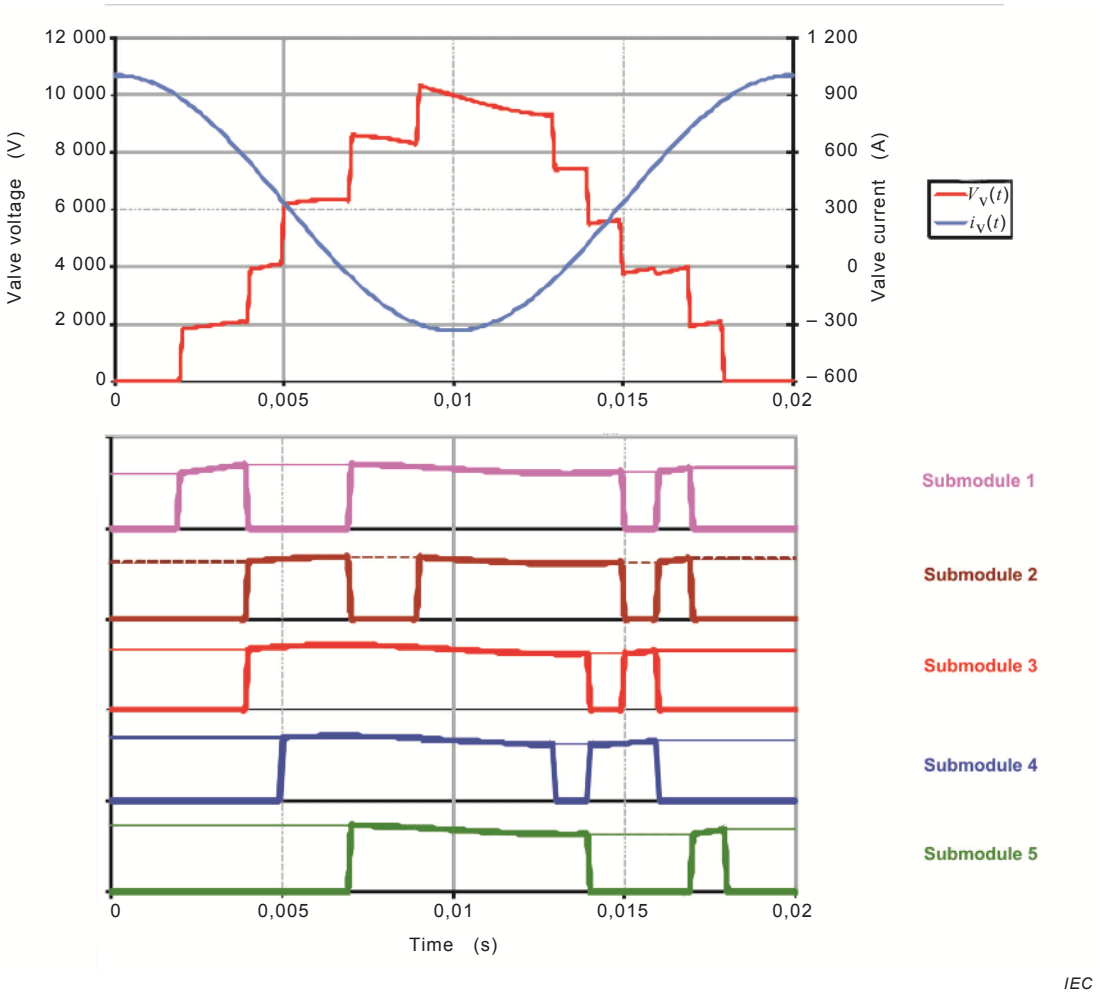


Figure A.15 – Valve voltage, current and switching behaviour for a hypothetical MMC valve consisting of 5 submodules

It will be observed that two of the submodules undergo three complete on/off cycles during the fundamental frequency cycle, while the other three undergo only two. Table A.3 summarises the 24 switching events during the cycle.

If the switching energies E_{on}, E_{off} and E_{rec} can be represented as functions of voltage and current, either mathematically or via look-up tables, the switching energy can be calculated for each event and then summed for the complete valve.

Although this is only a purely hypothetical example, it illustrates the complex and unpredictable nature of the switching behaviour of the MMC valve, and the fact that this behaviour is very much influenced by the algorithms used for balancing the capacitor voltages.

Table A.3 – Summary of switching events from Figure A.15

Time ms	**Current** A	**Submodule no.**	**Submodule voltage** V	**State change**	**Switching energy**
2	873	1	1 800	Bypassed – active	E_{off_T2}
4	539	1	2 087	Active – bypassed	$E_{on\_T2} + E_{rec\_D1}$
4	539	2	1 900	Bypassed – active	E_{off_T2}
4	539	3	2 000	Bypassed – active	E_{off_T2}
5	333	4	2 100	Bypassed – active	E_{off_T2}
7	–59	1	2 087	Bypassed – active	$E_{on\_T1} + E_{rec\_D2}$
7	–59	2	2 039	Active – bypassed	E_{off_T1}
7	–59	5	2 200	Bypassed – active	$E_{on\_T1} + E_{rec\_D2}$
9	–302	2	2 039	Bypassed – active	$E_{on\_T1} + E_{rec\_D2}$
13	–59	4	1 865	Active – bypassed	E_{off_T1}
14	127	3	1 858	Active – bypassed	$E_{on\_T2} + E_{rec\_D1}$
14	127	4	1 865	Bypassed – active	E_{off_T2}
14	127	5	1 919	Active – bypassed	$E_{on\_T2} + E_{rec\_D1}$
15	333	1	1 852	Active – bypassed	$E_{on\_T2} + E_{rec\_D1}$
15	333	2	1 883	Active – bypassed	$E_{on\_T2} + E_{rec\_D1}$
15	333	3	1 858	Bypassed – active	E_{off_T2}
16	539	1	1 852	Bypassed – active	E_{off_T2}
16	539	2	1 883	Bypassed – active	E_{off_T2}
16	539	3	1 946	Active – bypassed	$E_{on\_T2} + E_{rec\_D1}$
16	539	4	1 998	Active – bypassed	$E_{on\_T2} + E_{rec\_D1}$
17	725	1	1 979	Active – bypassed	$E_{on\_T2} + E_{rec\_D1}$
17	725	2	2 010	Active – Bypassed	$E_{on\_T2} + E_{rec\_D1}$
17	725	5	1 919	Bypassed – active	E_{off_T2}
18	873	5	2 079	Active – bypassed	$E_{on\_T2} + E_{rec\_D1}$

The example also shows how effective the simple capacitor balancing strategy outlined above can be, even with switching times limited to very coarse steps of 1 ms. An initial voltage range of 400 V (1 800 V to 2 200 V) has converged to a 133 V range (1 946 V to 2 079 V) after only

one cycle. In practice a much faster update rate would be used, giving even faster convergence.

Although the example shows only a single fundamental cycle, an analysis of this type would need to extend over several cycles in order to obtain representative average results.

A.5 Other losses

A.5.1 Snubber losses

Although many MMC-type valves are able to operate without snubber circuits, in some cases snubber circuits might nevertheless be fitted to alleviate the switching stresses on the semiconductor devices or (in the case of the cascaded two-level converter) to assist with voltage sharing amongst the series-connected semiconductors.

Snubber circuits fall into two main types:

– “turn-on” snubbers, which involve an inductance in series with the semiconductor device and are intended to limit the rate of change of current and therefore reduce the turn-on stress in the IGBT and the recovery stress on the opposing diode;
– “turn-off” snubbers, which involve a capacitance in parallel with the semiconductor device and are intended to limit the rate of rise of voltage after turn-off and therefore reduce the turn-off stress on the IGBT.

Each hard switching event in an MMC building block will result in energy being dissipated in the snubber circuits, the amount of energy depending on the instantaneous voltage and current in the affected semiconductor device.

Where a turn-on snubber is fitted, each MMC building block state change involving turn-on of an IGBT will result in an energy dissipation $E_{\mathrm{sn\_on}}$ being dissipated in the snubber components.

Where a turn-off snubber is fitted, each MMC building block state change involving turn-off of an IGBT will result in an energy dissipation $E_{\mathrm{sn\_off}}$ being dissipated in the snubber components.

The sensitivity of $E_{\mathrm{sn\_on}}$ and $E_{\mathrm{sn\_off}}$ to the voltage and current at the time of switching will depend on the design of the snubber and should be demonstrated by suitable tests or simulations. Then, the determination of the snubber losses in the MMC building block over a complete cycle requires an understanding of the voltage and current at each switching event. The calculation may be performed in a very similar way to that discussed above for the semiconductor switching losses.

A.5.2 DC voltage-dependent losses

A.5.2.1 General

The d.c. voltage-dependent losses of the valve are simply the U^2/R losses in resistive components connected in parallel with the valve or with parts of the valve.

In an MMC valve, these resistive components fall into two main categories: those that are connected in parallel with the MMC building block d.c. capacitor of each MMC building block (such as capacitor discharge resistors) and those that are connected in parallel with the complete valve or large parts of the valve (for example water cooling pipes).

A.5.2.2 DC voltage-dependent losses with MMC building block – Analytical method

Resistive components connected in parallel with the d.c. capacitor of each MMC building block experience a voltage that is predominantly d.c. but with a large ripple component.

Making an assumption that the resistance parallel with each MMC building block is identical to each other (a hypothesis actually not true due to leakage currents in IGBTs and diodes etc.), the power dissipation can be simplified as:

$$P_{\mathrm{V4}} = \frac{1}{R} \cdot \sum_{i} U_{\mathrm{rms\_}i}{}^{2} \tag{A.18}$$

The rms voltage of the i^{th} MMC building block:

$$U_{\mathrm{rms\_}i} = \sqrt{\frac{1}{T} \cdot \int_{t=0}^{T} u_{\mathrm{i}}(t)^{2} \cdot \mathrm{d}t} \tag{A.19}$$

where

$u_i(t)$ is the instantaneous value (including d.c. component) of the voltage across the i^{th} resistive component, determined either by numerical simulation or analytical calculation.

For all the capacitors in the valve, typically, the voltage comprises a constant d.c. component, low order harmonics (a large part) and high order harmonics (relatively small). If the capacitor voltage balancing algorithm can effectively suppress the difference among the capacitor voltages, an approximation using mean voltage of the capacitors can be applied.

For all capacitors in the valve:

$$P = N_{\mathrm{tc}} \cdot C \cdot U_{\mathrm{cav}} \cdot \frac{\mathrm{d}U_{\mathrm{cav}}}{\mathrm{d}t} \tag{A.20}$$

where

P is the charging power on the valve as expressed by system parameters;

N_{tc} is the number of MMC building blocks per valve;

U_{cav} is the mean voltage of the capacitors.

This is not easy to give out an analytical result for U_{cav}, but noting that:

$$\int P = \frac{1}{2} \cdot N_{\mathrm{tc}} \cdot C \cdot (U_0 + \Delta U)^2 - \frac{1}{2} \cdot N_{\mathrm{tc}} \cdot C \cdot U_0{}^{2} \approx N_{\mathrm{tc}} \cdot C \cdot U_0 \cdot \Delta U \tag{A.21}$$

where

ΔU is the rms ripple of the mean voltage of capacitors.

In the above equation, the term $\Delta\ U^2$ has been neglected. Consequently, the power dissipation can be expressed by input parameters.

Note that the power dissipation is relatively large when the converter is absorbing reactive power from the a.c. network, due to the increasing ripple voltage.

For redundant levels, two possible scenarios should be considered.

a) The capacitor voltages are constant even when the redundant levels are shorted, which means that the redundant levels just participate in the balancing action, but not in building the d.c. voltage. As the redundant levels are shorted, the total losses will decrease, but the single MMC building block loss will increase due to the increasing ripple.

b) The capacitor voltages are not constant, which means that all MMC building blocks are input to build the d.c. voltage. As the redundant levels are shorted, the total losses and the single MMC building block loss will both increase due to the increasing d.c. component of each capacitor.

A.5.2.3 DC voltage-dependent losses with valve – Analytical method

For resistive components connected in parallel with the complete valve or large parts of the valve such as water cooling pipes, the voltage experienced can also be achieved by a statistical approach.

For any MMC building block, the probability of being in the active state is identical to the others, which is proportional to the valve voltage:

$$p_{\mathrm{c}}(\omega t) = \frac{u_{\mathrm{v}}(\omega t)}{N_{\mathrm{tc}} \cdot u_{\mathrm{c\_av}}(\omega t)} \tag{A.22}$$

where

N_{tc} is the number of MMC building blocks per valve;

$u_{\mathrm{v}}\ (\omega t)$ is the valve voltage as a function of time;

$u_{\mathrm{c\_av}}\ (\omega t)$ is the mean MMC building block d.c. capacitor voltage as a function of time.

Whether for complete valve or parts of the valve, the voltage between the resistive components can be expressed as:

$$u(\omega t) = \frac{n \cdot u_{\mathrm{v}}(\omega t)}{N_{\mathrm{tc}}} \tag{A.23}$$

where

n is the total number of MMC building blocks in parallel with the resistive components (for complete valve, $n = N_{\mathrm{tc}}$).

For a typical sinusoidal modulation, the analytical result can be expressed as:

$$P_{\mathrm{av}} = \frac{1}{2\pi} \cdot \int_0^{2\times\pi} \frac{\left(\frac{n \cdot u_{\mathrm{v}}(\omega t)}{N_{\mathrm{tc}}}\right)^2}{R} \cdot \mathrm{d}(\omega t) = \frac{1}{2\pi} \cdot \int_0^{2\cdot\pi} \frac{n^2}{{N_{\mathrm{tc}}}^2} \cdot \frac{\left(\frac{U_{\mathrm{d}}}{2} \pm U_C\right)^2}{R} \cdot \mathrm{d}(\omega t)$$

$$P_{\mathrm{av}} = \frac{n^2 \cdot U_{\mathrm{d}}^2}{4 \cdot N_{\mathrm{tc}}^2 \cdot R} \cdot \left[1 + \frac{M^2}{2}\right] \tag{A.24}$$

where

M is the modulation index.

NOTE For numerical solution, the valve is simulated in some detail with sufficiently detailed representation of the control system, or detailed resistance parallel with MMC building block capacitors and the valve or valve sections such as: resistive voltage grading circuits (d.c. grading circuits), resistive voltage dividers for voltage measurement, water cooling pipework, shunt resistive losses across capacitor dielectric material, discharge resistors across d.c. capacitors.

A.5.3 Valve electronics power consumption

A.5.3.1 General

The basic principle of the valve electronics power consumption is almost the same as that described in IEC 62751-1. With the MMC topology, the difference is that the power consumption of the valve electronics for each MMC building block varies from cycle to cycle, since the IGBT on-off operation status is not instantaneously the same in all MMC building blocks. Hence, it is necessary to take an average value to evaluate the power consumption.

A.5.3.2 Topology of power supply circuit

A.5.3.2.1 General

Two types of power supply circuit have been assumed, the first in which the power supply is connected across each IGBT and the second in which the power supply is connected between the terminals of the submodule d.c. capacitor.

A.5.3.2.2 Type A

The power circuit is connected to the collector and to the emitter of each VSC level. The circuit derives the power from the voltage across VSC level and supply to the valve electronics. For easy understanding, the concept is shown in Figure A.16

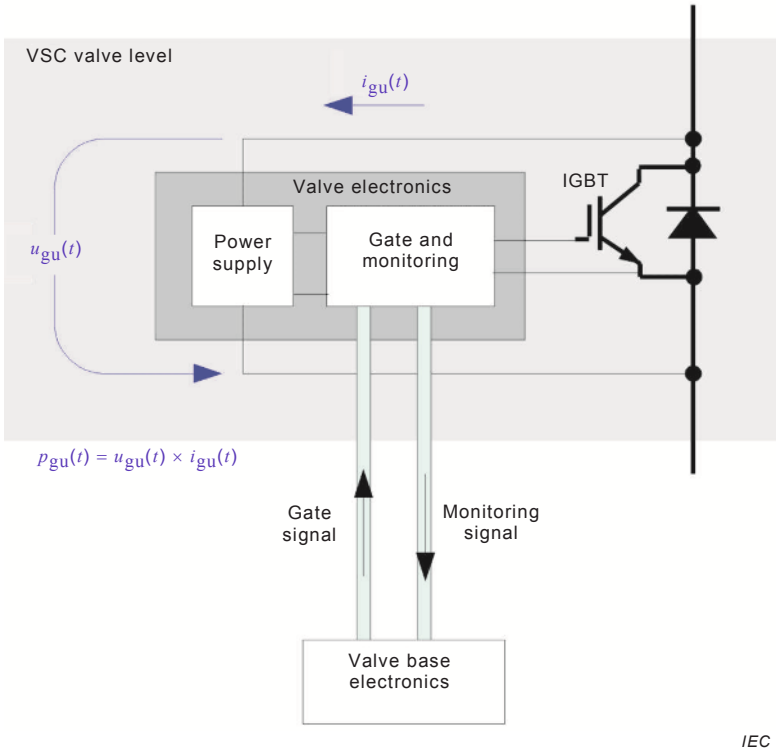


Figure A.16 – Power supply from IGBT terminals

In this case, the instantaneous power consumed in the power supply is given by multiplying the voltage and current as shown in the figure. Then, in order to obtain the average value, the instantaneous power is integrated for one second.

After taking average, the average power of every VSC level is summed up to obtain the total power consumption of the valve.

When the power circuit is integrated into the snubber circuit, the power consumption may be included in the snubber circuit loss.

This Type A can be applied to the VSC level of the CTL cell as shown Figure A.17.

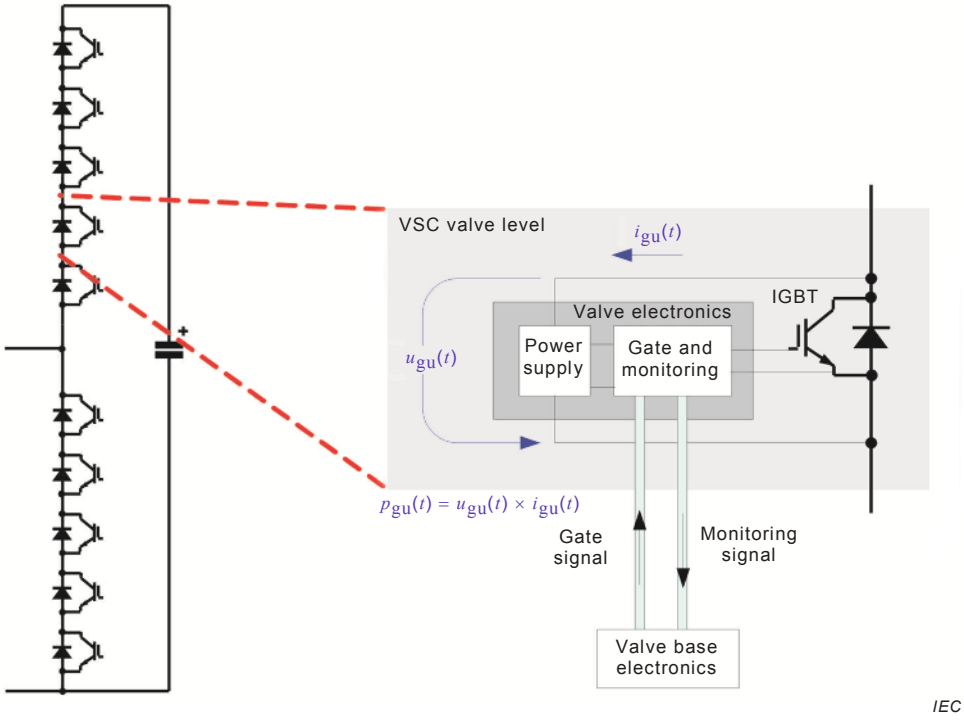


Figure A.17 – Power supply from IGBT terminals in cell

A.5.3.2.3 Type B

The power circuit is connected to the terminals of d.c. capacitor in the submodule. The circuit derives the power from the voltage of the d.c. capacitor and supply to the valve electronics. The concept is shown in Figure A.18.

In this case, the power circuit feeds the power to two IGBTs in the submodule. The number of power circuits is equal to the number of submodules. Then, the number for summation is the number of submodules to obtain the total power consumption of the valve.

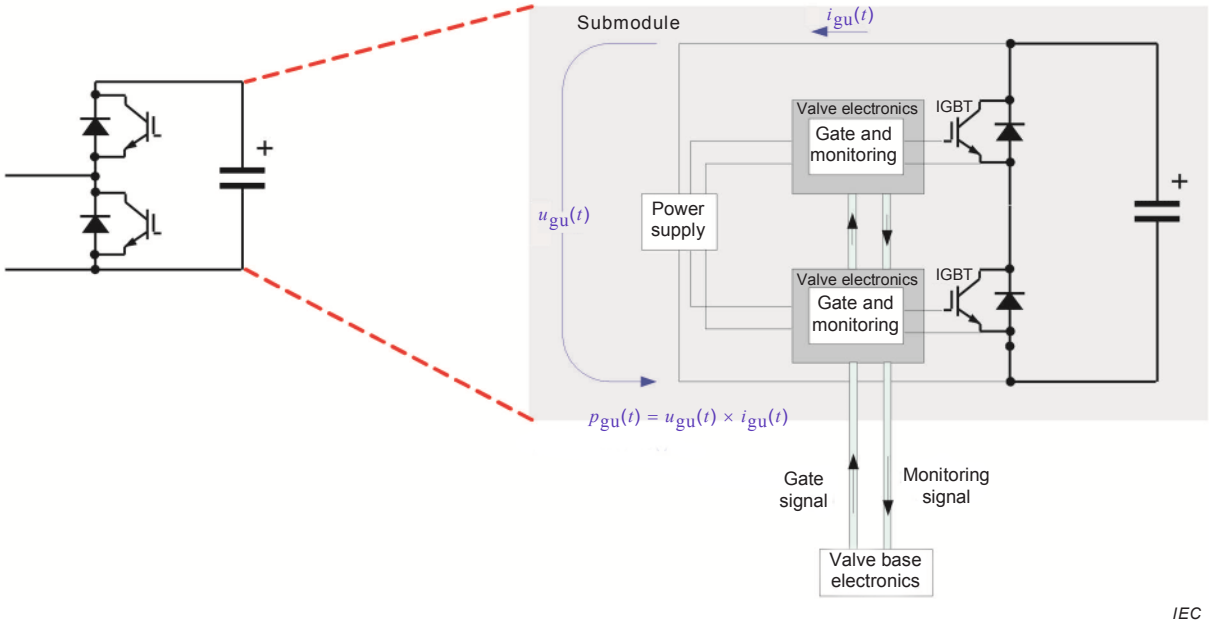


Figure A.18 – Power supply from d.c. capacitor in submodule

This type B mainly applies to the submodule-type valve. It is not considered to be easy to apply to CTL since insulation between the power supply and IGBT requires much higher voltage withstand capability.

A.6 Application to other variants of valve

A.6.1 General

The previous analysis has considered only the two-level, “half-bridge” MMC building block. Although this is a well-known variant of the valve, it is not the only variant that is possible. “Full-bridge” variants of MMC building blocks are also possible, as are MMC building blocks based on three-level or other multi-level converter arrangements.

A.6.2 Two-level full-bridge MMC building block

A “full-bridge” MMC building block is shown in Figure A.19. This performs the same function as the half-bridge MMC building block but has additional flexibility, in that the capacitor can be inserted into the circuit in either polarity. However, this circuit contains four IGBTs instead of two, and therefore suffers from much higher conduction losses per MMC building block (for a given current, approximately twice that of the half-bridge MMC building block).

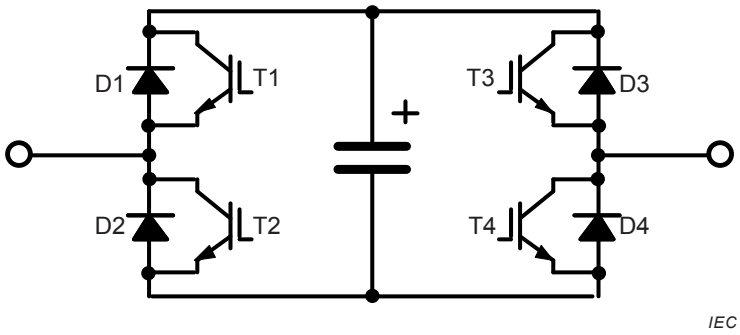


Figure A.19 – One “full-bridge”, two-level MMC building block

The full-bridge MMC building block has four possible conducting states for each polarity of current: active positive, active negative, upper bypass and lower bypass, plus the fifth blocking state. The two “bypass” states are redundant.

If “active positive” is taken to be the state in which the left hand terminal is positive with respect to the right-hand terminal, then the eight combinations of current direction and MMC building block state are as follows:

– current →, upper bypass: D1+T3 conducting
– current →, lower bypass: T2+D4 conducting
– current →, active positive: D1+D4 conducting
– current →, active negative: T2+T3 conducting
– current ←, upper bypass: T1+D3 conducting
– current ←, lower bypass: D2+T4 conducting
– current ←, active positive: T1+T4 conducting
– current ←, active negative: D2+D3 conducting

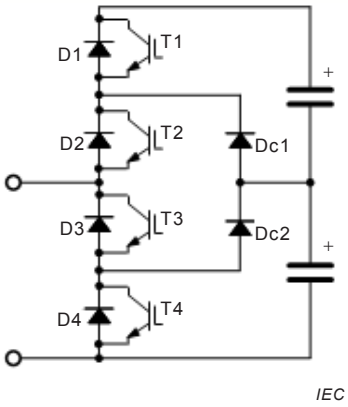
In contrast to the half-bridge MMC building block, where current flows mainly in diodes in rectifier mode and IGBTs in inverter mode, the IGBTs and diodes in the full-bridge MMC building block carry approximately the same current. Consequently the conduction losses are approximately the same in both rectifier and inverter modes, which is not the case for the half-bridge MMC building block.

Although the conduction losses of a full-bridge MMC building block are approximately twice as high as those of a half-bridge MMC building block operating at the same current, the full-bridge arrangement allows the converter to achieve a peak converter a.c. voltage that exceeds the d.c. pole-to-pole voltage and thus permits a lower a.c. current. The overall conduction losses of the full-bridge converter are therefore less than twice those of a half-bridge converter.

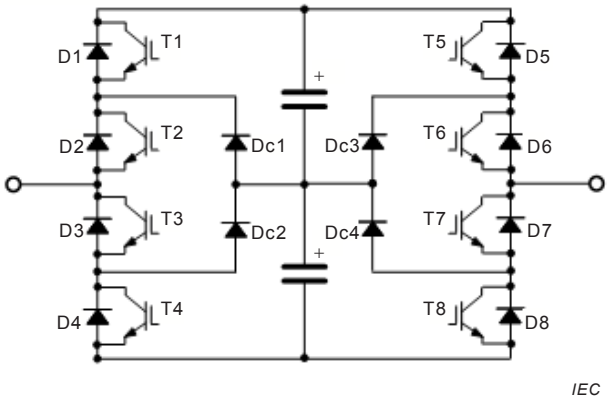
For a given voltage and current, the switching losses of the full-bridge MMC building block are the same as for the half-bridge MMC building block. This is because each individual switching event only affects one side of the bridge at a time.

A.6.3 Multi-level MMC building blocks

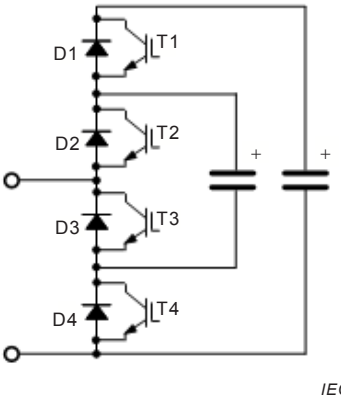
The MMC building blocks (submodules) shown in Figure A.7 and Figure A.19 and used in the traditional “two-level” converter, produce two discrete values of output voltage in each permitted polarity. In principle it is possible to conceive of MMC building block designs based on larger numbers of output levels. For example, there are four possible designs of MMC building block based on “three-level” converter topologies, as shown on Figure A.20.



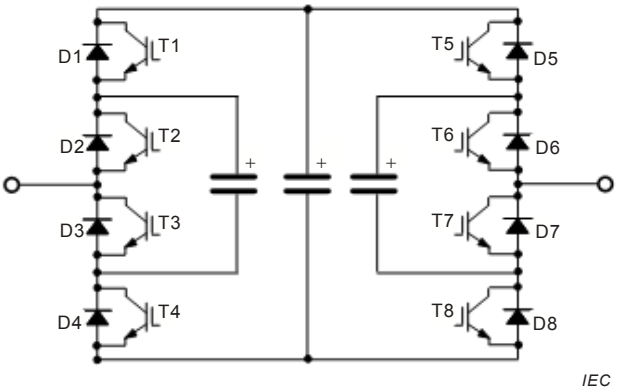
a) Three-level NPC half-bridge



b) Three-level NPC full-bridge



c) Three-level flying capacitor half-bridge



d) Three-level flying capacitor full-bridge

Figure A.20 – Four possible variants of three-level MMC building block

The three-level half-bridge variants each have twice as many semiconductor devices per MMC building block as the two-level half-bridge MMC building block, and at any given time two semiconductor devices per MMC building block are always in conduction. On the other hand the output voltage of the three-level MMC building block is twice that of the two-level MMC building block, so the overall conduction losses of the valve are essentially the same as those of a valve based on the two-level half-bridge MMC building block.

Likewise, the three-level full-bridge variants have approximately twice the conduction losses (per MMC building block) of the two-level full-bridge MMC building block, but the overall conduction losses of the valve are essentially the same as those of a valve based on the two-level full-bridge MMC building block.

Analysis of the switching losses of such converters is slightly more complex than for the two level converters, but the principle still holds true that each switching event results in either the turn-on of an IGBT and the turn-off of a diode, or vice-versa. Consequently, for a given voltage rating, there should be no significant difference between the switching loss of a three-level MMC building block and the combined switching losses of the two, two-level MMC building blocks to which it is equivalent.

Other variants can also be imagined, with both half-bridge and full-bridge variants with four, five or even more levels, and even with asymmetrical output voltages (for example +2 V, +1 V, 0 and -1 V).

Bibliography

IEC 60747-1, *Semiconductor devices – Part 1: General*

IEC 60747-2, *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*

IEC 60747-9, *Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)*

IEC 61803, *Determination of power losses in high-voltage direct current (HVDC) converter stations*

IEC TR 62543, *High-voltage direct current (HVDC) transmission using voltage sourced converters (VSC)*

CIGRÉ Technical Brochure No. 269, *VSC Transmission*,

CIGRÉ Technical Brochure No. 447, *Component Testing of VSC System for HVDC Applications*,

CIGRÉ Technical Brochure No. 492, *Voltage Source Converter (VSC) HVDC for Power Transmission – Economic Aspects and Comparison with other a.c. and d.c. Technologies*,

Analysis of metrological requirements for electrical measurement of HVDC station losses; A Bergman, IEEE Transactions on Instrumentation and Measurement, Ref. IM-11-5175.

A Comparison of Two Methods of Estimating Losses in the Modular Multi-Level Converter, C D M Oates & C C Davidson, EPE Conference, Birmingham, UK, September 2011.

This page deliberately left blank

This page deliberately left blank

British Standards Institution (BSI)

BSI is the national body responsible for preparing British Standards and other standards-related publications, information and services.

BSI is incorporated by Royal Charter. British Standards and other standardization products are published by BSI Standards Limited.

About us

We bring together business, industry, government, consumers, innovators and others to shape their combined experience and expertise into standards -based solutions.

The knowledge embodied in our standards has been carefully assembled in a dependable format and refined through our open consultation process. Organizations of all sizes and across all sectors choose standards to help them achieve their goals.

Information on standards

We can provide you with the knowledge that your organization needs to succeed. Find out more about British Standards by visiting our website at bsigroup.com/standards or contacting our Customer Services team or Knowledge Centre.

Buying standards

You can buy and download PDF versions of BSI publications, including British and adopted European and international standards, through our website at bsigroup.com/shop, where hard copies can also be purchased.

If you need international and foreign standards from other Standards Development Organizations, hard copies can be ordered from our Customer Services team.

Subscriptions

Our range of subscription services are designed to make using standards easier for you. For further information on our subscription products go to bsigroup.com/subscriptions.

With **British Standards Online (BSOL)** you'll have instant access to over 55,000 British and adopted European and international standards from your desktop. It's available 24/7 and is refreshed daily so you'll always be up to date.

You can keep in touch with standards developments and receive substantial discounts on the purchase price of standards, both in single copy and subscription format, by becoming a **BSI Subscribing Member**.

PLUS is an updating service exclusive to BSI Subscribing Members. You will automatically receive the latest hard copy of your standards when they're revised or replaced.

To find out more about becoming a BSI Subscribing Member and the benefits of membership, please visit bsigroup.com/shop.

With a **Multi-User Network Licence (MUNL)** you are able to host standards publications on your intranet. Licences can cover as few or as many users as you wish. With updates supplied as soon as they're available, you can be sure your documentation is current. For further information, email bsmusales@bsigroup.com.

BSI Group Headquarters

389 Chiswick High Road London W4 4AL UK

Revisions

Our British Standards and other publications are updated by amendment or revision.

We continually improve the quality of our products and services to benefit your business. If you find an inaccuracy or ambiguity within a British Standard or other BSI publication please inform the Knowledge Centre.

Copyright

Useful Contacts:

Customer Services
Tel: +44 845 086 9001
Email (orders): orders@bsigroup.com
Email (enquiries): cservices@bsigroup.com

Subscriptions
Tel: +44 845 086 9001
Email: subscriptions@bsigroup.com

Knowledge Centre
Tel: +44 20 8996 7004
Email: knowledgecentre@bsigroup.com

Copyright & Licensing
Tel: +44 20 8996 7070
Email: copyright@bsigroup.com

bsi.

...making excellence a habit.™