BS EN 62343-4-1:2016

BSI Standards Publication

Dynamic modules

Part 4-1: Software and hardware interface — 1 x 9 wavelength selective switch

bsi.

National foreword

This British Standard is the UK implementation of EN 62343-4-1:2016. It is identical to IEC 62343-4-1:2016.

The UK participation in its preparation was entrusted by Technical Committee GEL/86, Fibre optics, to Subcommittee GEL/86/3, Fibre optic systems and active devices.

A list of organizations represented on this committee can be obtained on request to its secretary.

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Dynamic modules - Part 4-1: Software and hardware interface - 1 x 9 wavelength selective switch (IEC 62343-4-1:2016)

Modules dynamiques - Partie 4-1 : Interface logicielle et matérielle - Commutateur sélectif en longueur d'onde 1 x 9 (IEC 62343-4-1:2016)

Dynamische Module - Teil 4-1: Software und Hardware Schnittstelle - 1 x 9 Wellenlängenselektiver Schalter (IEC 62343-4-1:2016)

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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European foreword

The text of document 86C/1304/CDV, future edition 1 of IEC 62343-4-1, prepared by SC 86C “Fibre optic systems and active devices” of IEC/TC 86 “Fibre optics” was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62343-4-1:2016.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2017-01-08
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2019-04-08

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In the official version, for Bibliography, the following note has to be added for the standard indicated :

IEC 62343-3-3	NOTE	Harmonized as EN 62343-3-3.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu

Publication	Year	Title	EN/HD	Year
IEC 60050-731	-	International Electrotechnical Vocabulary - Chapter 731: Optical fibre communication	-	-
IEC 62343	-	Dynamic modules - General and guidance	EN 62343	-

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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DYNAMIC MODULES –

Part 4-1: Software and hardware interface – 1 x 9 wavelength selective switch

FOREWORD

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International Standard IEC 62343-4-1 has been prepared by subcommittee SC86C: Fibre optic systems and active devices, of IEC technical committee 86: Fibre optics.

The text of this standard is based on the following documents:

CDV	Report on voting
86C/1304/CDV	86C/1346/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62343 series, published under the general title *Dynamic modules*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

A wavelength selective switch (WSS) is a dynamic module, which is mainly used in a reconfigurable optical add drop multiplexer (ROADM) system to switch all wavelength signals to their respective required output port in dense wavelength division multiplexing (DWDM) networks. The WSS module has one input port and a plurality of output ports (i.e. 1 x N WSS) and can be used reversely, such as N input ports and one output port, depending on its application. It is electrically controlled with software, which directs each wavelength signal among an input DWDM signal from one input port to the required output port for each wavelength signal.

DYNAMIC MODULES –

Part 4-1: Software and hardware interface – 1 x 9 wavelength selective switch

1 Scope

This part of IEC 62343 describes and provides specifications for a software and hardware interface for the 1 x 9 wavelength selective switch.

These switches can be controlled by resident firmware with this interface. This standard addresses the configuration and function to control a WSS. This interface is intended to enable a user or host to retrieve the switch status and/or adjust relevant switch and attenuation settings.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-731, *International Electrotechnical Vocabulary – Chapter 731: Optical fibre communication* (available at http://www.electropedia.org)

IEC 62343, *Dynamic modules - General and guidance*

3 Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-731 and IEC 62343, as well as the following apply.

3.1.1
wavelength selective switch
WSS
dynamic module with one or more input ports and one or more output ports, which is mainly used in a reconfigurable optical add drop multiplexer (ROADM) system to switch each wavelength signal on each input port independently to its required output port in DWDM networks

Note 1 to entry: It is electrically controlled with software.

Note 2 to entry: It can be used inverted, exchanging input and output ports.

Note 3 to entry: Each wavelength signal can be independently attenuated.

3.2 Abbreviations

For the purposes of this document, the following abbreviations apply.

DWDM dense wavelength division multiplexing
WSS wavelength selective switch

ROADM	reconfigurable optical add drop multiplexer
HC	host controller
DPRAM	dual-port RAM
FPGA	field programmable gate array
DSP	digital signal processor
R/W	read or write
RW	read and write
RO	read only
CE	chip enable
OE	output enable
TxD	transmitted data
RxD	received data

4 Basic configuration of WSS interface

The software interface is intended to provide an access to the functions of the WSS module and be the primary interface to command the unit. The HC controls the WSS module by sending control signal, as well as command data, to the WSS module via a 12-bit address bus, a 16-bit data bus, and DPRAM related signal lines such as Read/Write, Chip Enable, and Output Enable. The HC also receives from the WSS module response signals and status data.

Any address within the DPRAM can be written to via the HC, however many of these values will be overwritten upon the application of a command to the WSS module. The addresses, which are identified as inputs, can be found further along in this document. In addition to the DPRAM interface, RS232 serial communication is also supported by the WSS module.

The WSS module has a non-volatile memory to store the latest setting when requested. A functional diagram of the WSS module controls is illustrated in Figure 1 below.

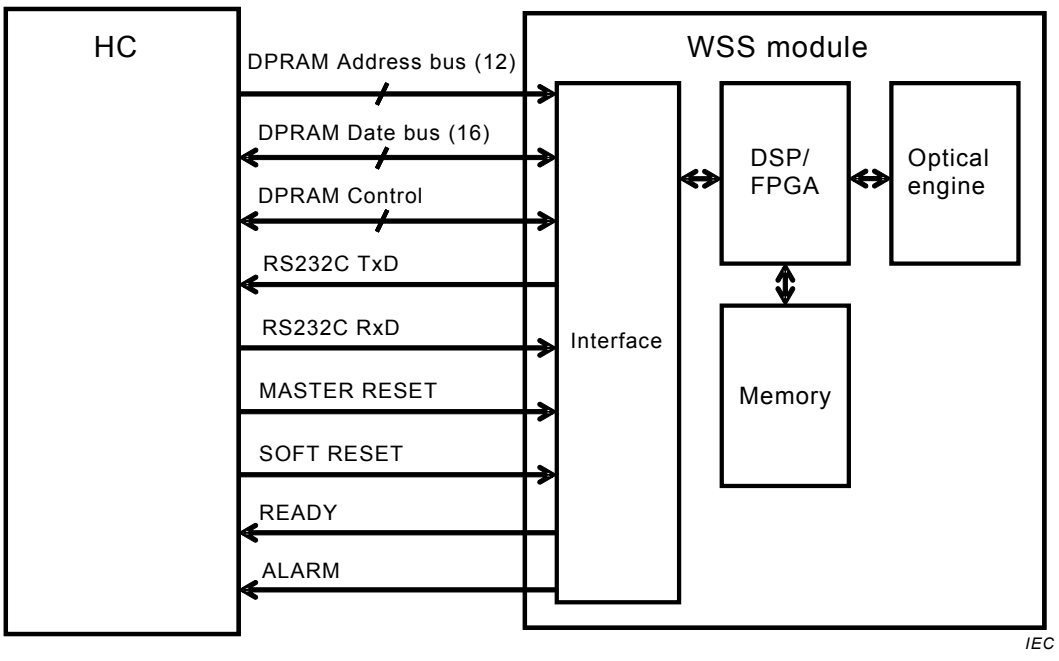

Figure 1 – Basic configuration of WSS interface

5 Software interface

The signals between the HC and the WSS module are low voltage +3,3 V logic levels. The definitions of the signals and memory map are described in Table 1 and Table 2. Annex A provides additional information on pin assignment. Annex B provides additional information DPRAM memory map and timing charts.

Table 1 – Software interface

No	Functional block	Name	Input/output	Definitions
1	DPRAM	Address (12-bit wide)	Input	12-bit address bus of DPRAM.
		Data (16-bit wide)	Input/output	16-bit wide data bus of DPRAM.
		START	Input	WSS module start input signal. This strobe is generated by the HC to command the WSS module to perform a specified task defined in command word 2. This signal is an active low input signal.
		DONE	Output	Done output signal. A level high is generated by the WSS module when a specified task is completed.
		ERROR	Output	Error output signal. A level high is generated by the WSS module when it detects an error condition.
		BUSY	Output	Busy output signal. This signal indicates that both the WSS module and HC are trying to access the same dual port RAM address at the same time. This signal is an active low signal.
				Read/write enable (R/W) input signal. This signal is generated by the HC to enable reading of data from dual port RAM, or writing of data to dual port RAM.
				Chip enable (CE) input signal. This signal is generated by the HC to select the dual port RAM devices. This signal is an active low signal.

No	Functional block	Name	Input/output	Definitions
				Chip output enable (OE) input signal. This signal is generated by the HC to enable the dual port RAM to send out data on the data bus. This signal is an active low signal.
2	RS232C	TxD	Output	Transmitted data (TxD): This signal is active when data is transmitted from the WSS module to the HC. When no data is transmitted, the signal is held in the mark condition.
		RxD	Input	Received data (RxD): This signal is active when the WSS module receives data from the HC. When no data is transmitted, the signal is held in the mark condition.
3	Module control	MASTER RESET	Input	Input signal. This strobe is generated by the HC to command the WSS module to perform Master reset which affects optical configurations of the module. This signal is an active low input signal.
		SOFT RESET	Input	Input signal. This resets the WSS module DSP without affecting optical state of the WSS module. This signal is an active low input signal.
		READY	Output	This signal is asserted (logic '0') by the WSS module to inform the HC that transmission may begin.
		ALARM	Output	This signal is generated by the WSS module when a hardware alarm or a software alarm is generated.

Table 2 – DPRAM memory map

No.	Address	Content	R/W	Notes
1	0x0001	Hardware and software version	RO	The hardware and software versions are embedded.
2	0x0020	Command register	RW	
3	0x0021	Command code register	RW	
4	0x0022	Command data 1 register	RW	
5	0x0023	Status register	RW	
6	0x0025	Error code register	RW	
7	0x0028	WSS case temperature	RO	
8	0x0029	Hardware error register	RO	
9	0x0034	Command data 2 register	RW	
10	0x0035	Command data 3 register	RW	

6 Hardware interface – Electrical connector

The electrical connector on the WSS module is an 80-contact receptacle. Annex A provides additional information on connector form.

Annex A
(informative)

Hardware interface details

Annex A describes two kinds of interfaces. All specifications in Annex A are informative. It is recommended that the user chooses either connector form A or B. Table A.1 gives details on connector form, Table A.2 on pin assignment, Table A.3 on the supply voltages and currents for WSS module, Table A.4 on low voltage TTL thresholds and Table A.5 on power consumption.

Table A.1 – Connector form

No	Parameter	Connector form A	Connector form B
1	Connector form	Samtec CLT-140-02-G-D-BE-A	Samtec CLP-140-02-S-D

Table A.2 – Pin assignment

No	Functional block	Name	Pin assignment A	Pin assignment B
1	Dual port RAM	Address (12-bit wide)	Address bit 0 to 11, pin 51 to 62	DPRA 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 Pin 70, 68, 66, 64, 62, 60, 58, 56, 54, 52, 48
		Data (16-bit wide)	Data bit 0 to 15, pin 1 to 16	DPRD 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15 Pin 44, 42, 40, 38, 36, 34, 32, 30, 28, 26, 24, 22, 20, 18, 16, 14
		START	START, pin 21	nSTART, pin 27
		DONE	DONE, pin 23	DONE, pin 25
		ERROR	ERROR, pin 25	ERROR, pin 23
		BUSY	BUSY, pin 26, low	nBUSY, pin 29
		Read Write from RAM	Read Write from RAM, pin 45	R/nW, pin 15
		RAM Chip Enable	RAM Chip Enable, pin 47	nCE, pin 13
		RAM Chip Output Enable	RAM Chip Output Enable, pin 48	nOE, pin 17
2	RS232C	TxD	TxD, pin 65	TxD, pin 51
		RxD	RxD, pin 66	RxD, pin 53
3	Module control	MASTER RESET	MASTER RESET, pin 19	nRST, pin 74
		SOFT RESET	HARD RESET, pin 46	nSWRST, pin 67
		READY	CTS, pin 20	nREADY, pin 61
		ALARM	WDERR, pin 24	ALARM, pin 31 or nFAULT, pin 33

Table A.3 – Supply voltages and currents

No	Parameter	Supply voltage and current A			Supply voltage and current B			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
1	Supply voltage +3,3 V	+3,14	+3,3	+3,5	NA	NA	NA	V
2	Supply voltage +5,0 V	+4,75	+5,0	+5,25	+4,75	+5,0	+5,6	V
3	Supply voltage +5,0 V-Analog	+4,75	+5,0	+5,25	+4,75	+5,0	+5,6	V
4	Supply voltage +15,0 V-Analog	+14,25	+15,0	+15,75	NA	NA	NA	V
5	Supply voltage -15,0 V-Analog	-15,75	-15,0	-14,25	NA	NA	NA	V
6	Supply current +3,3 V	NA	NA	+3,0	NA	NA	NA	A
7	Supply current +5,0 V	NA	NA	+2,0	NA	NA	+7,0	A
8	Supply current +5,0 V-Analog	NA	NA	+2,0	NA	NA	NA	A
9	Supply current +15,0 V-Analog	NA	NA	+1,0	NA	NA	NA	A
10	Supply current -15,0 V-Analog	NA	NA	1,0	NA	NA	NA	A

All the WSS control signals are LVTTL CMOS (3,3 V). The voltage level thresholds are as specified in Table A.4 below.

Table A.4 – Low voltage TTL thresholds

No	Parameter	Low voltage TTL thresholds A		Low voltage TTL thresholds B		Unit
		Min.	Max.	Min.	Max.	
1	Logic low input level	NA	+0,8	-0,2	+0,8	V
2	Logic high input level	+2,0	+5,5	+2,0	+3,45	V
3	Logic low output level	NA	+0,4	NA	+0,4	V
4	Logic high output level	+2,4	+3,3	+2,8	NA	V

Table A.5 – Power consumption

No	Parameter	Power consumption A	Power consumption B	Unit
		Max.	Max.	
1	Power consumption	10	33[a]	W

[a] Including warm-up.

Annex B
(informative)

DPRAM memory map details and timing charts

Annex B describes two types of DPRAM interfaces. All specifications in Annex B are informative. It is recommended that the user chooses either specification A or B. Table B.1 provides the DPRAM memory map for specification A. Table B.2 provides the DPRAM memory map for specification B. Table B.3 provides the signal time specification for both the A and B interfaces. Figure B.1 through to Figure B.8 show the timing relationships of the signals.

Table B.1 – DPRAM memory map specification A

Address	Content (16 bits)	Direction	Note
0x0001	Hardware and firmware version	From WSS module	The hardware and firmware versions are embedded.
0x0020	Command register	From host controller	
0x0021	Command code register		
0x0022	Command data 1		
0x0023	Status 1	From WSS module	Indicates command execution status, ready or error
0x0024	Status 2		Status code (contains results of executed command)
0x0025	Error code		
0x0028	WSS module temperature		Temperature of WSS. This address will be updated upon receiving any command.
0x0029	Hardware failure register		
0x0034	Command data 2	From host controller	
0x0035	Command data 3		
Starting at 0x200	Required port and differential attenuation for each channel	From host controller	Attenuation spectrum and port settings required
Starting at 0x400	Port setting and accumulated differential attenuations for each channel	From WSS module	Port settings and running sum of differential attenuation
Starting at 0x600	Stored port and accumulated attenuations for each channel read from non-volatile RAM	From WSS module	Every time "store" command is issued, the stored value is also copied at 0x600
0x0803	Attenuation range (controllable range)		The default stored value is 20 dB.
Starting at 0x900	Wavelength of each channel	From WSS module	Channel wavelength information
0x0F00-0x0FFF	User's reserved	From host controller	Confirmation module access

Table B.2 – DPRAM memory map specification B

Address	Content	R/W	Data type	Initial value	Note
Device identification and version information registers					
0x0000	Supplier identifier	RO	Number	Invariant	Assigned by customer (constant compiled into the code-base)
0x0001	Version number	RO	Number	Invariant	This is a reduced detail version of the version number. It includes both hardware and software versions.
0x0002	Part identifier	RO	Number	Invariant	Assigned by customer (constant compiled into the code-base)
0x0003	Hardware version high	RO	Version (high 16 bits)	Invariant	Stored in NVRAM in the device, non customer configurable
0x0004	Hardware version low	RO	Version (low 16 bits)	Invariant	Stored in NVRAM in the device, non customer configurable
0x0005	FPGA version high	RO	Version (high 16 bits)	Invariant	Constant compiled into boot-loader code base (within FPGA configuration)
0x0006	FPGA version low	RO	Version (low 16 bits)	Invariant	Constant compiled into boot-loader code base (within FPGA configuration)
0x0007	Firmware version high	RO	Version (high 16 bits)	Loaded whenever code is restarted	Constant compiled into the code base and embedded in the file header
0x0008	Firmware version low	RO	Version (low 16 bits)	Loaded whenever code is restarted	Constant compiled into the code base and embedded in the file header
0x0009	Boot-loader version high	RO	Version (high 16 bits)	Invariant	Constant compiled into boot-loader code base (within FPGA configuration)
0x000A	Boot-loader version low	RO	Version (low 16 bits)	Invariant	Constant compiled into boot-loader code base (within FPGA configuration)
0x000B	NVRAM version high	RO	Version (high 16 bits)	Loaded whenever code is restarted	Constant embedded in NVRAM, compiled into the code base and embedded in the file header
0x000C	NVRAM version low	RO	Version (low 16 bits)	Loaded whenever code is restarted	Constant embedded in NVRAM, compiled into the code base and embedded in the file header
0x000D	CAL version high	RO	Version (high 16 bits)	Loaded whenever code is restarted	Constant embedded in NVRAM, compiled into the code base and embedded in the file header
0x000E	CAL version high	RO	Version (low 16 bits)	Loaded whenever code is restarted	Constant embedded in NVRAM, compiled into the code base and embedded in the file header
0x000F	Serial number high	RO	Version (high 16 bits)	Invariant	Integer portion of the serial number (upper 16 bits); stored in NVRAM
0x0010	Serial number low	RO	Version (low 16 bits)	Invariant	Integer portion of the serial number (lower 16 bits); stored in NVRAM
0x0011	Year of manufacture	RO	Number (2003 to 65536)	Invariant	Year of manufacture as an integer; stored within calibration data
0x0012	Month of manufacture	RO	Number (1 to 12)	Invariant	Month of manufacture as an integer; stored within calibration data

Address	Content	R/W	Data type	Initial value	Note
0x0013	Day of manufacture	RO	Number (1 to 31)	Invariant	Day of manufacture as an integer; stored within calibration data
0x0014	Current file location	RO	Number (0 to 2)	First valid code found (3 to 5)	This is the location of the currently executing code within the device. The value location is 3 for the primary code version, 4 for the secondary code version or 5 for the third code version.
0x0015-0x001F	Reserved	NA	NA	NA	Reserved
Command control and status reporting registers					
0x0020	Command register	RW	NA	NA	
0x0021	Command code register	RW	NA	NA	
0x0022	Command data 1 register	RW	NA	NA	
0x0023	Status register	RW	NA	NA	
0x0024	Reserved	RW	NA	NA	
0x0025	Error code register	RW	NA	NA	
0x0026	ALMHI case temperature duplicate	RO	± 0,1 °C: i.e. 10 °C = 100 and -0,4 °C = 0xFFFC	Stored value	
0x0027	ALMLO case temperature duplicate	RO		Stored value	
0x0028	Current case temperature duplicate	RO		0x7FFF (unread)	
0x0029	Hardware error register	RO	Bit field	0x0000	
0x002A	Alarm register high	RO	Bit field	0x0000	
0x002B	Alarm register low	RO	Bit field	NA	
0x002C	Hardware error register latched	RO	Bit field	Stored value	
0x002D	Alarm register latched high	RO	Bit field	Stored value	
0x002E	Alarm register latched low	RO	Bit field	Stored value	
0x002F	Reserved	NA	NA	NA	
0x0030	Download binary file size(upper16)	RW	Number (Upper 16 bits)	0x0000	Size of the file being transferred (upper 16 bits)
0x0031	Download binary file size(lower16)	RW	Number (Lower 16 bits)	0x0000	Size of the file being transferred (lower 16 bits)
0x0032	Download buffer offset	RO	Number	0x0A00	Offset of the download buffer from the start of the DRPAM
0x0033	Download buffer size	RO	Number	0x0400	Size within the DRPAM of the download buffer
0x0034	Command data 2 register	RW	NA	0x0000	
0x0035	Command data 3 register	RW	NA	0x0000	
0x0036	Command data 4 register	RW	NA	0x0000	
Basic configuration registers					

Address	Content	R/W	Data type	Initial value	Note
0x0037	Start-up state	RO	Number	(1 to 3)	The currently stored start-up configuration. This controls the behaviour of the device on a warm start. Possible values are: 1 Start factory default 2 Start all blocked 3 Start last saved
0x0038	Channel spacing	RO	Number	50	The module's channel spacing in GHz (stored status)
0x0039-0x003F	Reserved	NA	NA	NA	Reserved
0x0040-0x0049	Reserved for insertion loss data	NA	NA	0x7FFF	Reserved for insertion loss data
0x004A-0x004F	Reserved	NA	NA	NA	Reserved for port expansion
File download registers					
0x0050	Overall file size high	RO	Number (high 16 bits)	0x0000	
0x0051	Overall file size low	RO	Number (low 16 bits)	0x0000	
0x0052	Current block offset high	RO	Number (high 16 bits)	0x0000	
0x0053	Current block offset low	RO	Number (low 16 bits)	0x0000	
0x0054	Current block length	RO	Number	0x0000	
0x0055	Current block CRC high	RO	Number (high 16 bits)	0x0000	
0x0056	Current block CRC low	RO	Number (low 16 bits)	0x0000	
0x0057	Overall file CRC high	RO	Number (high 16 bits)	0x0000	
0x0058	Overall file CRC low	RO	Number (low 16 bits)	0x0000	
0x0059	File validate status	RO	Bit field	0x0000	
0x005A	File save status	RO	Bit field	0x0000	
0x005B	Hardware version – file high	RO	Number (high 16 bits)	0x0000	
0x005C	Hardware version – file low	RO	Number (low 16 bits)	0x0000	
0x005D	FPGA version – file high	RO	Number (high 16 bits)	0x0000	
0x005E	FPGA version – file low	RO	Number (low 16 bits)	0x0000	
0x005F	Firmware version – file high	RO	Number (high 16 bits)	0x0000	
0x0060	Firmware version – file low	RO	Number (low 16 bits)	0x0000	
0x0061	Boot-loader version – file high	RO	Number (high 16 bits)	0x0000	

Address	Content	R/W	Data type	Initial value	Note
0x0062	Boot-loader version – file low	RO	Number (low 16 bits)	0x0000	
0x0063	NVRAM version – file high	RO	Number (high 16 bits)	0x0000	
0x0064	NVRAM version – file low	RO	Number (low 16 bits)	0x0000	
0x0065	CAL version – file high	RO	Number (high 16 bits)	0x0000	
0x0066	CAL version – file low	RO	Number (low 16 bits)	0x0000	
0x0067-0x01FF	Reserved	NA	NA	NA	Reserved
Port and attenuation configuration registers					
0x0200-0x0263	Required port and attenuation	RW	Array of one hundred 16-bit values	As specified by the "start-up state"	One 16-bit word per channel; upper byte is the port; lower byte is the attenuation. The port is a number from 1 to the number of ports in the device. Attenuation is a number from 0 to 150 and is measured in 0,1 dB increments. If the port or the attenuation is set to 0xFF, the channel will be blocked. The first channel is stored in the first memory location. This array is used to determine which channels are to be updated when a switch command is received.
0x0264-0x02FF	Reserved	NA	NA	NA	Reserved for channel expansion
0x0300-0x0363	Current port and attenuation	RO	NA	As specified by the "start-up state"	One 16-bit word per channel; upper byte is the port; lower byte is the attenuation. The port is a number from 1 to the number of ports in the device. Attenuation is a number from 0 to 150 and is measured in 0,1 dB increments. If the port or the attenuation is set to 0xFF, the channel will be blocked. The first channel is stored in the first memory location. This array represents the current configuration of the switch.
0x0364-0x03FF	Reserved	NA	NA	NA	Reserved for channel expansion
0x0400 0x0463	Stored port and attenuation	RO	NA	As specified by the "start-up state"	One 16-bit word per channel; upper byte is the port; lower byte is the attenuation. The port is a number from 1 to the number of ports in the device. Attenuation is a number from 0 to 150 and is measured in 0,1 dB increments. If the port or the attenuation is set to 0xFF, the channel will be blocked. The first channel is stored in the first memory location. This array represents the current configuration of the switch.
0x0464-0x04FF	Reserved	NA	NA	NA	Reserved for channel expansion
Reserved space					
0x0500-0x09FF	Reserved	NA	NA	NA	Reserved
File transfer buffer					

Address	Content	R/W	Data type	Initial value	Note	
0x0A00-0x0DFF	Download buffer	RW	NA	NA	If the size in bytes of the block in the buffer is odd, the last byte will be in the upper byte of the last used 16-bit word.	
Manufacturer specific diagnostics						
0x0E00-0x0EFF	Manufacturer diagnostics	NA	NA	NA	Reserved for manufacturer diagnostics	
Monitored signal and alarm configuration registers						
0x0F00	Current case temperature	RO	± 0,1 °C: i.e. 10 °C = 100 and -0,4 °C = 0xFFFC	0x7FFF (unread)	This is the current case temperature of the module	It is an instantaneous sample that is updated once every 10 s. It is a signed value measured in steps of 0,1 °C. The accuracy of this value is not guaranteed, and it is not calibrated. The value 0x7FFF or 32768 indicates that the rail has not been sampled yet or is not being sampled.
0x0F01	Current device temperature	RO		0x7FFF (unread)	This is the current temperature of the optical package	
0x0F02	TEC current	RO	± mA	0x7FFF (unread)	The number of mA being used by the temperature controller	This is an instantaneous sample that is updated once every 10 s. The value 0x7FFF or 32768 indicates that the rail has not been sampled yet or is not being sampled.
0x0F03	Supply voltage (5V)	RO	± mV	0x7FFF (unread)	This is the current (5 V) supply voltage of the DWP device measured in mV	
0x0F04	Internal power rail 13v4	RO	± mV	0x7FFF (unread)	These are internally generated power rails on the DWP device. They are instantaneous samples that are updated once every 10 s. They are signed values measured in mV. The value 0x7FFF or 32768 indicates that the rail has not been sampled yet or is not being sampled.	
0x0F05	Internal power rail 12v4	RO	± mV	0x7FFF (unread)		
0x0F06	Internal power rail 3v3	RO	± mV	0x7FFF (unread)		
0x0F07	Internal power rail 2v5	RO	± mV	0x7FFF (unread)		
0x0F08	Internal power rail 1v8	RO	± mV	0x7FFF (unread)		
0x0F09	Internal power rail 1v5	RO	± mV	0x7FFF (unread)		
0x0F0A	Internal power rail N2V	RO	± mV	0x7FFF (unread)		
0x0F0B	Internal power rail N5V	RO	± mV	0x7FFF (unread)		
0x0F0C-0x0F1F	Reserved	NA	NA	NA	Reserved for expansion of monitoring options	
0x0F20	ALMHI case temperature	RO	± 0,1 °C	Stored value	This is the level at which an alarm will be reported. It is directly compared against the corresponding monitored signal. A value of 0x7FFF indicates to the device that the alarm will be ignored.	
0x0F21	ALMHI device temperature	RO	± 0,1 °C	Stored value		
0x0F22	ALMHI TEC current	RO	± mA	Stored value		
0x0F23	ALMHI supply voltage	RO	± mV	Stored value		

Address	Content	R/W	Data type	Initial value	Note
0x0F24	ALMHI internal rail 13v4	RO	± mV	Stored value	
0x0F25	ALMHI internal power 12v4	RO	± mV	Stored value	
0x0F26	ALMHI internal power 3v3	RO	± mV	Stored value	
0x0F27	ALMHI internal power 2v5	RO	± mV	Stored value	
0x0F28	ALMHI internal power 1v8	RO	± mV	Stored value	
0x0F29	ALMHI internal power 1v5	RO	± mV	Stored value	
0x0F2A	ALMHI internal power N2V	RO	± mV	Stored value	
0x0F2B	ALMHI internal power N5V	RO	± mV	Stored value	
0x0F2C	ALMHI VCOM	RO	± mV	Stored value	
0x0F2D	ALMHI temperature shutdown	RO	± 0,1 °C	Stored value	This is the upper limit of the temperature range of the device. At or above this limit the device will shut down the optional components. A value of 0x7FFF indicates to the device that the alarm will be ignored.
0x0F2E	ALMHI TEC current OOR	RO	± mA	Stored value	These are secondary alarms; if triggered the alarm events are recorded and it is not possible to clear them. A value of 0x7FFF indicates to the device that the alarm will be ignored.
0x0F2F	ALMHI supply voltage OOR	RO	± mV	Stored value	
0x0F30	ALMHI VCOM OOR	RO	± mV	Stored value	
0x0F31-0x0F3F	Reserved	NA	NA	NA	Reserved for expansion of monitoring options
0x0F40	ALMHI hysteresis case temperature	RO	± 0,1 °C	Stored value	After the alarm has triggered because it is above the high threshold, it will remain active until it drops back below this threshold. A value of 0x7FFF indicates to the device that the hysteresis level is ignored and that the alarm will be cleared as soon as the signal drops below the high threshold. ("Temperature Shutdown", "TEC Current OOR", "Supply OOR" and "VCOM OOR" are special cases as they are duplicates and compare against other values.)
0x0F41	ALMHI hysteresis device temperature	RO	± 0,1 °C	Stored value	
0x0F42	ALMHI hysteresis TEC current	RO	± mA	Stored value	
0x0F43	ALMHI hysteresis supply voltage (5V)	RO	± mV	Stored value	
0x0F44	ALMHI hysteresis internal rail 13v4	RO	± mV	Stored value	
0x0F45	ALMHI hysteresis internal power 12v4	RO	± mV	Stored value	
0x0F46	ALMHI hysteresis internal power 3v3	RO	± mV	Stored value	
0x0F47	ALMHI hysteresis internal power 2v5	RO	± mV	Stored value	
0x0F48	ALMHI hysteresis internal power 1v8	RO	± mV	Stored value	
0x0F49	ALMHI hysteresis internal power 1v5	RO	± mV	Stored value	

Address	Content	R/W	Data type	Initial value	Note
0x0F4A	ALMHI hysteresis internal power N2V	RO	± mV	Stored value	
0x0F4B	ALMHI hysteresis internal power N5V	RO	± mV	Stored value	
0x0F4C	ALMHI hysteresis VCOM	RO	± mV	Stored value	
0x0F4D	ALMHI hysteresis temperature shutdown	RO	± 0,1 °C	Stored value	
0x0F4E	ALMHI hysteresis TEC current OOR	RO	± mA	Stored value	
0x0F4F	ALMHI hysteresis supply OOR	RO	± mV	Stored value	
0x0F50	ALMHI VCOM OOR	RO	± mV	Stored value	
0x0F51-0x0F5F	Reserved	NA	NA	NA	Reserved for expansion of monitoring options
0x0F60	ALMLO case temperature	RO	± 0,1 °C	Stored value	This is the level at or below which an alarm will be reported. It is directly compared against the corresponding monitored signal. A value of 0x7FFF indicates to the device that the alarm will be ignored.
0x0F61	ALMLO device temperature	RO	± 0,1 °C	Stored value	
0x0F62	ALMLO TEC temperature	RO	± mA	Stored value	
0x0F63	ALMLO supply voltage (5V)	RO	± mV	Stored value	
0x0F64	ALMLO internal rail 13v4	RO	± mV	Stored value	
0x0F65	ALMLO internal power 12v4	RO	± mV	Stored value	
0x0F66	ALMLO internal power 3v3	RO	± mV	Stored value	
0x0F67	ALMLO internal power 2v5	RO	± mV	Stored value	
0x0F68	ALMLO internal power 1v8	RO	± mV	Stored value	
0x0F69	ALMLO internal power 1v5	RO	± mV	Stored value	
0x0F6A	ALMLO internal power N2V	RO	± mV	Stored value	
0x0F6B	ALMLO internal power N5V	RO	± mV	Stored value	
0x0F6C	ALMLO VCOM	RO	± mV	Stored value	
0x0F6D	ALMLO temperature shutdown	RO	± 0,1 °C	Stored value	This is the lower limit of the temperature range of the device. At or below this limit the device will shut down the optical components. A value of 0x7FFF indicates to the device that the alarm will be ignored.
0x0F6E	ALMLO TEC current OOR	RO	± mA	Stored value	These are secondary alarms; if triggered the alarm events are recorded, and it is not possible to clear them. A value of 0x7FFF indicates to the device that the alarm will be ignored.

Address	Content	R/W	Data type	Initial value	Note
0x0F6F	ALMLO supply OOR	RO	± mV	Stored value	
0x0F70	ALMLO VCOM OOR	RO	± mV	Stored value	
0x0F71-0x0F7F	Reserved	NA	NA	NA	Reserved for expansion of monitoring options
0x0F80	ALMLO Hysteresis Case Temp.	RO	± 0,1 ºC	Stored value	After the alarm has triggered because it is at or below the low threshold, it will remain active until it rises above this threshold. It is directly compared against the corresponding monitored signal. A value of 0x7FFF indicates to the device that the hysteresis level is ignored and that the alarm will be cleared as soon as the signal rises above the low threshold.
0x0F81	ALMLO hysteresis device temperature	RO	± 0,1 ºC	Stored value	
0x0F82	ALMLO hysteresis TEC current	RO	± mA	Stored value	
0x0F83	ALMLO hysteresis supply voltage (5V)	RO	±mV	Stored value	
0x0F84	ALMLO hysteresis internal rail 13v4	RO	± mV	Stored value	
0x0F85	ALMLO hysteresis internal power 12v4	RO	± mV	Stored value	
0x0F86	ALMLO hysteresis internal power 3v3	RO	± mV	Stored value	
0x0F87	ALMLO hysteresis internal power 2v5	RO	± mV	Stored value	
0x0F88	ALMLO hysteresis internal power 1v8	RO	± mV	Stored value	
0x0F89	ALMLO hysteresis internal power 1v5	RO	± mV	Stored value	
0x0F8A	ALMLO hysteresis internal power N2V	RO	± mV	Stored value	
0x0F8B	ALMLO hysteresis internal power N5V	RO	± mV	Stored value	
0x0F8C	ALMLO hysteresis VCOM	RO	± mV	Stored value	
0x0F8D	ALMLO hysteresis temperature shutdown	RO	± 0,1 ºC	Stored value	
0x0F8E	ALMLO hysteresis TEC current OOR	RO	± mA	Stored value	
0x0F8F	ALMLO hysteresis supply OOR	RO	± mV	Stored value	
0x0F90	ALMLO hysteresis VCOM OOR	RO	± mV	Stored value	
0x0F91-0x0F9F	Reserved	NA	NA	NA	Reserved for expansion of monitoring options.
0x0FA0	ALM STATE case temperature	RO	Number (0 to 5)	0 (Un-initialized)	These registers represent the alarm conditions or state. The valid values are: 0 Un-initialized or disabled 1 Below lower threshold 2 Within low hysteresis (it only transitions through this state if it has been below the lower threshold) 3 Within specification 4 Within high hysteresis (it only transitions through this state if it has been above the upper threshold) 5 Above the upper threshold
0x0FA1	ALM STATE device temperature	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FA2	ALM STATE TEC current	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FA3	ALM STATE supply voltage (5v)	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FA4	ALM STATE internal rail 13v4	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FA5	ALM STATE internal power 12v4	RO	Number (0 to 5)	0 (Un-initialized)	

Address	Content	R/W	Data type	Initial value	Note
0x0FA6	ALM STATE internal power3v3	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FA7	ALM STATE internal power2v5	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FA8	ALM STATE internal power1v8	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FA9	ALM STATE internal power1v5	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FAA	ALM STATE internal power N2V	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FAB	ALM STATE internal power N5V	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FAC	ALM STATE VCOM	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FAD	ALM STATE temperature shutdown	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FAE	ALM STATE TEC current OOR	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FAF	ALM STATE supply OOR	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FB0	ALM STATE VCOM OOR	RO	Number (0 to 5)	0 (Un-initialized)	
0x0FB1-0x0FBF	Reserved	NA	NA	NA	Reserved for expansion of monitoring options
0x0FC0-0x0FFF	Reserved	NA	NA	NA	Reserved

Table B.3 – Signal time specification

No.	Parameter	Description	Specification A			Specification B			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
DPRAM read cycle timing									
1	t_{RC}	Read cycle time	150	NA	NA	55	248	NA	ns
2	t_{AA}	Address to data valid	NA	NA	40	NA	NA	55	ns
3	t_{ACE}	CE low to data valid	NA	NA	40	NA	NA	55	ns
4	t_{DOE}	OE low to data valid	NA	NA	20	NA	NA	25	ns
5	t_{DH}	Output hold from CE or OE change to high, depending upon which occurs first.	5	NA	NA	NA	NA	NA	ns
6	t_{OHA}	Output hold from address change	5	NA	40	3	NA	NA	ns
7	t_{AH}	Address hold from CE or OE change to high depending upon which occurs first.	20	NA	NA	NA	NA	NA	ns
8	t_{CERH}	CE high before next read cycle	0	NA	NA	NA	NA	NA	ns
9	t_{OEH}	OE high before next read cycle	0	NA	NA	NA	NA	NA	ns
10	t_{LZOE}	OE low to previous data become invalid	NA	NA	NA	3	NA	NA	ns
11	t_{HZOE}	OE high to new data become invalid	NA	NA	NA	NA	NA	25	ns
12	t_{LZCE}	CE low to previous data become invalid	NA	NA	NA	3	NA	NA	ns
13	t_{HZCE}	CE high to new data become invalid	NA	NA	NA	NA	NA	25	ns
DPRAM write cycle timing									
14	t_{WC}	Write cycle time	150	NA	NA	55	NA	NA	ns
15	t_{AW}	Address valid to write end	40	NA	NA	35	NA	NA	ns
16	t_{SCE}	CE low to write end	40	NA	NA	35	NA	NA	ns
17	t_{PWE}	Write pulse width	40	NA	NA	35	NA	NA	ns
18	t_{AHW}	Address hold after write	20	NA	NA	0	NA	NA	ns
19	t_{CEWH}	CE high before next write cycle	20	NA	NA	NA	NA	NA	ns
20	t_{RWH}	R/W high before next write cycle	0	NA	NA	NA	NA	NA	ns
21	t_{SD}	Data set-up to write end	40	NA	NA	20	NA	NA	ns
22	t_{HD}	Data hold from CE or R/W changing to high, depending upon which occurs first	20	NA	NA	0	NA	NA	ns
23	t_{AC}	Address to CE	NA	NA	NA	0	NA	NA	ns
24	t_{CA}	CE to address	NA	NA	NA	0	NA	NA	ns
25	t_{SA}	Address setup write start	NA	NA	NA	0	NA	NA	ns
26	t_{HZWE}	R/W low to data writable	NA -	NA	NA	NA	NA	25	ns
27	t_{LZWE}	R/W high to data write inhibit	NA	NA	NA	0	NA	NA	ns
Power on timing									
28	t_{CPS}	Command lines power on set-up time	NA	NA	5	NA	NA	NA	ms
29	t_{RPS}	Response from module at power on set-up time	NA	NA	100	NA	NA	NA	µs
30	$t_{Initial}$	Initialization time	NA	NA	5	NA	NA	NA	s
Start timing									
31	t_{SPW}	Start pulse width	220	NA	NA	NA	NA	NA	ns

No.	Parameter	Description	Specification A			Specification B			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
32	$t_{SPdelay}$	Response from module after start	NA	NA	10	NA	NA	NA	us
33	t_{SP}	Start command process time	150	NA	NA	NA	NA	NA	ms
34	t_{SS}	Address to start	NA	NA	NA	90	94	110	ns
35	t_{DC}	Done cycle	NA	NA	NA	NA	NA	4,5	s
36	t_{SR}	Address to ready	NA	NA	NA	90	94	110	ns
37	t_{SC}	Ready cycle	NA	NA	NA	NA	NA	4,5	s
38	t_{SE}	Address to error	NA	NA	NA	90	94	110	ns
39	t_{EC}	Error cycle	NA	NA	NA	NA	NA	4,5	s
Master reset timing									
40	t_{MRPW}	Master reset pulse width	220	NA	NA	NA	NA	NA	ns
41	$t_{MRdelay}$	Response from module after reset pulse	NA	NA	10	NA	NA	NA	us
42	t_{MRP}	Master reset process time	NA	NA	5	NA	NA	NA	s
Soft reset timing									
43	t_{SRPW}	Soft reset pulse width	220	NA	NA	NA	NA	NA	ns
44	$t_{SRdelay}$	Response from module after reset pulse	NA	NA	10	NA	NA	NA	us
45	t_{SRP}	Soft reset process time	NA	NA	200	NA	NA	NA	ms
DPRAM busy timing									
46	t_{BPW}	Busy signal pulse Width	20	NA	NA	NA	NA	NA	ns
The DPRAM busy signal will be set to low when either both sides write the same location or any one side writes and the other side reads the same location at the same time. The signal will not be low if both sides read the same location at the same time. The BUSY signal will stay low until the scenario disappears. Due to the discrete signal handshaking arrangement, use of this signal should not be required.									
Alarm timing									
47	t_{AR}	Alarm reset process	NA	NA	500	NA	NA	NA	ms

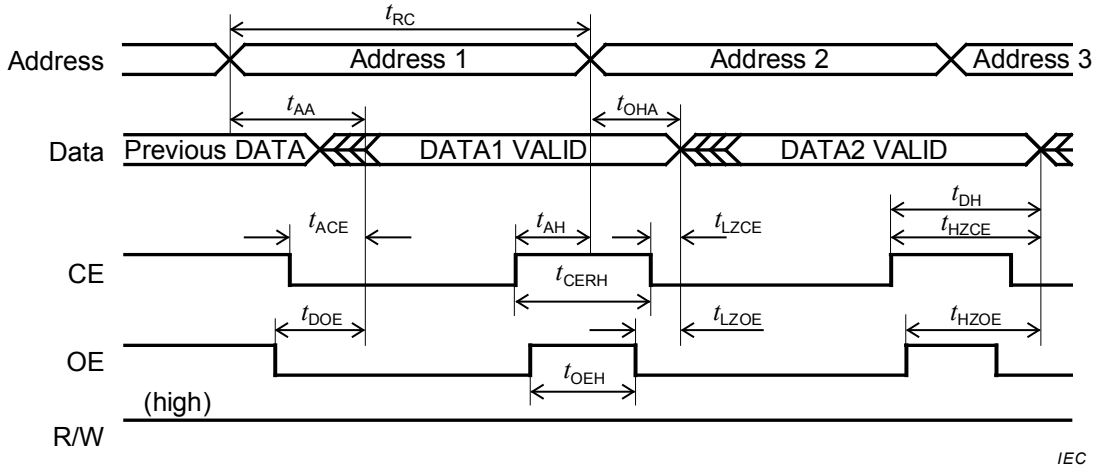

Figure B.1 – DPRAM READ CYCLE timing

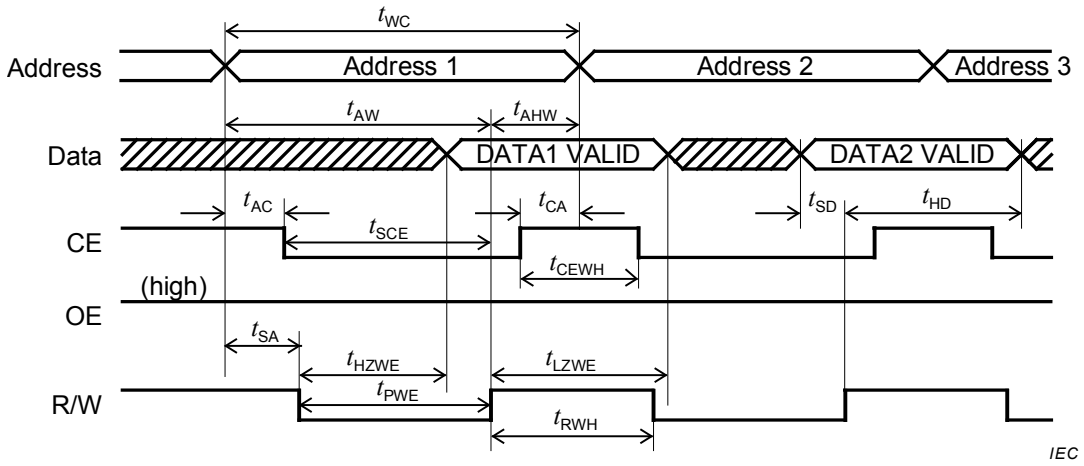

Figure B.2 – DPRAM WRITE CYCLE timing

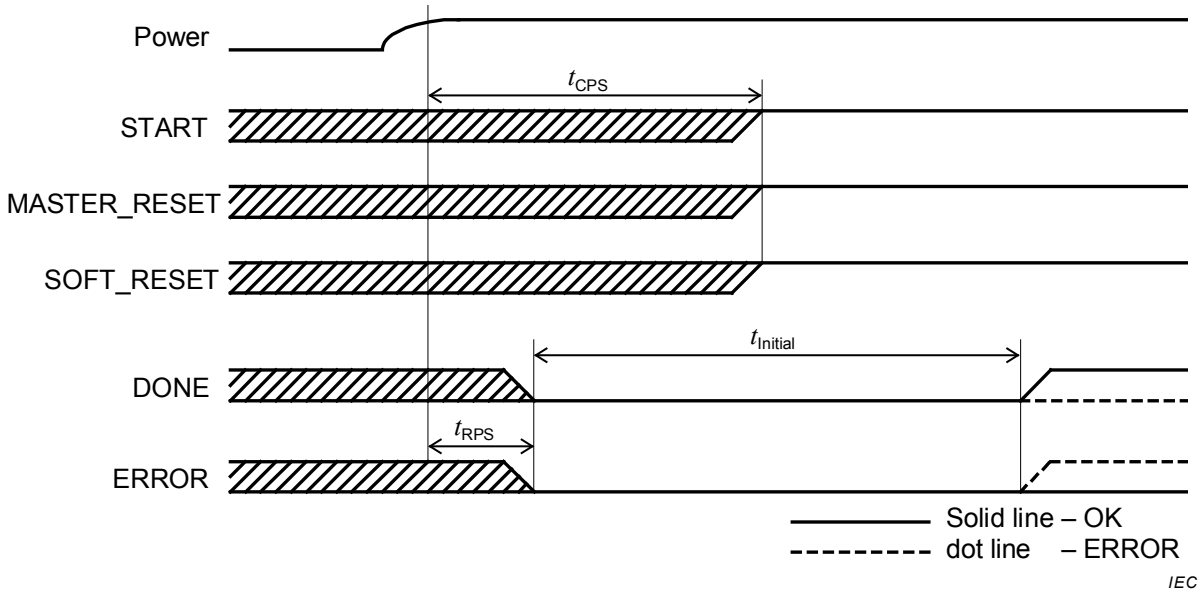

Figure B.3 – POWER ON timing

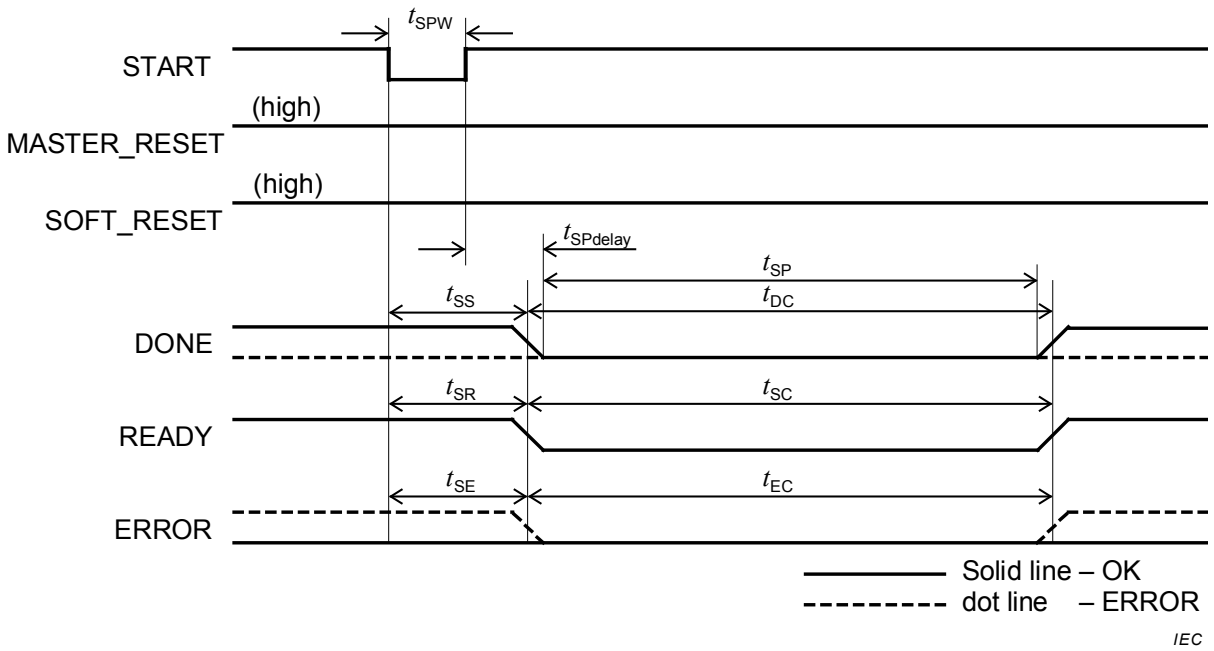

Figure B.4 – START timing

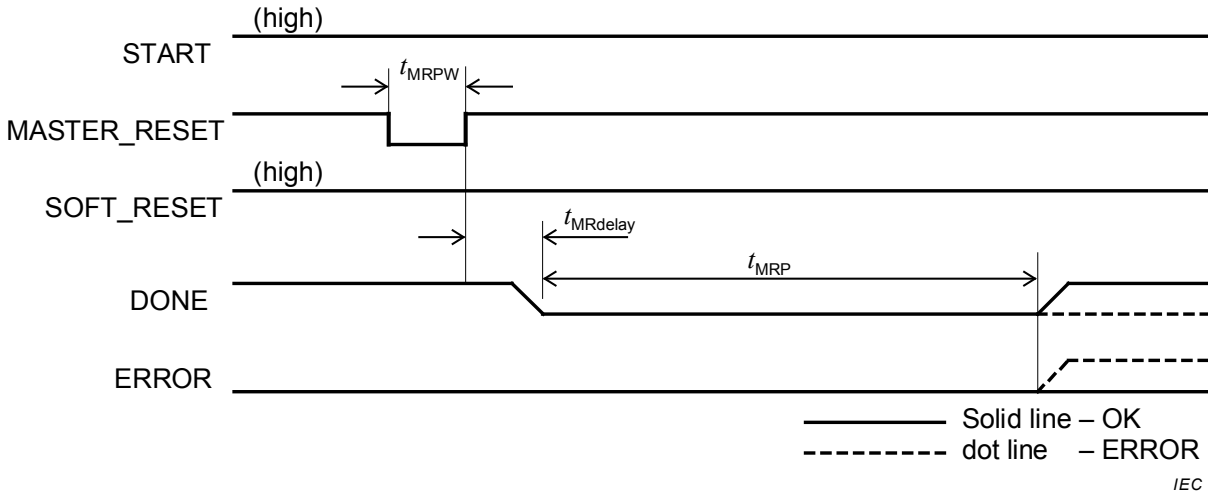

Figure B.5 – MASTER RESET timing

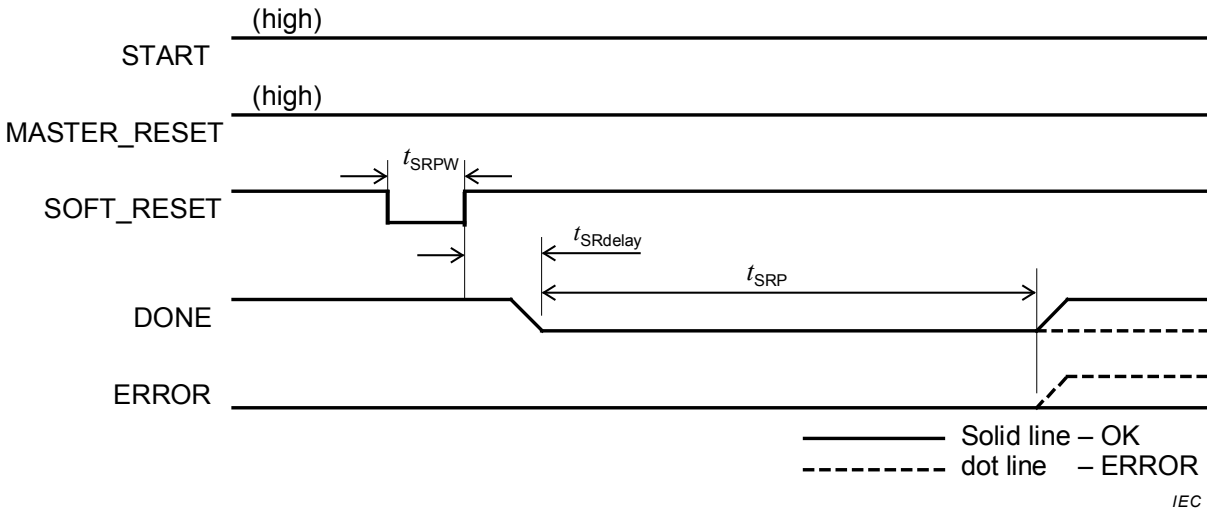

Figure B.6 – SOFT RESET timing

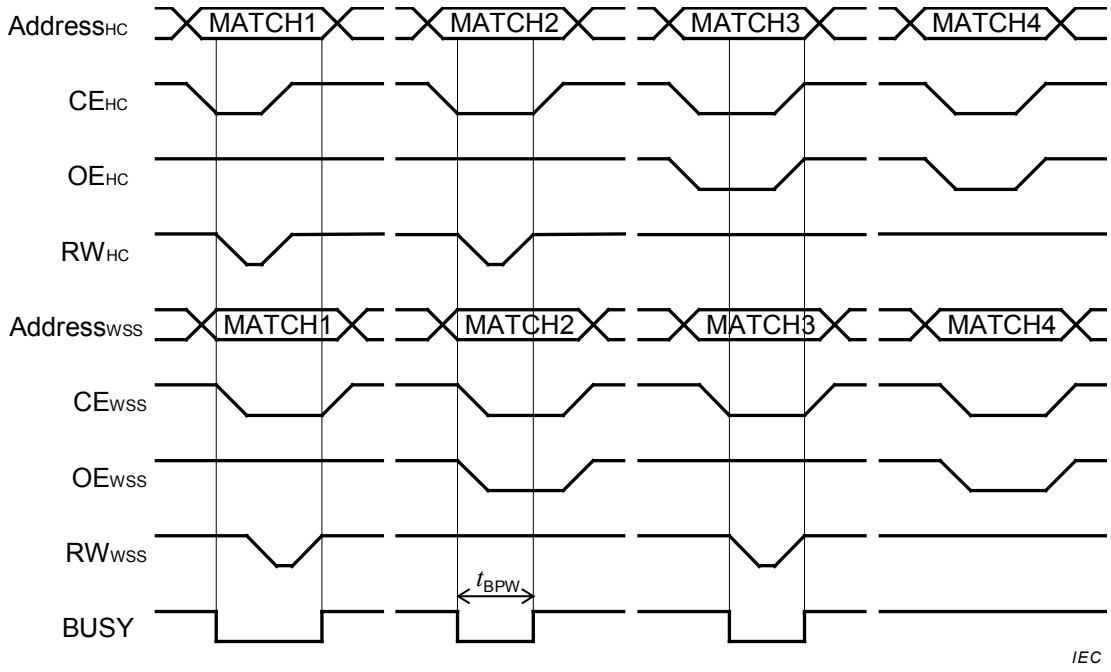

Figure B.7 – DPRAM BUSY timing

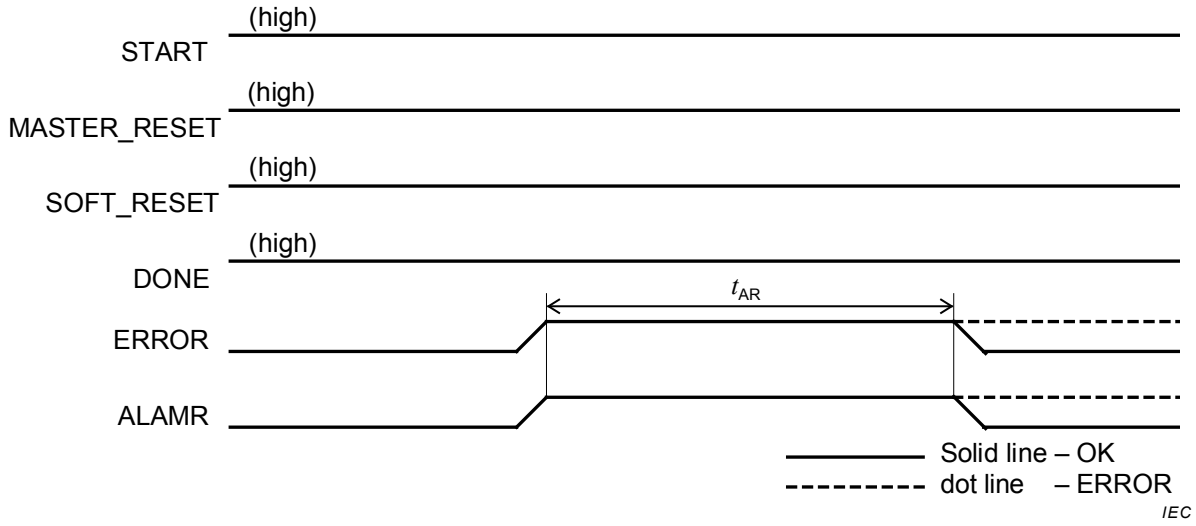

Figure B.8 – ALARM timing

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1 Under consideration

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