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BSI Standards Publication

Integrated circuits — Measurement of impulse immunity

Part 3: Non-synchronous transient injection method

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National foreword

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The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

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Integrated circuits - Measurement of impulse immunity - Part 3: Non-synchronous transient injection method

(IEC 62215-3:2013)

Circuits intégrés -
Mesure de l'immunité aux impulsions -
Partie 3: Méthode d'injection de transitoires non synchrones
(CEI 62215-3:2013)

Integrierte Schaltungen -
Messung der Störfestigkeit gegen Impulse -
Teil 3: Asynchrones Transienteneinspeisungs-Verfahren
(IEC 62215-3:2013)

CENELEC

European Committee for Electrotechnical Standardization
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Foreword

The text of document 47A/881/CDV, future edition 1 of IEC 62215-3, prepared by SC 47A “Integrated circuits” of IEC/TC 47 “Semiconductor devices” was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62215-3:2013.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2014-05-21
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2016-08-21

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 62215-3:2013 was approved by CENELEC as a European Standard without any modification.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 60050	Series	International Electrotechnical Vocabulary (IEV)	-	-
IEC 61000-4-4	2012	Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test	EN 61000-4-4	2012
IEC 61000-4-5 + corr. October	2005 2009	Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test	EN 61000-4-5	2006
IEC 62132-4	2006	Integrated circuits - Measurement of electromagnetic immunity, 150 kHz to 1 GHz - Part 4: Direct RF power injection method	EN 62132-4	2006
ISO 7637-2	2011	Road vehicles - Electrical disturbances from conduction and coupling - Part 2: Electrical transient conduction along supply lines only	-	-

CONTENTS

INTEGRATED CIRCUITS – MEASUREMENT OF IMPULSE IMMUNITY –

Part 3: Non-synchronous transient injection method

1 Scope

This part of IEC 62215 specifies a method for measuring the immunity of an integrated circuit (IC) to standardized conducted electrical transient disturbances. The disturbances, not necessarily synchronized to the operation of the device under test (DUT), are applied to the IC pins via coupling networks. This method enables understanding and classification of interaction between conducted transient disturbances and performance degradation induced in ICs regardless of transients within or beyond the specified operating voltage range.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050 (all parts), *International Electrotechnical Vocabulary (IEV)* (available at <http://www.electropedia.org>)

IEC 61000-4-4:2012, *Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test*

IEC 61000-4-5:2005, *Electromagnetic compatibility (EMC) – Part 4-5: Testing and measurement techniques – Surge immunity test*

IEC 62132-4:2006, *Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 4: Direct RF power injection method*

ISO 7637-2:2011, *Road vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-131 and IEC 60050-161, some of which have been added for convenience, as well as the following apply.

3.1
auxiliary equipment
equipment not under test but is indispensable for setting up all the functions and assessing the correct performance (operation) of the equipment under test (EUT) during its exposure to the disturbance

3.2
burst
sequence of a limited number of distinct impulses or an oscillation of limited duration

3.3
coupling network
electrical circuit for transferring energy from one circuit to another with well-defined impedance and known transfer characteristics

3.4
performance degradation
undesired departure in the operational performance of any device, equipment or system from its intended performance

Note 1 to entry: The term “degradation” can apply to temporary or permanent failure.

3.5
DUT
device under test
device, equipment or system being evaluated

Note 1 to entry: In this part of IEC 62215, it refers to a semiconductor device being tested.

Note 2 to entry: This note applies to the French language only.

3.6
EMC
electromagnetic compatibility
ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment

3.7
global pin
pin that carries a signal or power which enters or leaves the application board without any active device in between

3.8
immunity
ability of a device, equipment or system to perform without degradation in the presence of an electromagnetic disturbance

3.9
jitter
short-term variations of the significant instants of a digital signal from their ideal positions in time

3.10
local pin
pin that carries a signal or power which does not leave the application board

Note 1 to entry: The signal or power remains on the application board as a signal between two components with or without additional EMC circuitry.

3.11
response signal
signal generated by the DUT for the purpose of monitoring for detecting performance degradation

3.12
electromagnetic ambient
totality of electromagnetic phenomena existing at a given location

3.13
transient
pertaining to or designating a phenomenon or a quantity which varies between two consecutive steady states during a time interval which is short compared with the time-scale of interest

3.14
surge voltage
transient voltage wave propagating along a line or a circuit and characterized by rapid increase followed by a slower decrease of the voltage

3.15
VS
power supply input

3.16
Z_L
line impedance of a trace on the test board

4 General

Electrical transients are a common part of the EMC environment of electrical and electronic devices. These transients are generated often on power nets and are directly applied or coupled to the terminals of integrated circuits which may affect the functionality of the device. The knowledge about the impulse immunity level enables the optimization of the IC as well as the definition of application requirements.

The transient waveforms are dependent on the application area of the DUT. Typical transient waveforms are burst and surge voltages as specified in IEC 61000-4-4 and IEC 61000-4-5 for industrial and consumer applications and in ISO 7637-2 for automotive application to get reproducible and comparable results for different DUTs.

The impulse immunity measurement method as described in this standard uses impulses with different amplitude and rise times, duration, energy and polarity in a conductive mode to the IC. In this test method the test time or the number of the applied impulses has to be chosen in a way that statistical effects are covered.

This method is similar to immunity test method of integrated circuits in the presence of conducted RF disturbances defined in IEC 62132-4. As in IEC 62132-4, the disturbance signal can be injected into I/O pins, supply pins and into the PCB reference via defined coupling networks. The EMC test board for this method can be the same as the one specified in IEC 62132-4.

The pin injection test method evaluates the performance of individual IC pins or groups of them when subjected to a transient waveform. Both positive and negative polarity transients, referenced to ground are applied. The basic test implementation is shown in Figure 1 .

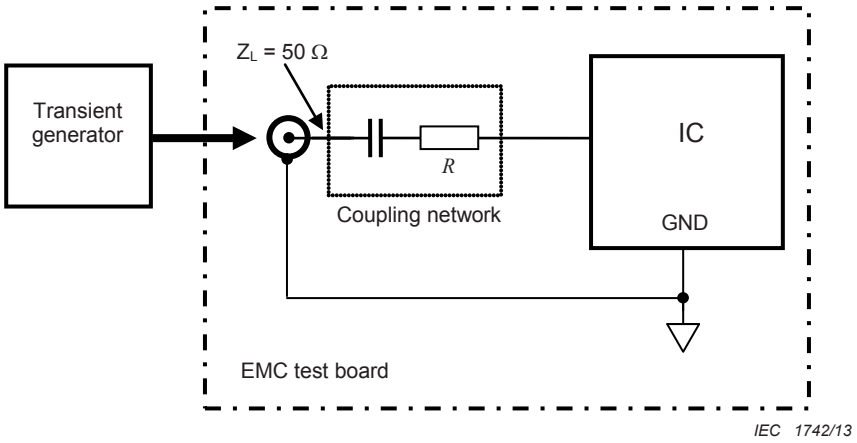

Figure 1 – Typical pin injection test implementation

5 Coupling networks

5.1 General on coupling networks

The transient disturbances are applied to the IC pin under test via defined coupling networks implemented on the PCB and connected to a device pin with respect to the pin functionality and the disturbance signal. Coupling networks are defined for:

- supply injection;
- input injection;
- output injection;
- multiple pin injection.

The coupling network shown in Figure 1 is identical to that used for RF immunity testing in IEC 62132-4. The series resistance (R) can be used to control the injected current, if required. The capacitance (C) is a DC block with a value selected to represent coupling effects in practice and to provide sufficient signal bandwidth while not excessively loading the connected pin (see Annex B). Default values of the series resistor and DC block capacitor are 0 Ω and 1 nF (representing capacity of 10 m parallel lines), respectively. A different capacity value may be used if required for correct functionality. The actual value of resistor and capacitor, including the rationale for their selection, shall be documented in the test report.

5.2 Supply injection network

5.2.1 Direct injection

For supply pins directly connected to the power net a direct injection as shown in Figure 2 shall be used. For these tests the coupling and decoupling networks of the transient generators standardized in IEC 61000-4-4 and IEC 61000-4-5 for industrial or ISO 7637-2 for automotive applications are used.

Mandatory blocking capacitors (C_{BL}), filter or protection components at the supply pin have to be used as recommended by the manufacturer.

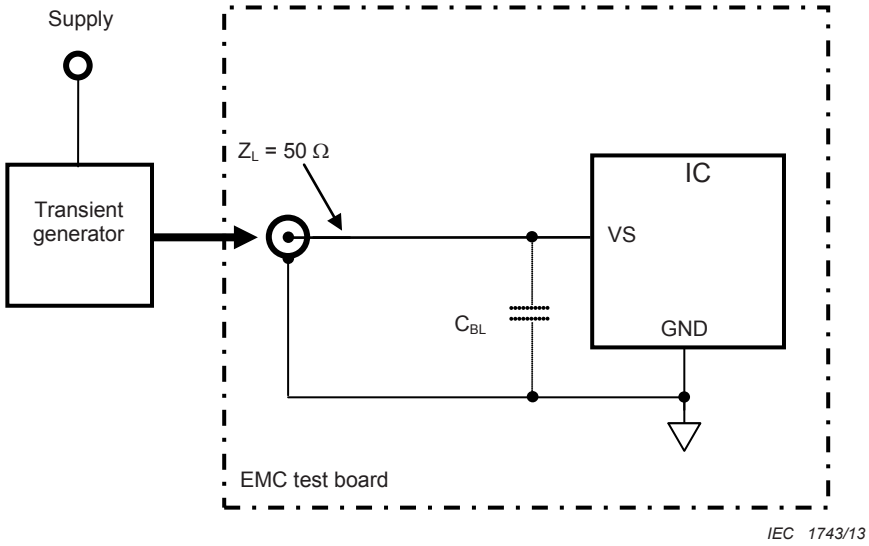

Figure 2 – Supply pin direct injection test implementation

5.2.2 Capacitive coupling

For supply pins which are not directly connected to the power net, such as global distributed sub-supply nets isolated by power converters, the test circuitry shall be implemented as shown in Figure 3. The default values of the coupling network are 0 Ω for the resistor and 1 nF for the coupling capacitor. The external DC power supply should be decoupled from the supply pin(s) of the DUT with impedance (Z) greater than 400 Ω (default) over the frequency range of the test impulse spectrum. Other values for coupling and decoupling networks are possible but must be stated in the test report (see also Clause 11).

Mandatory blocking capacitors, filter- or protection components at the supply pin have to be used as recommended by the manufacturer.

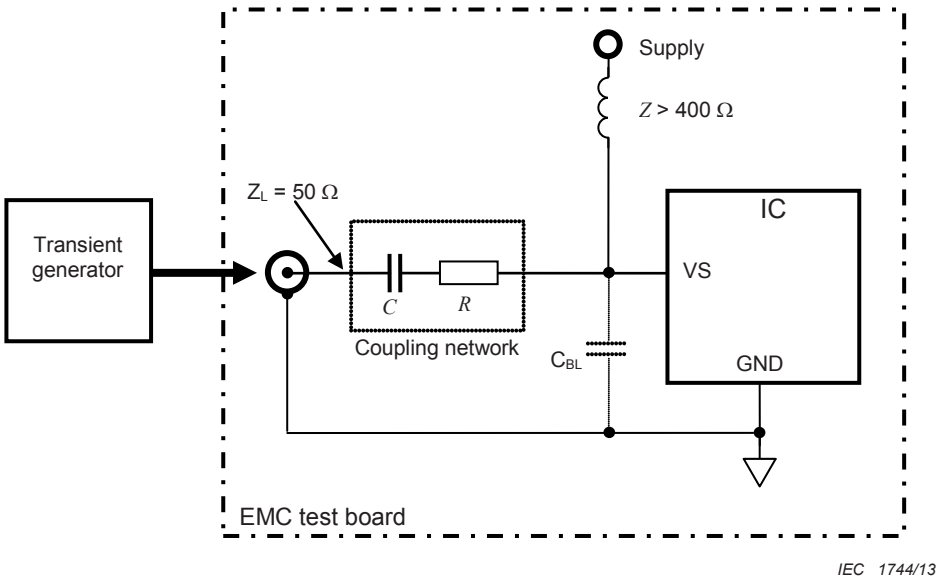

Figure 3 – Supply pin capacitive injection test implementation

5.3 Input injection

For general purpose I/O pins configured as inputs or input-only pins and globally connected, the test circuitry shall be implemented as shown in Figure 4. The default values of the

coupling network are 0 Ω for the resistor and 1 nF for the coupling capacitor. External signal sources (e.g. signal generator) which are connected to the input signal connector should be decoupled from the input pin(s) of the DUT with impedance (Z) greater than 400 Ω (default) over the frequency range of the test impulse spectrum. Other values for coupling and decoupling networks are possible but shall be stated in the test report. The input shall be configured as recommended by the manufacturer, only mandatory components have to be applied (e.g. with an appropriate external pull up resistor (R_U), a pull down resistor (R_D) or a series resistor (R_S)). The DUT function shall not be affected by the coupling network.

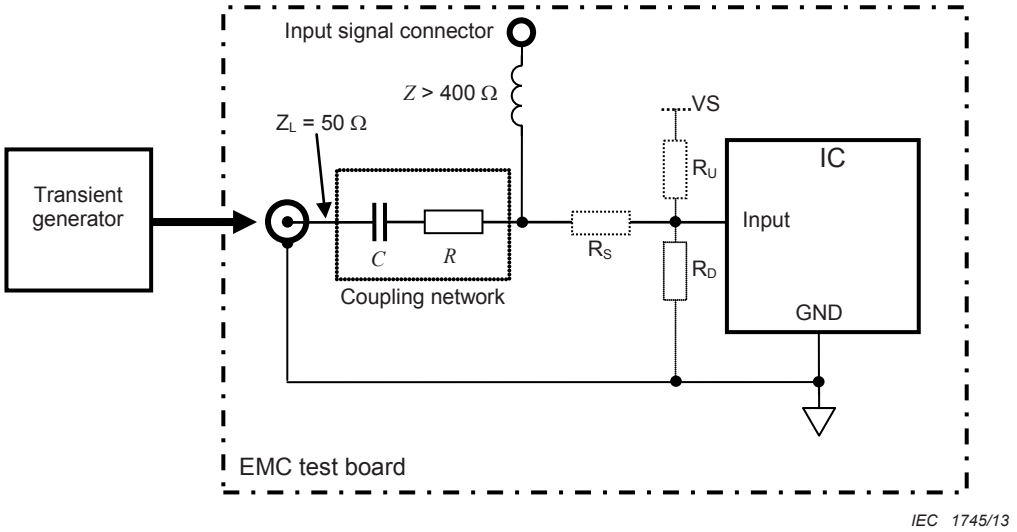

Figure 4 – Input pin injection test implementation

5.4 Output injection

For general purpose I/O pins configured as outputs or output-only pins and globally connected, the test circuitry shall be implemented as shown in Figure 5. The default values of the coupling network are 0 Ω for the resistor and 1 nF for the coupling capacitor. External signal processing units or loads which are connected to the output signal connector should be decoupled from the output pin(s) of the DUT with impedance (Z) greater than 400 Ω (default) over the frequency range of the test impulse spectrum. Other values can be assigned to the coupling and decoupling networks but they shall be stated in the test report. The output shall be configured and loaded (e.g. with an appropriate external capacitive load (C_L)) as specified by the manufacturer. Only mandatory external components according to the specification should be connected during test.

For output pins, the DC block capacitance shall not exceed the rated capacitive load of this output to prevent an unacceptable deviation of the output signal.

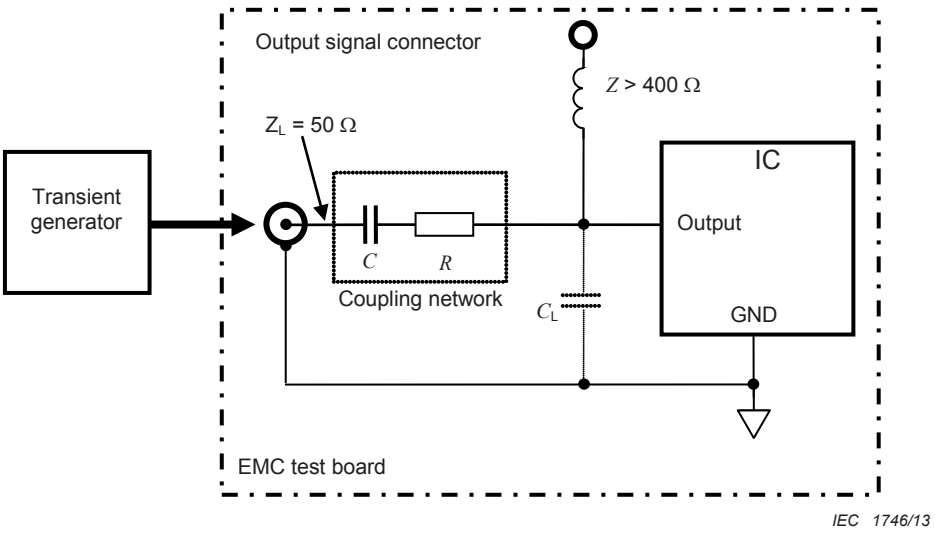

Figure 5 – Output pin injection test implementation

5.5 Simultaneous multiple pin injection

For parallel coupling to multiple pins or pin groups a coupling network consisting of one injection point and a capacitive impulse signal splitter can be used as shown in Figure 6. The default values of those coupling networks are the same as for respective single pins.

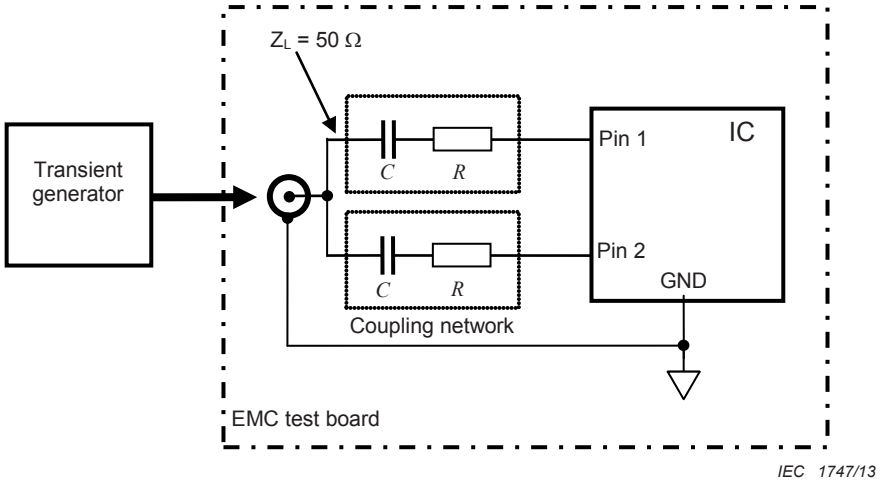

Figure 6 – Multiple pin injection test implementation

6 IC configuration and evaluation

6.1 IC configuration and operating modes

For the impulse immunity test the IC shall be set in normal operating conditions according to the typical data sheet values. This means the supply voltage shall be set to the nominal value and not to the minimum and maximum values given in the data sheet. Depending on the IC functionality relevant IC operation modes should be selected. Attempts should be made to fully exercise all functions and modes of operation that significantly influence the immunity of the DUT. If possible, the IC stimulation should be done as expected in a typical application or by auxiliary equipment not affecting the immunity performance of the DUT. When a watchdog function is available, it may be disabled during the test to collect additional information.

Mandatory components listed in the data sheet, which are necessary for the IC functionality or stimulation, shall be applied. The position of mandatory components and test board layout shall be designed not to affect adversely the test results of the IC.

NOTE To fulfil a certain test level, additional components can be necessary. Such components are regarded as mandatory for such applications.

6.2 IC monitoring

The DUT should be monitored such that immunity performance can be determined as completely as possible. The monitoring shall be implemented such that the immunity performance of the DUT is not affected.

In mixed signal ICs various response signals can be generated depending on implemented functions or installed software programs. The response signal can be monitored for indications of susceptibility that include, but are not limited to, the following parametric and functional characteristics:

- cycle-to-cycle jitter, frequency, or duty cycle of a periodic waveform;
- signal transition time (rise or fall) of the output waveform;
- signal source voltage, current or resistance;
- spikes, glitches or other transient phenomena on the output waveform;
- DUT reset;
- DUT hang;
- DUT latch-up;
- digital data loss or deviation;
- memory content corruption.

Monitoring can be done by I/O signal detection, oscilloscopes, voltmeter, logic analyser, data analyser etc. considering certain failure criteria.

For monitored response signals, failure criteria have to be defined individually for the dedicated IC impulse immunity test. A failure criterion is defined by a nominal signal value and an allowed tolerance.

6.3 IC performance classes

The IC immunity is categorised in IC performance classes as follows:

Class A_{IC}: all monitored functions of the IC perform within the defined tolerances during and after exposure to disturbance;

Class B_{IC}: short time degradation of one or more monitored signals during exposure to disturbance is not evaluable for IC only. Therefore this classification may not be applicable for ICs (see Note);

Class C_{IC}: at least one of the monitored functions of the IC is out of the defined tolerances during the disturbance but returns automatically to the defined tolerances after the exposure to disturbance;

Class D_{IC}: at least one monitored function of the IC does not perform within the defined tolerances during exposure and does not return to normal operation by itself. The IC returns to normal operation by manual intervention;

- Class $D1_{IC}$: the IC returns to normal operation by manual intervention: (e.g. reset);
- Class $D2_{IC}$: the IC returns to normal operation by power cycling the device;

Class E_{IC}: at least one monitored function of the IC does not perform within the defined tolerances after exposure and cannot be returned to proper operation.

NOTE Short time degradation of one or more monitored signals can be tolerable in the application by its error handling. This error handling is unknown in most cases for IC test.

7 Test conditions

7.1 General

Unless otherwise specified in the manufacturer's specifications, the following ambient conditions shall apply.

7.2 Ambient electromagnetic environment

The electromagnetic ambient shall not affect responses of the DUT.

7.3 Ambient temperature

The ambient temperature during the test shall be (23 ± 5) °C.

7.4 IC supply voltage

The supply voltage(s) shall be set to the nominal supply voltage(s) as specified by the IC manufacturer with a tolerance of ± 5 %.

8 Test equipment

8.1 General requirements for test equipment

All equipment used in this test shall be immune to the applied transient such that the test results will not be influenced. The test equipment shall meet the following test equipment requirements.

8.2 Cables

Coaxial cables are recommended to carry the disturbance signal to protect the test environment and prevent cross coupling of disturbance signals to stimulation and monitoring signals. For proper test signal delivery under high voltage test conditions, a cable rated for the maximum test voltage to be applied shall be specified and used.

8.3 Shielding

To ensure proper ambient environments on DUT functionality or to suppress coupling to the environment, testing in a shielded room may be required.

8.4 Transient generator

A transient generator according to IEC 61000-4-4, IEC 61000-4-5 or ISO 7637-2 shall be used.

8.5 Power supply

The DUT shall be powered by a source that is not affected by the injected disturbance signal. If a battery is used, it shall meet the IC requirements and the supply voltage level shall be checked to maintain a consistent operating environment.

8.6 Monitoring and stimulation equipment

The monitoring and stimulation equipment should not be affected by the injected disturbance signal. Care should be taken that the monitoring and stimulation equipment do not adversely affect the DUT or the test result.

8.7 Control unit

A control unit is recommended to automate control of the transient generator, stimulate the IC and acquire data from the performance monitoring.

9 Test set up

9.1 General

A block diagram of the test set-up for the non-synchronous transient immunity test is shown in Figure 7. The transient generator injects the disturbance into the IC pin under test via the coupling network on the EMC test board. The output of the transient generator is directly connected to the coaxial connector of the coupling network. The transient generator ground shall be connected to the reference ground provided by the EMC test board. A response signal driven from the IC is monitored for any indication of susceptibility while the IC is powered and a required functional stimulation is applied. The system can be controlled by a control unit.

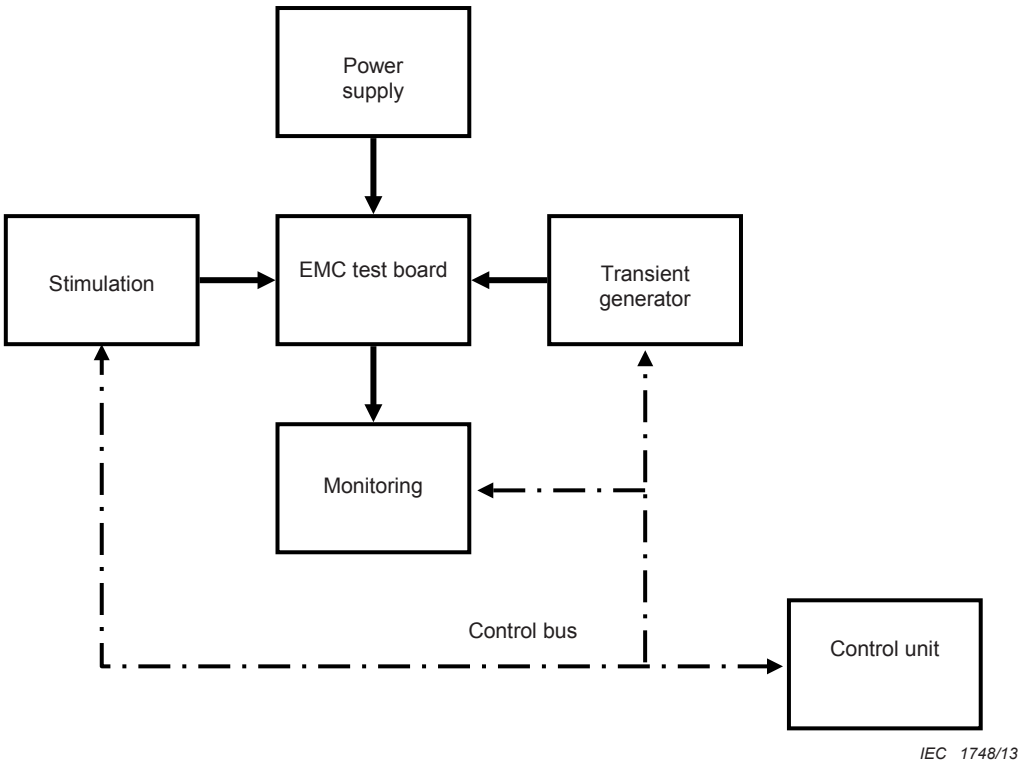

Figure 7 – Test set-up diagram

9.2 EMC test board

An EMC test board carrying the DUT, mandatory components and the necessary coupling and decoupling networks is required to perform this test method. The test board is also described in IEC 62132-4.

The use of a printed circuit board with a common ground plane for impulse testing of ICs is recommended. The DUT should be placed on the test board without sockets. If a socket is used care should be taken that the inductance of the socket does not significantly affect the test results especially for fast transients.

It is the main purpose of this standard to test the impulse immunity of the DUT only. Therefore, external protection components of the DUT shall be removed except when they are mandatory

for proper function of the IC (e.g. blocking capacitors, timer capacitors, etc.). Such mandatory components shall be placed directly at the IC and grounded on the same ground plane. Return paths from mandatory blocking components to the DUT or the shield of a transmission line should not have slits.

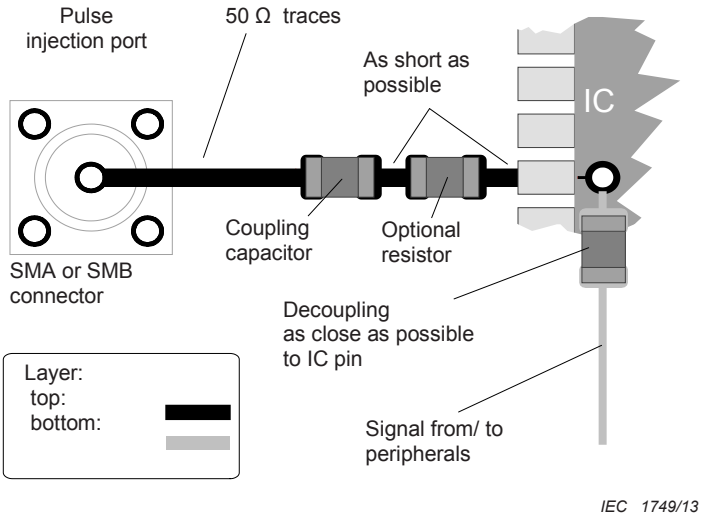

Figure 8 – Example of the routing from the injection port to a pin of the DUT

The trace from impulse injection port connector to the coupling network should be a 50 Ω transmission line (see example in Figure 8). The end of the transmission line to the pin of the DUT should be as short as possible. A trace length equal to 1/20 of the shortest wavelength applied is a reasonable target. For transients defined in the time domain, the trace length can be calculated by:

$$l_t \leq \frac{t_r \cdot v_p}{20} \quad (1)$$

$$v_p = \frac{c}{\sqrt{\varepsilon_r}} \quad (2)$$

where

l_t is trace length (cm)

t_r is rise time (ns)

c is speed of light (m/s)

v_p is propagation speed (cm/ns)
(e.g. air: v_p = 30 cm/ns, PCB material FR4: v_p = 14,8 cm/ns)

ε_r is relative permittivity

Shorter trace lengths are advantageous.

The ground plane shall not have slits in the return paths of traces carrying coupled signals. If not possible, slits in the return paths of coupled signal carrying traces shall not exceed 1/20 of the shortest wave length.

To have a reliable ground reference, the impedance between the DUT ground pin(s) and the shield of any transmission line providing the coupled signal shall be as low as possible.

Therefore using a ground plane on PCB to minimise the impedance of the ground connections is strongly recommended. The impulse decoupling network should be placed as close as possible to the pin where the impulse is injected.

If it is not possible to follow these rules, the deviations shall be described in the test report.

The impulse immunity test board can be based on the RF immunity test board of IEC 62132-4 with some modifications. Additional test board recommendations are provided in Annex A.

10 Test procedure

10.1 Test plan

The test plan shall include all conditions regarding the DUT and transients to be applied:

- selection of relevant impulses, test levels and polarity according to the target application and related basic standards;
- generator settings (repetition rate, number of impulses, output impedance);
- operation mode(s);
- monitored function and failure criteria;
- pin to be coupled.

NOTE In case of a device having a large number of pins, only a representative selection of pins depending on their type and location can be tested. The rationale for their selection are documented in the test report.

10.2 Test preparation

Energise the DUT and complete an operational check to verify proper function of the device (i.e. run DUT test code) in the ambient test condition. During the operational check, the transient generator and any stimulation and monitoring equipment shall be powered and connected to the PCB; however, the output of the transient generator shall be disabled. The performance of the DUT shall not be degraded by ambient conditions.

10.3 Characterization of coupled impulses

For consistent and repeatable testing it is necessary to characterize the generator output voltage signal under open load conditions as specified in IEC 61000-4-4, IEC 61000-4-5 or ISO 7637-2 respectively. Additionally, it is important that the coupled impulses are characterized at the DUT landing pad under open load condition. This characterization includes the impulse generator, connection lines, coupling network, mandatory components and used decoupling networks. The transfer characteristic can be estimated by the signal difference between the signal at the impulse generator output under open load conditions and the measured signal at the DUT landing pad. Both measurements should be done using an oscilloscope as defined in the respective impulse definition standard.

10.4 Impulse immunity measurement

With the EMC test board energized and the DUT being operated in the intended test mode, measure the immunity to the injected transient disturbance signal.

The applied test level shall be increased according to the test plan in steps until a malfunction is observed or the maximum test level is reached. The test shall be performed with voltage step sizes not greater than those specified in the test plan. The voltage levels listed in the test plan are the characterized transient generator output impulses under open load conditions.

At each test level, the transient signal shall be applied for a minimum of 10 s (or at least the time necessary for the DUT to respond and the monitoring system to detect any performance degradation).

For definition of the minimum dwell time statistical coverage of process timing and disturbing impulse events, thermal stress and life time test have to be considered. Typical values have to be established for standard applications. The default value is 10 min.

Test schedule in detail:

1) Connect all the equipment as shown in Figure 7.
2) Verify the proper operation of the DUT.
3) Set the transient generator for the desired voltage level.
4) Set the transient generator for the desired polarity.
5) Inject the transient for the required dwell time. Monitor the DUT performance during transient injection for performance degradation.
6) If testing at additional voltage levels is desired, go to step 3.

10.5 Interpretation and comparison of results

Results may be directly compared as long as measurements have been carried out under the same conditions. If comparison is intended, the devices should be running the same code and the test environment shall be as consistent as possible. The same kind of test boards shall be used.

For determination of IC performance classes it has to be considered if the deviation of a monitored signal is caused by an IC function or by a superposition of the disturbance signal to the functional signal. If the functional signal degradation is caused by an IC activity it shall be differentiated whether this activity is an intended (e.g. protection function as overvoltage, undervoltage, overcurrent protection, etc.) or an unintended misoperation.

10.6 Transient immunity acceptance level

The transient immunity acceptance level of an IC, if any, is to be agreed upon between the manufacturer and the user of the IC in respect to the target application of the IC. Typical application levels are described in Annexes C and D.

11 Test report

The test report shall provide all necessary information to interpret and reproduce the test results. It should contain:

- test conditions;
- test parameters as test impulses, test levels, test duration, dwell time, repetition rate according to basic standards;
- EMC test board information;
- tested pins, operation modes, software, monitoring and failure criteria, performance results;
- any deviation from the described standard method;
- coupling characteristic.

Annex A
(informative)

Test board recommendations

A.1 Board description – mechanical

The typical board size is (100^{+3}_{-1}) mm by (100^{+3}_{-1}) mm (such that it can be used with other IC test methods). Holes may be added at the corners of the board, as shown in Figure A.1. All edges of the board should be tinned for at least 5 mm, or made conducting in order to make proper contact. As an alternative, edges may be gold-plated.

The vias at the outer edge of the board should be at least 5 mm away from that edge.

A.2 Board description – electrical

A.2.1 Board design – electrical

The EMC test board drawing in Figure A.1 should be taken as a guide. A double layer board is proposed as a minimum requirement. However, if functionally needed, layers 2 and 3 or others may be added in-between such that a multi-layer board appears.

Layer 1 is always used as the ground plane. Layer 4 allows other signals, but should be left as much intact as possible, to be a ground plane as well. At least the area in layer 1, underneath the IC, is left as a ground plane for which the characteristic impedances need to be defined.

The PCB should be made such that only the IC package remains on one side (top side) and all other components and trace patterns remain on the opposite side (bottom side).

For proper function of the board under high voltage conditions care has to be taken that flashovers are avoided (e.g. careful board layout, component selection).

A.2.2 Ground planes

The ground planes (layers 1 and 4) are inter-connected by means of vias. These vias should be placed at the following positions over the board as described in Table A.1:

Table A.1 – Position of vias over the board

Via position	Location
1	All around, at the edges of the board
2	Just outside the DUT area
3	Just inside, underneath the IC area

The ground plane at layer 1 is continued in-between vias at position 2. As such the ground plane at layer 1 is continued over the whole board.

If possible, the same should be done for layer 4, but the possibility to do so depends on the IC package and the space available.

A.2.3 Pins

A.2.3.1 Location of functionally necessary components

All functionally necessary components, other than the IC, are mounted on layer 4. It is therefore necessary to feed I/O and other required pins from layer 1 to layer 4. The loop areas, trace length, via placement and component orientation should be optimised such that minimum loop areas are obtained.

A.2.3.2 DIL packages

These packages do not require vias, as plated-through hole pins are considered present or established by the pins themselves.

A.2.3.3 SO, PLCC, QFP packages

These packages require the use of vias. The vias should preferably be centred in the pads used for soldering the ICs. Preferably, these vias should be placed at position 3, Table A.1 to minimise the loop-area involved in which the IC currents will flow.

A.2.3.4 PGA, BGA

Under consideration.

A.2.4 Vias

A.2.4.1 Via type

All vias at position 1 shall have a hole diameter of 0,8 mm. All other vias shall have a diameter of $\geq$ 0,2 mm.

A.2.4.2 Via distance

A maximum lateral distance between vias is required for measurements up to 1 GHz.

- Vias connecting layer 1 with layer 4 are at a maximum distance of 10 mm in-between.
- Vias accompanying signal traces should be as close as possible to those vias connecting layers 1 to 4, to create small return signal loops.

A.2.5 Additional components

All additional components should be mounted at layer 4. They are placed in such a way that they do not interfere with the constraints as set for layer 1 and 4 and vias in-between.

A.2.6 Supply decoupling

To obtain reproducible data of measurement, adequate supply decoupling is required in accordance with the test board specifications. Decoupling capacitors on the test board are classified into two groups described below. The values and layout positions of the decoupling capacitors and other decoupling components are stated in the individual test report.

- IC decoupling capacitors:

  Supply decoupling for the IC is in accordance with the manufacturer's recommendations. IC decoupling capacitors, if any, are connected to the ground plane in layer 4, underneath the IC, to maintain the proper operation of the DUT. The value and layout position of a decoupling capacitor of each supply pin of the DUT may be as advised by the manufacturer, or otherwise, as long as this is stated in the test report.

- Power supply decoupling for the test board:

Impedance of the test board power supply and impulse signal path may affect the measurement results if the test board is not adequately designed. To control the supply impedance of the test board for any external power supply that may be used in the measurement, a group of decoupling capacitors is located on the test board. Their values and layout positions are as described in the individual measurement standards, or otherwise, as long as this is stated in the test report.

A.2.7 I/O load

Additional components necessary to load or activate the IC should be mounted on layer 4, preferably directly underneath the IC package area.

All dimensions are in mm

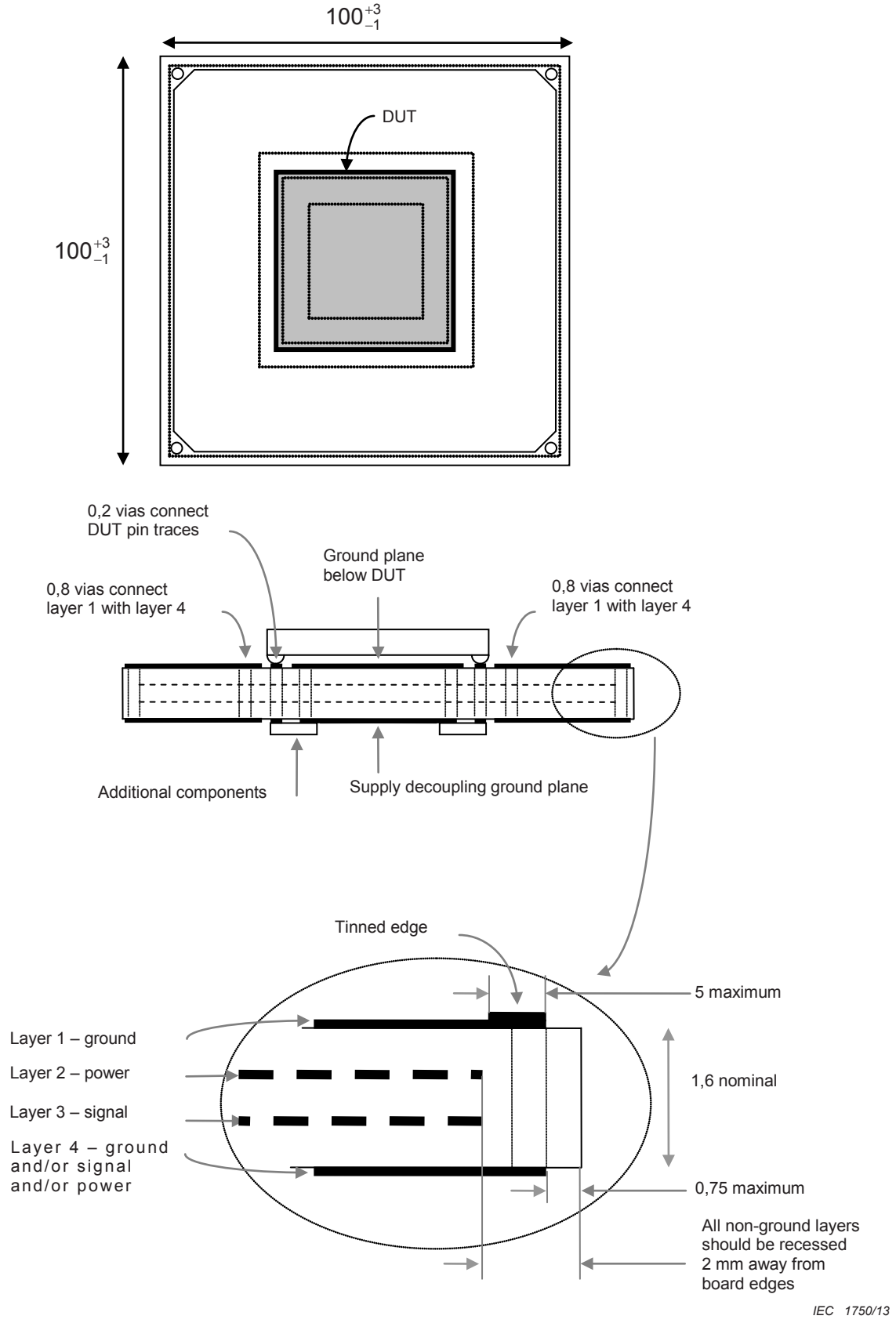

Figure A.1 – Typical EMC test board topology

A.3 Example of test board with different coupling networks

Multiple injection test structures may be implemented on a single EMC test board in order to fully-characterize an IC. A schematic example showing of all the available injection test structures implemented on a single board is contained in Figure A.2. For ICs with additional supply, ground, input or output pins, the appropriate test structure can be replicated. Multiple supply and ground pins of the same name (i.e. VS1, VS2, etc.) should be grouped together, connected to a single test structure, and tested as a single pin. A blocking capacitor (C_{BL}) required by the manufacturer is connected between the supply and local ground as shown. The value of this decoupling **capacitor is as stated in the device user guide.**

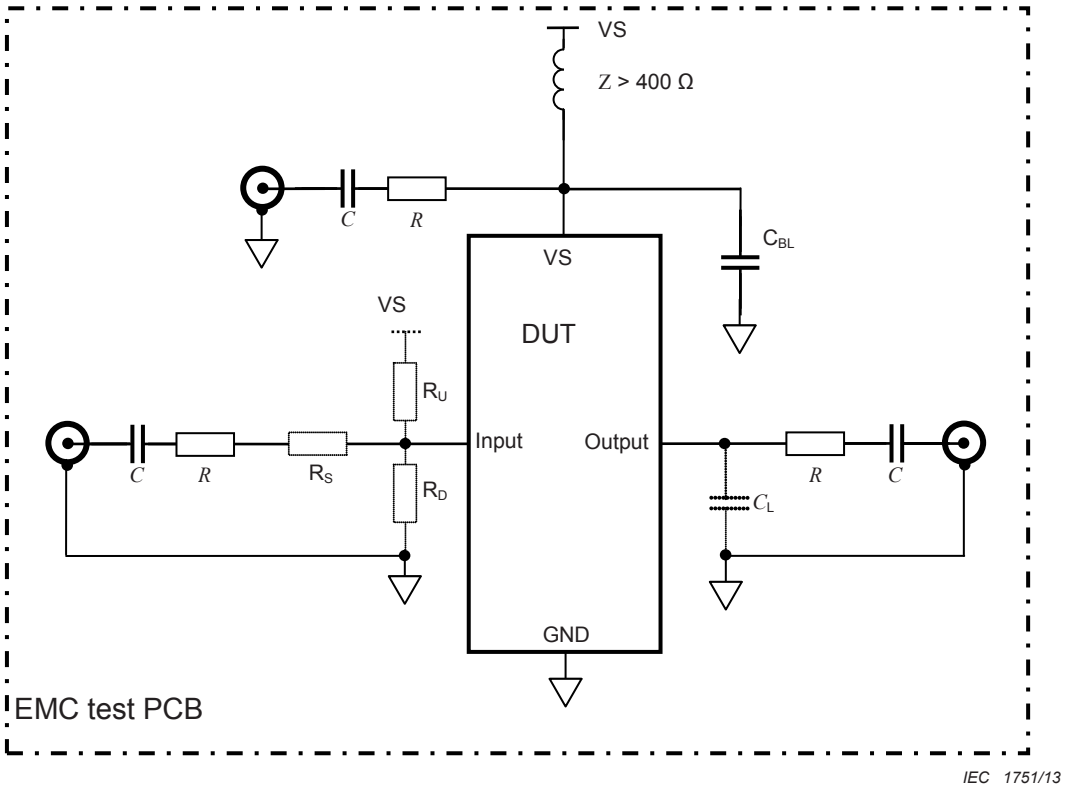

Figure A.2 – Example of implementation of multiple injection structures

Annex B
(informative)

Selection hints for coupling and decoupling network values

B.1 General requirements

The coupling and decoupling networks are defined with respect to the expected transient environment and coupling phenomena of IC applications. The capacitor values for indirect capacitive coupling are taken from the capacity per unit length with 100 pF/m. For global pins connected to the wire harness a wire length of 10 m is considered as representative. For this kind of connected pins the default value of the coupling capacitor is 1 nF. For local pins remaining on the application board, trace length is in the range of 0,05 m up to 0,2 m and can be represented by a coupling capacitor from 10 pF to 47 pF.

B.2 Coupling and decoupling networks for global IC pins

B.2.1 Coupling and decoupling networks for power supply pins

B.2.1.1 Direct injection into supply pins

For supply pin(s) directly connected to and powered via the transient generator in the test setup, the coupling and decoupling networks are provided by the generator as specified in IEC 61000-4-4, IEC 61000-4-5 or ISO 7637-2 respectively.

For supply pin(s) not directly connected to and powered via the transient generator in the test setup, the following coupling networks should be used:

For fast impulses (rise time < 10 ns):

Coupling network: generator internal network or C = 1 nF (ceramic SMD), R = 0 Ω

Decoupling network: L = 5 μH ± 10 % for automotive
(optional matching to e.g. fixed values 50 Ω, 150 Ω or 400 Ω)
L = 50 μH ± 10 % for industrial
(optional matching to e.g. fixed values 50 Ω, 150 Ω or 400 Ω)

For slow impulses (rise time >= 1 μs):

Coupling network: generator internal network or C = 100 nF, R = 0 Ω

Decoupling network: L = 5 μH ± 10 % for automotive
(optional matching to e.g. fixed values 50 Ω, 150 Ω or 400 Ω)
L = 50 μH ± 10 % for industrial
(optional matching to e.g. fixed values 50 Ω, 150 Ω or 400 Ω)
diode for decoupling of positive impulses towards the power net and power switch for disconnecting power net when negative impulses are applied (devices rating according to expected current and voltage values)

B.2.1.2 Capacitive coupling into supply pins

For sub-supply pin(s) not directly connected to and powered via the transient generator in the test setup the following coupling networks shall be used:

For fast and slow impulses:

Coupling network: C = 1 nF (ceramic SMD), R = 0 Ω

Decoupling network: choke with approximately Z ~ 400 Ω, for automotive and industrial (optional matching to e.g. fixed values 50 Ω, 150 Ω or 400 Ω)

B.2.2 Coupling and decoupling networks for I/O pin(s)

For fast and slow impulses

Coupling network: C = 1 nF (ceramic SMD), R = 0 Ω

Decoupling network: Choke with approximately Z ~ 400 Ω, for automotive and industrial (optional matching to e.g. fixed values 50 Ω, 150 Ω or 400 Ω)

B.3 Coupling and decoupling networks for local pins

Depending on the definition of the load to a specific IC pin, an adapted coupling – decoupling structure may be used. The values for this structure shall be chosen in such a way that:

- the maximum load of the pin shall not be exceeded;
- the impulses shall be sufficiently coupled to meet application requirements;
- the decoupling inductance/choke shows a high impedance compared to the coupling capacitor impedance.

Coupling networks for coupling on PCB traces shall be: C = 10 pF to 47 pF (ceramic SMD), R = 0 Ω.

Annex C
(informative)

Industrial and consumer applications

C.1 General information

For industrial applications, the IC shall be tested according to typical impulse disturbances as defined by IEC 61000-4-4 and IEC 61000-4-5.

C.2 Definition of pin types

Based on typical applications, the IC pin(s) should be classified according to Table C.1.

Table C.1 – Definition of pin types

Pin category	Pin type	Pin type examples	Test circuit	Test circuit values according to Table C.2	Remarks
Local	Power supplies	I/O, core, analog, PLL	Fig. 3	L1	
	Inputs	General purpose input ports, reset, IRQ, amplifier input or analog input	Figs. 4, 6	L2	Inputs can respond to injections as valid signals. 10 pF to emulate board trace coupling.
	Output	General purpose outputs Output port	Figs. 5, 6	L3	10 pF to emulate board trace coupling.
	Oscillator	Crystal oscillator	Fig. 4	L4	Sensitive to loading. Injection with low capacitance (1 pF to 5 pF).
Global	Power supplies	Main supply	Figs. 2, 3	G1	Subject to fast transients, surge. 1 nF for coupling into battery or AC mains power supply if the pin is not directly connected to the power net.
	Inputs	General purpose input port	Figs.4, 6	G2	Inputs can respond to injections as valid signals. 1 nF for long wire to wire or wire to case coupling.
	Outputs	General purpose output port	Figs.5, 6	G3	1 nF for long wire to wire or wire to case coupling.
	Communication I/Os	SCI, USB, Ethernet, I^2C	Figs.4,5	G2, G3	Long lines, various protection requirements, 1 nF for long wire to wire coupling.

Some pins of devices intended for use in industrial and consumer applications may be global or local depending on the specific application. In this case these pins should be tested with the more severe global test levels. Furthermore, in the case of a large number of global pins, a representative sample of pins depending on their type and location may be tested.

C.3 Test types

The test circuit value Table C.2 shows recommended population values for single pin injection. If these values or options cannot be used for proper device operation or evaluation, the deviations shall be described in the test report. For multiple pin injection the values for the coupling networks should be set as for the respective single pins.

Table C.2 – Test circuit values

Test	Type	Figure	C	R	Z	R_S	R_U	R_D	C_L	C_{BL}
L1	Power supply	3	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
L2	Input	4	10 pF	0	n.p.	0	10 kΩ	10 kΩ	n.a.	n.a.
L3	Output	5	10 pF	0	n.p.	0	n.p.	n.p.	47 pF	n.a.
L4	Sensitive input	4	1 pF to 5 pF	0	n.p.	0	n.p.	n.p.	n.a.	n.a.
G1	Power supply	2, 3[a]	n.a. 1 nF	n.a. 0	n.a. 50 μH	n.a. n.a.	n.a. n.a.	n.a n.a.	n.a. n.a.	as required
G2[b]	Input	4	1 nF	0	n.p.	0	10 kΩ	10 kΩ	n.a.	n.a.
G3[b]	Output	5	1 nF	0	n.p.	n.a.	n.a.	n.a.	47 pF	n.a.

tbd – to be defined.

n.p. – not populated unless required for proper operation.

n.a. – not applicable.

R_U / R_D – populate either pull-up or pull-down.

[a] If the power supply pin is not directly connected to the power net and the generator internal coupling network, as specified in IEC 61000-4-4 and IEC61000-4-5, cannot be used.

[b] For communication I/Os other values regarding proper operation may be necessary.

C.4 Impulse characteristics

Impulse characteristics shall be equivalent to injection characteristics described in IEC 61000-4-4 and IEC 61000-4-5.

C.5 Test levels

Test levels will be set as determined by the application requirements (e.g., motor control, metering, appliance device, industrial controller) (see Table C.3).

Table C.3 – Example of IC impulse test level (IEC 61000-4-4)

Pin number	**Test**	**Type**	**Configuration**	**Polarity**	**Initial test injection voltage** (V)	**Final test injection voltage** (V)	**Injection voltage step** (V)	**Impulse dwell time** (s)
1	L2	Input	Pull up	positive	500	4 000	500	60
1	L2	Input	Pull up	negative	500	4 000	500	60
4	L1	Power supply	–	positive	500	4 000	500	60
4	L1	Power supply	–	negative	500	4 000	500	60
16	L4	Sensitive input	Crystal oscillator	positive	500	4 000	500	60
16	L4	Sensitive input	Crystal oscillator	negative	500	4 000	500	60
23	G2	Communication input	Serial input port	positive	500	4 000	500	60
23	G2	Communication input	Serial input port	negative	500	4 000	500	60

Test injection values will be recorded as the open circuit voltage of the generator.

Annex D
(informative)

Vehicle applications

D.1 General information

For vehicle application the IC shall be tested according to typical impulse disturbances as defined in ISO 7637-2. Clauses D.2 to D.4 can be used for test level selections at defined pin types.

D.2 Definition of IC pin types

Based on typical applications, the IC pin(s) should be classified according to Table D.1.

Table D.1 – IC pin type definition

Pin type	**Coupling of transient disturbances**	**Transient disturbances** (according to ISO 7637-2)
1	Pins directly connected to vehicle battery supply lines	ISO impulse 1, ISO impulse 2a, ISO impulses 3a/3b
2	Pins directly connected to wiring harness	ISO impulses 3a/3b
3	Pins indirectly connected to wiring harness vehicle battery supply lines (trough expected but not mandatory specified filter or protection devices)	ISO impulse 1, ISO impulse 2a, ISO impulses 3a/3b
4	Pins indirectly connected to wiring harness I/O lines (trough expected but not mandatory specified filter or protection devices)	ISO impulses 3a/3b
5	Pins not directly connected to vehicle wiring harness (only relevant for cross coupling on PCB, coupling networks must be adapted)	ISO impulses 3a/3b

D.3 Test level

The test level depends on the application area of the IC. To meet relevant application requirements for different pin types, the recommended transient test levels are defined in Tables D.2 and D.3.

Table D.2 – Transient test level 12 V (ISO 7637-2)

Impulse	Limit classes	Global pin				Local pin	Performance classes
		type 1 direct **test level** (V)	**type 2** capacitive 1 nF **test level** (V)	**type 3** direct filtered **test level** (V)	**type 4** capacitive 1 nF filtered **test level** (V)	**type 5** capacitive 10 pF **test level** (V)	**A_{IC}, C_{IC}, D_{IC}**
ISO 1	I	-75	n.a.	-75	n.a.	n.a.	C_{IC}
	II	-112		-112			
	III	-150		-150			
ISO 2a	I	37	n.a.	37	n.a.	n.a.	A_{IC}, C_{IC}
	II	55		55			
	III	112		112			
ISO 3a	I	-112	-112	-112	-112	-112	A_{IC}, C_{IC}
	II	-165	-165	-165	-165	-165	
	III	-220	-220	-220	-220	-220	
ISO 3b	I	75	75	75	75	75	A_{IC}, C_{IC}
	II	112	112	112	112	112	
	III	150	150	150	150	150	
Depending on test level and maximum ratings of the IC, external protection may be required. By pin selection for test it has to be checked whether a transient exposure is expected in the application of the IC or not.							

Table D.3 – Transient test level 24 V (ISO 7637-2)

Impulse	Limit classes	Global pin				Local pin	Performance classes
		type 1 direct **test level** (V)	**type 2** capacitive 1 nF **test level** (V)	**type 3** direct filtered **test level** (V)	**type 4** capacitive 1 nF filtered **test level** (V)	**type 5** capacitive 10 pF **test level** (V)	**A_{IC}, C_{IC}, D_{IC}**
ISO 1	I	-300	n.a.	-300	n.a.	n.a.	C_{IC}
	II	-450		-450			
	III	-600		-600			
ISO 2a	I	37	n.a.	37	n.a.	n.a.	A_{IC}, C_{IC}
	II	55		55			
	III	112		112			
ISO 3a	I	-150	-150	-150	-150	-150	A_{IC}, C_{IC}
	II	-220	-220	-220	-220	-220	
	III	-300	-300	-300	-300	-300	
ISO 3b	I	150	150	150	150	150	A_{IC}, C_{IC}
	II	220	220	220	220	220	
	III	300	300	300	300	300	
Depending on test level and maximum ratings of the IC, external protection may be required. By pin selection for test it has to be checked whether a transient exposure is expected in the application of the IC or not.							

The repetition time and impulse parameters shall be according to ISO 7637-2 and noted in the test report.

For the test duration it shall be considered that the impulses are not synchronized with the IC functional timing. For a statistical coverage a minimum test time of 10 min per impulse type is recommended.

For test impulse amplitudes higher than the operating voltage it is expected that protection circuits in the IC will be activated and lead to an additional thermal load of the IC. Therefore the test time should be longer than the thermal time constant of the IC in its test setup. A test time of 10 min per test impulse is recommended. If other test time values are used they have to be noted in the test report.

D.4 Example of IC transient test specification

The transient test specification for ICs shall be developed in respect to the target application. To define relevant pins and appropriate test levels, the IC pins shall be classified in pin types as defined in Table D.1. Based on the pin type and the supply system, the related test levels can be selected out of Tables D.2 or D.3. Depending on the IC function and the desired functionality during or after the transient disturbances, the dwell times or number of impulses, monitoring conditions and functional status classes have to be defined. An example of a transient test specification is given in Table D.4.

Table D.4 – Example of transient test specification

Pin no.	Pin type	V_{bat}/VS (V)	Impulse 1			Impulse 2			Impulse 3a			Impulse 3b		
			V_P (V)	FPSC	No. of impulses / dwell time (min)	V_P (V)	FPSC	No. of impulses / dwell time (min)	V_P (V)	FPSC	No. of impulses / dwell time (min)	V_P (V)	FPSC	No. of impulses / dwell time (min)
3	2	12/5	n.a.	–	–	± 30	A_{IC}	100	-60	A_{IC}	10	40	A_{IC}	10
4	2	12/5	n.a.	–	–	± 30	C_{IC}	100	-60	C_{IC}	10	40	C_{IC}	10
7	4	12/5	n.a.	–	–	± 9,6	C_{IC}	50	– 19,2	C_{IC}	10	12,8	C_{IC}	10
12	4	12/5	n.a.	–	–	± 9,6	C_{IC}	50	– 19,2	C_{IC}	10	12,8	C_{IC}	10
32	2	12/5	n.a.	–	–	± 30	C_{IC}	100	-60	C_{IC}	10	40	C_{IC}	10
33	2	12/5	n.a.	–	–	± 30	C_{IC}	100	-60	C_{IC}	10	40	C_{IC}	10
36	5	12/3,3	n.a.	–	–	± 3,3	C_{IC}	50	-3,3	C_{IC}	10	3,3	C_{IC}	10
38	5	12/3,3	n.a.	–	–	± 3,3	D_{IC}	50	-3,3	E_{IC}	10	3,3	D_{IC}	10

V_{bat} = Vehicle battery supply voltage

VS = IC operating voltage (for multiple operating voltages of the IC)

V_P = maximum test impulse voltage (expected in the application)

FPSC = Functional performance status class (defined for the specific IC)

n.a. = not applicable

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