BS EN 62116:2014

BSI Standards Publication

Utility-interconnected photovoltaic inverters — Test procedure of islanding prevention measures

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National foreword

This British Standard is the UK implementation of EN 62116:2014. It is identical to IEC 62116:2014. It supersedes BS EN 62116:2011, which will be withdrawn on 2 April 2017.

The UK participation in its preparation was entrusted to Technical Committee GEL/82, Photovoltaic Energy Systems.

A list of organizations represented on this committee can be obtained on request to its secretary.

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Utility-interconnected photovoltaic inverters - Test procedure of islanding prevention measures (IEC 62116:2014)

Onduleurs photovoltaïques interconnectés au réseau public - Procédure d'essai des mesures de prévention contre l'îlotage (CEI 62116:2014)

Photovoltaik-Wechselrichter für den Anschluss an das Stromversorgungsnetz - Prüfverfahren für Maßnahmen zur Verhinderung der Inselbildung (IEC 62116:2014)

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Foreword

The text of document 82/813/FDIS, future edition 2 of IEC 62116, prepared by IEC/TC 82 "Solar photovoltaic energy systems" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62116:2014.

The following dates are fixed:

– latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2015-01-25

– latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2017-04-02

This document supersedes EN 62116:2011.

EN 62116:2014 includes the following significant technical changes with respect to EN 62116:2011:

<table>
<tr><th></th><th>Previous edition</th><th>Present edition</th></tr>
<tr><td>3.7</td><td rowspan="11">Real power</td><td rowspan="11">Active power</td></tr>
<tr><td>5.1</td></tr>
<tr><td>5.4</td></tr>
<tr><td>6.1 b)</td></tr>
<tr><td>6.1 d)</td></tr>
<tr><td>6.1 e)</td></tr>
<tr><td>6.1 g)</td></tr>
<tr><td>Table 1</td></tr>
<tr><td>Table 6</td></tr>
<tr><td>Table 7</td></tr>
<tr><td>Table 9</td></tr>
<tr><td>5.2</td><td>A PV array or PV array simulator (preferred) may be used.
If the EUT can operate in utility-interconnected mode from a storage battery, a DC power source may be used in lieu of a battery as long as the DC power source is not the limiting device as far as the maximum EUT input current is concerned.</td><td>A DC power source, such as a PV array simulator, a PV array, or a current and voltage limited DC power supply with series resistance may be used.
If the EUT can operate in utility-interconnected mode from a storage battery, a DC power source may be used in lieu of a battery as long as the DC power source shall not be the limiting device as far as the maximum EUT input current is concerned.</td></tr>
</table>

Table 5	EUT input voltage 90 %	EUT input voltage 75 %
	EUT input voltage 10 %	EUT input voltage 20 %
	EUT Trip Settings Manufacturer specified voltage and frequency trip settings	Voltage and frequency trip settings according to National standards and/or local code
Tables 6 & 7 (Heading)	Percent change in real load, reactive load from nominal	Percent change in active load, reactive load from nominal output power

Major changes with respect to the previous edition concern the DC power source and test conditions.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 62116:2014 was approved by CENELEC as a European Standard without any modification.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

Publication	Year	Title	EN/HD	Year
IEC/TS 61836	-	Solar photovoltaic energy systems - Terms, definitions and symbols	CLC/TS 61836	-

CONTENTS

INTRODUCTION

Islanding is a condition in which a portion of an electric power grid, containing both load and generation, is isolated from the remainder of the electric power grid. This situation is one which electric power providers (utilities) regularly contend with. When an island is created purposely by the controlling utility – to isolate large sections of the utility grid, for example – it is called an intentional island. Conversely, an unintentional island can be created when a segment of the utility grid containing only customer-owned generation and load is isolated from the utility control.

Normally, the customer-owned generation is required to sense the absence of utility-controlled generation and cease energizing the grid. However, when the generation and load within the segment are well balanced prior to the isolation event, the utility is providing little power to the grid segment, thus making it difficult to detect when the isolation occurs. Damage can occur to customer equipment if the generation in the island, no longer under utility control, operates outside of normal voltage and frequency conditions. Customer and utility equipment can be damaged if the main grid recloses into the island out of synchronization. Energized lines within the island present a shock hazard to unsuspecting utility lineworkers who think the lines are dead.

The PV industry has pioneered the development of islanding detection and prevention measures. To satisfy the concerns of electric power providers, commercially-available utility-interconnected PV inverters have implemented a variety of islanding detection and prevention (also called anti-islanding) techniques. The industry has also developed a test procedure to demonstrate the efficacy of these anti-islanding techniques; that procedure is the subject of this document.

This standard provides a consensus test procedure to evaluate the efficacy of islanding prevention measures used by the power conditioner of utility-interconnected PV systems. Note that while this document specifically addresses inverters for photovoltaic systems, with some modifications the setup and procedure may also be used to evaluate inverters used with other generation sources or to evaluate separate anti-islanding devices intended for use in conjunction with PV inverters or other generation sources acting as or supplementing the anti-islanding feature of those sources.

Inverters and other devices meeting the requirements of this document can be considered non-islanding, meaning that under reasonable conditions, the device will detect island conditions and cease to energize the public electric power grid.

UTILITY-INTERCONNECTED PHOTOVOLTAIC INVERTERS – TEST PROCEDURE OF ISLANDING PREVENTION MEASURES

1 Scope

The purpose of this International Standard is to provide a test procedure to evaluate the performance of islanding prevention measures used with utility-interconnected PV systems.

This standard describes a guideline for testing the performance of automatic islanding prevention measures installed in or with single or multi-phase utility interactive PV inverters connected to the utility grid. The test procedure and criteria described are minimum requirements that will allow repeatability. Additional requirements or more stringent criteria may be specified if demonstrable risk can be shown. Inverters and other devices meeting the requirements of this standard are considered non-islanding as defined in IEC 61727.

This standard may be applied to other types of utility-interconnected systems (e.g. inverter-based microturbine and fuel cells, induction and synchronous machines). However, technical review may be necessary for other than inverter-based PV systems.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC/TS 61836, *Solar photovoltaic energy systems – Terms, definitions and symbols*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 61836 as well as the following apply.

3.1
PV array simulator
DC power source used to simulate PV array output

3.2
EUT
equipment under test
inverter or anti-islanding device on which these tests are performed

Note 1 to entry: This note applies to the French language only.

3.3
MPPT
maximum power point tracking
PV array control strategy used to maximize the output of the system under the prevailing conditions

Note 1 to entry: This note applies to the French language only.

3.4
non-islanding inverter
inverter that will cease to energize a utility distribution system that is out of the nominal operation specifications for voltage and/or frequency

[SOURCE: IEC 61727:2004, 3.8.1]

3.5
island
state in which a portion of the electric utility grid, containing load and generation, continues to operate isolated from the rest of the grid

Note 1 to entry: The generation and loads may be any combination of customer-owned and utility-owned.

3.6
intentional island
island that is intentionally created, usually to restore or maintain power to a section of the utility grid affected by a fault

Note 1 to entry: The generation and loads may be any combination of customer-owned and utility-owned, but there is an implicit or explicit agreement between the controlling utility and the operators of customer-owned generation for this situation.

3.7
quality factor
$\boldsymbol{Q_\mathrm{f}}$
a measure of the strength of resonance of the islanding test load

Note 1 to entry: In a parallel resonant circuit, such as a load on a power system

$$Q_\mathrm{f} = R\sqrt{\frac{C}{L}}$$

where

Q_f is quality factor

R is effective load resistance

C is reactive load capacitance (including shunt capacitors)

L is reactive load inductance

With C and L tuned to the power system fundamental frequency, Q_f for the resonant circuit drawing active power, P, reactive powers Q_L, for inductive load and Q_C for capacitive load, Q_f can be determined by

$$Q_\mathrm{f} = (1/P)\sqrt{|Q_\mathrm{L}| \cdot |Q_\mathrm{C}|}$$

where

P is active power, in W

Q_L is inductive load, in $\mathrm{VAr_L}$

Q_C is capacitive load, in $\mathrm{VAr_C}$

3.8
run-on time
$\boldsymbol{t_\mathrm{R}}$
amount of time that an unintentional island condition exists, calculated as the interval between the opening of the switch S1 (Figure 1) and the cessation of EUT output current

3.9
stopping signal
signal provided by the inverter indicating it has ceased energizing its utility grid-connected output terminals

SEE: Annex C.

3.10
unintentional island
islanding condition in which the generation within the island that is supposed to cease energizing the utility grid instead continues to energize the utility grid

4 Testing circuit

The testing circuit shown in Figure 1 shall be employed. Similar circuits shall be used for three-phase output.

Parameters to be measured are shown in Table 1 and Figure 1. Parameters to be recorded in the test report are discussed in Clause 7.

Table 1 – Parameters to be measured in real time

Parameter	Symbol	Units
EUT DC input [a, b]		
DC voltage	V_{DC}	V
DC current	I_{DC}	A
DC power	P_{DC}	W
Irradiance [c]	G	W/m^2
EUT AC output		
AC voltage [b, d, e]	V_{EUT}	V
AC current [b, d, e]	I_{EUT}	A
Active power [b]	P_{EUT}	W
Reactive power [b]	Q_{EUT}	VAr
Voltage waveform [d, e, f, g]		
Current waveform [d, e, f, g]		
EUT (relay) output control signal [d]		
Run-on time	t_R	s
Stopping signal [h]	SS	--
Test load [b]		
Resistive load current	I_R	A
Inductive load current	I_L	A
Capacitive load current	I_C	A
AC (utility) power source		
Utility active power [i]	P_{AC}	W
Utility reactive power [i]	Q_{AC}	VAr
Utility current [i]	I_{AC}	A

[a] If applicable.

[b] Record values measured before switch S1 is opened.

[c] Recorded when the test is carried out using a PV array. Pyranometer should be fast response silicon-type not thermopile-type.

[d] The response time of voltage and current transducer shall be suitable for the sampling rate used.

[e] The waveform, AC voltage and current shall be measured on all phases.

[f] The waveform data shall be recorded from the beginning of the islanding test until the EUT ceases output. The measurement of time shall have an accuracy and resolution of better than 1 ms.

[g] When the waveform is recorded, the synchronizing signal of the S1 opening and stopping signal may be simultaneously recorded.

[h] If available from the EUT.

[i] Signal shall be filtered as necessary to provide fundamental (50 Hz or 60 Hz) frequency value. Fundamental values will ignore incidental harmonics, caused by utility voltage distortion, absorbed by the load and EUT filtering capacitors.

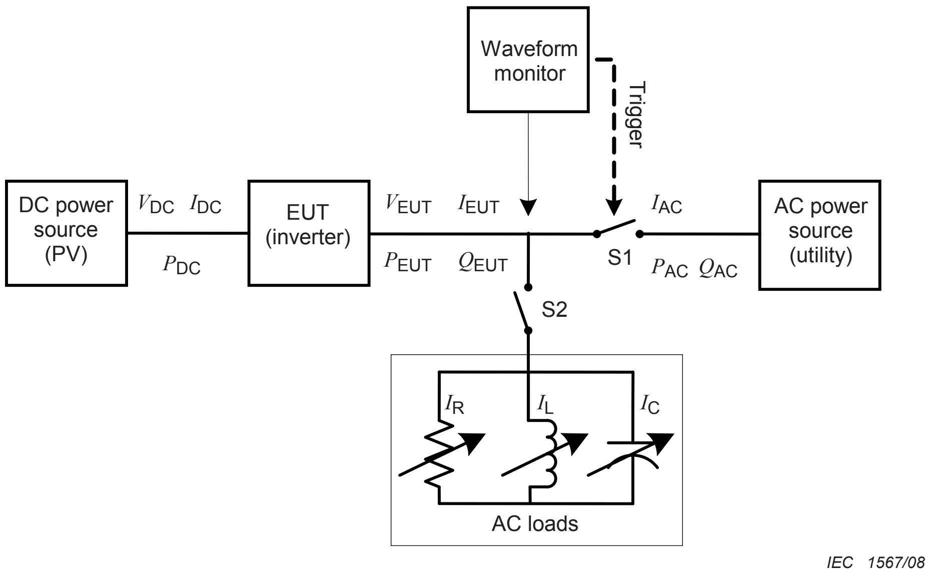

Figure 1 – Test circuit for islanding detection function in a power conditioner (inverter)

5 Testing equipment

5.1 Measuring instruments

Waveform observation shall be measured by a device with memory function, for example, a storage or digital oscilloscope or a high speed data acquisition system. The waveform measurement/capture device shall be able to record the waveform from the beginning of the islanding test until the EUT ceases to energize the island. For multi-phase EUT, all phases shall be monitored. A waveform monitor designed to detect and calculate the run-on time may be used.

For multi-phase EUT, the test and measurement equipment shall record each phase current and each phase-to-neutral or phase-to-phase voltage, as appropriate, to determine fundamental frequency active and reactive power flow over the duration of the test. A sampling rate of 10 kHz or higher is recommended. The minimum measurement accuracy shall be 1 % or less of rated EUT nominal output voltage and 1 % or less of rated EUT output current. Current, active power, and reactive power measurements through switch S1 used to determine the circuit balance conditions shall report the fundamental (50 Hz or 60 Hz) component.

5.2 DC power source

5.2.1 General

A DC power source, such as a PV array simulator, a PV array, or a current and voltage limited DC power supply with series resistance may be used.

If the EUT can operate in utility-interconnected mode from a storage battery, a DC power source may be used in lieu of a battery as long as the DC power source shall not be the limiting device as far as the maximum EUT input current is concerned.

The DC power source shall provide voltage and current necessary to meet the testing requirements described in Clause 6.

5.2.2 PV array simulator

A unit intended to be energized directly from a photovoltaic source shall be energized from a supply that simulates the current-voltage characteristics and time response of a photovoltaic array. The tests shall be conducted at the input voltage defined in Table 2 below, and the current shall be limited to 1,5 times the rated photovoltaic input current, except when specified otherwise by the test requirements.

A PV array simulator is recommended, however, any type of power source may be used if it does not influence the test results.

Table 2 – Specification of array simulator (test conditions)

Items [a]	Conditions
Output power	Sufficient to provide maximum EUT output power and other levels specified by test conditions of Table 5.
Response speed [b]	The response time of a simulator to a step in output voltage, due to a 5 % load change, should result in a settling of the output current to within 10 % of its final value in less than 1 ms.
Stability	Excluding the variations caused by the EUT MPPT, simulator output power should remain stable within 2 % of specified power level over the duration of the test: from the point where load balance is achieved until the island condition is cleared or the allowable run-on time is exceeded.
Fill factor [c]	0,25 to 0,8.

[a] For the purposes of this standard, it is assumed that there is no influence of cell technology on islanding detection.

[b] Response speed is indicated to avoid the influence caused by the MPPT control system, the ripple frequency on the DC side of a EUT, or the active methods of anti-islanding.

[c] Fill factor = $(V_{mp} \times I_{mp})/(V_{oc} \times I_{sc})$, where V_{mp} and I_{mp} are the maximum power point voltage and current, respectively, V_{oc} is the open circuit voltage, and I_{sc} is the short circuit current. It should be maintained at one value for all test conditions.

5.2.3 Current and voltage limited DC power supply with series resistance

A DC power source used as the EUT input source shall be capable of EUT maximum input power (so as to achieve EUT maximum output power) at minimum and maximum EUT input operating voltage.

The power source should provide adjustable current and voltage limit, set to provide the desired short circuit current and open circuit voltage when combined with the series and shunt resistance described below.

A series resistance (and, optionally, a shunt resistance) should be selected to provide a fill factor within the range shown in Table 2.

5.2.4 PV array

A PV array used as the EUT input source shall be capable of EUT maximum input power at minimum and maximum EUT input operating voltage (see Table 3). Testing is limited to times when the irradiance varies by no more than 2 % over the duration of the test as measured by a silicon-type pyranometer or reference device. It may be necessary to adjust the array configuration to achieve the input voltage and power levels prescribed in 6.1.

Table 3 – PV array test conditions

Items	Conditions
Output power	Sufficient to provide maximum EUT output power and other levels specified by test conditions of Table 5.
Climate condition	Irradiance, ambient temperature, etc.
To achieve a balanced load condition, the output of the PV array shall be stable. Thus, it is important to perform the test only during times of stable irradiance (e.g., clear sky, near solar noon).	

5.3 AC power source

The utility grid or other AC power source may be used as long as it meets the conditions specified in Table 4.

Table 4 – AC power source requirements

Items	Conditions
Voltage	Nominal ± 2,0 %
Voltage THD	< 2,5 %
Frequency	Nominal ± 0,1 Hz
Phase angle distance [a]	120° ± 1,5°
[a] Three-phase case only.	

5.4 AC loads

On the AC side of the EUT, variable resistance, capacitance, and inductance shall be connected in parallel as loads between the EUT and the AC power source. Other sources of load, such as electronic loads, may be used if it can be shown that the source does not cause results that are different than would be obtained with passive resistors, inductors, and capacitors.

All AC loads shall be rated for and adjustable to all test conditions. The equations for Q_f are based upon an ideal parallel RLC circuit. For this reason, non-inductive resistors, low loss (high Q_f) inductors, and capacitors with low effective series resistance and effective series inductance shall be utilized in the test circuit. Iron core inductors, if used, shall not exceed a current THD of 2 % when operated at nominal voltage. Load components should be conservatively rated for the voltage and power levels expected. Resistor power ratings should be chosen so as to minimize thermally-induced drift in resistance values during the course of the test.

Active and reactive power should be calculated (using the measurements provided in Table 1) in each of the R, L and C legs of the load so that these parasitic parameters (and parasitics introduced by variacs or autotransformers) are properly accounted for when calculating Q_f.

6 Test for single or multi-phase inverter

6.1 Test procedure

The following test is designed for an EUT consisting of a single or multi-phase inverter[1]. The test uses an RLC load, resonant at the EUT nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For a multi-phase EUT, the load shall be balanced across all phases

1 Annex B describes the test for an independent islanding detection device (relay).

and the switch S1 as in Figure 1 shall open all phases[2]. This test shall be performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating.

EUT settings for voltage and frequency trip parameters (magnitude and timing) can affect the measured run-on time. Passing this test verifies that the unit will provide adequate islanding protection for the settings tested as well as for tighter settings (e.g., an EUT that passes the test with frequency trip settings of ± 1,5 Hz of nominal should also trip within the maximum measured run-on time for settings of, say, ± 0,5 Hz.) Conversely, when adjusted to settings outside of those tested, the EUT may experience extended run-on times. Frequency settings of ±1,5 Hz around nominal frequency and voltage settings of ± 15 % around nominal voltage, for the purposes of this test procedure, should be wide enough to address the majority of utility requirements. Note that as trip settings are widened, more aggressive active anti-islanding schemes may be required that could negatively impact power quality.

Table 5 – Test conditions

Condition	EUT output power, P_{EUT}	EUT input voltage [c]	EUT trip settings [d]
A	Maximum [a]	> 75 % of rated input voltage range	Voltage and frequency trip settings according to National standards and/or local code
B	50 % to 66 % of maximum	50 % of rated input voltage range, ±10 %	Voltage and frequency trip settings according to National standards and/or local code
C	25 % to 33 % [b] of maximum	< 20 % of rated input voltage range	Voltage and frequency trip settings according to National standards and/or local code

[a] Maximum EUT output power condition should be achieved using the maximum allowable input power. Actual output power may exceed nominal rated output.

[b] Or minimum allowable EUT output level if greater than 33 %.

[c] Based on EUT rated input operating range. For example, if range is between X volts and Y volts, 75 % of range = $X + 0{,}75 \times (Y - X)$. Y shall not exceed 0,8 × EUT maximum system voltage (i.e., maximum allowable array open circuit voltage). In any case, the EUT should not be operated outside of its allowable input voltage range.

[d] The manufacturer shall specify the applicable standard, code or utility based trip settings with which the unit shall be tested. The manufacturer may also choose more stringent trip settings to demonstrate compatibility with a greater number of utility requirements. The recommended settings shown below should address the majority of utility requirements.

Parameter	Magnitude	Timing s
Over voltage	115 % of nominal voltage	2
Under voltage	85 % of nominal voltage	2
Over frequency	1,5 Hz above nominal frequency	1
Under frequency	1,5 Hz below nominal frequency	1

If fast over and under voltage and frequency settings are provided, similarly extended values should also be specified by the manufacturer.

a) Determine the EUT test output power, P_{EUT}, to be used from Table 5. Test conditions A, B, and C may be performed in any order convenient to testing.

b) By adjusting the DC input source, operate the EUT at the selected P_{EUT} and measure EUT reactive power output, Q_{EUT}, as follows. The utility disconnect switch S1 should be closed. With no local load connected (that is, S2 is open so that the RLC load is not connected at this time), and the EUT connected to the utility (S1 is closed), turn the EUT on and

2 A loss of one or two phases in a three-phase system is not considered an islanding phenomenon.

operate it at the output determined in step a). Measure the fundamental frequency (50 Hz or 60 Hz) active and reactive power flow, P_{AC} and Q_{AC}. The active power should equal P_{AC}. The reactive power, $Q_{AC,}$ measured in this step is designated Q_{EUT} in the following steps.

NOTE 1 EUT output for condition A is achieved by providing sufficient (excess) input power to allow the unit to produce its maximum output without causing it to shutdown. Condition B is achieved by adjusting the DC input power source, if the EUT provides this mode of operation. Condition C is achieved using inverter control to limit the output power, if the EUT provides this mode of operation.

c) Turn off the EUT and open S1.

When the load component levels are adjusted using real-time measurement of resistive, inductive, and capacitive power levels, it may be necessary to leave S1 closed.

d) Adjust the RLC circuit to have $Q_f = 1{,}0 \pm 0{,}05$[3] using the following steps:

1) Determine the amount of inductive reactance required in the resonant RLC circuit using the relation $Q_L = Q_f \times P_{EUT} = 1{,}0 \times P_{EUT}$.
2) Connect an inductor as the first element of the RLC circuit. Adjust the inductance to Q_L.
3) Connect a capacitor in parallel with the inductor. Adjust the capacitive reactance so that $Q_C + Q_L = -Q_{EUT}$.
4) Connect a resistor that results in the power consumed by the RLC circuit equaling P_{EUT}.

NOTE 2 Active and reactive power are calculated (using the measurements provided in Table 1) for each of the R, L and C legs of the load so that these parasitic parameters (and parasitics introduced by variacs or autotransformers) are properly accounted for when calculating Q_f.

e) Connect the RLC load configured in step d) to the EUT by closing S2. Close S1 and turn the EUT on, making certain that the power output is as determined in step a). Adjust R, L, and C as necessary to ensure that the fundamental (50 Hz or 60 Hz) component of current I_{AC} through S1 is 0,0 A with a tolerance of ±1 % of the rated current of the EUT on a steady state basis in each phase.[4]

The purpose of the procedure up to this point is to zero out the fundamental frequency components (50 Hz or 60 Hz) of active and reactive power, or to zero out the fundamental frequency component of current flow, at the utility disconnect switch. System resonance will typically generate harmonic currents in the test circuit. These harmonic currents will typically make it impossible to zero out an r.m.s. measurement of power or current flow at the disconnect switch. Because of test equipment measurement error and some impact from harmonic currents, it may be necessary to make small adjustments in the test circuit to achieve worst case islanding behavior. Step h) is performed to make these small adjustments.

f) Open the utility-disconnect switch S1 to initiate the test. Run-on time, t_R, shall be recorded as the time between the opening of switch S1 and the point at which the EUT output current drops and remains below 1 % of its rated output levels. Annex C gives some information related to the use of a gate blocking signal.

g) For test condition A in Table 5 (100 %), adjust the active load and only one of the reactive load components (either capacitance, C, or inductance, L, may be chosen) to each of the load imbalance conditions shown in the shaded portion of Table 6. The values in Table 6 represent changes from the nominal values determined in steps d) and e) as a percentage of those nominal values. The values in Table 6 show the active and reactive power flow at S1 in Figure 1, with positive value denoting power flow from the EUT to the AC power source. After each adjustment, an island test is run and run-on time is recorded. If any of

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3 The appropriate value for Q_f was investigated using 723 measurement points in Japan. A value of Q_f was calculated as the ratio of the contract demand (kW) at the measurement point to the installed shunt capacitor (kVAr) needed to make the power factor 1,0 at that point. Based on the variety of load conditions encountered, $Q_f = 1{,}0$ appears to be suitable test condition.

4 Certain anti-islanding algorithms will sufficiently perturb the fundamental frequency current through S1 such that the 1 % limit cannot be achieved on a continuous basis. Averaging of the r.m.s. current over a number of cycles in a manner that captures the quiescent magnitude of this current shall be utilized for the determination of matched load during this quiescent period.

the recorded run-on times are longer than the one recorded for the rated balance condition, i.e. test f), then the non-shaded parameter combinations also require testing. If no run-on time exceeds the one of balance condition, then this part of the test sequence is deemed to be completed.

h) For test conditions B and C, adjust only one of reactive load components (either capacitance, C, or inductance, L, may be chosen) by approximately 1,0 % per test, within a total range of 95 % to 105 % of the operating point as shown in Table 7. The values in Table 7 show the reactive power flow at S1 in Figure 1, with positive value denoting power flow from EUT to AC power source. After each adjustment, an island test is run and run-on time is recorded. If run-on times are still increasing at the 95 % or 105 % points, additional 1 % increments shall be taken until run-on times begin decreasing. Test C load conditions may be achieved using inverter control to limit the output power rather than using the power supply to limit the power.

Table 6 – Load imbalance (real, reactive load) for test condition A (EUT output = 100 %)

% change in active load, reactive load from nominal output power				
–10, +10	–5, +10	0, +10	+5, +10	+10, +10
–10, +5	–5, +5	0, +5	+5, +5	+10, +5
–10, 0	–5, 0		+5, 0	+10, 0
–10, –5	–5, –5	0, –5	+5, –5	+10, –5
–10, –10	–5, –10	0, –10	+5, –10	+10, –10
The numbers in each cell, e.g. +M, +N, are used to represent the % change for active and reactive power. The first number M represents the active power % and the second number N represents the reactive power %. Actual load values shall be within ±1 % of those specified.				

Table 7 – Load imbalance (reactive load) for test condition B (EUT output = 50 % to 66 %) and test condition C (EUT output = 25 % to 33 %)

% change in active load, reactive load from nominal output power
0, –5
0, –4
0, –3
0, –2
0, –1
0, 1
0, 2
0, 3
0, 4
0, 5
In Table 7 the numbers in each box, e.g. +M, +N, are used to represent the % change for active and reactive power. The first number M represents the active power % and the second number N represents the reactive power %. Actual load values shall be within ±1 % of those specified.

6.2 Pass/fail criteria

An EUT is considered to comply with the requirements for islanding protection when each case of recorded run-on time is less than 2 s or meets the requirements of local codes.

7 Documentation

At a minimum, the following information shall be recorded and maintained in the test report.

a) Specifications of EUT. Table 8 provides an example of the type of information that should be provided.
b) Measurement results. Table 9 provides an example of the type of information that should be provided. Actual measured values should be recorded.
c) Block diagram of test circuit.
d) Specifications of the test and measurement equipment. Table 10 provides an example of the type of information that should be provided.
e) Any test configuration or procedure details such as methods of achieving specified load and EUT output conditions.
f) Any additional information required by the testing laboratory's accreditation.
g) Specify the evaluation criterion from 6.2 that was utilized to determine if the product passed or failed the test.

Table 8 – Specification of the EUT provided by the manufacturer (example)

Parameter	Value	Remarks
1) Rating		
a) Maximum output power		
b) DC voltage range		
c) DC current limits		
d) AC voltage range		
e) Frequency range		
f) AC current limits		
g) Efficiency		
h) Voltage and frequency trip settings (magnitude and timing)		
i) Other software settings		
j) Firmware version		
2) Others		
a) Displays		
b) Temperature range		
c) Humidity		
d) Size		
e) Weight		

Table 9 – List of tested condition and run on time (example)

No.	P_{EUT} [a] (% of EUT rating)	Reactive load (% of Q_L in 6.1d)1))	P_{AC} [b] (% of nominal)	Q_{AC} [c] (% of nominal)	Run on time (ms)	P_{EUT} (W)	Actual Q_f	V_{DC}	Remarks [d]
1	100	100	0	0					Test A at BL
2	66	66	0	0					Test B at BL
3	33	33	0	0					Test C at BL
4	100	100	–5	–5					Test A at IB
5	100	100	–5	0					Test A at IB
6	100	100	–5	+5					Test A at IB
7	100	100	0	–5					Test A at IB
8	100	100	0	+5					Test A at IB
9	100	100	+5	–5					Test A at IB
10	100	100	+5	0					Test A at IB
11	100	100	+5	+5					Test A at IB
12	66	66	0	–5					Test B at IB
13	66	66	0	–4					Test B at IB
14	66	66	0	–3					Test B at IB
15	66	66	0	–2					Test B at IB
16	66	66	0	–1					Test B at IB
17	66	66	0	1					Test B at IB
18	66	66	0	2					Test B at IB
19	66	66	0	3					Test B at IB
20	66	66	0	4					Test B at IB
21	66	66	0	5					Test B at IB
22	33	33	0	–5					Test C at IB
23	33	33	0	–4					Test C at IB
24	33	33	0	–3					Test C at IB
25	33	33	0	–2					Test C at IB
26	33	33	0	–1					Test C at IB
27	33	33	0	1					Test C at IB
28	33	33	0	2					Test C at IB
29	33	33	0	3					Test C at IB
30	33	33	0	4					Test C at IB
31	33	33	0	5					Test C at IB

[a] P_{EUT}: EUT output power.

[b] P_{AC}: Active power flow at S1 in Figure 1. Positive means power from EUT to utility. Nominal is the 0 % test condition value.

[c] Q_{AC}: Reactive power flow at S1 in Figure 1. Positive means power from EUT to utility. Nominal is the 0 % test condition value.

[d] BL: balance condition, IB: imbalance condition.

Table 10 – Specification of testing equipment (example)

Items	Specifications	Remarks
1) DC power source (or PV array simulator)		
a) Voltage range	0 to 400,0 V (0,1 V step)	
b) Current range	0 to 30,0 A (0,1 A step)	
2) AC power source		
a) Output wiring	Single phase, 3 wires	
b) Output capacity	16 kVA	
c) Output voltage (accuracy)	0 V_{rms} to 576 V_{rms} (0,2 V_{rms})	
d) Output frequency (accuracy)	5 Hz to 1 100 Hz (0,01 Hz)	
e) Voltage stability	±100 ppm/°C (typical) ±100 ppm/8 h (typical)	
f) Output voltage distortion	0,05 % max.	
3) Digital meter		
a) Voltage range	15/30/60/150/300/600 V	
b) Current range	0,5/1/2/5/10/20 A	
c) Frequency range (accuracy)	DC, 10 Hz to 50 kHz (0,5 %)	
d) Measurement items	Voltage (V) Current (A) Active power (W) Reactive power (VAr) Volt-ampere (VA) Power factor (PF) Frequency (Hz) Electric energy (Wh)	
4) Waveform recorder		
a) Sampling speed	100 ksample/s	
b) Recording device	Thermal printer	
c) Time accuracy	±500 ppm (typical)	
5) AC load		
a) Resistive load		
Maximum voltage	250 V (DC or AC)	
Current range	2,5 to 50 A (0,3 Ω step)	
Capacity	10 kVA	
b) Inductive load		
Maximum voltage	250 V (DC or AC)	
Current range	2,5 to 50 A (0,3 Ω step)	
Capacity	10 kVA	
c) Capacitive load		
Maximum voltage	200 V	
Current range	0,2 to 50 A	

Annex A
(informative)

Islanding as it applies to PV systems

A.1 General

Islanding is a condition in which a portion of an electric power grid containing both load and generation is isolated from the remainder of the electric power grid. An unintentional island occurs when the generation powering the load is not under the control of the authorities responsible for regulating the power (voltage, frequency, etc.), and when such generation is not intended (approved) to power the load. For example, while a customer-owned PV system may be designed to operate the customer's local loads when the power from the public power system (i.e. utility) is unavailable, it is typically not allowed to attempt to power other customers.

Loss of public power can occur for a number of reasons:

– as a result of a fault that is detected by the public power company, causing a disconnecting device to operate,
– accidental opening of the normal public power source by equipment failure,
– utility switching of the distribution system and loads,
– human error or malicious mischief,
– act of nature.

Unintentional islanding by a customer generator should be avoided for reasons including the following:

– Because the public power company cannot control voltage and frequency in the island, there is the possibility of damage to customer equipment in a situation over which the public power company has no control. The public power company, along with the customer generator, can be found liable for electrical damage to customer equipment connected to their lines that is the result of voltage or frequency excursions outside of the acceptable ranges.
– Islanding may interfere with the restoration of normal service by the public power company.
– Islanding may create a hazard for utility line-workers by causing a line to remain energized when it is assumed to be disconnected from all energy sources.
– Reclosing into an island may result in re-tripping the line or damaging the distributed resource equipment, or other connected equipment, because of out-of-phase closure.

Most islands can be easily avoided by monitoring public power system voltage and frequency and only allowing inverter operation when these parameters are within acceptable limits. It is possible, however, that the power supplied by a customer generator (or a collection of such generators) matches the load so closely that voltage and frequency limits would not be exceeded if the system were islanded, as discussed in Begovic *et al*[5]. Unless other means are incorporated into the controls, a system could operate as long as the generation and load remain relatively matched. Although this situation is extremely unlikely, it remains a concern. There is, therefore, a need for additional controls to detect unintentional islanding conditions and remove the PV system from the circuit until the public power system is restored to normal service.

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5 Begovic, M., Ropp, M., Rohatgi, A., Pregelj, A., "Determining the Sufficiency of Standard Protective Relaying for Islanding Prevention in Grid-Connected PV Systems," *Proceedings of the 2nd World Conference and Exhibition on Photovoltaic Solar Energy Conversion*, Vienna, Austria, July, 1998.

Tightening voltage and frequency windows has been suggested as a means to eliminate this problem, but this only reduces the probability of an island occurring, rather than eliminating the possibility. Tightening operating windows also increases the occurrence of nuisance tripping.

A more satisfactory solution to the problem of detecting a balanced unintentional island is the use of an inverter that incorporates a task-specific anti-islanding scheme that includes the measurement of other parameters or methods of destabilizing the grid in the absence of public power control.

A.2 Impact of distortion on islanding

The islanded load total demand distortion (TDD [6]) has an impact on the probability of establishing a distributed resource island. Increased distortion can have several results that impact the ability of an inverter to operate. These include additional voltage zero crossings and reduced total power factor. An inverter that has been designed to operate at unity power factor and low distortion will not continue operating with high load distortion.

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6 TDD, total demand distortion, is defined in IEEE 519-1992 as the total root-sum-square harmonic distortion, in percent of the maximum demand total load current (15 min or 30 min demand).

Annex B
(informative)

Test for independent islanding detection device (relay)

B.1 General

There are cases where the islanding protection system (EUT) is separate from the inverter. When the system employs an active method of islanding detection that interacts with a specific inverter, the test method described in the main body of this standard shall be employed. If an island detection method is used that does not rely on interaction with the inverter, the procedure described below may be used.

B.2 Testing circuit

The testing circuit shown in Figure B.1 shall be employed. Similar circuits shall be used for three-phase output.

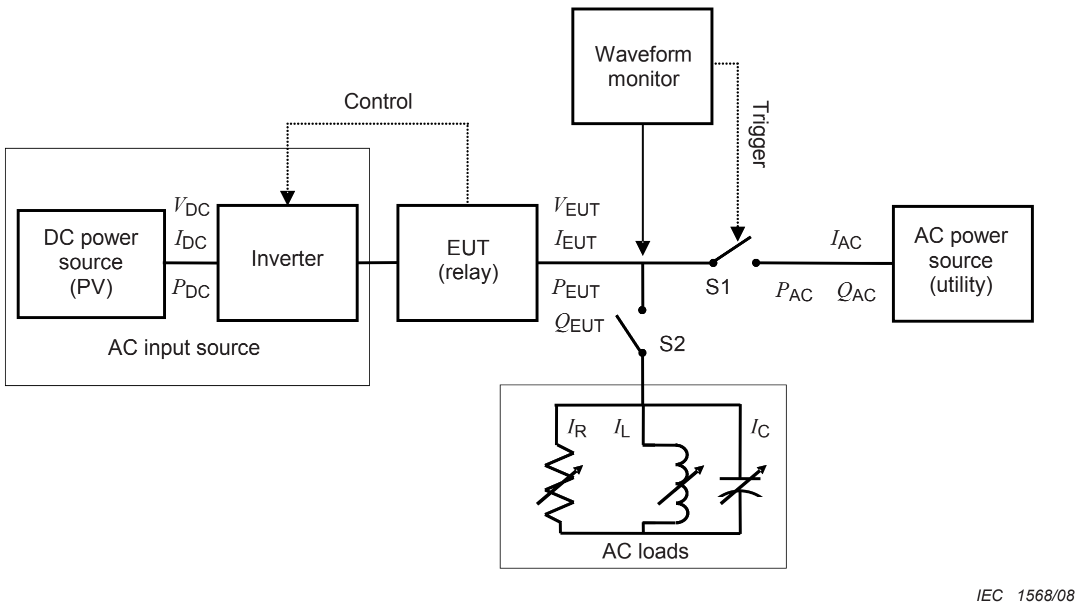

Figure B.1 – Test circuit for independent islanding detection device (relay)

B.3 Testing equipment

B.3.1 General

Same as Clause 5 with the exception of the AC input source described below and acting in place of the DC input source with an inverter in terms of power generation.

B.3.2 AC input source

A separate AC input may be required if not provided by the EUT manufacturer as part of the test as shown Figure B.1.

The AC input source shall provide voltage and current necessary to meet the testing requirements described in Clause 6.

B.4 Testing procedure

This test procedure provides a method for evaluating an independent islanding detection device, such as a relay. As in 6.1, this test procedure develops a resonant circuit that is balanced with the PV system output. Since, in this case, the EUT has no generation capability of its own, a separate AC source shall be used to provide power on the EUT side of switch S1, as shown in Figure B.1. This AC source shall be capable of providing the rated power defined by the EUT rating. If the EUT affects the islanding detection feature by controlling the AC power source, then the test setup shall include the appropriate functionality in the AC source and the connection between the source and the EUT.

B.5 Documentation

Same as Clause 7.

Annex C
(informative)

Gate blocking signal

C.1 General

A stopping signal is one that provides an indication that the EUT has ceased energizing the utility grid. One form of stopping signal, provided in some utility-interconnected inverters, is the gate blocking signal as described in Annex C. Some jurisdictions may require that all inverters provide a gate blocking signal that can be measured directly.

C.2 Gate blocking signal used in photovoltaic systems

Utility-interconnected inverters for PV systems convert DC power into AC power, performing PWM control[7] using semiconductor-based power switching devices such as IGBTs[8], thyristors, and GTOs[9]. In many cases, an on-off "gate blocking" signal is provided by the control circuitry between the microprocessor and the power switching device. This signal provides a means for separate control functions (e.g., internal fault monitoring, utility voltage and frequency trip functions) to halt the operation of the switching devices and therefore the power generation of the inverter. When this signal is in the active blocking state, the inverter will cease generating power. Thus, this signal provides an indication of a tripping action such as the end of the islanding event. Run-on time can then be defined as the time between the opening of the islanding test switch and the point when the gate blocking signal indicates a stop condition.

C.3 Monitoring the gate blocking signal

In some inverter designs the control circuit comprises discrete components so a gate blocking signal is accessible and easily measured.

In other inverter designs, a micro-processor drives the switching device directly, so all control and monitoring functions are handled by the microprocessor, which simply stops firing the switching device when necessary. In this case there may be no external gate blocking signal. Also, so called smart-switching devices incorporate control (microprocessor) and power switching functions in a single sealed package with no access to the internal control signals. Finally, inverters incorporating battery backup may not cease the operation of the bridge, but, to maintain operation of critical loads isolated from the utility connection, will instead open a switch to isolate the inverter from the utility grid. Other signals available in these designs may include some uncertainty (e.g., a delay) as to when the switching device actually ceases operation.

It should be noted that while the gate blocking signal will indicate when the power switching device has ceased operation, the inverter will not instantly cease energizing its output terminals. The unit will provide a decaying AC output, the characteristics of which will depend on the design of the reactive components on the inverter output. Therefore, the most accurate indication that the inverter has ceased energizing its output is to monitor the output current and verify that they have dropped below expected levels, as described in 6.1, step f).

---

7 PWM control: pulse width modulation control.

8 IGBTs: insulated gate bipolar transistors.

9 GTOs: gate turn-off thyristors.

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IEC 61727:2004, *Photovoltaic (PV) systems – Characteristics of the utility interface*

IEEE 519-1992, *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*

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