BS EN 61988-1:2011

BSI Standards Publication

Plasma display panels

Part 1: Terminology and letter symbols

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National foreword

This British Standard is the UK implementation of EN 61988-1:2011. It is identical to IEC 61988-1:2011. It supersedes BS EN 61988-1:2003 which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

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CENELEC

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Europäisches Komitee für Elektrotechnische Normung

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Foreword

The text of document 110/236/CDV, future edition 2 of IEC 61988-1, prepared by IEC/TC 110, Flat panel display devices, was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 61988-1:2011.

This document supersedes EN 61988-1:2003.

EN 61988-1:2011 includes the following significant technical changes with respect to EN 61988-1:2003:

– Additional terms were added in Clause 3.

The following dates are fixed:

– latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2012-05-30
– latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2014-08-30

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

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Endorsement notice

The text of the International Standard IEC 61988-1:2011 was approved by CENELEC as a European Standard without any modification.

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Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 61988-2-1	201X[1)]	Plasma display panels - Part 2-1: Measuring methods - Optical and optoelectrical	EN 61988-2-1	201X[1)]

[1)] At draft stage.

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

PLASMA DISPLAY PANELS –

Part 1: Terminology and letter symbols

FOREWORD

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International Standard IEC 61988-1 has been prepared by IEC technical committee 110: Flat panel display devices.

This second edition cancels and replaces the first edition published in 2003, and constitutes a technical revision. The main technical changes with regard to the previous edition are as follows:

– Additional terms were added in Clause 3.

The text of this standard is based on the following documents:

CDV	Report on voting
110/236/CDV	110/286/RVC

Full information on the voting for the approval on this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 61988 series, under the general title *Plasma display panels*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

PLASMA DISPLAY PANELS –

Part 1: Terminology and letter symbols

1 Scope

This part of IEC 61988 gives the preferred terms, their definitions and symbols for colour AC plasma display panels (AC PDP); with the object of using the same terminology when publications are prepared in different countries. Guidance on the technology is provided in the annexes.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61988-2-1:–, *Plasma display panels – Part 2-1: Measuring methods – Optical and optoelectrical*[1]

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
AC PDP

NOTE See AC plasma display panel.

3.2
AC plasma display panel
AC PDP
plasma display panel in which the gas discharge region is insulated from the electrodes that are driven with AC voltage pulses

3.3
address bias
Vba
data bias
common voltage applied to all address electrodes during addressing

3.4
address cycle period
time interval between initiation of the closest spaced successive address pulses

3.5
address discharge
discharge that changes the state of a PDP subpixel

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1 Second edition, to be published.

3.6
address electrode
data electrode
electrode, orthogonal to the scan electrode, that is used in driving the subpixels with the image data

3.7
address period
time interval including the reset step and the address step

3.8
address pulse
data pulse
incremental voltage pulse applied to a single address (data) electrode for addressing, to select a subpixel according to an image to be displayed

NOTE See scan pulse.

3.9
address step
time interval needed to address all pixels in the panel in a given subfield as applied to the ADS method

3.10
address voltage
Va
data voltage
amplitude of the voltage pulses applied to the address (data) electrode during addressing (excludes the address bias on the electrode)

3.11
address while display method
AWD method
grey scale drive technique that addresses only a portion of the pixels of the panel in any time within a sustain period

NOTE See also ADS.

3.12
addressability
number of pixels in the horizontal and vertical directions, that can have their luminance changed

NOTE Usually expressed as the number of horizontal pixels by the number of vertical pixels. This term is not synonymous with resolution. See resolution.

3.13
addressing
setting or changing the state of a subpixel with an address pulse

3.14
ADS method
address, display-period separation method
grey scale drive technique that consists of addressing all the pixels in the panel in one time period and sustaining all the pixels in the panel in a separate time period

3.15
ageing
manufacturing process consisting of operating the panel under conditions that stabilize its performance

3.16
annealing
process of heating the glass above its annealing point and cooling at a controlled rate to minimize dimensional changes during subsequent high temperature cycles

3.17
anode
positively charged surface of a device that collects electrons from the discharge

NOTE In an AC PDP, the cathode and anode exchange their roles on alternate half-cycles.

3.18
APL
average picture level
time average of a video signal during the active scanning time integrated over a frame period, which is expressed as a percentage of the full white signal level while designating 0 % as the black signal level

NOTE There are two types of APL. See pre-gamma APL and post-gamma APL.

3.19
aspect ratio
ratio of screen width to screen height

3.20
auto power control
APC
circuit means to control the peak and/or average power of the display

3.21
auxiliary anode
anode in a DC PDP whose discharge contributes to supply priming particles to ignite a discharge in a cell

3.22
back plate
rear plate
plate furthest from the viewer

3.23
back-filling

NOTE See filling.

3.24
bake

NOTE See bakeout and baking.

3.25
bakeout
high temperature processing of a vacuum system and/or PDP to assist in achieving low pressures

3.26
baking
high temperature process used to evaporate water and decompose organic materials

NOTE Baking is used to clean the parts by dispersing unwanted material into the atmosphere.

3.27
barrier rib
rib that separates the cells of the panel, electrically, optically and physically

NOTE The barrier ribs may extend from the front plate to the back plate and control the spacing between the plates.

3.28
binder burnout
process during which organic binders are remove by decomposition and/or oxidation

3.29
black level luminance
luminance of the panel in its minimum luminance state in a dark ambient

NOTE See 6.3.3.3 of IEC 61988-2-1:– (Ed. 2).

3.30
black matrix
black material placed in the space between subpixel areas in order to improve contrast by reducing reflectivity

3.31
black stripe
black material placed in the space between subpixel areas in order to improve contrast by reducing reflectivity, having the form of stripes

NOTE Black stripe is a specific type of black matrix contrast enhancement.

3.32
black uniformity, sampled
uniformity of the black level luminance expressed in terms of the percentage non-uniformity (difference in luminance between measuring points divided by the average black level luminance) at the specified measuring points

3.33
***BRCR*-#/#**

NOTE See bright room contrast ratio #/#.

3.34
breakdown voltage
smallest voltage between the cathode and the anode causing a gas discharge to grow to a breakdown condition

3.35
bright defect
defect in the image reproduction that appears brighter than the correct image

3.36
bright room contrast ratio #/#
***BRCR*-#/#**
contrast ratio with ambient illumination on the screen other than the nominal 100/70 levels

NOTE The symbol #/# describes the ambient illumination on the vertical plane/horizontal plane (see 6.4 of IEC 61988-2-1:– (Ed. 2)).

3.37
bright room contrast ratio 100/70
***BRCR*-100/70**
contrast ratio with an ambient illumination on the screen of 100 lx on the vertical plane and 70 lx on the horizontal plane

NOTE See 6.4 of IEC 61988-2-1:– (Ed. 2).

3.38
brightness
visual and subjective quality of how bright an object appears, or how much visible light is coming off the object being perceived by the eye

NOTE See luminance.

3.39
bulk erase

NOTE See full-screen erase.

3.40
bulk write

NOTE See full-screen write.

3.41
burn-in
process of increasing the reliability performance of hardware employing functional operation of every item in a prescribed environment with successive corrective maintenance at every failure during the early failure period

3.42
bus electrode
high conductivity electrode intimately connected along its length to the transparent electrode in order to reduce total resistance

3.43
cathode
negatively charged surface of a device that emits secondary electrons to the discharge

NOTE In an AC PDP, the cathode and anode exchange their roles on alternate half-cycles.

3.44
cell
physical structure of a subpixel or a subpixel itself (adjective – referring to the characteristics of a single cell)

3.45
cell defect
cell showing a dark defect or a bright defect, or an unstable cell

3.46
cell pitch
subpixel pitch

3.47
cell voltage
Vc
time-dependent voltage across the gas in a plasma display cell

3.48
centre firing voltage
average of the first-on voltage and the last-on voltage

3.49
centre minimum sustain voltage
average of the first-off voltage and the last-off voltage

3.50
chromatic uniformity
uniformity of the chromaticity produced by different areas of the screen

3.51
closed rib
rib structure which has walls on all sides of the cell

NOTE Examples are box type, mesh type, waffle type, hexagonal type, honeycomb type, etc. It is permissible to have different rib heights on each side.

3.52
column electrode
address electrode

NOTE The column electrode was historically continuous in the vertical direction. When the panel is oriented in portrait orientation, the column electrode can be aligned horizontally. See row electrode.

3.53
contrast ratio
ratio of white luminance to black luminance of the image, including light reflected from the display

NOTE This ratio is strongly dependent on the ambient light and two forms are reported, bright room contrast ratio (BRCR) and dark room contrast ratio (DRCR). See 6.3 and 6.4 of IEC 61988-2-1:–, Ed. 2.

3.54
contrast ratio, sampled
CR
ratio of a white luminance to a black luminance at the specified measuring points

NOTE See 6.3 and 6.4 of IEC 61988-2-1:– (Ed. 2).

3.55
coplanar PDP

NOTE See surface discharge PDP.

3.56
crosstalk
phenomenon initiated by a discharge in one cell that causes an unwanted discharge in a neighbouring cell

3.57
dark defect
defect in the image reproduction that appears less bright than the correct image

3.58
dark room contrast ratio
DRCR
contrast ratio measured in a dark room ambient, typically less than 1 lx

NOTE See 6.3 of IEC 61988-2-1:– (Ed. 2).

3.59
data bias

NOTE See address bias.

3.60
data electrode

NOTE See address electrode.

3.61
data pulse

NOTE See address pulse.

3.62
data voltage

NOTE See address voltage.

3.63
DC PDP

NOTE See DC plasma display panel.

3.64
DC plasma display panel
DC PDP
plasma display panel in which the conductive electrodes are directly in contact with the gas discharge

3.65
dielectric layer
layer or layers of non-conductive material that cover the electrodes, on which charges are accumulated from the discharge

NOTE The accumulated charge allows the memory function in AC PDPs.

3.66
dielectric voltage
Vd
voltage across a dielectric layer due to the wall charge that usually varies with time

$$Vd = Qw/Cd$$

where Qw is the wall charge and Cd is the effective dielectric layer capacitance

NOTE Charges other than wall charges may also appear on the dielectric surfaces, so that the total voltage across a dielectric can be greater than its dielectric voltage.

3.67
diffuse reflection
diffusion by reflection in which, on the macroscopic scale, there is no regular reflection

3.68
direct laminated filter
front optical filter attached directly to the front of the panel

3.69
discharge current
component of current of a gas discharge resulting from the flow of electrons and ions in the gas

3.70
discharge delay time
formative delay plus statistical delay

NOTE When applying the addressing waveform, the peak of the discharge in an AC PDP generally occurs after the statistical delay plus the formative delay.

3.71
displacement current
current flowing through the capacitance of a plasma display panel resulting from the changing voltage applied to the electrodes

NOTE Does not include the discharge current.

3.72
display anode
anode electrode of a DC PDP that is driven with positive DC voltage for the display discharge

3.73
display diagonal
screen diagonal
diagonal dimension of the addressable screen area

3.74
display electrode
scan and/or sustain electrodes in a three-electrode type PDP that provide the principal power for the plasma discharge

3.75
display period
time interval of a subfield other than the address period where all of the sustain pulses in a given subfield are applied to the panel

NOTE This term is only used for the ADS method.

3.76
driving waveform
time-dependent voltage of a driving signal

3.77
drying process
manufacturing process that removes water and other volatile materials from the PDP sub-assemblies

NOTE This often involves heating in an oven.

3.78
dynamic false contour
phenomenon wherein moving images create false contours

3.79
dynamic margin
margin that remains when addressing is active

NOTE This term can be applied to various margins such as sustain margin or write margin, etc.

3.80
dynamic sustain range
sustain voltage range that allows proper addressing of all pixels over the entire range of write voltage

3.81
efficacy

NOTE See luminous efficacy.

3.82
energy recovery circuit
circuitry that recaptures the reactive power of the plasma display panel capacitance by means of an inductance

3.83
erase
operation that generates a discharge, generally between the address and scan electrodes, to set subpixels to an off state

3.84
erase margin
ΔVer
erase voltage range that allows proper addressing of all pixels at the specified operating conditions

3.85
erase pulse
voltage waveform applied to an electrode pair to selectively change the state of a subpixel from on to off

3.86
erase voltage
Ver
voltage of the erase waveform applied between the electrode pair that receives the erase pulse

3.87
erase waveform
time-dependent voltage signal applied to an electrode pair to selectively change the state of a subpixel from on to off

NOTE The erase wave form includes the address bias, the scan bias, the address pulse and the scan pulse.

3.88
evacuating
manufacturing process of removing the atmospheric gases by a vacuum process

3.89
exhaust tube
exhaust tubulation
exhaust pipe
tubular port in the device envelope that is connected to an external vacuum pump to evacuate the air from the device during processing

NOTE This is typically a glass tube that can be closed after filling with the appropriate gas by melting.

3.90
exoemission
delayed spontaneous emission of electrons from the cathode due to earlier excitation by the gas discharge particles such as electrons, ions and ultraviolet photons

NOTE Exoemission from the cathode surface such as MgO typically decays slowly after the excitation event and can continue at low current levels for times as long as seconds, minutes or even hours. The exoemission current also usually depends on the temperature of the cathode and the amount of initial gas discharge excitation.

Exoemission is very important for priming addressing discharges and it frequently has a major impact on the maximum reliable addressing rate.

3.91
field
time interval during which a subset of all of the pixels is addressed and sustained at the full range of grey levels

NOTE See subfield.

EXAMPLE: In the case of an interlaced display, half of the pixels are addressed during the odd field and the other half are addressed during the even field.

3.92
filling
process of filling the panel with gas after evacuating all of the air

3.93
firing
high temperature manufacturing process where various materials mixed with glass frit are heated to make electrodes, barrier ribs or dielectric layers, etc.

NOTE The heating is used to sinter the glass frit.

3.94
firing voltage
Vf
smallest sustain voltage at which a sustain discharge sequence spontaneously starts in a cell

NOTE Not to be confused with the breakdown voltage. Typically, cells have slightly different firing voltages.

3.95
firing voltage range
ΔVf
range of sustain voltages between the first-on voltage and the last-on voltage or the difference in voltage between the two

3.96
first-off
cell which turns off at the largest sustain voltage as the sustain voltage is decreased

NOTE Defective cells are ignored.

3.97
first-off voltage
Vsm_n
sustain voltage for first-off

3.98
first-on
cell which turns on at the smallest sustain voltage as the sustain voltage is increased

NOTE Defective cells are ignored.

3.99
first-on voltage
Vf_1
minimum firing voltage
sustain voltage for first-on

3.100
formative delay
t_f
time between the initiating priming particle event and the peak of the discharge when measured in an AC PDP, or the time between the initiating priming particle event and the time when the gas discharge current rises to one half of the final steady state discharge current when measured in a DC PDP

NOTE When applying the addressing waveform, the peak of the discharge in an AC PDP generally occurs after the statistical delay plus the formative delay.

3.101
frame
period during which all of the pixels in the panel are addressed

3.102
front optical filter
transparent filter mounted on the front of a panel directly or separately to reduce the ambient light reflection, to enhance colour reproduction by the colour and colour density of the filter, to reduce IR emission from the panel, to reduce EMI by the electrical conductivity of the filter, to improve the mechanical strength of the module and so on

3.103
front plate
transparent plate facing the viewer

3.104
full-colour display
display capable of showing at least 3 primary colours, the colour gamut of which includes a white area (e.g. containing D50, D65, D75) and having at least 64 grey scale per primary

3.105
full-screen erase
bulk erase
operation of applying a voltage waveform to the panel that switches all of the cells in the panel to the off state

3.106
full-screen write
bulk write
operation of applying a voltage waveform to the panel that switches all of the cells in the panel to the on state

3.107
gap
distance in the gas between the anode and the cathode

NOTE The relevant gaps within the PDP are the sustain gap, the plate gap and the interpixel gap.

3.108
gas
normally neutral, but ionizable atmosphere, that fills the PDP

NOTE It is typically a mixture of various inert gaseous elements, such as xenon, neon and helium.

3.109
gas discharge
phenomenon in a gas accompanied with light emission and significant current flow

3.110
gas mixture
composition of the gas inside the PDP

NOTE This is typically expressed as the partial pressure percentages of the constituent gasses.

3.111
glass filter
glass based front optical filter which is not directly bonded to the panel

3.112
half-select
applied drive level to non-selected cells that lie along the address or scan electrodes performing an addressing (write or erase) operation

3.113
high strain point glass
glass that has a strain point (the temperature at which the viscosity is $10^{13,5}$ Pa-s) that is relatively high, and shows little compaction or deformation at temperatures of the thermal processes

3.114
image retention
continued presence of a weak image (or its inverse) after a bright image is removed

NOTE It disappears after a few minutes operation.

3.115
image shadowing
reduction in luminance of the white surround of a black object, extending horizontally or vertically from the black object

3.116
image smear
noticeable tail on a moving object caused by a slow decay of light emission from the phosphor

NOTE May be a different colour than that of the moving object when the decay times of the various phosphors are different.

3.117
image sticking
long-time remnant of an image on the screen after the image signal is changed

3.118
image streaking
variance in luminance with changing vertical or horizontal line load

3.119
interconnect pad
single electrode at the edge of a PDP that is used for connection to external circuits

3.120
interconnect pad group
group of interconnect pads that attaches to a single connector

3.121
interconnect pad group spacing
width of the non-conductive area between adjacent interconnect pad groups

3.122
interconnect pad pitch
distance between the centre of the pads of an interconnect pad group

3.123
interconnect pad spacing
dimension of the non-conductive area between the individual interconnect pads

3.124
interconnect pad width
width of the interconnect pad

3.125
interpixel gap
gap between a sustain or scan electrode of one pixel and an adjacent sustain or scan electrode of another pixel

3.126
ion bombardment
impact of energetic ions on a solid surface

NOTE The transfer of energy from the ion to the surface may cause electron, ion or neutral emission and chemical or thermal changes in the surface. These changes may result in permanent damage to the protecting layer of an AC PDP, the cathode electrode of a DC PDP and the phosphor in any PDP.

3.127
last-off
last cell which turns off as the sustain voltage is decreased

NOTE Defective cells are ignored.

3.128
last-off voltage
Vsm_1
sustain voltage for last-off

3.129
last-on
last cell to turn on as the sustain voltage is increased

NOTE Defective cells are ignored.

3.130
last-on voltage
Vf_n
maximum firing voltage
sustain voltage for last-on

3.131
lateral discharge PDP
type of PDP in which the sustain discharge occurs between the two lateral walls of the cell and not on a surface

NOTE The anode and the cathode are on different lateral walls. The axis of the discharge, directly between the cathode and the anode, is orthogonal to the plate gap.

3.132
lifetime
time period during which a device continues to function, often further qualified as luminance lifetime or operating lifetime

3.133
low melting point glass
glass that has a softening point (the temperature at which the viscosity of the glass is approximately $4{,}5 \times 10^6$ Pa-s) that is relatively low

NOTE Glass, being amorphous and not crystalline, does not “melt” but becomes progressively more fluid as it becomes hotter.

3.134
luminance deviation
ΔL_i
difference in luminance in the measured points compared to the average luminance

3.135
luminance lifetime
time period during which the device continues to function at 50 % or more of its initial luminance

3.136
luminance maintenance
ratio of the current luminance to the initial luminance

3.137
luminance uniformity
uniformity of luminance produced by different areas of the PDP

NOTE Usually expressed in the inverse sense of the non-uniformity, or the difference in luminance at specified measuring points as a percentage of the average luminance. See 6.2 of IEC 61988-2-1:– (Ed. 2).

3.138
luminous efficacy
panel luminous efficacy
η
incremental luminous flux (measured as the luminous flux of a white display minus the luminous flux of a black display) divided by the incremental power input applied to the sustain driver for operating the panel (measured as the white display power minus the black display power)

NOTE Expressed in lumens/watt. See also module luminous efficacy and power cord efficiency.

3.139
luminous efficiency
efficiency of visible light power produced only from the sustain power applied to the gas discharge

NOTE This is expressed as a percentage (often misapplied to luminous efficacy).

3.140
magnesium oxide
MgO
protective layer material that has a high secondary electron emission yield

NOTE This is the most common material used for this purpose.

3.141
margin
voltage range over which proper operation is achieved

NOTE The important margins are the sustain margin and the write margin. See also static margin and dynamic margin.

3.142
matrix PDP
plasma display panel organised as a matrix of cells in rows and columns

3.143
maximum dynamic sustain voltage limit
maximum sustain voltage over the entire range of write voltage that allows proper addressing of all pixels

3.144
maximum firing voltage
Vf_n

NOTE See last-on voltage.

3.145
maximum sustain voltage
Vs_{max}
largest sustain voltage that allows proper addressing of all pixels at the specified operating conditions

3.146
maximum write voltage
Vwr_{max}
largest write voltage that allows proper addressing of all pixels at the specified operating conditions

3.147
maximum write voltage limit
largest write voltage over the entire range of sustain voltages that allows proper addressing of all pixels

3.148
memory coefficient
α_M
ratio of two times the memory margin to the firing voltage defined as

$$\alpha_M = 2(Vf - Vsm)/Vf$$

where Vf is the firing voltage and Vsm is the minimum cell sustain voltage

3.149
memory margin
ΔVmm
difference of the firing voltage and the minimum cell sustain voltage for a single cell

3.150
memory type PDP
reference to a plasma display panel that has a memory effect

NOTE The cells which are on, continue to be in the on-state and cells which are in the off-state, remain off (until switched).

3.151
minimum cell sustain voltage
Vsm
smallest sustain voltage that maintains the sustain discharge sequence in a cell

NOTE Typically, cells have slightly different minimum cell sustain voltages.

3.152
minimum dynamic sustain voltage limit
minimum sustain voltage over the entire range of write voltage that allows proper addressing of all pixels

3.153
minimum firing voltage
Vf_1

NOTE See first-on voltage.

3.154
minimum luminance
luminance of the display when displaying a black image with the power on

NOTE See 6.3.3.3 and 6.4.4.3 of IEC 61988-2-1:– (Ed. 2).

3.155
minimum sustain voltage
Vs_{min}
smallest sustain voltage that allows proper addressing of all pixels at the specified operating conditions

3.156
minimum sustain voltage range
ΔVsm
range of sustain voltages between the first-off voltage and the last-off voltage or the difference in voltage between the two

3.157
minimum write voltage
Vwr_{min}
smallest write voltage that allows proper addressing of all pixels at the specified operating conditions

3.158
minimum write voltage limit
smallest write voltage over the entire range of sustain voltages that allows proper addressing of all pixels

3.159
module
plasma display device including electronic sub-assemblies

3.160
module luminous efficacy
η_m
luminous flux of a full-screen white display without any external contrast enhancement filter divided by the total power consumption of the module

NOTE See 6.9 of IEC 61988-2-1:– (Ed. 2).

3.161
module luminous efficiency
efficiency of visible light power produced in a module having a full-screen white display without any external contrast enhancement filter, divided by the total power consumption of the module

3.162
monochrome PDP
PDP with a fixed colour hue, typically neon orange

3.163
moving picture resolution
number of picture lines on the display screen corresponding to the resolution limit of the visibility of moving pictures

NOTE Moving picture resolution is not determined only by the physical pixel number of the panel but also by the moving picture performance in terms of motion artifacts. The resolution is expressed in picture lines in the document and it can be easily converted to well known TV lines.

3.164
multi-colour display
display with the capability to produce multiple colours, but typically not having a full-colour capability

3.165
mura
anomalous non-uniformity of the reproduced image

3.166
off-cell
cell in the off-state

3.167
off-state
state of a cell which does not discharge while being excited by the sustain waveform

3.168
on-cell
cell in the on-state

3.169
on-state
state of a cell which discharges on every half-cycle of the sustain waveform

3.170
operating lifetime
time period during which a device meets its functions satisfactorily

3.171
operating window
multidimensional range of voltages that allows proper addressing of all pixels

3.172
opposed discharge PDP
two-electrode type PDP geometry in which the discharge occurs between the electrodes located on opposite plates

3.173
panel
plasma display device excluding its electronic sub-assemblies

3.174
panel luminous efficacy
luminous efficacy
η
incremental luminous flux (measured as the luminous flux of a white display minus the luminous flux of a black display) divided by the incremental power input applied to the sustain driver for operating the panel (measured as the white display power minus the black display power)

NOTE Expressed in lumens/watt. See also module luminous efficacy and power cord efficacy.

3.175
peak luminance
maximum luminance value of the screen

3.176
phosphor baking
thermal process during which the organic binders in the phosphor layer are decomposed and solvents evaporated

3.177
phosphor burn-in
image that continues to be visible after the stimulus for that image is removed, caused by the phosphor degradation

NOTE Phosphor burn-in does not disappear. Burn-in is not used in the sense of definition 3.41.

3.178
phosphor degradation
gradual reduction in phosphor performance (luminance decreases or colour shifts) during processing or during operation

3.179
phosphor layer
thin coating of phosphor that converts ultra violet radiation from the gas discharge into visible radiation

3.180
pixel
smallest element of the display that can reproduce the full range of luminances and colours of the display

NOTE Often, the pixel is composed of three primary colour subpixels (red, blue and green).

3.181
pixel pitch
separation between the centre of two adjacent pixels

3.182
plasma display
display using a plasma display panel

3.183
plasma display panel
PDP
display device in which the electrical drive excites an electrical discharge in the gas within the device

NOTE The discharge may produce visible radiation directly or ultraviolet radiation which may excite phosphors of the appropriate colour.

3.184
plasma tube array
PTA
technology to realize devices in which the glass tubes are arrayed with a combination of films having electrodes

NOTE 1 The glass tube has the function of light emission by a gas discharge powered by applying a voltage on external electrodes.

NOTE 2 PTA is a basic technology to realize devices not only for display but also for light source, etc.

3.185
plasma tube array display
PTAD
AC plasma display device using plasma tube array technology

3.186
plate
subassembly created by depositing layers on a substrate

NOTE The layers can include metallic electrodes, dielectric layers, barrier ribs, phosphors, secondary electron emitting materials, etc.

3.187
plate gap
gap between the front and rear plates measured between the internal surfaces over the electrodes

3.188
post-gamma APL
average picture level of the internal video signal that does not have gamma correction

NOTE 1 The signal levels in this internal video signal are proportional to the luminance of the pixels in a PDP module.

NOTE 2 The post-gamma APL is derived from a measurement point situated after the inverse gamma correction circuit. See pre-gamma APL. The inverse gamma function can be expressed as:

$$Y = (Y')^{-gamma}$$

where

Y is the video signal that does not have gamma correction,

Y' is the video signal that has gamma correction which is usually generated at the video source, and

gamma is gamma coefficient which has a typical value of 2,2.

3.189
power consumption
total power required by the PDP, which is a function of the display image

NOTE In a PDP, the power consumption is a strong function of the image displayed.

3.190
power cord efficacy
set efficacy
η_{pc}
ratio of the luminous flux generated by the display to the power consumed in the whole panel, drive circuits, signal processors, tuners, power supplies, etc. while displaying a full white image

NOTE Expressed in lumens/watt.

3.191
power cord efficiency
set efficiency
efficiency of visible light power generated by the display to the power consumed in the whole panel, drive circuits, signal processors, tuners, power supplies, etc. while displaying a full white image

NOTE Expressed in watts/watt. This is highly variable depending on the luminance, active image area and luminance limiting. For most applications, one should use power cord efficacy.

3.192
pre-gamma APL
average picture level of the gamma corrected video input signal

NOTE The pre-gamma APL is derived from a measurement point situated before the inverse gamma correction circuit. See post-gamma APL.

3.193
priming
method to generate priming particles (electrons, metastables, ions, etc.) that aids in starting a gas discharge

3.194
priming particles
particles in cells that aid initiating a discharge, such as ions, electrons, excited atoms, metastable atoms and photons

3.195
priming pulse
voltage waveform that generates a gas discharge for priming

3.196
protective layer
layer with low sputter yield and high secondary electron emission that covers the dielectric layer in an AC PDP

3.197
pulse memory operation
DC PDP driving system that exhibits inherent memory

3.198
quantum efficiency
measure of efficiency as a direct ratio of the output particles (quanta) to the input particles (quanta)

NOTE For plasma display panel phosphors, the number of photons of visible radiation produced from each absorbed ultraviolet photon is the phosphor quantum efficiency.

3.199
ramp waveform
type of reset (setup) waveform in which the applied voltage linearly increases or decreases with time

NOTE This waveform produces a very low intensity discharge that is useful for priming and for setting the wall voltage to a value just below the breakdown voltage of the cell.

3.200
rear plate
back plate
plate furthest from the viewer

3.201
reflected luminance
luminance of the screen resulting from ambient illumination with the display power source turned off

3.202
reflective layer
coating placed beneath the phosphor layer to enhance the luminance of the display

3.203
refresh type PDP
PDP that has no memory effect

NOTE See memory type PDP.

3.204
reset
setup
process that primes and sets up the wall voltage to a well defined level for addressing

3.205
reset step
time interval for the reset process

3.206
reset waveform
setup waveform
waveform that primes and sets up the wall voltage to a well-defined level for the addressing operation

3.207
resolution
ability of the display to reproduce objects that are close together and which remain distinguishable

NOTE Often confused with addressability.

3.208
row electrode
display electrode

NOTE The row electrode was historically continuous in the horizontal direction. When the panel is oriented in portrait orientation, the row electrode could be aligned vertically. See column electrode.

3.209
sandblasting
manufacturing process of abrading a surface with fine sand-like particles

NOTE This process is used to create three-dimensional surfaces in plates or slits in a sheet. This process is used in PDP manufacture to shape the barrier ribs.

3.210
scan bias
Vbscan
common voltage applied to all scan electrodes during addressing

3.211
scan electrode
electrode that addresses one line of pixels at a time and also sustains

3.212
scan pulse
incremental voltage pulse applied to the scan electrode that selects a line of subpixels in a periodic predetermined order by enabling address discharges

3.213
scan voltage
Vscan
amplitude of the voltage pulses applied to the scan electrode during addressing (excludes the scan bias)

3.214
scratch defect
optical defect in a transparent substrate that has the size and appearance of a scratch

3.215
screen area
maximum image reproducing area of the device

NOTE Sometimes also called active area.

3.216
screen height
V
height of screen area

3.217
screen width
H
width of the screen area

3.218
seal
bonding between the front plate and rear plate, that forms a hermetic seal to contain the gas

3.219
sealing
process of hermetically bonding the plates

NOTE This may be a high temperature process during which the solder glass (frit) is softened to effect bonding of the front plate and rear plate.

3.220
secondary electron emission
process wherein energetic particles (electrons or ions) impinge on a surface and produce free electrons

3.221
self erase
process by which a waveform may turn off a cell which has been discharging

NOTE This can occur when the wall charge at the end of a discharge cycle is great enough to initiate a spurious discharge that erases the wall charge.

3.222
setup
reset
process that primes and sets up the wall voltage to a well defined level for addressing

3.223
setup waveform
reset waveform
waveform that primes and sets up the wall voltage to a well-defined level for the addressing operation

3.224
single substrate PDP
surface discharge PDP

3.225
specular reflection
reflection in accordance with the laws of geometrical optics, without diffusion

3.226
static margin
static sustain margin

3.227
static sustain margin
ΔVss
difference between the first-off voltage and the first-on voltage with addressing operations turned off

NOTE This is measured by observing the states of a panel or a group of cells while raising and lowering the sustain voltage. See sustain margin.

3.228
statistical delay
t_s
time for creation of a single priming particle that initiates the first avalanche of the discharge process associated with the formative delay

NOTE While applying the addressing waveform, the peak of the discharge generally occurs after the statistical delay plus the formative delay.

3.229
striped rib
rib structure formed by long parallel walls situated on only two sides of the cell

3.230
subfield
one portion of a field period in which a selected set of pixels will produce a specific amount of light

NOTE Multiple subfields are composed to make a field in order to achieve grey scale in plasma displays.

3.231
subpixel
smallest element of a display that can be addressed, typically a primary colour element

3.232
subpixel arrangement
description of the positions of the colour subpixels making up a pixel

3.233
subpixel pitch
spacing of the subpixels in the plane of a plate

NOTE Typically different along the row and column directions and may be different between different colour subpixels.

3.234
substrate
bare sheet material used as the base structural element to make plate(s)

NOTE Commonly this is glass material.

3.235
surface discharge
discharge in an AC PDP in which the display electrodes are on the same substrate surface

3.236
surface discharge PDP
form of an AC PDP in which the display electrodes are on the same surface

NOTE Also called coplanar PDP or single substrate PDP.

3.237
sustain
mode of operation of an AC PDP wherein electrodes are driven with an a.c. voltage and the cells either continue discharging or remain inactive

NOTE This AC drive provides the principal energy to the display.

3.238
sustain address bias
Vbsus
common voltage applied to all sustain electrodes during addressing

3.239
sustain driver
circuit that generates the sustain waveform

3.240
sustain duty factor
percentage of time when the sustain driver is active during a field period for the ADS method

3.241
sustain electrode
electrode in a three-electrode type PDP that sustains, but is not driven with scan pulses

NOTE Sustain electrodes are frequently connected together inside the panel.

3.242
sustain frequency
f_s
frequency of the sustain waveform during a display period

NOTE See sustain pulse number.

3.243
sustain gap
gap between the sustain electrode and the scan electrode within a cell

3.244
sustain loading
change in luminance of a display image due to state changes in a large number of pixels located anywhere in the panel (not related to the APC)

3.245
sustain margin
ΔVs
sustain voltage range that allows proper addressing of all pixels at the specified operating conditions

3.246
sustain pulse
single pulse of the sustain waveform (one half cycle)

3.247
sustain pulse number
number of sustain pulses that a subpixel receives per frame

3.248
sustain voltage
Vs
zero to peak voltage level of the sustain waveform

3.249
sustain waveform
time dependent voltage(s) generated by the sustain driver(s) that facilitates the sustain operation

NOTE The sustain waveform typically consists of two different waveforms that drive different electrodes in the plasma display panel so that the subpixels are stimulated by the difference of these two waveforms.

3.250
sustainer

NOTE See sustain driver.

3.251
thermal compaction
densification of substrates during a thermal cycle that is observed as shrinkage or deformation in patterns on the substrates

3.252
three-electrode type PDP
AC PDP having three electrodes per cell, the pair of display electrodes which provide the AC power to the discharge cells and the address electrode on the opposite substrate which provide voltages for writing and erasing individual cells

NOTE See surface discharge PDP.

3.253
tipoff
final vacuum closure of the panel, usually a glass exhaust tubulation that is softened and sealed or a metal exhaust tubulation that is crimped closed

3.254
Townsend discharge
self-sustaining plasma discharge described by Townsend

NOTE It is a discharge wherein space charge effects can be neglected. This is the discharge mode appearing at currents below those needed for a glow discharge.

3.255
transparent electrodes
electrodes that are composed of transparent conductors such as tin oxide or indium-tin oxide

3.256
two-electrode type PDP
plasma display panel using only two electrodes per cell that are driven with, not only the sustain waveforms, but also with the write and erase waveforms

NOTE Usually composed of two plates with orthogonal sets of electrodes (see opposed discharge PDP).

3.257
unstable cell
cell that changes luminance in an uncontrollable way

3.258
visible defect
imperfection that prevents the device from displaying the proper visual image

3.259
Vt closed curve
plot of discharge threshold conditions with two axes for the voltage differences: (a) between sustain electrodes, and (b) between a sustain and an address electrode, for the three-electrode type PDP

NOTE The curve is a closed hexagon, each side corresponding to one of the six different inter-electrode discharges. The Vt closed curve is used for device characterization, wall voltage measurement and operation analysis of a PDP cell.

3.260
waffle rib
type of closed rib in the shape of a Belgian waffle

3.261
wall charge
Qw
net accumulation of negative or positive charge on the dielectric layer surface of a cell that influences the voltage across the gas

NOTE See A.1.2.

3.262
wall voltage
Vw
voltage across the gas due to the wall charge that usually varies with time

NOTE The wall voltage is equal to the combination of the corresponding dielectric voltages. For three (or more) electrode devices, there will be multiple wall voltages, one corresponding to each pair of electrodes.

3.263
wall voltage transfer curves
curves used for device characterisation that describe the quantity of the change in wall voltage due to the discharge as a function of the initial voltage across the gas

NOTE The initial voltage across the gas depends on both the applied sustain voltage and the initial wall voltage.

3.264
white chromatic uniformity
chromatic uniformity of a full white screen at the specified measuring points (expressed as the difference in chromatic coordinates)

NOTE See 6.5 of IEC 61988-2-1:– (Ed. 2).

3.265
window luminance
$L_{\#}$
luminance measured in a selected window of the total screen area

NOTE The symbol # is the fraction of the screen area, typically 4 %, that measures at least 500 pixels. $L_{0,04}$ is the 4 % window luminance defined in 6.1 of IEC 61988-2-1:– (Ed. 2).

3.266
write
operation that generates a discharge, generally between the address and scan electrodes, to set subpixels to an on-state

3.267
write margin
ΔVwr
write voltage range that allows proper addressing of all pixels at the specified operating conditions

3.268
write pulse
voltage waveform derived from the difference of the address pulse and the scan pulse, not including the components of the address bias or the scan bias

3.269
write voltage
Vwr
maximum voltage of the write waveform

3.270
write waveform
time-dependent voltage signal applied to an electrode pair to selectively change the state of a subpixel from off to on

NOTE The write waveform includes the address bias, the scan bias, the address pulse and the scan pulse.

4 Symbols

4.1 General

The two lists in this clause summarize the symbols for PDP. The first list is ordered by the term name and the second is ordered by symbol.

4.2 Symbol list by term name

The following list contains all the terms that have assigned symbols.

Term	Symbol	Units
Address bias	Vba	volts
Address voltage	Va	volts
Bright room contrast ratio #/#	*BRCR*-#/#	ratio
Bright room contrast ratio 100/70	*BRCR*-100/70	ratio
Cell voltage	Vc	volts
Chromatic uniformity	Δx_i and Δy_i	dimensionless
Contrast ratio, sampled	*CR*	ratio
Dark room contrast ratio (DRCR)	*DRCR*	ratio

Dielectric voltage	Vd	volts
Erase voltage	Ver	volts
Firing voltage	Vf	volts
Firing voltage range	ΔVf	volts
First-off voltage	Vsm_{n}	volts
First-on voltage	Vf_{1}	volts
Formative delay	t_{f}	seconds
Last-off voltage	Vsm_{1}	volts
Last-on voltage	Vf_{n}	volts
Luminance deviation	ΔL_{i}	cd/m^2
Luminous efficacy	η	lumen/watt
Maximum firing voltage	Vf_{n}	volts
Maximum sustain voltage	Vs_{max}	volts
Maximum write voltage	Vwr_{max}	volts
Memory coefficient	α_{M}	ratio
Memory margin	ΔVmm	volts
Minimum cell sustain voltage	Vsm	volts
Minimum firing voltage	Vf_{1}	volts
Minimum sustain voltage	Vs_{min}	volts
Minimum sustain voltage range	ΔVsm	volts
Minimum write voltage	Vwr_{min}	volts
Module luminous efficacy	η_{m}	lumen/watt
Power cord efficacy	η_{pc}	lumen/watt
Scan bias	$Vbscan$	volts
Scan voltage	$Vscan$	volts
Screen height	V	millimetres
Screen width	H	millimetres
Static sustain margin	ΔVss	volts
Statistical delay	t_{s}	seconds
Sustain address bias	$Vbsus$	volts
Sustain frequency	fs	Hz
Sustain margin	ΔVs	volts
Sustain voltage	Vs	volts
Wall charge	Qw	coulombs
Wall voltage	Vw	volts
Window luminance	$L_{\#}$	cd/m^2
Write margin	ΔVwr	volts
Write voltage	Vwr	volts

4.3 Symbol list by symbol

The following table summarizes the terms for all of the assigned symbols.

Symbol	Term	Units
BRCR-#/#	Bright room contrast ratio #/#	ratio
BRCR-100/70	Bright room contrast ratio 100/70	ratio
CR	Contrast ratio, sampled	ratio
DRCR	Dark room contrast ratio (DRCR)	ratio
fs	Sustain frequency	hertz
H	Screen width	millimetres
$L_{\#}$	Window luminance	cd/m^2
Qw	Wall charge	coulombs
t_{f}	Formative delay	seconds
t_{s}	Statistical delay	seconds
V	Screen height	millimetres
Va	Address voltage	volts
Vba	Address bias	volts
$Vbscan$	Scan bias	volts
$Vbsus$	Sustain address bias	volts
Vc	Cell voltage	volts
Vd	Dielectric voltage	volts
Ver	Erase voltage	volts
Vf	Firing voltage	volts
Vf_1	First-on voltage (Minimum firing voltage)	volts
Vf_{n}	Last-on voltage (Maximum firing voltage)	volts
Vs	Sustain voltage	volts
Vs_{max}	Maximum sustain voltage	volts
Vs_{min}	Minimum sustain voltage	volts
$Vscan$	Scan voltage	volts
Vsm	Minimum cell sustain voltage	volts
Vsm_{n}	First-off voltage	volts
Vsm_1	Last-off voltage	volts
Vw	Wall voltage	volts
Vwr	Write voltage	volts
Vwr_{max}	Maximum write voltage	volts
Vwr_{min}	Minimum write voltage	volts
α_{M}	Memory coefficient	ratio
ΔLi	Luminance deviation	cd/m^2
ΔVf	Firing voltage range	volts
ΔVmm	Memory margin	volts
ΔVs	Sustain margin	volts
ΔVsm	Minimum sustain voltage range	volts
ΔVss	Static sustain margin	volts

ΔVwr	Write margin	volts
Δx_i and Δy_i	Chromatic uniformity	dimensionless
η	Luminous efficacy	lumen/watt
η_m	Module luminous efficacy	lumen/watt
η_{pc}	Power cord efficacy	lumen/watt

Annex A
(informative)

Description of the technology

A.1 Basic operation

A.1.1 General

The general colour AC (alternating current) plasma display panel consists of two substrates hermetically joined at their edges with sealing glass to form a vacuum tight vessel. This panel is filled with a gas having an appropriate electrical discharge characteristic and VUV (vacuum ultraviolet) emission characteristic. Applied pulses between the electrodes of the panel cause discharges within the gas and the emission of VUV. The VUV radiation excites a colour phosphor within the panel, typically a red, green or blue phosphor. These phosphors then emit their characteristically coloured light, effecting conversion of the VUV into visible radiation.

A.1.2 Discharge characteristics of principal PDP cells

The key characteristic of the gas is that no electrical discharge takes place when the initial applied voltage is below a certain voltage threshold. This voltage is called the “firing voltage”. Electrical discharges, however, do commence when the initial voltage exceeds the firing voltage (see Figure A.1).

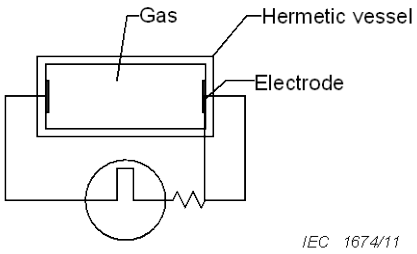

Figure A.1a – Principal structure of a DC PDP cell driven by DC voltage pulses

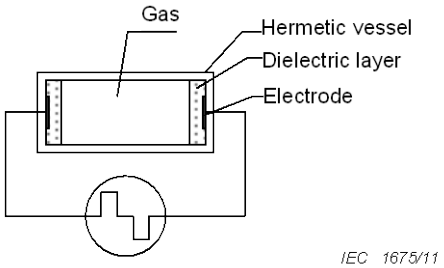

Figure A.1c – Principal structure of an AC PDP cell driven by AC voltage pulses

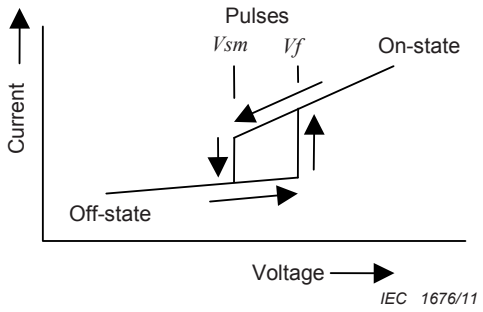

Figure A.1b – Current vs. voltage characteristic of a DC PDP cell driven by DC voltage pulses

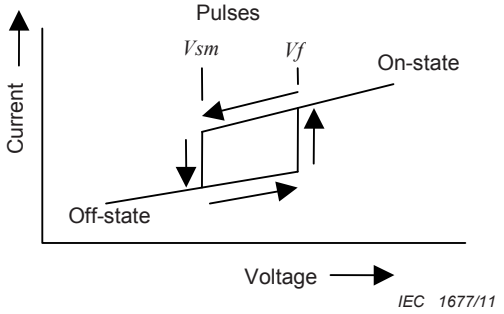

Figure A.1d – Current vs. voltage characteristic of an AC PDP cell driven by AC voltage pulses

Figure A.1 – Principal structures and discharge characteristics of a DC PDP cell and an AC PDP cell

A.1.3 Principal AC mode discharge characteristics

An AC PDP is special in that the electrodes are covered with dielectric coatings (see Figure A.1). Since the dielectric coating is an insulator, a voltage can exist between the

electrode and the surface in contact with the gas. The voltage across the gas is composed of two components: the voltage between the electrodes and the voltage due to charge on the dielectrics. The voltage across the gas is frequently not equal to the voltage applied between the electrodes because the voltage due to charge on the dielectric layers is usually not zero.

One component of the voltage across a dielectric layer results from the charge deposited on the surface of that dielectric layer by the gas discharge. That voltage is proportional to the charge and inversely proportional to the capacitance between the surface of the dielectric and the electrode under the dielectric. A second voltage component is the applied drive voltage capacitively divided between the dielectric layer, the gas and the opposite dielectric layer, but this voltage component is usually not significant.

When charge is transferred by the gas discharge from one dielectric surface to the opposing dielectric surface, the potentials on the two surfaces change in opposite directions. A charge transfer therefore changes the voltage across the gas. However, charges on the two surfaces that are equal and of the same polarity do not change the voltage across the gas[2].

The component of voltage across the dielectric layer that contributes to a voltage across the gas is called the dielectric voltage. This dielectric voltage should not be confused with the actual physical voltage across the dielectric layer that might be used, for instance, to determine the dielectric breakdown characteristics.

When a gas discharge occurs, negative charges from the ionised gas accumulate on the positive dielectric surface and positive charges accumulate on the opposing negative dielectric surface. This induces voltage changes across both dielectrics. Instantaneously, the charge deposition reduces the voltage across the cell. Depending on the drive voltage and the previous state of charge, the charge on the surfaces may be increasing, decreasing or even reversing. The final configuration of charges on the surfaces when the gas discharge extinguishes can add or subtract from the externally applied voltage to modify the voltage across the gas.

The final net charge transferred between the surfaces (ignoring the unintended, same-sign charges common to both surfaces) is called the wall charge and the voltage it induces across the gas is called the wall voltage. The total voltage across the gas, including the drive voltage, is called the cell voltage. combining the two dielectric voltages also yields the wall voltage.

To visualize the AC mode of operation, consider driving all the electrodes on one plate with one alternating voltage and all the electrodes on the opposite plate with an out of phase AC drive, with the difference of the two drives just below the firing voltage. In cells whose dielectrics are uncharged, the wall voltage will not add to or subtract from the applied electrode voltage and so the gas in those cells will not break down.

If the wall voltages on the dielectrics add enough to the drive voltage, a gas discharge is ignited. The discharge can transfer charge from the dielectric on one electrode to the dielectric on the paired electrode. This will leave a charge condition such that the dielectric voltage will aid the discharge on the reverse polarity cycle. Of course, after the next discharge, the charge returns to the initial condition. Under this drive condition, cells that discharge on either polarity (the on-cells) will continue to discharge on successive polarity reversals. The cells that did not discharge will remain inactive (the off cells).

This characteristic of an AC PDP wherein cells remain in the same state of discharge is called “memory function”.

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2 Such similar sign charges affect the total voltage across the dielectrics, but tend to cancel each other with respect to the voltage across the gas. These common mode charges are typically ignored in the discussion of plasma display panels because they have almost no effect on panel operation. They occur, unintentionally, due to dielectric leakage and stray lateral charge emission between neighbouring cells.

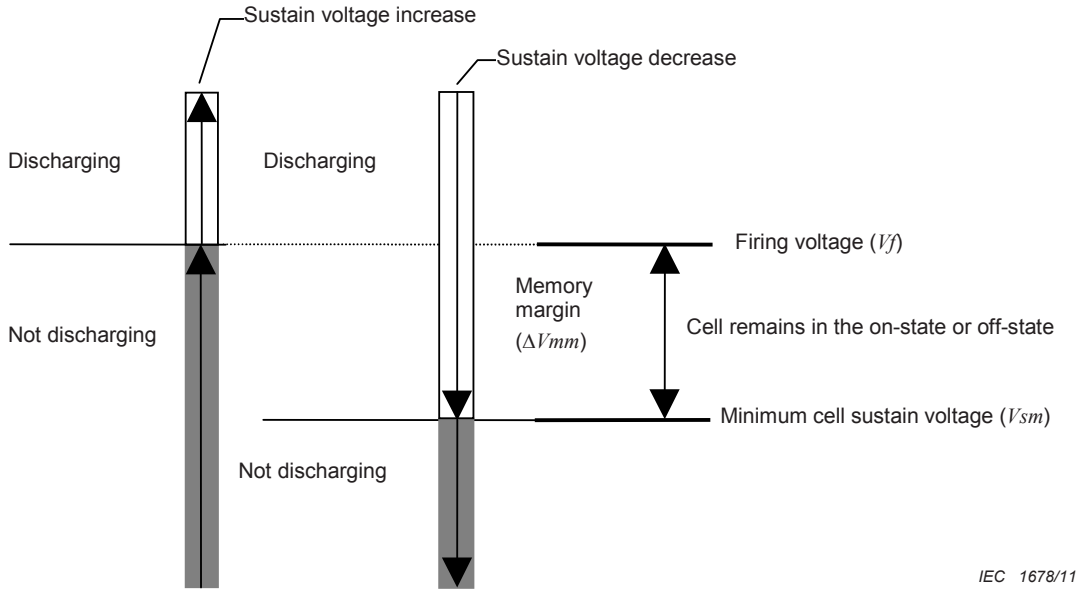


Figure A.2 – Discharge characteristics of a cell (single cell static characteristics)

A.1.4 Single cell static characteristics

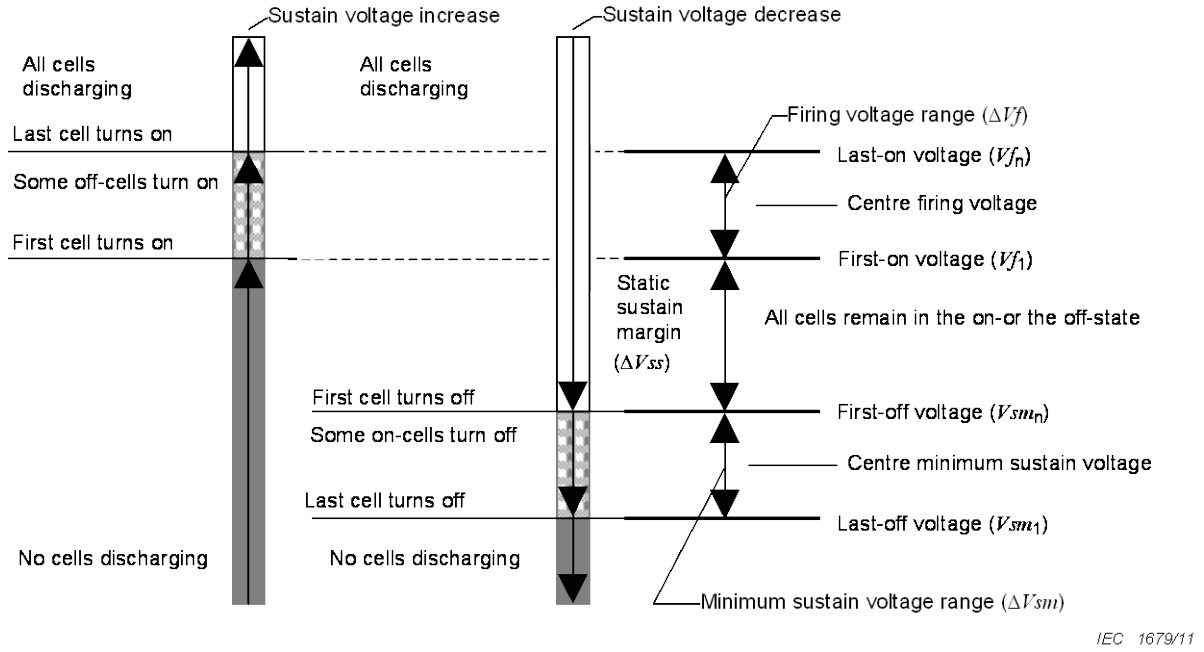
We shall now consider a PDP cell is driven with increasing sustain voltage (see Figure A.2). When the voltage rises to a certain value, the cell starts to discharge continuously and the voltage is called the "firing voltage (Vf)". After that, the voltage decreases and reaches a certain value, the cell stops discharging and the voltage is called the "minimum cell sustain voltage (Vsm)". The voltage range between the firing voltage and the minimum cell sustain voltage is called the "memory margin (ΔVmm)". If the sustain voltage is adjusted in the range of memory margin, the cell remains in the on or the off-state.

A.1.5 Static characteristics of cells

Further, in the case of the practical panel with a lot of cells, there will be many different values of firing voltage and minimum sustain voltage. Consider the case when the sustain voltage rises slowly from the state of a panel having all cells off (see Figure A.3). The voltage at which the first cell turns on is called the "first-on voltage (Vf_1)". The voltage at which essentially all cells have turned on and all the cells remain in the on-state after raising the voltage further is called the "last-on voltage (Vf_n)". Then consider what happens as the sustain voltage is decreased. The voltage at which a cell turns off while decreasing the sustain voltage is called the "first-off voltage (Vsm_n)". The voltage at which essentially all of the cells are turned off is called the "last-off voltage (Vsm_1)".

The sustain voltage applied to operate PDP should be less than the "first-on voltage"; or else off cells will sporadically turn on. The sustain voltage should also be greater than the "first-off voltage," or else on-cells will sporadically turn off. The difference between these two voltages is called the "static sustain margin (ΔVss)".

The difference between the "first-on voltage" and the "last-on voltage" is called the "firing voltage range (ΔVf)". Similarly, the difference between the "first-off voltage" and the "last-off voltage" is the "minimum sustain voltage range (ΔVsm)". These ranges and the centre values of the turn-on voltage and the turn-off voltage are useful statistical measures of the panel uniformity.



where

$\Delta Vss = Vf_1 - Vsm_n$

$\Delta Vf = Vf_n - Vf_1$

$\Delta Vsm = Vsm_n - Vsm_1$

Figure A.3 – Static characteristics of cells in a panel or a group of cells

A.1.6 Addressing mechanism

The electrodes in principal two-electrode type PDPs are organized in matrix fashion, with horizontal and vertical electrodes. The intersections of these electrodes make cells that can be individually addressed. In an AC PDP, these discharges can take place in the following manner. When one horizontal electrode and one vertical electrode are selected with pulses of opposite polarities, then the voltage difference at their intersection is the difference between each address (data) and scan waveforms, and when these are higher than the firing voltage, this causes a strong gas discharge (see Figures A.4 and A.5).

Consider a cell at the intersection between a selected address (data) electrode and a non-selected scan electrode pair. The gap voltage will only be the voltage difference between the selected address (data) electrode voltage (address (data) bias + address (data) voltage) and the non-selected scan electrode voltage (only scan bias). This voltage will not initiate a gas discharge. The voltage difference between non-selected electrodes is, of course, only the difference between biases and will not initiate discharge. The sharp threshold in the gas discharge characteristic that enables a discharge only at fully selected cells permits individual cells of the panel to be turned on independently by appropriately addressing the electrodes. Drives and responses at such an intersection are diagrammed in Figure A.5.

Usually, to turn off the cells narrow pulses are applied. When the pulse width is shortened, the charge is not transferred sufficiently to reverse the wall charge in the cell and this results in partially charged dielectrics. Such a narrowed discharge pulse results in switching an on-cell to an off-cell.

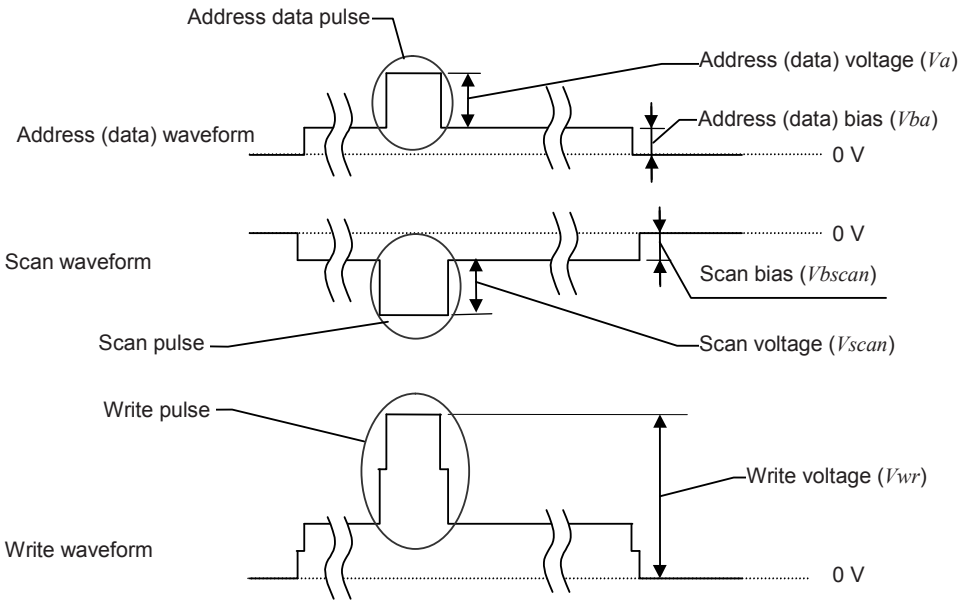


Figure A.4 – Write waveform components

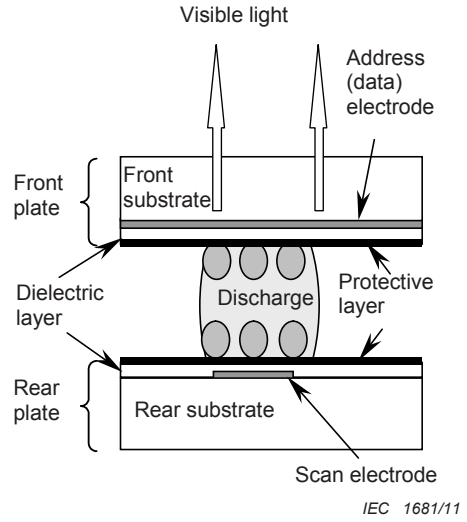


Figure A.5a – PDP principal structure of two-electrode type AC PDP

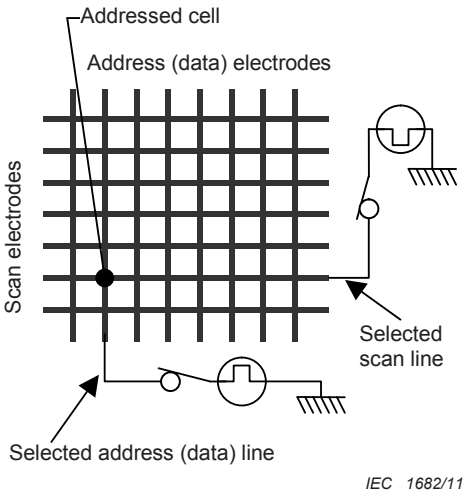


Figure A.5b – Electrodes layout of two-electrode type PDP

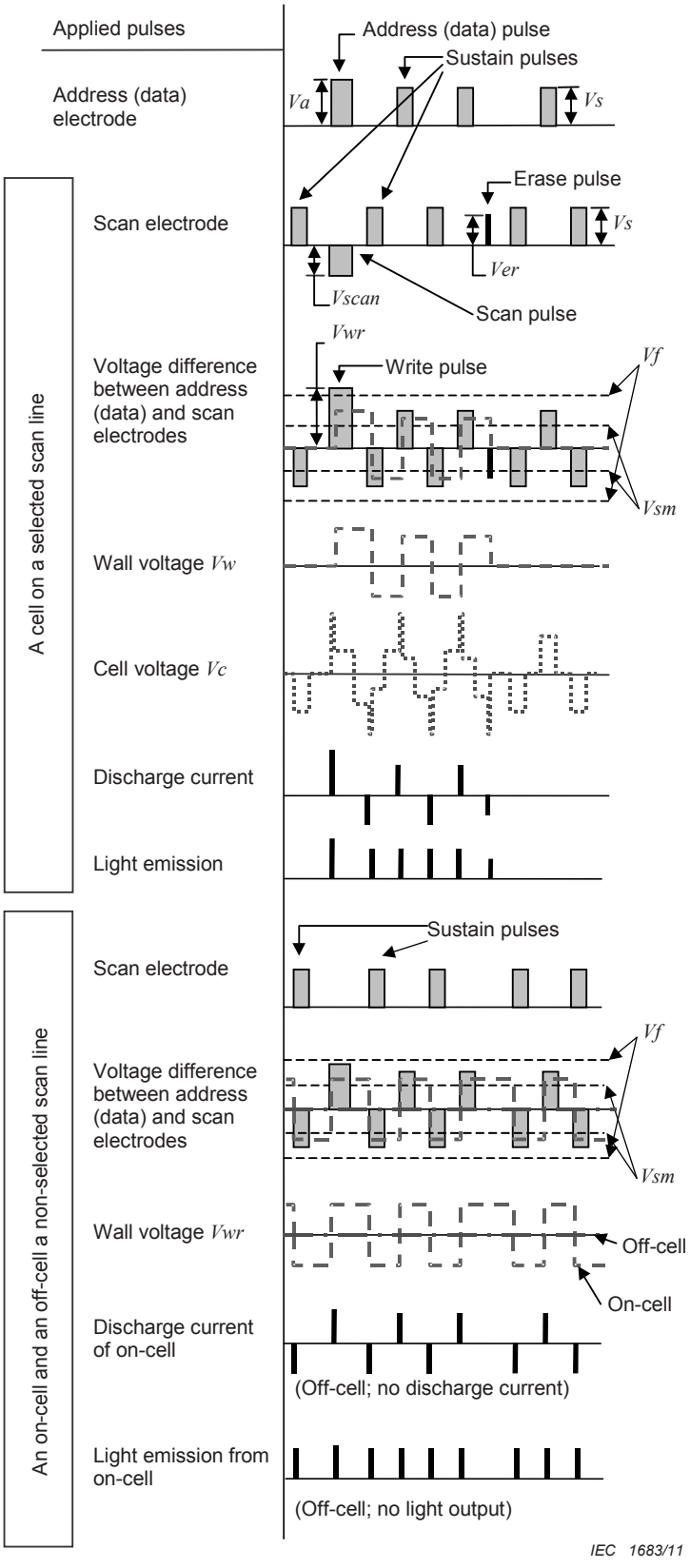


Figure A.5c – Addressing waveform

Figure A.5 – Operation of a two-electrode type AC PDP

A.1.7 Dynamic versus static drive

Up until this point in the discussion, events such as sustain, write and erase have been considered separately. In reality, measurements of firing voltage, first-on, last-on, first-off and last-off voltages in the operation of the panel without write cycles provide useful information about the operation of the panel. Measurements performed without write cycles are referred to as static measurements. However, adding the write cycles to set cells on or cells off influences the firing voltage and the voltages corresponding to first-on, last-on, first-off and last-off events.

In Figure A.6, the effect of changing the amplitudes of both the write voltage and the sustain voltage are graphed. The area within the window shows the satisfactory operation, (i.e. the on-cells remain on, the off-cells remain off, cells written to turn on do turn on, and cells written to turn off do turn off). Adding the turn-on and turn-off requirements to the simple maintenance of on- or off-state reduces the margins and the dynamic margins are smaller than the static margins.

The dynamic margin is the region between the maximum voltage and the minimum voltage where addressing is performed correctly under the actual operating conditions. At a specified operating condition (e.g. at a constant sustain voltage or a constant write voltage) the operative voltage range between maximum operating voltage and minimum operating voltage is called the “operating margin”.

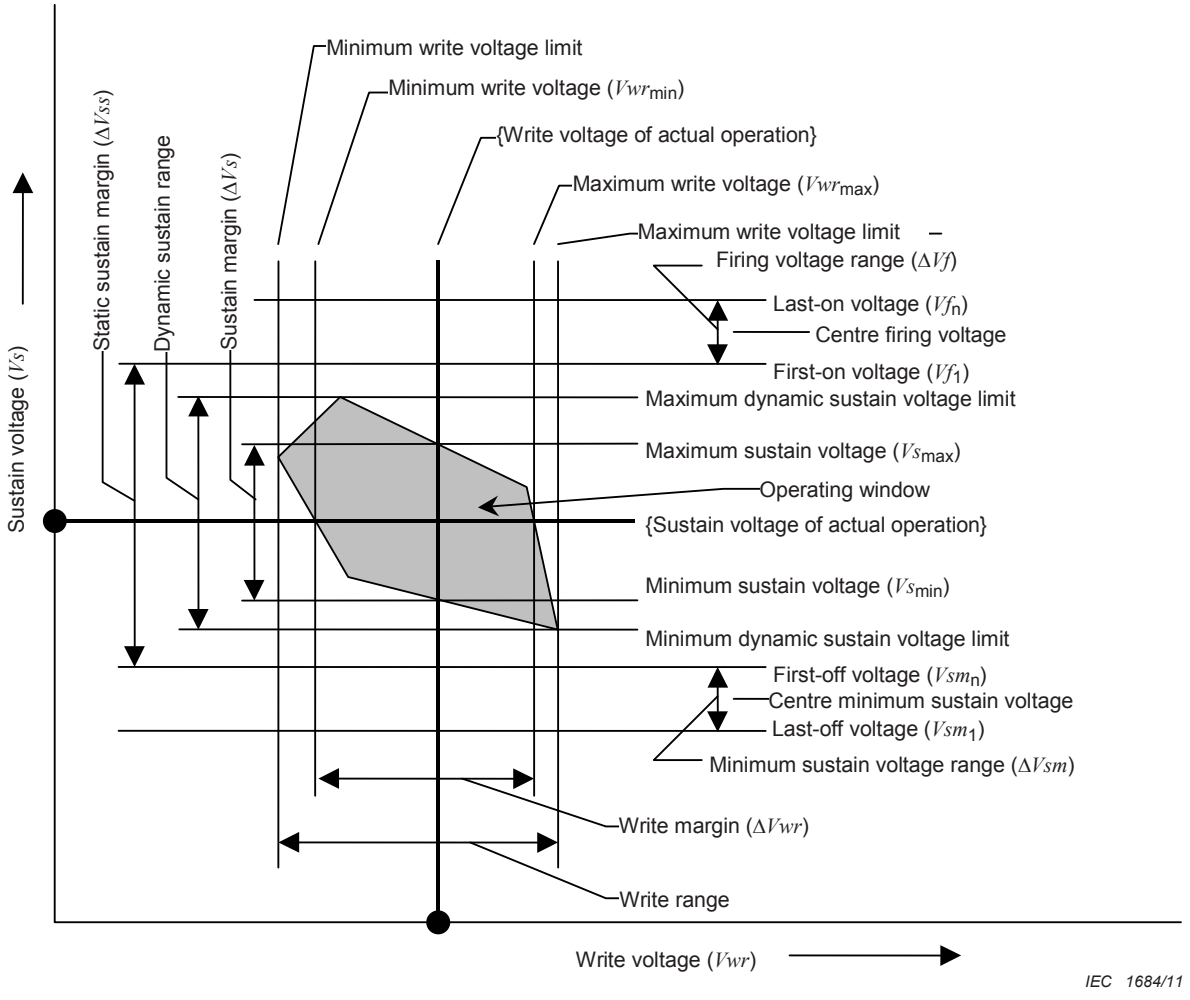


Figure A.6 – Relation between margins and applied voltages

A.2 Three-electrode type AC PDP

A.2.1 Cell structure of a three-electrode type surface discharge AC PDP

Colour AC PDP has evolved into three electrode structures. This geometry is shown in Figure A.7.

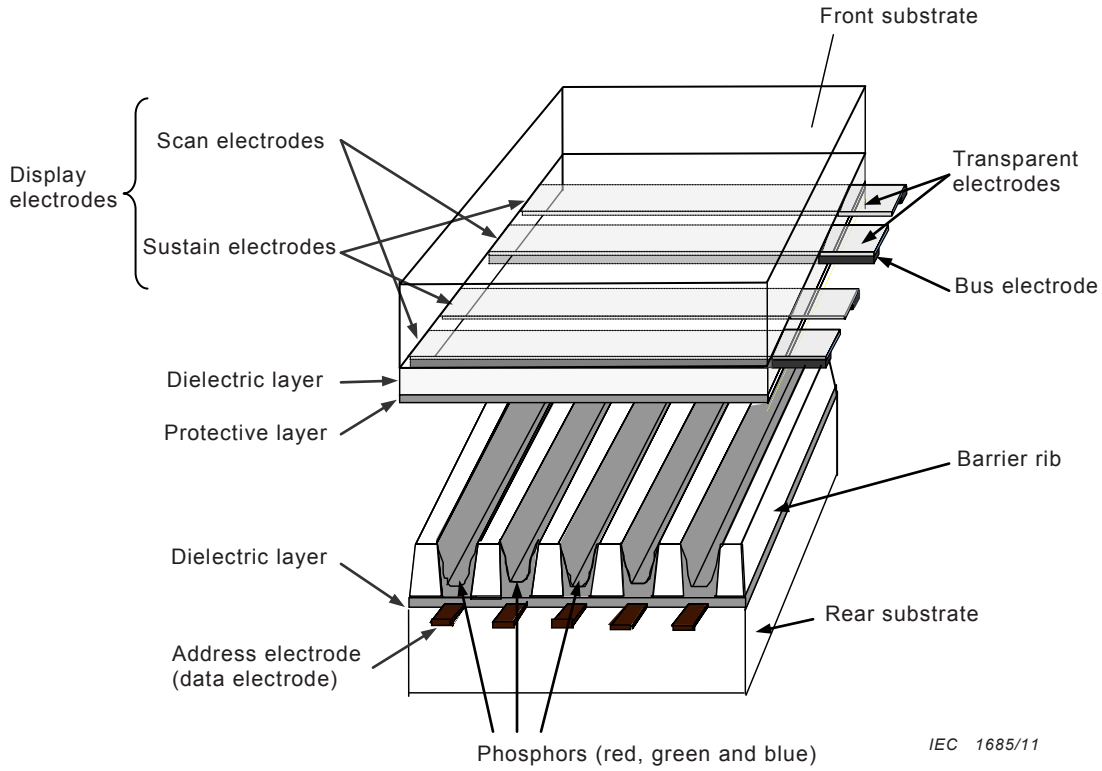


Figure A.7 – Structure of a three-electrode type, surface discharge colour AC PDP

Multiple parallel display electrodes (the scan and sustain electrodes) are deposited on the front substrate.

These display electrodes consist of a wide transparent electrode and a narrow bus electrode. The much more conductive bus electrode is adjacent to and electrically connected to the transparent electrode. The display electrodes are covered by a transparent dielectric layer that is, in turn, covered by a protective layer.

Multiple parallel address (data) electrodes, which are orthogonal to the display electrodes, are formed on the rear substrate. These are covered with a dielectric layer. Barrier ribs are made on the dielectric layer between the address (data) electrodes. The three primary colour phosphor materials (red, green and blue) are deposited in sequence in the valleys formed by the barrier ribs and the dielectric layer.

A.2.2 Electronic drive of three-electrode type AC PDP

A plasma display panel has connections to the sustain electrodes (typically connected in common), the scan electrodes (typically common to a row of cells) and address (data) electrodes (typically common to a column of cells). The drives for these electrodes are the sustain, the scan and the address (data) drives.

AC sustain pulses that are lower than the maximum operating sustain voltage but higher than the minimum operating sustain voltage are applied between the pairs of display electrodes. Write and erase pulses are applied between the address (data) and scan electrodes. As discussed before, when an applied pulse has a voltage greater than the firing voltage (Vf), an electrical discharge is ignited in the discharge gap. The generated charges are accumulated on the dielectric layer to reduce the electric field made by the applied voltage and then the discharge stops. When the discharge transfers enough charge to predispose the cell to discharge on the next reverse polarity sustain cycle, the cell is said to be written or turned on. If the discharge is turned off early and the wall charge has been neutralized, the cell is no longer predisposed to discharge on the next sustain cycle. Such a cell is said to be erased or turned off. The discharge current and light emission from an on-cell are pulse-shaped.

A.2.3 Driving methods

There are two types of drive philosophies, ADS (address, display-period separation) and AWD (address while display) methods. The ADS method is more commonly used.

A.2.4 ADS (address-, display-period separation) method

Grey scale of the plasma display can be realised by using an address-, display-period separation method. ADS has been developed for the purpose to simplify the electronic driving circuits and to realise a stable operation with a wide operating margin of three-electrode type AC PDPs.

A second is typically divided into 50 or 60 fields. In principle, each field is divided into 8 sub-fields. The display data are input during the address period. Each subfield has different number of sustain pulses that realise different luminance of each subfield. A 256 level grey scale can be realised with combinations of the different luminance produced in each subfield (see Figure A.8).

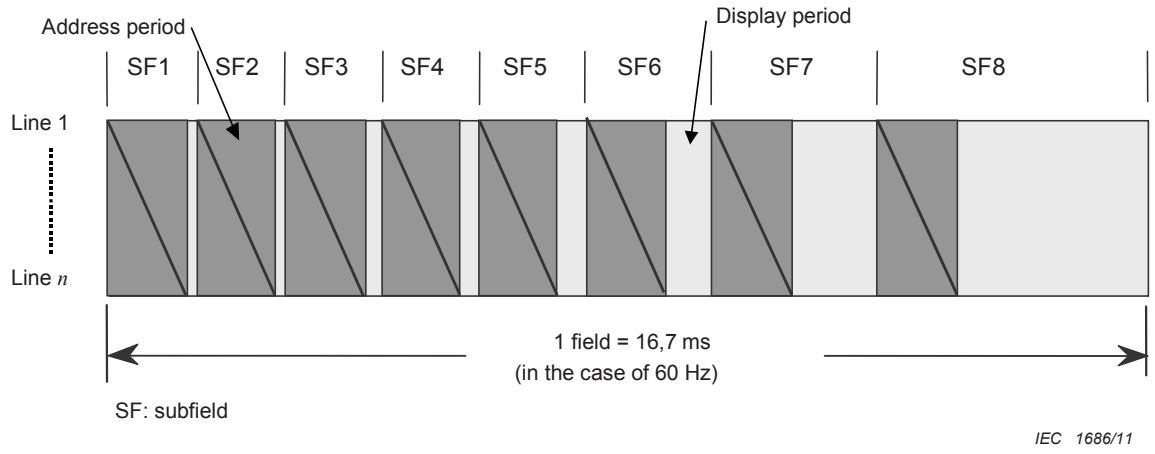


Figure A.8 – Address-, display-period separation method

The subfields in the ADS method are composed of address period and display period. The address period consists of a reset and an address step (see Figure A.9).

Reset step: Principally discharges in all subpixels in the picture are ignited by a bulk write. This results in making a wall charge on the protective layer of the pixels. The charges are then erased or set in an on-level by applying the appropriate bulk erase. As a result, the surface conditions of all the cells become uniform in a reset step.

Address step: The discharges in the selected subpixels are ignited by applying a scan pulse to a scan electrode and address (data) pulses to address (data) electrodes at the same time. Wall charges are accumulated on the dielectric in the selected subpixels to be displayed. The scan pulses are negative and applied sequentially to the many scan electrodes. The positive address (data) pulses are applied on the address (data) electrodes to set the appropriate wall charge in cells that should be sustained for the corresponding number of sustain pulses in the subfield. A sustain address bias can be applied to the sustain electrodes during addressing to assist in forming the wall charges.

Display period: The subpixels in which the wall charges are accumulated in address step are picked up by the first sustain pulse which makes a discharge in the selected pixels resulting in accumulating sufficient wall charges to be sustained by the following sustain pulses to display.

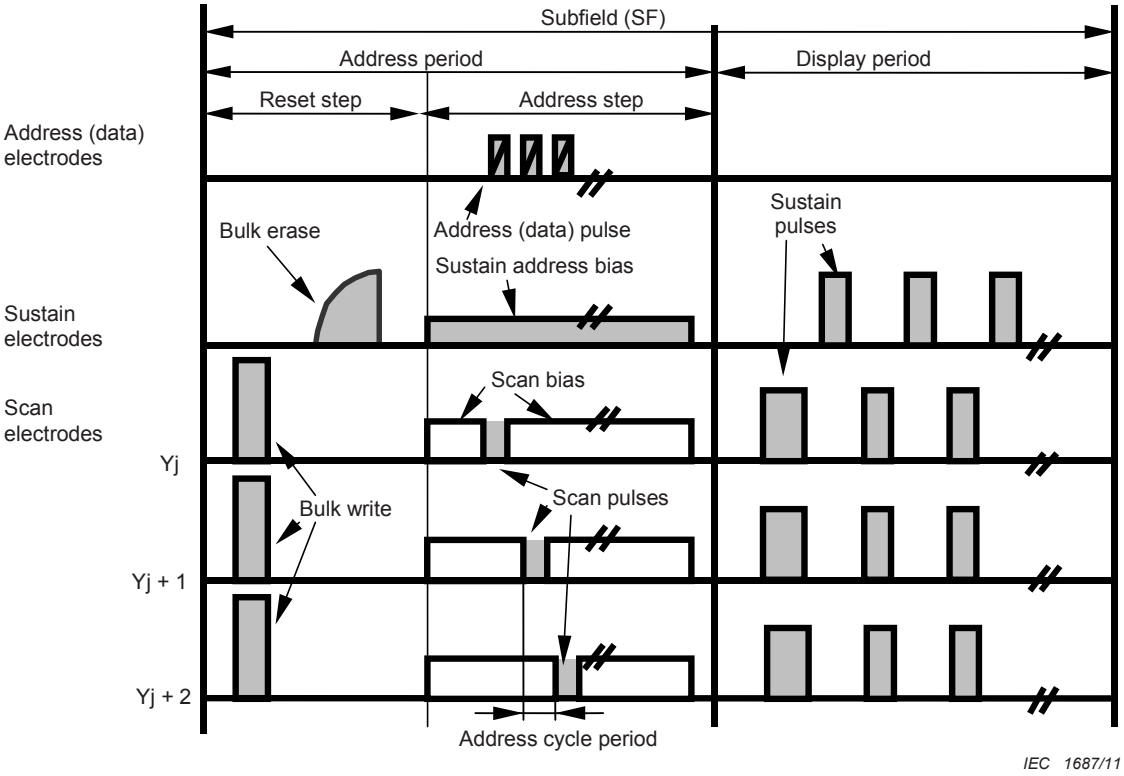


Figure A.9 – A driving waveform for ADS method applied to a three-electrode type PDP

A.2.5 AWD (address while display) method

An address while display method also uses a subfield technique similar to the ADS method. But the address period and the display period is not separated within a panel (see Figure A.10). The reset and address (data) waveform of each line is inserted between and combined with continuous sustain pulses. After a predetermined period the line is erased and a subfield of the line finishes. AWD has been generally used for driving two-electrode type AC PDPs. But the electronic driving circuits are not simple and the operating pulses tend to be narrow, resulting in a smaller operating margin compared to the ADS method with the driving of three-electrode type AC PDPs.

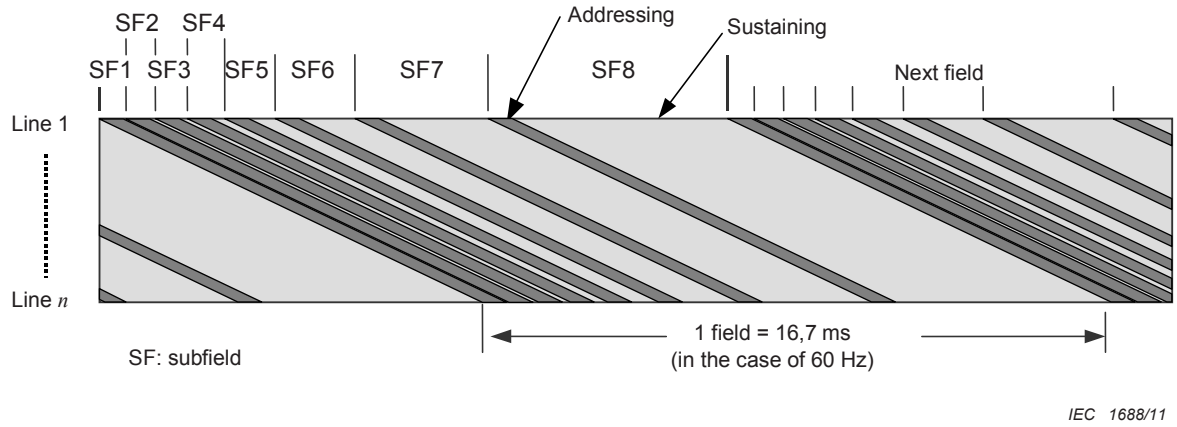


Figure A.10 – Address while display method

Annex B
(informative)

Relationship between voltage terms and discharge characteristics

Table B.1 shows the relation between terms for voltages used to describe the discharge characteristics of PDPs.

Table B.1 – Relation between static, dynamic and operating discharge characteristics in a cell, a panel or a group of cells

		Cell	Panel or group of cells			Value type
		Static	Static	Dynamic	Operating	
Sustain voltages	Turn-on voltages	Firing voltage (Vf)	Last-on voltage (Vf_n)	–	–	Max.
			First-on voltage (Vf_1)	Maximum dynamic sustain voltage limit	Maximum sustain voltage (Vs_{max})	Min.
			Centre firing voltage	–	–	Centre
			Firing voltage range (ΔVf) $\Delta Vf = Vf_n - Vf_1$	–	–	Range
	Turn-off voltages	Minimum cell sustain voltage (Vsm)	First-off voltage (Vsm_n)	Minimum dynamic sustain voltage limit	Minimum sustain voltage (Vs_{min})	Max.
			Last-off voltage (Vsm_1)	–	–	Min.
			Centre minimum sustain voltage	–	–	Centre
			Minimum sustain voltage range (ΔVsm) $\Delta Vsm = Vsm_n - Vsm_1$	–	–	Range
	Margin	Memory margin (ΔVmm) $\Delta Vmm = Vf - Vsm$	Static sustain margin (ΔVss) $\Delta Vss = Vf_1 - Vsm_n$	Dynamic sustain range	Sustain margin (ΔVs) $\Delta Vs = Vs_{max} - Vs_{min}$	Range
Write voltages		–	–	Maximum write voltage limit	Maximum write voltage (Vwr_{max})	Max.
		–	–	Minimum write voltage limit	Minimum write voltage (Vwr_{min})	Min.
	Margin	–	–	Write range	Write margin (ΔVwr) $\Delta Vwr = Vwr_{max} - Vwr_{min}$	Range

Annex C
(informative)

Gaps

An AC PDP has several kinds of gaps and they are important to drive the panel properly (see Figure C.1).

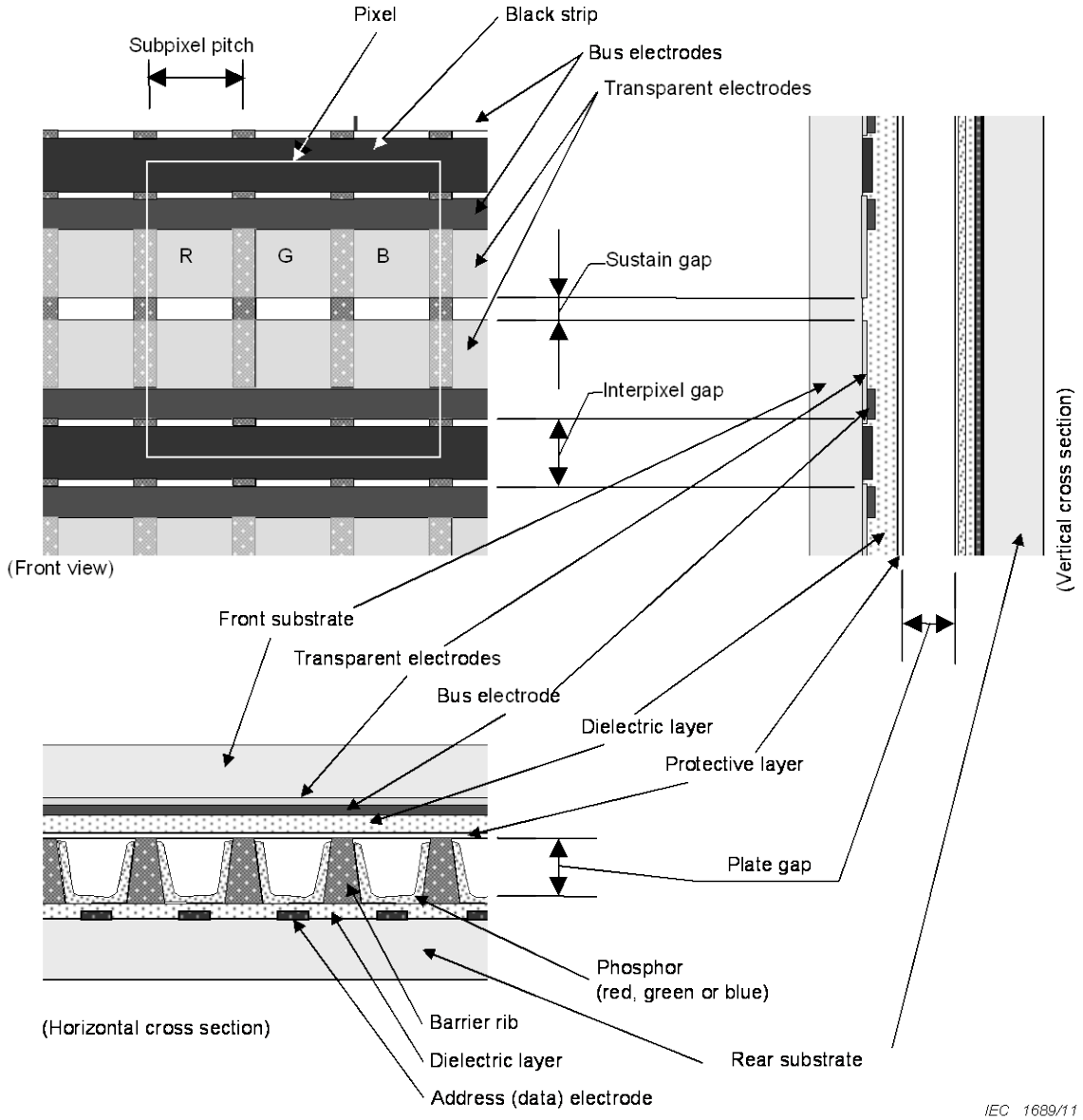


Figure C.1 – Gaps (sustain gap, plate gap and interpixel gap) in a three-electrode type AC PDP

Annex D
(informative)

Manufacturing

D.1 General

The manufacturing process for the three-electrode type surface discharge colour AC PDPs is described in the flow chart in Figure D.1. The steps shown in Figure D.1 are discussed below in the sequence for front plate, rear plate and finishing.

D.2 Front plate

The transparency requirement of the front plate is met by using glass. Typically, a high strain point glass plate is used to eliminate the distortion and to reduce the shrinkage that can occur in the thermal processes. Indium tin oxide (ITO) or SnO_2 is used for transparent electrodes. The ITO film, for example, is made by sputtering or ion plating and then patterned with photo-lithography processes.

However the resulting ITO resistivities are higher than desired, so higher conductivity bus electrodes are formed along the edge of the ITO electrodes. These can be silver (Ag) or chrome-copper-chrome (Cr/Cu/Cr). A silver electrode is made with a printing method by photo-lithography using a photo-sensitive Ag paste with frit glass. A chrome-copper-chrome electrode is made using sputtering and photolithographic patterning.

These electrodes are covered with transparent thick-film dielectric layer(s) to create the capacitive layer required for AC operation. Screen printing, slit coating, roll coating, and green sheet methods are used to make dielectric layer. It is important to keep an excellent uniformity and high transparency as these characteristics affect the display performance.

The panel has a large fraction of reflective materials (the phosphors are all white). The resulting image could look washed-out in a bright room. Placing black materials (called the black stripe) on the front plate in the unused areas decreases the reflectivity, thereby increasing the contrast of the image, and prevents undesired spreading of discharge light. The black stripe is made with a printing method or a photolithography under the dielectric layer.

The surface of the dielectric layer is coated with a protective layer that provides high secondary electron emission as well as sputter-resistance against ion bombardment. This quality of this protective layer is one of the most important factors in realizing good performance. MgO (magnesium oxide) is the most common material for the PDP protective layer. It is generally made by electron beam deposition. Some new methods are expected to manufacture more efficiently; these include ion plating, reactive sputtering, sol-gel method, etc.

A sealing glass layer is applied to the perimeter of the display area and pre-fired. This sealing glass will join the frame and rear plates in the assembly of the panel.

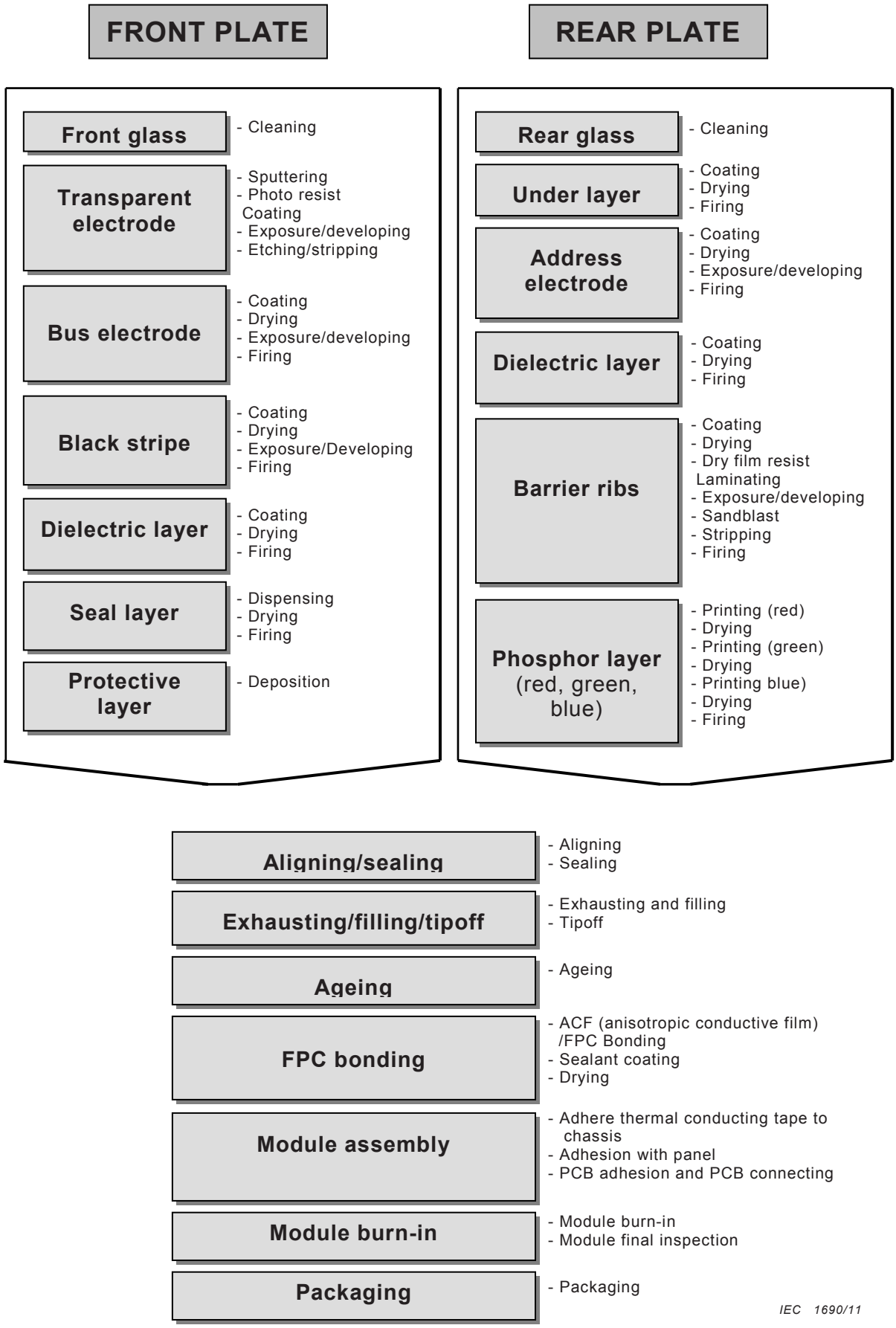


Figure D.1 – PDP manufacturing flow chart

D.3 Rear plate

Typically, a high strain point glass substrate is also used to eliminate thermal processing distortion by reducing the shrinkage that can occur during the thermal processes.

The address (data) electrodes are applied using processes similar to the bus electrode processes.

The dielectric layer for the rear plate is slightly different from the dielectric layer on the front plate. A white dielectric layer, rather than a transparent one, both protects the address (data) electrodes and reflects the visible light emitted from phosphors toward the front plate and on to the viewer, increasing luminance. The application processes are similar to those for the dielectric layer of the front plate.

In order to avoid a degradation of colour purity due to optical and ion migration crosstalk between neighbouring discharge cells in the horizontal direction, thick film barrier ribs are formed between the address (data) electrodes. Fabrication methods include printing, sandblasting, lift-off, photo-lithography, etc.

The three primary phosphors are deposited in the valleys formed between the barrier ribs and the top of the address (data) electrodes. Printing, coating and photo-lithography or electro-phoretic deposition is commonly used to make the phosphor deposits.

At some step a small hole is made in a corner of the rear plate to connect to the vacuum system. An exhaust tube may be attached by glass sealing or fritting with a sealing glass.

D.4 Finishing

After assembling the frame and rear plates, the panel goes through the firing process in which the low-melting point frit glass seals the plates together. A vacuum baking process is provided to remove the contamination adsorbed on the inner surface of the panel assembly and to activate the protective layer. Finally, a penning gas mixture is admitted into the panel.

The panel is then operated with voltage pulses somewhat higher than firing voltage. This ageing operation cleans and activates the protective layer. This lowers the operating voltage and increases the uniformity resulting in reduced variation of the operating voltage over different regions of the panel.

Then the panel is assembled with the electronic systems and built in a module.

Annex E
(informative)

Interconnect pad

A plasma display panel is connected to driving electronics through interconnect pads formed at the end of each electrode. The interconnect pads of address (data) and display electrodes (scan and sustain electrodes) are arranged on the outside surfaces of rear plate and front plate (see Figure E.1). Along each edge of the PDP, interconnect pads are divided into several groups and each interconnect pad group is separately connected to its associated electronic driving circuits. The width and the spacing of the interconnect pads are very important for the reliability of their electrical connection (see Figure E.2).

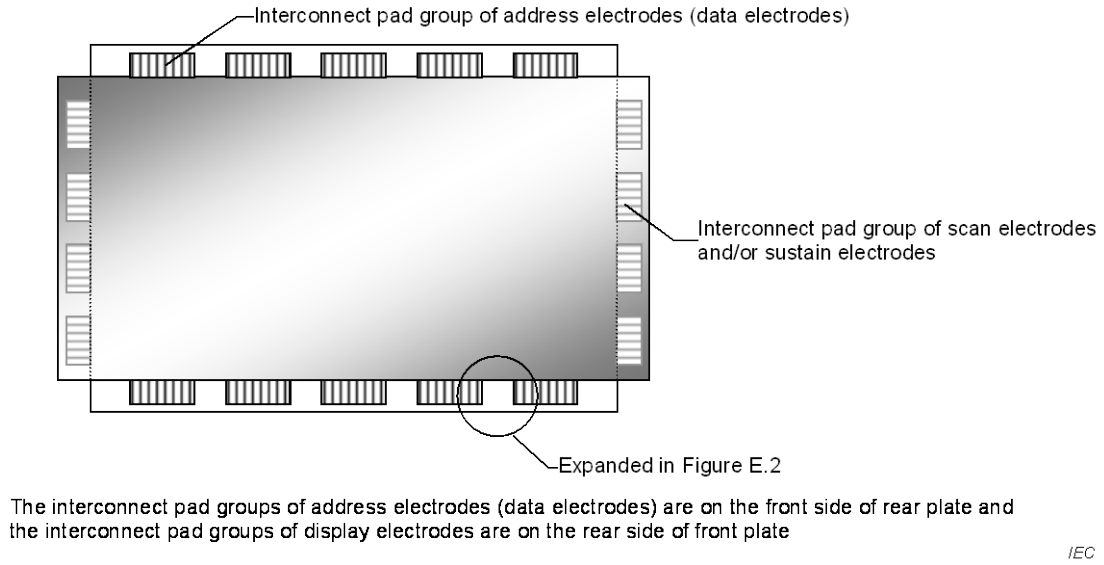


Figure E.1 – Interconnect pad group

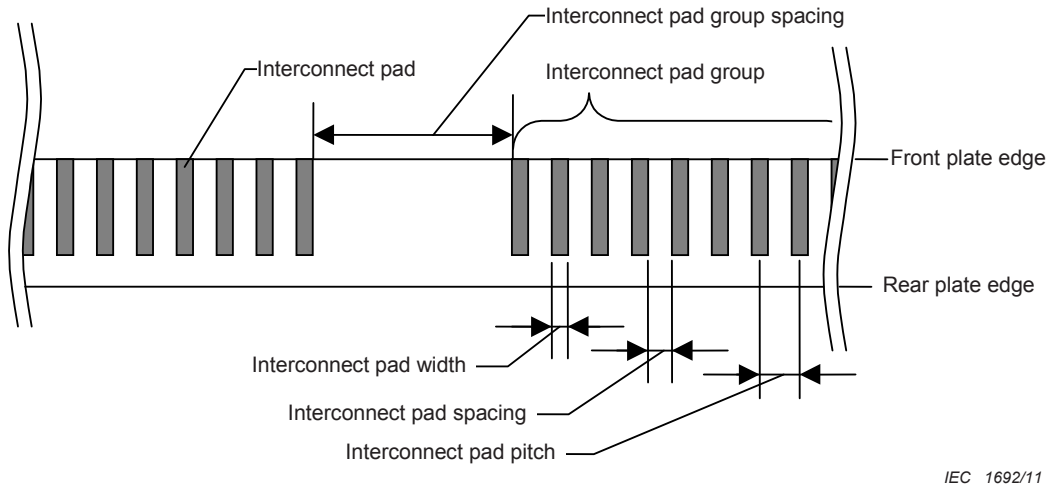


Figure E.2 – Dimensions of interconnect pads

Bibliography

[1] CIE 15:2004, *Colorimetry*

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