BS EN 61189-5-1:2016

BSI Standards Publication

Test methods for electrical materials, printed boards and other interconnection structures and assemblies

Part 5-1: General test methods for materials and assemblies — Guidance for printed board assemblies

bsi.

National foreword

This British Standard is the UK implementation of EN 61189-5-1:2016. It is identical to IEC 61189-5-1:2016.

The UK participation in its preparation was entrusted to Technical Committee EPL/501, Electronic Assembly Technology.

A list of organizations represented on this committee can be obtained on request to its secretary.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

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Compliance with a British Standard cannot confer immunity from legal obligations.

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English Version

Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 5-1: General test methods for materials and assemblies - Guidance for printed board assemblies (IEC 61189-5-1:2016)

Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures d'interconnexion et ensembles - Partie 5-1: Méthodes d'essai générales pour les matériaux et assemblages - Lignes directrices pour les assemblages de cartes à circuit imprimé (IEC 61189-5-1:2016)

Prüfverfahren für Elektromaterialien, Leiterplatten und andere Verbindungsstrukturen und Baugruppen - Teil 5-1: Allgemeine Prüfverfahren für Materialien und Baugruppen - Leitfaden für Baugruppen von Leiterplatten (IEC 61189-5-1:2016)

This European Standard was approved by CENELEC on 2016-08-09. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Avenue Marnix 17, B-1000 Brussels

European foreword

The text of document 91/1273/CDV, future edition 1 of IEC 61189-5-1, prepared by IEC/TC 91 "Electronics assembly technology" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 61189-5-1:2016.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2017-05-09
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2019-08-09

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Endorsement notice

The text of the International Standard IEC 61189-5-1:2016 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60068 (series)	NOTE	Harmonized as EN 60068 (series).
IEC 60068-1:2013	NOTE	Harmonized as EN 60068-1:2014.
IEC 60068-2-20	NOTE	Harmonized as EN 60068-2-20.
IEC 60068-2-58:2015	NOTE	Harmonized as EN 60068-2-58:2015.
IEC 61189-1	NOTE	Harmonized as EN 61189-1.
IEC 61189-5 (series)	NOTE	Harmonized as EN 61189-5 (series).
IEC 61189-5	NOTE	Harmonized as EN 61189-5.
IEC 61189-5-1:2016	NOTE	Harmonized as EN 61189-5-1:2016.
IEC 61189-5-2:2015	NOTE	Harmonized as EN 61189-5-2:2015.
IEC 61189-5-3:2015	NOTE	Harmonized as EN 61189-5-3:2015.
IEC 61189-5-4:2015	NOTE	Harmonized as EN 61189-5-4:2015.
IEC 61189-6	NOTE	Harmonized as EN 61189-6.
IEC 61190-1-1	NOTE	Harmonized as EN 61190-1-1.
IEC 61190-1-2	NOTE	Harmonized as EN 61190-1-2.
IEC 61190-1-3	NOTE	Harmonized as EN 61190-1-3.

IEC 61249-2-7	NOTE	Harmonized as EN 61249-2-7.
IEC 62137:2004	NOTE	Harmonized as EN 62137:2004.
ISO 9001	NOTE	Harmonized as EN ISO 9001.
ISO 9455-1	NOTE	Harmonized as EN 29455-1.
ISO 9455-2	NOTE	Harmonized as EN 29455-2.

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

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FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as “IEC Publication(s)”). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 61189-5-1 has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this standard is based on the following documents:

CDV	Report on voting
91/1273/CDV	91/1354/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 61189 series, published under the general title *Test methods for electrical materials, printed boards and other interconnection structures and assemblies*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

IEC 61189 relates to test methods for printed boards and printed board assemblies, as well as related materials or component robustness, irrespective of their method of manufacture.

The standard is divided into separate parts, covering information for the designer and the test methodology engineer or technician. Each part has a specific focus. Methods are grouped according to their application and numbered sequentially as they are developed and released.

In some instances test methods developed by other technical committees (for example, TC 104) have been reproduced from existing IEC standards in order to provide the reader with a comprehensive set of test methods. When this situation occurs, it will be noted on the specific test method. If the test method is reproduced with minor revisions, those paragraphs that are different are identified.

This part of IEC 61189 contains test methods for evaluating printed board assemblies as well as materials used in the manufacture of electronic assemblies. The methods are self-contained, with sufficient detail and description so as to achieve uniformity and reproducibility in the procedures and test methodologies.

It was decided by TC 91 that the contents of IEC 61189-5 and IEC 61189-6 be merged into a series of documents in the following way:

IEC 61189-5-1, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-1: General test methods for materials and assemblies – Guidance for printed board assemblies*

IEC 61189-5-2:2015, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-2: General test methods for materials and assemblies – Soldering flux for printed board assemblies*

IEC 61189-5-3:2015, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-3: General test methods for materials and assemblies – Soldering paste for printed board assemblies*

IEC 61189-5-4:2015, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-4: General test methods for materials and assemblies – Solder alloys and fluxed and non-fluxed solid wire for printed board assemblies*

IEC 61189-5-501:—, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-501: General test methods for materials and assemblies – Surface insulation resistance (SIR) testing of solder fluxes*[1]

IEC 61189-5-502:—, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-502: General test methods for materials and assemblies – SIR testing of assemblies* [1]

IEC 61189-5-503:—, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-503: General test methods for materials and assemblies – Conductive Anodic Filaments (CAF) testing of circuit* boards [1]

IEC 61189-5-504:—, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-504: General test methods for materials and assemblies – Process ionic contamination testing* [1]

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1 Under consideration.

The tests shown in this standard are grouped according to the following principles:

P: preparation/conditioning methods

V: visual test methods

D: dimensional test methods

C: chemical test methods

M: mechanical test methods

E: electrical test methods

N: environmental test methods

X: miscellaneous test methods including process control tests for the assembly process

To facilitate reference to the tests, to retain consistency of presentation and to provide for future expansion, each test is identified by a number (assigned sequentially) added to the prefix (group code) letter showing the group to which the test method belongs.

The test method numbers have no significance with respect to an eventual test sequence. This responsibility rests with the relevant specification that calls for the method being performed. The relevant specification, in most instances, also describes pass/fail criteria.

The letter and number combinations are for reference purposes to be used by the relevant specification. Thus, "5-2C01" represents the first chemical test method described in IEC 61189-5-2.

In short, in this example, 5-2 is the number of the part of IEC 61189, C is the group of methods, and 01 is the test number.

A list of all test methods included in the above-mentioned documents, is given in Annex A. This annex will be reissued whenever new tests are introduced.

TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

Part 5-1: General test methods for materials and assemblies – Guidance for printed board assemblies

1 Scope

This part of IEC 61189 is a catalogue of test methods representing methodologies and procedures that can be applied to test printed board assemblies.

This part of IEC 61189 contains the types of content of the IEC 61189-5 series, as well as guidance documents and handbooks for printed board assemblies.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

There are no normative references in this document.

3 Accuracy, precision and resolution

3.1 General

Measurement errors and uncertainties are inherent in all measurement processes. The information given below enables valid estimates of the amount of error and uncertainty to be taken into account.

Test data serve a number of purposes which include

- monitoring of a process;
- enhancing of confidence in quality conformance;
- arbitration between customer and supplier.

In any of these circumstances, it is essential that confidence can be placed upon the test data in terms of

- accuracy: calibration of the test instruments and/or system;
- precision: the repeatability and uncertainty of the measurement;
- resolution: the suitability of the test instrument and/or system.

3.2 Accuracy

The regime by which routine calibration of the test equipment is undertaken shall be clearly stated in the quality documentation of the supplier or agency conducting the test and shall meet the requirements of ISO 9001 or equivalent (see Bibliography).

The calibration shall be conducted by an agency having accreditation to a national or international measurement standards institute. There should be an uninterrupted chain of calibration to a national or international standard.

Where calibration to a national or international standard is not possible, round-robin techniques may be used and documented to enhance confidence in measurement accuracy.

The calibration interval shall normally be one year. Equipment consistently found to be outside acceptable limits of accuracy shall be subject to shortened calibration intervals. Equipment consistently found to be well within acceptable limits may be subject to relaxed calibration intervals.

A record of the calibration and maintenance history shall be maintained for each instrument. These records should state the uncertainty of the calibration technique (in ±% deviation) in order that uncertainties of measurement can be aggregated and determined.

A procedure shall be implemented to resolve any situation where an instrument is found to be outside calibration limits.

3.3 Precision

The uncertainty budget of any measurement technique is made up of both systematic and random uncertainties. All estimates shall be based upon a single confidence level, the minimum being 95 %.

Systematic uncertainties are usually the predominant contributor and will include all uncertainties not subject to random fluctuation. These include

- calibration uncertainties;
- errors due to the use of an instrument under conditions which differ from those under which it was calibrated;
- errors in the graduation of a scale of an analogue meter (scale shape error).

Random uncertainties result from numerous sources but can be deduced from repeated measurement of a standard item. Therefore, it is not necessary to isolate the individual contributions. These may include

- random fluctuations such as those due to the variation of an influence parameter. Typically, changes in atmospheric conditions reduce the repeatability of a measurement;
- uncertainty in discrimination, such as setting a pointer to a fiducial mark or interpolating between graduations on an analogue scale.

Aggregation of uncertainties: Geometric addition (root-sum-square) of uncertainties may be used in most cases. An interpolation error is normally added separately and may be accepted as being 20 % of the difference between the finest graduations of the scale of the instrument.

$$U_{\mathrm{t}} = \pm\sqrt{(U_{\mathrm{s}}^2 + U_{\mathrm{r}}^2)} + U_{\mathrm{i}}$$

where

U_{t} is the total uncertainty;

U_{s} is the systematic uncertainty;

U_{r} is the random uncertainty;

U_{i} is the interpolation error.

Determination of random uncertainties: Random uncertainty can be determined by repeated measurement of a parameter and subsequent statistical manipulation of the measured data. The technique assumes that the data exhibits a normal (Gaussian) distribution.

$$U_{\mathrm{r}} = \frac{t \times \sigma}{\sqrt{n}}$$

where

U_{r} is the random uncertainty;

n is the sample size;

t is the percentage point of the t distribution as shown in Table 1;

σ is the standard deviation (σ_{n-1}).

3.4 Resolution

It is paramount that the test equipment used is capable of sufficient resolution. Measurement systems used should be capable of resolving 10 % (or better) of the test limit tolerance.

It is accepted that some technologies will place a physical limitation upon resolution (for example, optical resolution).

3.5 Report

In addition to requirements detailed in the test specification, the report shall detail

a) the test method used;

b) the identity of the sample(s);

c) the test instrumentation;

d) the specified limit(s);

e) an estimate of measurement uncertainty and resultant working limit(s) for the test;

f) the detailed test results;

g) the test date and operators' signature.

3.6 Student's t distribution

Table 1 gives values of the factor t for 95 % and 99 % confidence levels, as a function of the number of measurements.

Table 1 – Student's *t* distribution

Sample size	*t* value 95 %	*t* value 99 %		Sample size	*t* value 95 %	*t* value 99 %
2	12,7	63,7		14	2,16	3,01
3	4,3	9,92		15	2,14	2,98
4	3,18	5,84		16	2,13	2,95
5	2,78	4,6		17	2,12	2,92
6	2,57	4,03		18	2,11	2,9
7	2,45	3,71		19	2,1	2,88
8	2,36	3,5		20	2,09	2,86
9	2,31	3,36		21	2,08	2,83
10	2,26	3,25		22	2,075	2,82
11	2,23	3,17		23	2,07	2,81
12	2,2	3,11		24	2,065	2,8
13	2,18	3,05		25	2,06	2,79

3.7 Suggested uncertainty limits

The following target uncertainties are suggested:

a) Voltage < 1 kV: ± 1,5 %
b) Voltage > 1 kV: ± 2,5 %
c) Current < 20 A: ± 1,5 %
d) Current > 20 A: ± 2,5 %

Resistance

e) Earth and continuity: ± 10 %
f) Insulation: ± 10 %
g) Frequency: ± 0,2 %

Time

h) Interval < 60 s: ± 1 s
i) Interval > 60 s: ± 2 %
j) Mass < 10 g: ± 0,5 %
k) Mass 10 g to 100 g: ± 1 %
l) Mass > 100 g: ± 2 %
m) Force: ± 2 %
n) Dimension < 25 mm: ± 0,5 %
o) Dimension > 25 mm: ± 0,1 mm
p) Temperature < 100 °C: ± 1,5 %
q) Temperature > 100 °C: ± 3,5 %
r) Humidity (30 – 75) % RH: ± 5 % RH

Plating thicknesses

s) Backscatter method: ± 10 %

t) Microsection: ± 2 µm

u) Ionic contamination: ± 10 %

4 Catalogue of approved test methods

This standard provides specific test methods in complete detail to permit implementation with minimal cross-referencing to other specific procedures. The use of generic conditioning exposures is accomplished in the methods by reference, for example, to those described in IEC 61189-1 and IEC 60068-1, and, when applicable, is a mandatory part of the test method standard.

Each method has its own title, number and revision status to accommodate updating and improving the methods as industry requirements change or demand new methodology. The methods are organized in test method groups and individual tests.

5 List of contents of the IEC 61189-5 series

The types of content of existing and planned standards in the IEC 61189-5 series is described in Annex A.

NOTE The details of the standards "under consideration" are not yet available.

Annex A
(informative)

Tests

Table A.1 gives a summary of the existing tests and of the tests under development.

Table A.1 – General test methods for materials and assemblies

IEC standard	Designation	Test
IEC 61189-5-2	C: Chemical test methods	
	5-2C01	Corrosion, flux
	5-2C02	Determination of acid value of liquid soldering flux potentiometric and visual titration methods
	5-2C03	Acid number of rosin
	5-2C04	Determination of halides in fluxes, silver chromate method
	5-2C05	Solids content, flux
	5-2C06	Quantitative determination of halide content in fluxes (chloride and bromide)
	5-2C07	Qualitative analysis of fluorides and fluxes by spot test
	5-2C08	Quantitative determination of fluoride concentration in fluxes
	5-2C09	Specific gravity
	5-2C10	Flux induced corrosion (copper mirror method)
	X: Miscellaneous test methods	
	5-2X01	Liquid flux activity, wetting balance method
	5-2X02	Spread test, liquid or extracted solder flux, solder paste and extracted cored wires or preforms
	5-2X03	Flux residues – Tackiness after drying
IEC 61189-5-3	X: Miscellaneous test methods	
	5-3X01	Paste flux viscosity – T-Bar spindle method
	5-3X02	Spread test, extracted solder flux, paste flux and solder paste
	5-3X03	Solder paste viscosity – T-Bar spin spindle method (applicable for 300 Pa•s to 1 600 Pa•s)
	5-3X04	Solder paste viscosity – T-Bar spindle method (applicable to 300 Pa•s)
	5-3X05	Solder paste viscosity – Spiral pump method (applicable for 300 Pa•s to 1 600 Pa•s)
	5-3X06	Solder paste viscosity – Spiral pump method (applicable to 300 Pa•s)
	5-3X07	Solder paste – Slump test
	5-3X08	Solder paste – Solder ball test
	5-3X09	Solder paste – Tack test
	5-3X10	Solder paste – Wetting test
	5-3X11	Determination of solder powder particle size distribution – Screen method for types
	5-3X12	Solder powder particle size distribution – Measuring microscope method
	5-3X13	Solder powder particle size distribution – Optical image analyser method
	5-3X14	Solder powder particle size distribution – Measuring laser diffraction method
	5-3X15	Determination of maximum solder powder particle size
	5-3X16	Solder paste metal content by weight

IEC standard	Designation	Test
IEC 61189-5-4	C: Chemical test methods	
	5-4C01	Determination of the percentage of flux on/in flux-coated and/or flux-cored solder
	X: Mechanical test methods	
	5-4X01	Spread test, extracted cored wires or preforms
	5-4X02	Spitting test of flux-cored wire solder
	5-4X03	Solder pool test
IEC 61189-5-501		Under consideration
IEC 61189-5-502		Under consideration
IEC 61189-5-503		Under consideration
IEC 61189-5-504		Under consideration

Annex B
(informative)

Guidance documents and handbooks

B.1 General

The documents listed in Clauses B.2 to B.23 relate to the specific soldering materials or test methods employed.

B.2 Handbook and guide to supplement IPC-J-STD-001

IPC-J-STD-001 and IPC-HDBK-001 do not exclude any acceptable process used to make the electrical connections, as long as the methods used will produce completed solder joints conforming to the acceptability requirements of the IPC-J-STD-001.

This handbook describes materials, methods, and verification criteria that, when applied as recommended or required, will produce quality soldered electrical and electronic assemblies. The intent of this handbook is to explain the ‘‘how-to,’’ the ‘‘why,’’ and fundamentals for these processes, in addition to implementing control over processes rather than depending on end-item inspection to determine product quality.

B.3 Guidelines for Electrically Conductive Surface Mount Adhesives (IPC-3406)

This document covers guidelines for selecting electrically conductive adhesives for use in assembly of components to printed circuit boards (PCB) or similar wiring inter-connect systems. The focus is on the use of adhesives as solder alternatives. The process discussion attempts to stay within the bounds of the existing solder assembly infrastructure as much as possible. Both major types of adhesives, isotropic (conducting equally in all directions) and anisotropic (unidirectional conductivity), are covered. The two major divisions of polymer adhesives, thermosets and thermoplastics, are described.

B.4 Users Guide for Cleanliness of Unpopulated Printed Boards (IPC-5701)

If you are in the electronics industry, sooner or later you have to, will, or should deal with the issue of the cleanliness of the unpopulated printed circuit boards (bare boards). Residues on circuit boards are directly related to the reliability of the produced hardware and can result in serious failures if not monitored and controlled.

This document is the product of the IPC Bare Board Cleanliness Assessment Task Group and was drafted to provide individuals who deal with these issues some guidance on how the issues should be approached and specified in purchase documents.

B.5 Guidelines for OEM’s in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards (IPC-5702)

Every electronics manufacturer, whether an original equipment manufacturer (OEM) or contract manufacturer (CM), will be faced with determining if the unpopulated printed boards used in the finished assembly have an adequate level of cleanliness. The question of ‘‘how clean is clean enough’’ has been asked repeatedly in the last decade in many IPC committees. This is a very complex topic, with many critical considerations. For this reason there is not an unique methodology that determines acceptability. This document was developed as guidance for the individual(s) responsible for determining these criteria for their company.

IPC-5701 covers many aspects of how cleanliness is measured on printed boards, as well as many critical factors to consider when specifying board cleanliness in purchasing documents. This reference, and associated technical papers, show the many inadequacies of current test methodologies, as well as explaining why there are no ‘‘golden numbers’’ for cleanliness. What is acceptably clean for one segment of the industry may be unacceptable for more demanding segments of the industry (e.g., medical or aerospace).

B.6 Surface Insulation Resistance Handbook (IPC-9201)

This document is intended to cover the broad spectrum of temperature-humidity (TH) testing, associated terminology, and suggested techniques for proper surface insulation resistance testing as defined in IEC 61189-5-5, Test Methods 5E01 and 5E02.

B.7 Material and Process Characterisation / Qualification Test Protocol for Assessing Electrochemical Performance (IPC-9202)

This material and process characterization/qualification test records changes in surface insulation resistance (SIR) on a representative sample of a printed circuit assembly (PCA). It quantifies any deleterious effects that might arise from solder flux or other process residues left on external surfaces after soldering, which can cause unwanted electro-chemical reactions that grossly affect reliability.

It uses test vehicles that are intended to be representative of the electronic circuits that are in production. It is a test yielding both quantitative and qualitative data.

This test may be used for *Process Qualification*, demonstrating that a proposed manufacturing process or process change can produce hardware with acceptable end-item performance related to cleanliness. Changes may involve any assembly process step, or a change in the printed board supplier, solder mask or metallization, soldering material supplier, conformal coating, etc. The test vehicle construction will vary depending upon the type of change being evaluated.

B.8 User Guide for the IPC/IEC B52 Process Qualification Test Vehicle (IPC-9203)

The electronics manufacturing process is often very complex, with dozens of variables that impact the quality and reliability of the manufactured assemblies in the end use environment. Two of the important variables for consideration are the kinds of residues that remain on the electronic assembly and the effects that these residues have on reliability. These two variables are most often referred to in discussions on assembly “cleanliness”.

Whilst there are several different ways to measure residues and their effects on electrical performance, the two most common approaches in the industry are ionic cleanliness testing, for determination of ionic residues, and surface insulation resistance (SIR) testing, for the evaluation of electrochemical failures in humid environments.

This document focuses on the IPC-B-52 standard test assembly and how it is used as an evaluation tool for electronics manufacturing processes from a “cleanliness” perspective.

B.9 PWB Assembly Soldering Process Guideline for Electronic Components (IPC-9502)

This document describes manufacturing solder process limits that components subjected to IPC-9501, IPC-9503, IPC-9504 and J-STD-020 would survive. It does not include optimum conditions for assembly, but rather guides to assure components are not damaged.

This document applies to both surface-mount (SM) and through-hole (TH) components that are wave soldered, reflowed or hand soldered. This document is intended to complement other industry documents, listed in applicable documents.

B.10 Aqueous Post Solder Cleaning Handbook (IPC-AC-62A)

This handbook addresses aqueous cleaning of electrical/electronic parts and application tools after soldering.

The content of the text is intended to provide a basic understanding of the subject and to serve as a guide to users or prospective users of aqueous cleaning technology, allowing selection or improvement of aqueous cleaning processes.

B.11 Guidelines for Cleaning of Printed Boards and Assemblies (IPC-CH-65A)

This manual is a road map for current and developing cleaning issues, rather than to function as a highly detailed document for all areas touched upon. In areas of cleaning where recent detailed IPC manuals already exist, the relevant sections in IPC-CH-65A will contain only sufficient information to make the reader reasonably knowledgeable. This guideline manual refers the reader to appropriate existing IPC documents (where they exist) for in-depth information on the particular subject. An example of such a reference IPC manual is IPC-AC-62, *Aqueous Cleaning Handbook.* It is only where existing IPC documents are not available that IPC-CH-65A will expand information beyond the basics in order to cover what is currently known about the subject. A benefit of this approach is that the manual does not become unwieldy and tends to foster a user-friendly environment.

Both bare board fabrication and assembly cleanliness issues are addressed. The fabrication and assembly sections are separated for ease of access. In the original IPC-CH-65, these sections were very much intertwined. However, it was recognized that for a subject such as the required cleanliness of finished bare boards, basically redundant teachings are required for both the fabrication and assembly sections.

B.12 Handbook (IPC-J-STD-005)

This handbook is a companion to the solder paste standard J-STD-005 and should be considered to be a guide to help assess the applicability of a solder paste for its use in surface-mount technology (SMT) processes. This document also suggests some test methods that can help with designing and testing solder pastes. It is intended for use by both vendors and users of solder paste.

Solder pastes are unique materials, whose performance in a surface-mount process depends on a variety of variables, many of them interacting. J-STD-005 provides test methods for classification of solder paste based on the use of a variety of testing techniques. However, these solder paste classifications do not have a direct correlation to identify the type and characteristics of a specific solder paste that is needed in any given SMT assembly process.

This document has been written as a guide to assess the applicability of a solder paste for a specific process, given the tremendous number of permutations of different materials, atmospheres and process variables currently available.

Where appropriate, references are given to papers and documents with further information. Due to the sheer number of possible interacting factors, specific solder paste selection criteria cannot be given. The solder paste selected and the assembly process used will need to form solder connections that meet the requirements of industry standards such as J-STD-001 and/or IPC-A-610.

B.13 Acceptability of Electronic Assemblies (IPC-HDBK-610)

This handbook is a companion reference to IPC-A-610C and IPC-A-610C Amendment 1 and was prepared using them. The amendment provides additional criteria and clarification statements. The amendment is included with this handbook following Appendix C and can be downloaded free of charge from the IPC website at the following link: http://www.ipc.org/TOC/IPC-HDBK-610-w-Amend-1.pdf.

The intent of this handbook is to explain the technical rationale for selected acceptability, process indicator and defect criteria and to provide information regarding assembly technology. Additional information is provided to give a broader understanding of the process considerations needed for the production of acceptable hardware.

B.14 Guidelines for Design, Selection and Application of Conformal Coatings (IPC-HDBK-830)

Conformal coatings are used in conjunction with printed circuit assemblies (PCAs). The designer and the users of conformal coatings for electronics applications should be aware of the properties of various types of conformal coatings and their interactions with PCAs to protect the PCAs in the end-use environment for the design-life of the PCA (or beyond). This document has been written to assist the designers and users of conformal coatings in understanding the characteristics of various coating types, as well as the factors that can modify those properties when the coatings are applied. Understanding and accounting for these materials can ensure the reliability and function of electronics.

The purpose of this handbook is to assist the individuals who either make choices regarding conformal coating or who work in coating operations. This handbook represents the compiled knowledge and experience of the IPC Conformal Coating Handbook Task Group. It is not enough to understand the properties of the various conformal coatings. The user needs to understand what is to be achieved by applying the conformal coating and how to verify that the desired results have been realized.

B.15 Solder mask Handbook (IPC-HDBK-840)

Solder masks are permanent protective coatings that perform a number of functions during the fabrication, assembly and end use of printed circuits. One of the main purposes of solder mask is to protect the circuitry from interacting with solder during the assembly process. A solder mask's job isn't solely restricted to the solder operation however, as it also helps to protect the laminate, holes and traces from collecting contaminants and from degrading during the service life of the circuit. It also acts as an insulator of known dielectric property between components and traces.

The main requirements of the solder mask (as a material qualification) are tested within the IPC-SM-840. However, increasing technical diversification created further testing needs. Not every technical requirement is relevant for every application and thus these requirements will not be part of a general material qualification. These properties are usually required for specific original equipment manufacturer's (OEM) approvals. This solder mask handbook provides the reader with the background knowledge to make an educated decision if specific properties are required and how to test them. It also provides significant educational information about process influences.

The purpose of this handbook is to provide additional supporting information for IPC-SM-840 regarding solder mask types, processes, characteristics and properties in order to assist with the correct selection and use of the most appropriate material for the intended application. It should be read in conjunction with the solder mask manufacturer's technical information and other solder mask specification documents, which may be relevant, such as those listed in Section 2 of IPC-HDBK-840.

B.16 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards (IPC-9252)

This document is presented to assist in selecting the test analyzer, test parameters, test data, and fixturing required to perform electrical test(s) on all unpopulated printed boards without embedded components (i.e., resistors, capacitors, etc.).

The users shall determine the test parameters and fixturing requirements to test for continuity (open), isolation (leakage/short), and other special characteristics (i.e., impedance, hipot, capacitance, current carrying capacity, etc.) that will satisfactorily evaluate the critical electrical characteristics of specific printed boards. The testing levels listed in this document define some of these parameters.

Electrical testing verifies that the printed networks on the boards are interconnected according to design requirements.

Electrical test does not ensure that the board can be assembled or that the board meets all of the customer's requirements. Many physical characteristics of the conductors (dimensional accuracy, solder mask, conductor geometry and nomenclature registration, presence of holes, etc.) can't be determined by electrical test. Other checks should be employed to confirm these characteristics.

B.17 In-Process DPMO and Estimated Yield for PCAs (IPC-9261A)

This document defines standard methodologies for calculating defects per million opportunities (DPMO) metrics related to electronic printed board assembly processes. It is intended for use in measuring in-process assembly steps rather than end product determination. Calculation of completed item DPMO is addressed in IPC-7912.

Additionally, a guide to defect categorization is provided that when used with J-STD-001 and IPC-A-610 can serve as a base for summarizing and reporting in-process defects.

Note that this document does not dictate the number of assemblies or data points needed to calculate DPMO metrics.

The purpose of this document is to define consistent methodologies for computation of **in-process** DPMO metrics for any defect evaluation stage in the assembly process.

This objective anticipates the following conditions in defect reporting and analysis.

- To facilitate process improvement, defects discovered at any stated inspection or test point should be assigned to their appropriate process step.
- All defects shall be reported at the inspection point they are found, even though one undetected previous defect may have caused the subsequent defects.
- Regardless of how these defects are assigned, the defect shall be attributed to either a component, placement, termination or assembly defect.
- The assumption is that each printed board assembly that is inspected will be 100 % inspected for all defects.
- The assumption of 100 % inspection efficiency is made. Care should be taken when comparing processes using manual inspection to those using automated vision inspection.
- When using a sampling inspection plan, the number of PCAs inspected determines the opportunity count, not the number processed.

B.18 Assembly Soldering Process Guideline for Electronic Components (IPC-9502 PWB)

This document describes manufacturing solder process limits that components subjected to IPC-9501, IPC-9503, IPC-9504 and J-STD-020 would survive. It does not include optimum conditions for assembly, but rather guides to ensure components are not damaged.

This document applies to both surface-mount (SM) and through-hole (TH) components that are wave soldered, reflowed or hand soldered. This document is intended to complement other industry documents, listed in applicable documents.

B.19 Users Guide for IPC-TM-650, Method 2.6.27, Thermal Stress, Convection Reflow Assembly Simulation (IPC-9631)

The intention of this document is to aid users of IPC-TM-650, Method 2.6.27, *Thermal Stress, Convection Reflow Assembly Simulation*. This test method has been developed because IPC-TM-650, Method 2.6.8, *Thermal Stress, Plated-Through Holes* (thermal stress by solder float) is no longer considered adequate for simulating the assembly process and stresses that many products now have to support. Over many years the assembly process has continued to diverge from wave soldering, with the addition of top, and then bottom, surface-mount devices, large BGA packages where solder joints are hidden, an ever increasing density of devices which increase the thermal mass and thermal stress needed to melt solder, and more recently the switch to higher melt temperature, lead-free solders. In summary, adding more and more cycles of the Method 2.6.8 solder float was no longer sufficient to screen out printed boards that would then fail during assembly due to the very different thermal stresses encountered. This document was developed by the IPC D-32, Thermal Stress Test Method Subcommittee, that developed IPC-TM-650, Method 2.6.27, with the understanding that the test method will require special equipment and the proper set-up and calibration of that equipment.

The IPC-TM-650, Method 2.6.27, is intended to establish a relative ability of printed boards, or representative coupons, to survive the thermal excursions associated with assembly and rework in a tin/lead or lead-free application using a convection oven, or alternate equipment with the capability to match the reflow profile of a convection oven. The test embraces relative robustness of the copper interconnection and dielectric materials subjected to the strain and resulting stress associated with a standardized thermal profile. The purpose is to establish an objective measurement of relative robustness ranking or comparing variables, or establishing minimum reliability requirements for copper interconnections and dielectric material in a printed board. The purpose of the test method is to provide the procedure for conditioning and reflowing of the test specimen prior to evaluation for compliance to the applicable performance specification, i.e., IPC-6012, IPC-6013, IPC-6018, etc.

The primary purpose of this document is to address concerns and considerations related to IPC-TM-650, Method 2.6.27. This document embraces how this test method was intended for use and the rationale behind some of the protocols and requirements. This document provides an adjunct document that improves the understanding, application, and the implication of results from using this test method.

B.20 High Temperature Printed Board Flatness Guideline (IPC-9641)

During the surface mount assembly process of an electronic package to a printed board through a reflow temperature profile, the flatness behavior of both the package and printed board are critical for the integrity of solder joint formation and reliability. While the deviation of the package from planarity during this process is critical, controlling the printed board flatness is equally important for preventing subsequent assembly-related issues, including open or bridging joints, which ultimately cause product failure. Board flatness is largely driven by a change in intrinsic properties through exposure to changes in temperature, with the final flatness state becoming a function of the entire temperature history or reflow profile and support boundary conditions. It is also driven by copper symmetry stack-up and metal pattern

balancing. The worst-case deviation of the printed board from flatness may be at room temperature, peak temperature during reflow, or at any temperature in between. Therefore, printed board flatness shall be characterized during the entire reflow thermal cycle, and not solely at room temperature at the beginning and end of the process. This document aims to provide guidance on methods and procedures for critically evaluating printed board flatness during a simulated temperature reflow cycle.

The purpose of this test method is to measure the shape and relative change in shape of a local area of interest (e.g., flip-chip ball grid array (FCBGA) land area) of printed boards through a range of temperatures typical during surface-mount and through-hole builds of integrated circuit packages to printed boards. The use of shape measurements and relative changes in shape will depend on the specific application and interest of the user performing the measurement. This guideline differs from and does not supersede IPC-TM-650, Method 2.4.22, which is used for inspection of bow and/or twist of bare printed boards at room temperature.

B.21 User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Testing) (IPC-9691A)

This document is the product of the IPC Electrochemical Migration (ECM) Task Group. It was drafted to provide guidance regarding how the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance test can best be used for evaluating the effects of mechanical stress, laminate material fracturing, ionic contamination, moisture content prior to press lamination, and other material processing characteristics on conductive anodic filament (CAF) resistance test method results. This CAF test method provides a proven standard for determining the risk of temperature, humidity and bias (THB) failure within rather than on the surface of printed circuit boards (PCBs), typically filament formation along the boundary between the resin and laminate reinforcement.

B.22 Mechanical Shock Test Guidelines for Solder Joint Reliability (IPC-JEDEC-9703)

With the growth of electronics and the increased accessibility and portability, drop shock and other mechanical impacts are increasingly a concern. This document attempts to improve past mechanical shock test methods, and ties test conditions back to the use-conditions. A method is proposed such that regardless of what level (system, board assembly, simplified single component board testing, etc.) of testing is conducted, there should be a correlation back to the use-condition. In order to fulfill this goal, additional metrologies are introduced to aid in these correlations.

Following the requisite introductory sections, the concept of use-conditions is introduced and suggestions are made on how use-condition data may be acquired and applied. Next, the testing methods for fully assembled systems are introduced. Options for test conditions are discussed and the data that should be collected is outlined.

Testing of subassemblies and components imitate actual use configurations less than the testing of fully assembled systems. However, the next two document sections outline considerations to ensure that testing carried out at these levels remains relevant to the intended use-condition.

Specific metrics to aid in correlations are outlined in Section 8. The informative annexes that close the document discuss the common considerations of all mechanical shock testing methods. These include a sample reporting format for test data, use and application of strain gauges, accelerometers, and high speed photography. A section on failure analysis is given. Finally, a review of finite element methods that may be applied to mechanical shock analysis is given to aid in more in-depth study of shock problems.

This document establishes mechanical shock test guidelines to assess solder joint reliability of printed circuits.

The three main categories discussed within are the following:

- methods to define mechanical shock use-conditions;
- methods to define system level, system board level and component test board level testing that correlate to the use-conditions;
- guidance on the use of experimental metrologies for mechanical shock tests.

B.23 Printed Circuit Assembly Strain Gage Test Guideline (IPC-JEDEC-9704A)

This document is meant to be used as a methodology for strain gauge placement and subsequent testing of printed circuit assemblies (PCAs) using strain gauges. The method describes specific guidelines for strain gage testing of PCAs during the printed board manufacturing process, including assembly, test, system integration, and other types of operations that may induce board flexure.

The suggested procedure enables printed board assemblers to conduct strain gauge testing independently, and provides a quantitative method for measuring board flexure, and assessing risk levels.

The topics covered include:

- test setup and equipment requirements;
- strain measurement;
- report format.

This document assumes the methodology is being used to test a surface-mount device such as ball grid array (BGA), small outline package (SOP), chip scale (size) package (CSP), and area-array surface-mount (SMT) connectors/sockets. In certain cases, the described test approach may be used for non-area-array discrete (SMT) devices such as capacitors or resistors.

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IEC 61189-5-3:2015, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-3: General test methods for materials and assemblies – Soldering paste for printed board assemblies*

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2 Under consideration.

IEC 61189-5-503:—, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-503: General test methods for materials and assemblies – Conductive Anodic Filaments (CAF) testing of circuit* boards [3]

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IEC 61190-1-1, *Attachment materials for electronic assembly – Part 1-1: Requirements for soldering fluxes for high-quality interconnections in electronics assembly*

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IPC-J-STD-005, *Requirements for Soldering Pastes*

IPC-J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*

IPC-JEDEC-9703, *Mechanical Shock Test Guidelines for Solder Joint Reliability*

IPC-JEDEC-9704A, *Printed Circuit Assembly Strain Gage Test Guideline*

IPC-HDBK-001, *Handbook and Guide to Supplement J-STD-001*

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IPC-5702, *Guidelines for OEM's in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Board*

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IPC-6013, *Qualification and Performance Specification for Flexible Printed Boards*

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IPC-9502, *PWB Assembly Soldering Process Guideline for Electronic Components*

IPC-9503, *Moisture Sensitivity Classification for Non-IC Components*

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IPC-9631, *Users Guide for IPC-TM-650, Method 2.6.27, Thermal Stress, Convection Reflow Assembly Simulation*

IPC-9641, *High Temperature Printed Board Flatness Guideline*

IPC-9691A, *User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Testing)*

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