BS EN 60749-26:2014

BSI Standards Publication

Semiconductor devices — Mechanical and climatic test methods

Part 26: Electrostatic discharge (ESD) sensitivity testing — Human body model (HBM)

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National foreword

This British Standard is the UK implementation of EN 60749-26:2014. It is identical to IEC 60749-26:2013. It supersedes BS EN 60749-26:2006 which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

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Published by BSI Standards Limited 2014

ISBN 978 0 580 76099 0
ICS 31.080.01

Compliance with a British Standard cannot confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 30 June 2014.

Amendments/corrigenda issued since publication

Amd. No.	Date	Text affected

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 60749-26

May 2014

ICS 31.080.01

Supersedes EN 60749-26:2006

English Version

Semiconductor devices - Mechanical and climatic test methods - Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM) (IEC 60749-26:2013)

Dispositifs à semiconducteurs - Méthodes d'essais mécaniques et climatiques - Partie 26: Essai de sensibilité aux décharges électrostatiques (DES) - Modèle du corps humain (HBM)
(CEI 60749-26:2013)

Halbleiterbauelemente - Mechanische und klimatische Prüfverfahren - Teil 26: Prüfung der Empfindlichkeit gegen elektrostatische Entladungen (ESD) - Human Body Model (HBM)
(IEC 60749-26:2013)

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CEN-CENELEC Management Centre: Avenue Marnix 17, B-1000 Brussels

Foreword

This document (EN 60749-26:2014) consists of the text of IEC 60749-26:2013 prepared by IEC/TC 47 "Semiconductor devices", in collaboration with Technical Committee 101.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2015-04-14
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2017-04-14

This document supersedes EN 60749-26:2006.

EN 60749-26:2014 includes the following significant technical changes with respect to EN 60749-26:2006:

a) descriptions of oscilloscope and current transducers have been refined and updated;

b) the HBM circuit schematic and description have been improved;

c) the description of stress test equipment qualification and verification has been completely re-written;

d) qualification and verification of test fixture boards has been revised;

e) a new section on the determination of ringing in the current waveform has been added;

f) some alternate pin combinations have been included;

g) allowance for non-supply pins to stress to a limited number of supply pin groups (associated non-supply pins) and allowance for non-supply to non-supply (i.e., I/O to I/O) stress to be limited to a finite number of 2 pin pairs (coupled non-supply pin pairs);

h) explicit allowance for HBM stress using 2 pin HBM testers for die only shorted supply groups.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 60749-26:2013 was approved by CENELEC as a European Standard without any modification.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu

Publication	Year	Title	EN/HD	Year
IEC 60749-27	-	Semiconductor devices - Mechanical and climatic test methods - Part 27: Electrostatic discharge (ESD) sensitivity testing - Machine model (MM)	EN 60749-27	-

CONTENTS

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)

1 Scope

This standard establishes the procedure for testing, evaluating, and classifying components and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

The purpose (objective) of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

ESD testing of semiconductor devices is selected from this test method, the machine model (MM) test method (see IEC 60749-27) or other ESD test methods in the IEC 60749 series. The HBM and MM test methods produce similar but not identical results; unless otherwise specified, this test method is the one selected.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-27, *Semiconductor devices – Mechanical and climatic test methods – Part 27: Electrostatic discharge (ESD) sensitivity testing – Machine model (MM)*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
associated non-supply pin
non-supply pin (typically an I/O pin) associated with a supply pin group

Note 1 to entry: A non-supply pin is considered to be associated with a supply pin group if either:

a) The current from the supply pin group (i.e., VDDIO) is required for the function of the electrical circuit(s) (I/O driver) that connect (high/low impedance) to that non-supply pin.

b) A parasitic path exists between non-supply and supply pin group (e.g., open-drain type non-supply pin to a VCC supply pin group that connects to a nearby N-well guard ring).

3.2
component
item such as a resistor, diode, transistor, integrated circuit or hybrid circuit

3.3
component failure
condition in which a tested component does not meet one or more specified static or dynamic data sheet parameters

3.4
coupled non-supply pin pair
two pins that have an intended direct current path (such as a pass gate or resistors, such as differential amplifier inputs, or low voltage differential signaling (LVDS) pins), including analogue and digital differential pairs and other special function pairs (e.g., D+/D-, XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP_DP/CCN_DN etc.)

3.5
data sheet parameters
static and dynamic component performance data supplied by the component manufacturer or supplier

3.6
withstand voltage
highest voltage level that does not cause device failure

Note 1 to entry: The device passes all tested lower voltages (see failure Window).

3.7
failure window
intermediate range of stress voltages that can induce failure in a particular device type, when the device type can pass some stress voltages both higher and lower than this range

Note 1 to entry: A component with a failure window may pass a 500 V test, fail a 1 000 V test and pass 2 000 V test. The withstand voltage of this device is 500 V.

3.8
human body model electrostatic discharge
HBM ESD
ESD event meeting the waveform criteria specified in this standard, approximating the discharge from the fingertip of a typical human being to a grounded device

3.9
HBM ESD tester
HBM simulator
equipment that applies an HBM ESD to a component

3.10
I_{ps}
peak current value determined by the current at time t_{max} on the linear extrapolation of the exponential current decay curve, based on the current waveform data over a 40 nanosecond period beginning at t_{max}

SEE: Figure 2 a).

3.11
I_{psmax}
highest current value measured including the overshoot or ringing components due to internal test simulator RLC parasitics

SEE: Figure 2 a).

3.12
no connect pin
package interconnection that is not electrically connected to a die

EXAMPLE: Pin, bump, ball interconnection.

Note 1 to entry: There are some pins which are labelled as no connect, which are actually connected to the die and should not be classified as a no connect pin.

3.13
non-socketed tester
HBM simulator that makes contact to the device under test (DUT), pins (or balls, lands, bumps or die pads) with test probes rather than placing the DUT in a socket

3.14
non-supply pins
all pins not categorized as supply pins or no connects

Note 1 to entry: This includes pins such as input, output, offset adjusts, compensation, clocks, controls, address, data, Vref pins and VPP pins on EPROM memory. Most non-supply pins transmit or receive information such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

3.15
package plane
low impedance metal layer built into an IC package connecting a group of bumps or pins (typically power or ground)

Note 1 to entry: There may be multiple package planes (sometimes referred to as islands) for each power and ground group.

3.16
pre-pulse voltage
voltage occurring at the device under test (DUT) just prior to the generation of the HBM current pulse

SEE: Clause C.2.

3.17
pulse generation circuit
dual polarity pulse source circuit network that produces a human body discharge current waveform

Note 1 to entry: The circuit network includes a pulse generator with its test equipment internal path up to the contact pad of the test fixture. This circuit is also referred to as dual polarity pulse source.

3.18
ringing
high frequency oscillation superimposed on a waveform

3.19
shorted non-supply pin
any non-supply pin (typically an I/O pin) that is metallically connected (typically $< 3\ \Omega$) on the chip or within the package to another non-supply pin (or set of non-supply pins)

3.20
spurious current pulses
small HBM shaped pulses that follow the main current pulse, and are typically defined as a percentage of I_{psmax}

3.21
socketed tester
an HBM simulator that makes contact to DUT pins (or balls, lands, bumps or die pads) using a DUT socket mounted on a test fixture board

3.22
static parameters
parameters measured with the component in a non-operating condition

Note 1 to entry: These may include, but are not limited to, input leakage current, input breakdown voltage, output high and low voltages, output drive current, and supply current.

3.23
step stress test hardening
ability of a component subjected to increasing ESD voltage stresses to withstand higher stress levels than a similar component not previously stressed

EXAMPLE: A component may fail at 1 000 V if subjected to a single stress, but fail at 3 000 V if stressed incrementally from 250 V.

3.24
supply pin
any pin that provides current to a circuit

Note 1 to entry: Supply pins typically transmit no information (such as digital or analogue signals, timing, clock signals, and voltage or current reference levels). For the purpose of ESD testing, power and ground pins are treated as supply pins.

3.25
test fixture board
specialized circuit board, with one or more component sockets, which connects the DUT(s) to the HBM simulator

3.26
t_{max}
time when I_{ps} is at its maximum value (I_{psmax})

SEE: Figure 2a).

3.27
trailing current pulse
current pulse that occurs after the HBM current pulse has decayed

SEE: Clause C.1.

Note 1 to entry: A trailing current pulse is a relatively constant current often lasting for hundreds of microseconds.

3.28
two pin tester
A low parasitic HBM simulator that tests DUTs in pin pairs where floating pins are not connected to the simulator thereby eliminating DUT-tester interactions from parasitic tester loading of floating pins

4 Apparatus and required equipment

4.1 Waveform verification equipment

All equipment used to evaluate the tester shall be calibrated in accordance with the manufacturer's recommendation. This includes the oscilloscope, current transducer and high voltage resistor load. Maximum time between calibrations shall be one year. Calibration shall be traceable to national or international standards.

Equipment capable of verifying the pulse waveforms defined in this standard test method includes, but is not limited to, an oscilloscope, evaluation loads and a current transducer.

4.2 Oscilloscope

A digital oscilloscope is recommended but analogue oscilloscopes are also permitted. In order to ensure accurate current waveform capture, the oscilloscope shall meet the following requirements:

a) Minimum sensitivity of 100 mA per major division when used in conjunction with the current transducer specified in 4.4;

b) Minimum bandwidth of 350 MHz;

c) For analogue scopes, minimum writing rate of one major division per nanosecond.

4.3 Additional requirements for digital oscilloscopes

Where a digital oscilloscope is used the following additional requirements apply:

a) Recommended channels: 2 or more;

b) Minimum sampling rate: 10^9 samples per second;

c) Minimum vertical resolution: 8-bit;

d) Minimum vertical accuracy: $\pm$ 2,5 %;

e) Minimum time base accuracy: 0,01 %;

f) Minimum record length: 10 k points.

4.4 Current transducer (inductive current probe)

a) Minimum bandwidth of 200 MHz;

b) Peak pulse capability of 12 A;

c) Rise time of less than 1 ns;

d) Capable of accepting a solid conductor as specified in 4.5;

e) Provides an output voltage per signal current as required in 4.2

(This is usually between 1 mV/mA and 5 mV/mA.);

f) Low-frequency 3 dB point below 10 kHz (e.g., Tektronix CT2) for measurement of decay constant t_d (see 5.2.3.2, Table 1, and Note below).

NOTE Results using a current probe with a low-frequency 3 dB point of 25 kHz (e.g., Tektronix CT1) to measure decay constant t_d are acceptable if t_d is found to be between 130 ns and 165 ns.

4.5 Evaluation loads

Two evaluation loads are necessary to verify tester functionality:

a) Load 1: A solid 18 – 24 AWG (non-US standard wire size 0,25 to 0,75 mm^2 cross-section) tinned copper shorting wire as short as practicable to span the distance between the two farthest pins in the socket while passing through the current probe or long enough to pass through the current probe and contacted by the probes of the non-socketed tester.

b) Load 2: A 500 Ω, $\pm$ 1 %, minimum 4 000 voltage rating.

4.6 Human body model simulator

A simplified schematic of the HBM simulator or tester is given in Figure 1. The performance of the tester is influenced by parasitic capacitance and inductance. Thus, construction of a tester using this schematic does not guarantee that it will provide the HBM pulse required for this standard. The waveform capture procedures and requirements described in Clause 5 determine the acceptability of the equipment for use.

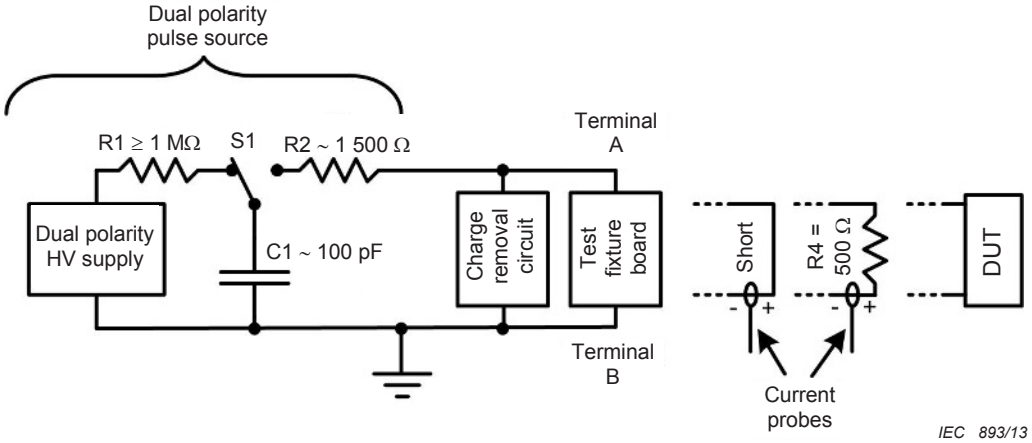


Figure 1 – Simplified HBM simulator circuit with loads

The charge removal circuit shown in Figure 1 ensures a slow discharge of the device, thus avoiding the possibility of a charged device model discharge. A simple example is a 10 kΩ or larger resistor (possibly in series with a switch) in parallel with the test fixture board. This resistor may also be useful to control parasitic pre-pulse voltages (See Annex C). The dual polarity pulse generator (source) shall be designed to avoid recharge transients and double pulses. It should be noted that reversal of terminals A and B to achieve dual polarity performance is not permitted. Stacking of DUT socket adapters (piggybacking or insertion of secondary sockets into the main test socket) is allowed only if the secondary socket waveform meets the requirements of this standard defined in Table 1.

NOTE 1 The current transducers (probes) are specified in 4.4.

NOTE 2 The shorting wire (short) and 500 Ω resistor (R4) are evaluation loads specified in 4.5.

NOTE 3 Component values are nominal.

4.7 HBM test equipment parasitic properties

Some HBM simulators have been found to falsely classify HBM sensitivity levels due to parasitic artifacts or uncontrolled voltages unintentionally built into the HBM simulators. Methods for determining if these effects are present and optional mitigation techniques are described in Annex C. Two-pin testers and non-socketed testers may have smaller parasitic capacitances and may reduce the effects of tester parasitics by contacting only the pins being stressed.

5 Stress test equipment qualification and routine verification

5.1 Overview of required HBM tester evaluations

The HBM tester and test fixture boards shall be qualified, re-qualified, and periodically verified as described in this clause. The safety precautions described in 5.8 shall be followed at all times.

5.2 Measurement procedures

5.2.1 Reference pin pair determination

The two pins of each socket on a test fixture board which make up the reference pin pair are (1) the socket pin with the shortest wiring path of the test fixture to the pulse generation circuit (terminal B) and (2) the socket pin with the longest wiring path of the test fixture from the pulse generation circuit (terminal A) to the ESD stress socket (See Figure 1). This information is typically provided by the equipment or test fixture board manufacturer. If more than one pulse generation circuit is connected to a socket then there will be more than one reference pin pair.

It is strongly recommended that on non-positive clamp fixtures, feed through test point pads be added on these paths to allow connection of either the shorting wire or 500 Ω load resistor during waveform verification measurements. These test points should be added as close as possible to the socket(s), and if the test fixture board uses more than one pulse generator, multiple feed through test points should be added for each pulse generator's longest and shortest paths.

NOTE A positive clamp test socket is a zero insertion force (ZIF) socket with a clamping mechanism. It allows the shorting wire to be easily clamped into the socket. Examples are dual in-line package (DIP) and pin grid array (PGA) ZIF sockets.

5.2.2 Waveform capture with current probe

5.2.2.1 General

To capture a current waveform between two socket pins (usually the reference pin pair), use the shorting wire (4.5, Load 1) for the short circuit measurement or the 500 Ω resistor (4.5, Load 2) for the 500 Ω current measurement and the inductive current probe (4.4).

5.2.2.2 Short circuit current waveform

Attach the shorting wire between the pins to be measured. Place the current probe around the shorting wire, as close to terminal B as practical, observing the polarity shown in Figure 1. Apply an ESD stress at the voltage and polarity needed to execute the qualification, re-qualification or periodic verification being conducted.

a) For positive clamp sockets, insert the shorting wire between the socket pins connected to terminals A and B and hold in place by closing the clamp.

b) For non-positive clamp sockets, attach the shorting wire between the socket pins connected to terminals A and B. If it is not possible to make contact within the socket, connect the shorting wire between the reference pin pair test points or socket mounting holes, if available. The design of the socket is important as some socket types may include contact springs (coils) in their design. These springs can add more parasitic inductance to the signal path and may affect the HBM waveform. Selecting sockets that minimize the use of springs (coils) is recommended, but if this is not possible, then keeping their length as short as possible is recommended.

c) For non-socketed testers, the shorting wire with the inductive current probe is placed on an insulating surface and the simulator terminal A and terminal B probes are placed on the ends of the wires.

5.2.2.3 500 Ω load current waveform

Place the current probe around the 500 Ω resistor's lead, observing the polarity as shown in Figure 1. Attach the 500 Ω resistor between the pins to be measured. The current probe shall be placed around the wire between the resistor and terminal B. Apply an ESD stress at the voltage and polarity needed to execute the qualification, re-qualification or periodic verification being conducted.

a) For socketed testers, follow procedures according to socket type as described in 5.2.2.2.

b) For non-socketed testers, place the test load and current probe on an insulating surface and connect the tester's probes to the ends of the test load.

5.2.3 Determination of waveform parameters

5.2.3.1 Use of waveforms

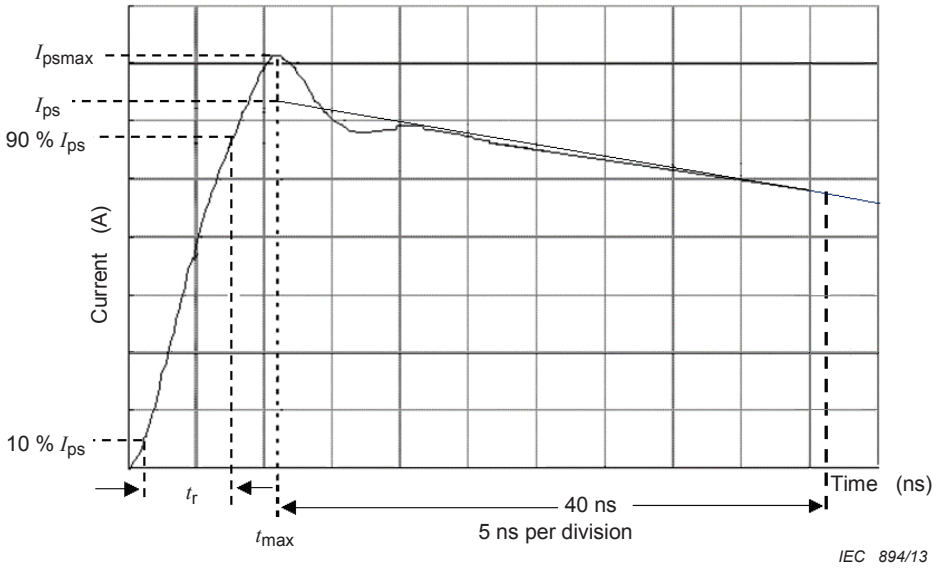
The captured waveforms are used to determine the parameter values listed in Table 1.

5.2.3.2 Short circuit waveform

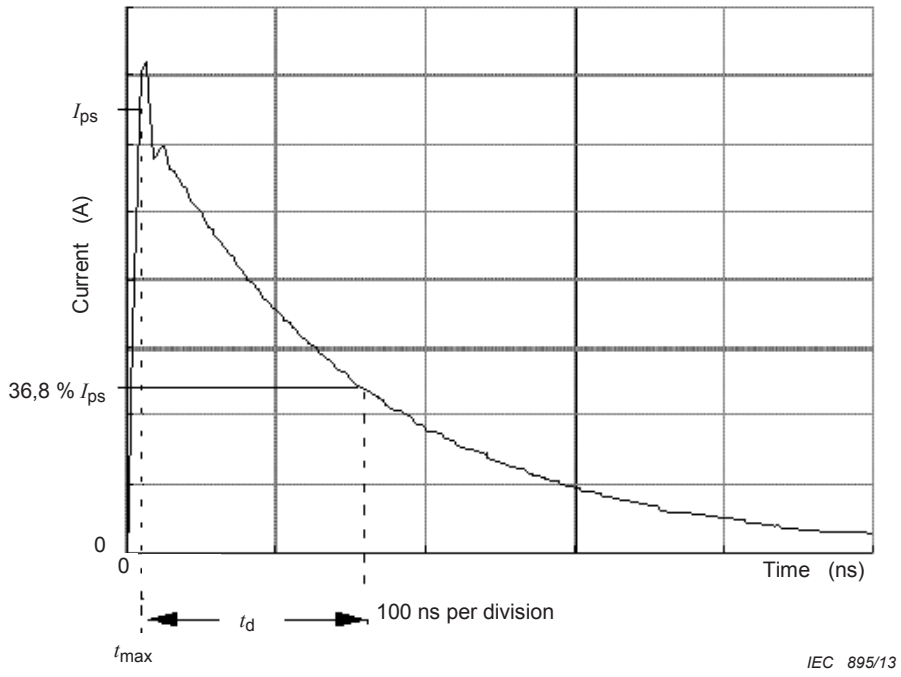
Typical short circuit waveforms are shown in Figures 2a), 2b) and 4. The parameters I_{ps} (peak current), t_r (pulse rise time), t_d (pulse decay time) and I_R (ringing) are determined from these waveforms. Ringing may prevent the simple determination of I_{ps}. A graphical technique for determining I_{ps} and I_R is described in 5.2.3.4 and Figure 4.

5.2.3.3 500 Ω load waveform

A typical 500 Ω load waveform is shown in Figure 3. The parameters I_{pr} (peak current with 500 Ω load) and t_{rr} (pulse rise time with 500 Ω load) are determined from this waveform.



a) Current waveform through a shorting wire (I_{psmax})



b) Current waveform through a shorting wire (t_d)

Figure 2 – Current waveform through shorting wires

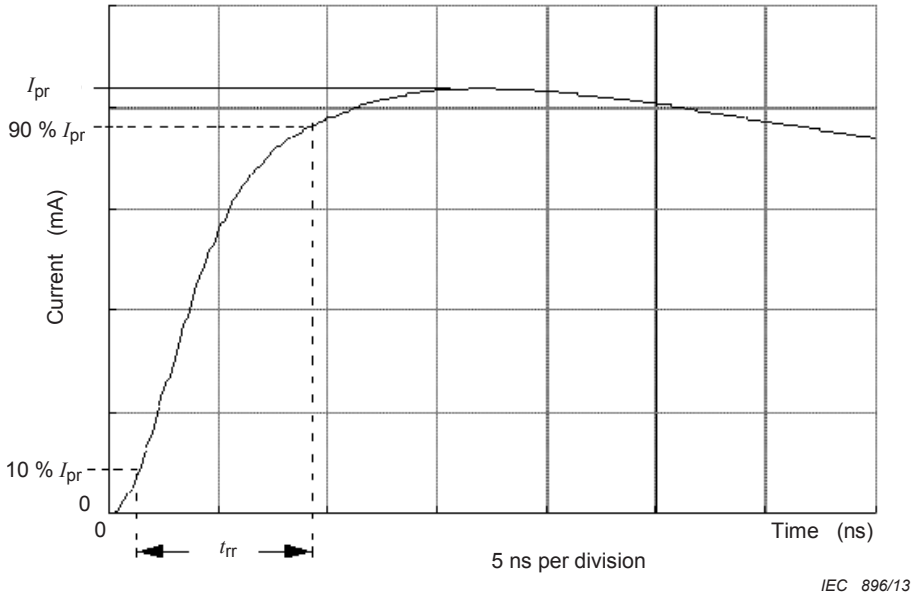


Figure 3 – Current waveform through a 500 Ω resistor

5.2.3.4 Graphical determination of I_{ps} and I_R (see Figure 4)

5.2.3.4.1 A line is drawn (manually or using numerical methods such as least squares) through the HBM ringing waveform from t_{max} to t_{max} + 40 ns to interpolate the value of the curve for a more accurate derivation of the peak current value (I_{ps}). t_{max} is the time when I_{psmax} occurs (see definition for t_{max} in Clause 3 and Figure 2a)).

5.2.3.4.2 The maximum deviation of the measured current above the straight line fit is Ring1. The maximum deviation of the measured current below the straight line fit is Ring2. The maximum ringing current during a short circuit waveform measurement is defined as:

$$I_R = |\text{Ring1}| + |\text{Ring2}|$$

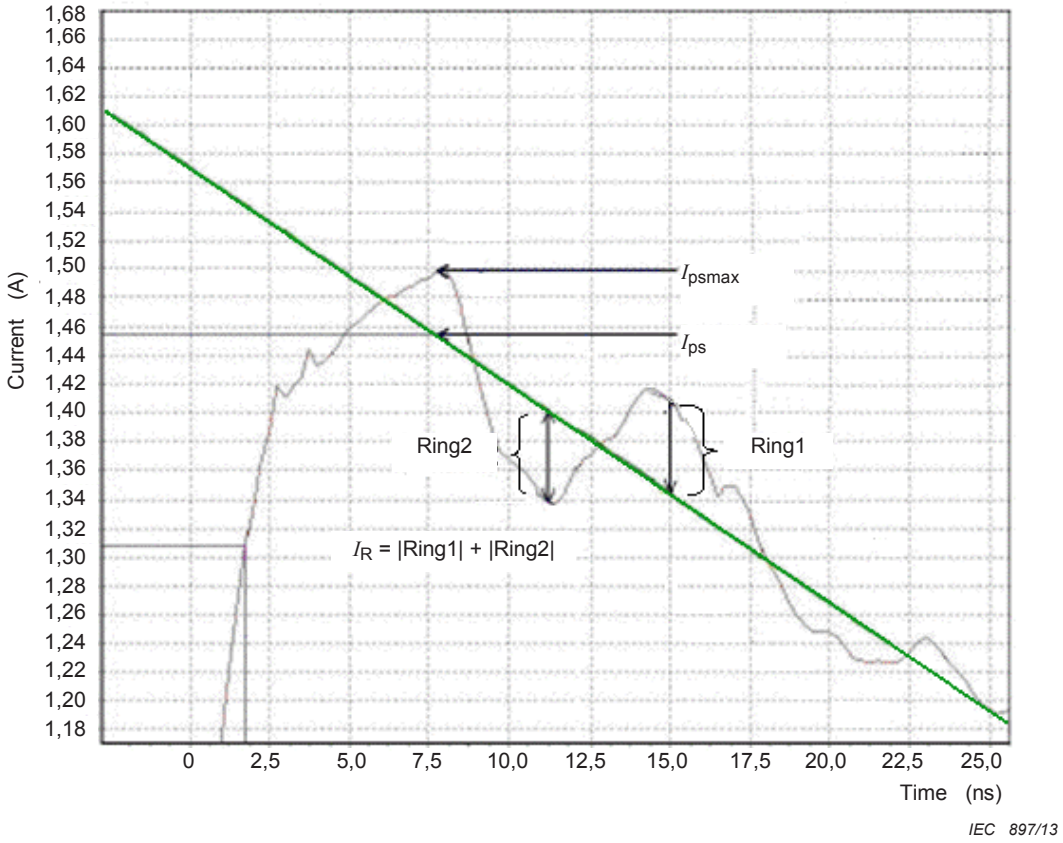


Figure 4 – Peak current short circuit ringing waveform

5.2.4 High voltage discharge path test

This test is only required for relay-based testers. This test is intended to ensure that the tester high voltage relays and the grounding relays that connect pulse generator(s) (i.e. terminal A) and current return paths (i.e. terminal B) to the DUT are functioning properly. The tester manufacturer should provide a recommended procedure and if needed, a verification board and software.

5.3 HBM tester qualification

5.3.1 HBM ESD tester qualification requirements

HBM ESD tester qualification as described in 5.3 is required in the following situations:

a) Acceptance testing when the ESD tester is delivered or first used.

b) Periodic re-qualification in accordance with manufacturer's recommendations. The maximum time between re-qualification tests is one year.

c) After service or repair that could affect the waveform.

5.3.2 HBM tester qualification procedure

5.3.2.1 Test fixture board, socket and pins for socketed testers only

Use the highest pin count test fixture board with a positive clamp socket for the tester waveform verification or the recommended waveform verification board provided by the manufacturer.

The reference pin pair(s) of the highest pin count socket on the board shall be used for waveform capture. Waveforms from every pulse generating circuit are to be recorded.

Electrical continuity for all pins on the test fixture board shall be verified prior to qualification testing. This can typically be done using the manufacturer's recommended self-test.

5.3.2.2 Short circuit waveform capture

a) For socketed testers, configure the test fixture board, shorting wire, and transducer for the short circuit waveform measurement as described in 5.2.2.2.

   For non-socketed testers, configure the test fixture board, shorting wire, and transducer for the short circuit waveform measurement as described in 5.2.2.2 c).

b) Apply five positive and five negative pulses at each test voltage. Record waveforms at 1 000, 2 000 and 4 000 V. Verify that the waveforms meet all parameters specified in Figures 2a) and 2b) and Table 1.

5.3.2.3 500 Ω load waveform capture

a) For socketed testers, configure the test fixture board, resistor, and transducer for the 500 Ω load waveform measurement as described in 5.2.2.3 a).

   For non-socketed testers, configure the test fixture board, resistor, and transducer for the 500 Ω load waveform measurement as described in 5.2.2.3 b).

b) Record waveforms at 1 000 and 4 000 V, both positive and negative polarities. Verify that the waveforms meet all parameters specified in Figure 3 and Table 1.

5.3.2.4 Spurious current pulse detection

Secondary pulses after the HBM pulses are generated by the discharge relay. Using the shorting wire configuration, initiate a 1 000 V pulse and verify that any pulses after the initial HBM pulse are less than 15 % of the amplitude of the main pulse.

For analogue oscilloscopes, setting the time base to 1 millisecond/division can detect these types of pulses. For digital oscilloscopes, current pulses after the initial current pulse can be observed, but advanced triggering functions such as sequential triggering or delayed triggering may be needed so secondary pulses are not missed due to low sampling rates.

5.4 Test fixture board qualification for socketed testers

Test fixture boards shall be qualified in a qualified tester prior to initial use or after repair. This procedure is also required when a previously qualified test fixture board is used in a different model HBM simulator from the one in which it was originally qualified. The procedure shall be applied to the reference pin pairs on all sockets of the new test fixture board. If there is not adequate physical access to the socket, follow the guidance of 5.2.2.2 b).

a) Configure the test fixture board, shorting wire, and current probe for the short circuit waveform measurement as described in 5.2.2.1 with a qualified tester.
b) Apply at least one positive and one negative 1 000 V pulse. All waveform parameters shall be within the limits specified in Figures 2a) and 2b) and Table 1.
c) Configure the test fixture board, 500 Ω resistor, and transducer for the 500 Ω load waveform measurement as described in 5.2.2.2.
d) Apply at least one positive and one negative 1 000 V pulse. All waveform parameters shall be within the limits specified in Figure 3 and Table 1.
e) Repeat for all additional reference pin pairs of all pulse generating circuits and sockets.

Table 1 – Waveform specification

Voltage level (V)	I_{peak} for short, I_{ps} (A)	I_{peak} for 500 Ω I_{pr} (A)	Rise time for short, t_r (ns)	Rise time for 500 Ω t_{rr} (ns)	Decay time for short, t_d (ns)	Maximum ringing current I_R (A)
125 (optional)	0,075-0,092	N/A	2,0-10	N/A	130-170	15 % of I_{ps}
250	0,15-0,19	N/A	2,0-10	N/A	130-170	15 % of I_{ps}
500	0,30-0,37	N/A	2,0-10	N/A	130-170	15 % of I_{ps}
1 000	0,60-0,74	0,37-0,55	2,0-10	5,0-25	130-170	15 % of I_{ps}
2 000	1,20-1,48	N/A	2,0-10	N/A	130-170	15 % of I_{ps}
4 000	2,40-2,96	1,5-2,2	2,0-10	5,0-25	130-170	15 % of I_{ps}
8 000 (optional)	4,80-5,86	N/A	2,0-10	N/A	130-170	15 % of I_{ps}

5.5 Routine waveform check requirements

5.5.1 Standard routine waveform check description

Waveforms shall be acquired using the short circuit method (5.2.2.2) on the reference pin pair for each socket. If necessary, the test fixture board being used may be removed and replaced with a positive clamp socket test fixture board to facilitate waveform measurements. For non-socketed testers the procedure of 5.2.2.2 c) is used. Stresses shall be applied at positive and negative 1 000 V or at the stress level to be tested during the use. The waveforms shall meet the requirements of Figures 2a) and 2b) and Table 1.

5.5.2 Waveform check frequency

The waveforms shall be verified according to this procedure at least once per shift. If ESD stress testing is performed in consecutive shifts, waveform checks at the end of one shift may also serve as the initial check for the following shift.

Longer periods between waveform checks may be used if no changes in waveforms are observed for several consecutive checks. Simpler waveform checks (5.5.2) may be used with longer period between waveform checks. For example, 5.5.2 tests may be done daily with tests according to 5.5.1 done monthly. The test frequency and method chosen shall be documented. If at any time the waveforms no longer meet the specified limits, all ESD stress test data collected subsequent to the previous satisfactory waveform check shall be marked invalid and shall not be used for classification.

If the tester has multiple pulse generation circuits, then the waveform for each pulse generation circuit shall be verified with a positive clamp socket test fixture board. The recommended time period between verification tests is once per shift. However, a rotational method of verification may be used to ensure all pulse generation circuits are functioning properly. For instance, on day 1, pulse generation circuit 1 would be tested. On day 2, pulse generation circuit 2 would be tested and on day 3, pulse generation circuit 3 would be tested, until all circuits have been tested, at which time circuit 1 would again be tested. The recommended maximum interval between tests of any one pulse generator is two weeks. However, if a pulse generation circuit fails, then all ESD stress tests subsequent to the previous satisfactory waveform check of that pulse generation circuit shall be marked invalid and shall not be used for classification.

5.5.3 Alternate routine waveform capture procedure

As an alternative to the detailed routine waveform analysis, a quick pass/fail waveform capture process can be instituted for routine verification. This method may be used in combination with 5.5.1 as described above.

a) Capture a waveform using a shorting wire evaluation load at +1 000 V.
b) Measure I_{psmax} (without adjustment for ringing) and ensure that it is between 0,60 A and 0,74 A.
c) Repeat at –1 000 V.
d) If the tester has multiple pulse sources, choose a pin pair combination from a different pulse source each day, rotating through each pulse source in turn as described in 5.5.2.

If I_{psmax} is within the values specified for both polarities and the waveforms appear normal, the tester is considered ready to use.

This measurement does not take into consideration I_{ps} ringing; this may affect the results. If there are any concerns about how the waveforms look, or if the measurements are close to the upper or lower specification limits, a complete waveform analysis (5.3.1) shall be performed.

The quick pass/fail test method shall be applied only to qualified test fixture boards for qualified ESD simulators. Test fixture boards and ESD simulator shall be qualified together using the test method in 5.3.1 before using test method in 5.5.2.

5.6 High voltage discharge path check

5.6.1 Relay testers

This test is required for either routine check method (5.5). Test the high voltage discharge and current return paths and all associated circuitry at the beginning of each day during which ESD stress testing is performed (see 5.2.4). The period between self-test diagnostic checks may be extended, providing test data support the increased interval. If any failure is detected, do not perform device testing with the sockets that are connected to the defective discharge paths. Repair the tester and then verify that the failed pins pass the self-test before resuming testing. Depending on the extent of the repair, it may be necessary to perform a complete re-qualification according to 5.3.2.

5.6.2 Non-relay testers

For testers utilizing mechanical switching instead of relay switching, the connections to pins shall be verified for each pin combination during the test. Making continuity measurements immediately prior to stress pulses or monitoring the ESD pulse current during stress pulse are examples of connection verification methods. This practice replaces the daily high voltage discharge path verification.

5.7 Tester waveform records

5.7.1 Tester and test fixture board qualification records

Retain the waveform records until the next re-qualification or for the duration specified by the user's internal record keeping procedures.

5.7.2 Periodic waveform check records

Retain the periodic waveform records at least one year for the duration specified by the user's internal record keeping procedures.

5.8 Safety

5.8.1 Initial set-up

During initial equipment set-up, a safety engineer or applicable safety representative shall inspect the equipment in its operating location to ensure that the equipment is not operated in a combustible (hazardous) environment.

5.8.2 Training

All personnel shall receive system operational training and electrical safety training prior to using the equipment.

5.8.3 Personnel safety

The procedures and equipment described in this document may expose personnel to hazardous electrical conditions. Users of this document are responsible for selecting equipment that complies with applicable laws, regulatory codes and both external and internal policy. Users are cautioned that this document cannot replace or supersede any requirements for personnel safety.

Ground fault circuit interrupters (GFCI) and other safety protection should be considered wherever personnel might come into contact with electrical sources.

Electrical hazard reduction practices should be exercised and proper grounding instructions for equipment shall be followed.

6 Classification procedure

6.1 Devices for classification

The devices used for classification testing shall have completed all normal manufacturing operations. Testing shall be performed using an actual device chip. It is not permissible to use a test chip representative of the actual chip or to assign threshold voltages based on data compiled from a design library or via software simulations. ESD classification testing shall be considered destructive to the component, even if no component failure is detected.

NOTE Test chip in this case means ESD test structure.

6.2 Parametric and functional testing

Prior to ESD stressing, parametric and functional testing using conditions required by the applicable part drawing or test specification shall be performed on all devices submitted. Parametric and functional test results shall be within the limits stated in the part drawing for these parameters.

6.3 Device stressing

A sample of three devices for each voltage level shall be characterized for the device ESD failure threshold using the voltage levels shown in Table 4. Finer voltage steps may optionally be used to obtain a more accurate measure of the failure threshold, and to improve detection of devices exhibiting failure windows. ESD testing should begin at the lowest level in Table 4 but may begin at any level. However, if the initial voltage level is higher than the lowest level in Table 4, and the device fails at the initial voltage, testing shall be restarted with three fresh devices at the next lowest level (e.g. if the initial voltage is 1 000 V and the device fails, restart the test at 500 V.) The ESD test shall be performed at room temperature.

It is recommended to verify continuity between device pins and the socket after inserting devices to be tested. Leakage measurements or curve tracing may be used.

For each voltage level a sample of three devices shall be stressed using one positive and one negative pulse with a minimum of 100 ms between pulses per pin for all pin combinations specified in Table 2 and Table 3. Separate samples may be used for different polarities.

NOTE In some ESD simulators, a charge removal circuit is not present. For these simulators, increasing the time between pulses to prevent a charge build-up is one method to reduce the risk for subsequent pin overstress. Alternatively, curve trace leakage tests after each pulse for all pins in the DUT will also remove this excess charge stored in the test fixture board or socket.

Three new components may be used at each voltage level or pin combination if desired. This will eliminate any step-stress hardening effects, and reduce the possibility of early failure due to cumulative stress. Due to potential failure windows, low ESD performance may not be detected if levels specified in Table 4 are skipped during testing. It is recommended not to skip any levels specified in Table 4.

It is permitted to further partition each pin combination set specified in Tables 2 and 3 and use a separate sample of three devices for each subset within the pin combination set.

It is permitted to partition testing of devices among different testers as long as all testers are qualified (in accordance with 5.3) and all pin combinations of Tables 2 and 3 are tested with at least one sample of three devices.

6.4 Pin categorization

6.4.1 General

HBM testing is done using pin combinations as described in Table 2 or Table 3. A flow chart for this categorisation process is given in Annex A. The purpose of the pin combinations is to test all of the major HBM current paths. Setting up the pin combinations requires knowledge of the device under test. Each pin of the device shall be classified as a no connect, supply pin or non-supply pin. These pin categories are defined in 6.4.2 – 6.4.3. Additionally supply pins shall be grouped into supply pin groups as described in 6.5.1. With this basic knowledge testing may be done using Table 3. With additional knowledge of the device to be tested, associated supplies may be defined as described in 6.6.2.2. With associated supplies defined lines 1 to N of Table 2 may be used. The additional information required for Table 2 allows the major current paths to be covered with fewer pin combinations saving test time and reducing potential overstress. Table 2 also eliminates non-supply to non-supply testing (i.e. I/O to I/O) except for special cases which are discussed in 6.4.4.2.

6.4.2 No connect pins

Verified no connect pins shall not be stressed and shall be left floating at all times.

There are some pins which are labelled as no connect, such as thermal panels, which are actually connected to the die and should be classified a supply pin or non-supply pin as outlined below.

Pins labelled as no connect but found to have an electrical connection to the die shall be:

- Classified as a supply pin, if metallically connected to a supply pin.
- Classified as a non-supply pin, if not metallically connected to a supply pin.

6.4.3 Supply pins

6.4.3.1 Supply pin categorisation

A supply pin is any pin that provides current to the circuit. While most supply pins are labelled such that they can be easily recognized as supply pins (examples: VDD, VDD1, VDD2, VDD_PLL, VCC, VCC1, VCC2, VCC_ANALOG, GND, AGND, DGND, VSS, VSS1, VSS2, VSS_PLL, VSS_ANALOG, etc.), others are not and require engineering judgment based on

their function in the normal circuit operation (examples: Vbias, Vref, etc.). Supply pins typically transmit no information such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

An example of a pin that appears to be a supply pin but may be treated as a non-supply pin is the VPP pin on EPROM memories. The VPP puts the memory into a special, rarely used, programming state and supplies the high voltage needed for programming the memory.

6.4.3.2 Other supply pin types

Any pin that is intended to be pumped above the positive supply or below the negative supply of its circuit block shall be treated as a supply pin (for example: positive and negative terminal pins connected to a charge pump capacitor).

Any pin that is connected to an internal power bus (or a power pin) by metal as described in 6.4.3 shall be treated as a supply pin (for example: a Vdd sensing pin).

Any pin that is intended to supply power to another circuit on the same chip shall be treated as a supply pin. However, if a pin is intended to supply power to a circuit on another chip but not to any circuit on the same chip, it may be treated as a non-supply pin.

6.4.4 Non–supply pins

6.4.4.1 Non-supply pins categorisation

All pins not categorized as supply pins or no connects are non-supply pins. This includes pins such as input, output, offset adjusts, compensation, clocks, controls, address, data, Vref pins and VPP pins on EPROM memory. Most non-supply pins transmit information such as digital or analogue signals, timing, clock signals, and voltage or current reference levels.

6.4.4.2 Direct coupled non-supply pin pairs

A coupled non-supply pin pair can have a potential ESD current path that does not involve power/supply rails. They include analogue and digital differential pairs and other special function pairs (e.g., D+/D-, XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP_DP/CCN_DN etc.). Coupled non-supply pin pairs are device specific and not all devices will have them. Examples include:

- Any non-supply pin pairs that may have current paths between them that does not involve the power/supply rails. This path may be through functional devices or through parasitic paths.
- Non-supply pin pairs directly interfacing with each other, such as differential inputs or differential outputs.
- Non-supply pin pairs that have a current path between them that consists of a single transistor or capacitor.

Engineering judgment should be used to identify all coupled non-supply pin pairs. See Annex D for a more extensive list of examples for coupled non-supply pins.

6.5 Pin groupings

6.5.1 Supply pin groups

6.5.1.1 Supply pin categorisation

The supply pins are partitioned into supply pin groups with each supply pin defined as a member of one and only one supply pin group. A supply pin that is not connected by metal to any other pin forms a single pin supply pin groups. Supply pins that are interconnected by metal on the chip or within the package form a supply pin group. The metal interconnects should be verified through reliable device documentation. However, excessive metal trace

resistance in the die interconnect associated with grouping these pins could lead to masking an ESD protection weakness in HBM testing.

If the pin inter-connect design is unknown, either measure the resistance between supply pins to determine the supply pin groups or treat each pin as a separate group.

If the resistance between any two pins is greater than 3 Ω, the pins should be placed into separate supply pin groups. The resistance is measured between any two supply pins with the same name. If there are more than two pins, then the worst case resistance should be determined by measurement.

6.5.1.2 Partitioning supply pin groups

Pins of a supply pin group may be divided into two or more subgroups such that each pin is a member of at least one subgroup. This partitioning may result in each pin being in its own subgroup. When a supply pin group is being connected to terminal B, all pins specified for terminal A are stressed separately to each subgroup. When dividing a supply pin group into subgroups, all the subgroups remain part of their supply pin group and are not tested against each other.

6.5.1.3 Supply pins connected by package plane

If a set of supply pins are connected by a package plane, as few as one pin (selected arbitrarily) from that set of pins may be used to represent the entire set as a supply pin group. The remaining pins in the set need not be stressed nor grounded and can be left floating during all testing. For example, if a supply pin group of 25 pins consists of five pins connected by metal only at the die level and 12 additional pins connected with one package plane and another with eight pins connected with a second package plane, the group should be represented by the five die-level connected pins and at least one pin from each package plane connected sets. Tester parasitics may be reduced by connecting all the pins of the group to terminal B instead of leaving the unselected pins floating. This is not necessary if a custom board has been built which isolates the unselected pins.

6.5.2 Shorted non-supply pin groups

For shorted non-supply pins that are connected by metal in a package plane and/or share a common bond pad, this set of pins forms a non-supply pin group. One pin of this non-supply pin group (selected arbitrarily) may be used to represent the entire set of shorted non-supply pins. The remaining pins in the set need not be stressed nor grounded and may be left floating during all testing.

NOTE This configuration is uncommon as non-supply pins typically are isolated from other pins in the package.

6.6 Pin stress combinations

6.6.1 Pin stress combination categorisation

Table 2 lists the preferred set of pin combinations required for device classification. Alternatively, Table 3 can be used. Furthermore, device stressing can be done using a combination of Table 2 and Table 3. For example, one could use pin combination set 1 through N from Table 2 and set N+1 from Table 3. Additional information and guidance on the use of the pin combinations are given in Annex A and Annex C. The test results and actual pin combinations sets used shall be recorded and maintained according to company record keeping procedures.

Active discrete devices (FETs, transistors, etc.) shall be tested using all possible pin-pair combinations (one pin connected to terminal A, another pin connected to terminal B) regardless of pin name or function. Integrated circuits with 10 pins or less may be tested with all pin-pair combinations.

Device stressing can be divided between two or more simulators if all simulators meet the requirements of Clause 5 and all intended pin combinations are stressed.

Table 2 – Preferred pin combinations sets

Pin combination set number [a]	Pin(s) connected to terminal B (ground)	Pin connected to terminal A (single pins, tested one at a time)
1	supply pin group 1 [b, c]	every supply pin except pins of supply pin group 1 [c, d]
		every non-supply pin associated with supply pin group 1 (see Annex C)
2	supply pin group 2 [b, c]	every supply pin except pins of supply pin group 2 [c, d]
		every non-supply pin associated with supply pin group 2 (see Annex C)
…	…	…
N	supply pin group N [b, c]	every supply pin except pins of supply pin group N [c, d]
		every non-supply pin associated with supply pin group N (see Annex C)
N+1	one pin of each coupled non-supply pin pair, one pair at a time	the other pin of the coupled non-supply pin pair

[a] In all combinations, pins not connected to either terminal A or terminal B shall be left unconnected (floating pins) during the stress pulse. All no connect pins are unconnected at all times.

[b] Supply pins may be all connected together as a single group, or divided into subgroups. Subgroups can be individual pins. Every pin connected to terminal A is stressed to each of these subgroups (see 6.4.1).

[c] A single pin may be used from supply pin groups known to be interconnected by a package plane (see 6.4.1.2).

[d] Supply pin-to-supply pin combinations may be stressed using only single polarity pulses (see 6.5.1.2).

Table 3 – Alternative pin combinations sets

Pin combination set number [c]	Pin(s) connected to terminal B	Pin connected to terminal A (single pins, tested one at a time)
1	supply pin group 1[a]	every supply pin except pins of supply pin group 1[a]
		every non-supply pin
2	supply pin group 2	every supply pin except pins of supply pin group 2
		every non-supply pin
…	…	…
N	supply pin group N	every supply pin except pins of supply pin group N
		every non-supply pin
N+1	all non-supply pins, except the pin under test (PUT)[b]	each non-supply pin (as the PUT)

[a] Only a single pin is used from supply pin groups known to be interconnected by a package plane.

[b] Non-supply pins connected to terminal B can be divided into subsets, such that each of these pins is a member of at least one subset. Every terminal A pin is stressed to each of these subsets.

[c] All pins not connected to either terminal A or terminal B shall be left unconnected (floating pins) during the stress pulse. All no connect pins are unconnected at all times.

6.6.2 Non-supply and supply to supply combinations (1, 2, … N)

6.6.2.1 Use of Tables 2 and 3

Table 2 and Table 3 are organized by the DUT's N supply pin groups. The first N rows of these tables have one unique supply pin group tied to terminal B. When pins are not connected by a package plane, pins within a supply pin group shall be stressed individually (when connected to terminal A). When tied to terminal B, as shown in tables, these pins shall all be connected either individually, or in groups, or tied together at the test board level.

6.6.2.2 Association of non-supply pins with supply pin groups (Table 2 only)

Each non-supply pin is associated with one or more supply pin groups (see 6.6.2). For example, for an I/O pin, the output drivers of the pin connect to the VCCIO supply group while the input receiver of the same pin connects to the VCC supply group. Additionally, this I/O pin may be connected to one or more grounds (e.g., VSS, VSSIO). This information is typically provided by the design team.

A non-supply pin is associated with a supply pin group if either:

a) The connection to that supply pin group is necessary for the function of the circuit.

b) A parasitic path exists between non-supply and supply pin group (e.g., open-drain type non-supply pin to a VCC supply pin group that connects to a nearby N-well guard ring).

In the testing described in Table 2, non-supply pins are only stressed against the supply pin groups with which they are associated. If the information on the association with supply pin groups for each non-supply pin is known, then non-supply pins may be stressed only to their associated supply pin groups (see Annex C). Stressing to supply pin groups not associated with a non-supply pin is not required. If this information is not available, then every non-supply pin shall be tested to each supply pin group as specified in lines 1 to N of Table 3.

This use of Table 2 is highly recommended for devices exceeding 8 supply pin groups.

NOTE Pin combinations 1 to N in Table 3 treats all non-supply pins as being associated with every supply pin group.

6.6.2.3 Stress polarities of supply pins (Tables 2 and 3)

When pins of supply pin groups are stressed to other supply pin groups it is permissible to perform all stresses with a single polarity.

NOTE For some devices under test it has been found that power supply stress with one polarity is more susceptible to tester parasitics than the opposite polarity. These parasitic currents can cause waveform distortion and anomalous test results. Since every supply is stressed on terminal A with respect to every other supply on terminal B, all supply pairs are normally tested twice. For low resistance power supply busses the positive stress of power group 1 on terminal A versus power supply group 2 on terminal B is essentially redundant to negative stress of Power supply group 2 on terminal A versus power supply group 1 on terminal B. Removing this testing redundancy allows testing only with the polarity which minimizes tester parasitic. For most technologies, such as CMOS circuits on p substrates, positive only testing is preferred. For some technologies negative only testing may be preferred.

6.6.2.4 Alternative pin stress method for non-supply pins (Tables 2 and 3)

A non-supply to supply pin stress may be replaced by its corresponding supply pin to non-supply pin stress. If only a single polarity stress is being replaced, the opposite polarity stress shall be used. As non-supply pins are typically not tied to other pins, this will require each supply pin of the supply pin group to be stressed to each non-supply pin individually. If the non-supply pin is tied to other pins, as noted in 6.5.2, all other non-supply pins of the group shall be left floating.

NOTE 1 Typically, the non-supply to supply pin negative polarity stress will be replaced with the supply to non-supply pin, positive polarity stress. This allowance is useful when the slew rate of the HBM pulse is impacted by parasitic tester capacitances.

NOTE 2 If this alternative test method is used on a supply pin group that has more than a small number of pins, tester parasitic capacitance will increase (i.e., slow down) the rise time of the signal. Longer rise times may cause dynamic ESD protection circuits not to function properly (See Clause C.3).

6.6.3 Non-supply to non-supply combinations

6.6.3.1 Use of Tables 2 and 3

Pin combination set N+1 in Table 2 specifies to stress each coupled non-supply pin pair.

6.6.3.2 Alternative non-supply to non-supply combinations

If information on non-supply pins to determine coupled pairs is not available, the pin combination set N+1 in Table 3 shall be used. This specifies to stress each non-supply pin individually (terminal A) with all other remaining non-supply pins tied together and connected to terminal B, except for those shorted non-supply pins that are metal connected to the pin under stress on the die, which will be left open as specified in 6.5.2.

6.6.3.3 Shorted non-supply pins (Table 3 only)

If using Table 3 for a device that has shorted non-supply pins that are connected on the die only and bonded out to multiple separate pins, then these pins shall be stressed individually according to combination set N+1 with the remainder of these connected pins left floating. If using Table 3 for a device that has shorted non-supply pins that are connected by a package plane or share a common bond pad, one of these pins (selected arbitrarily) may be used to represent the entire set of shorted non-supply pins. The remaining pins in the set need not be stressed nor grounded and should be left floating during all testing.

6.6.3.4 Partition allowance for non-supply pins (Table 3 only)

When using Table 3 it is permitted to partition the non-supply pins to be connected to terminal B into two or more subsets, such that each of these pins is a member of at least one subset. The subsets may be single pins. The pin connected to terminal A is to be stressed to each of these subsets separately. This process is repeated for each non-supply pin.

6.7 Testing after stressing

If a different sample group is tested at each stress level, it is permitted to perform the DC parametric and functional testing after all sample groups have been ESD tested.

7 Failure criteria

A part is defined as a failure if it fails the datasheet parameters using parametric and functional testing. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.

8 Component classification

ESD sensitive components are classified according to their HBM withstand voltage, regardless of polarity, as defined in Table 4. A component can be classified based on testing with any HBM simulator that meets all the parameters of Clause 4. If a component tests to a higher classification level on one HBM simulator than another, it is assigned the higher classification.

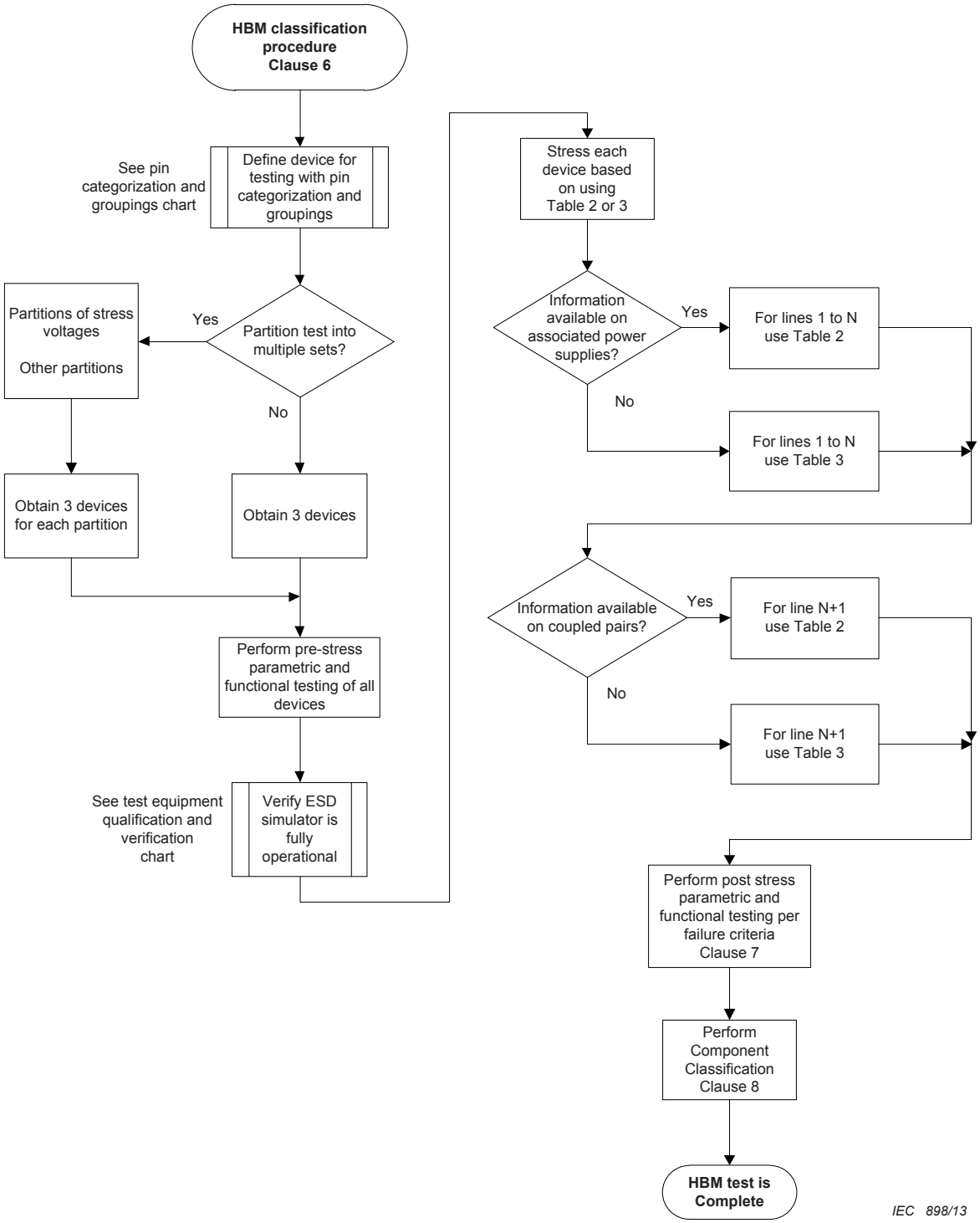
If different classification levels are seen from multiple testers, it is recommended to investigate further.

Table 4 – HBM ESD component classification levels

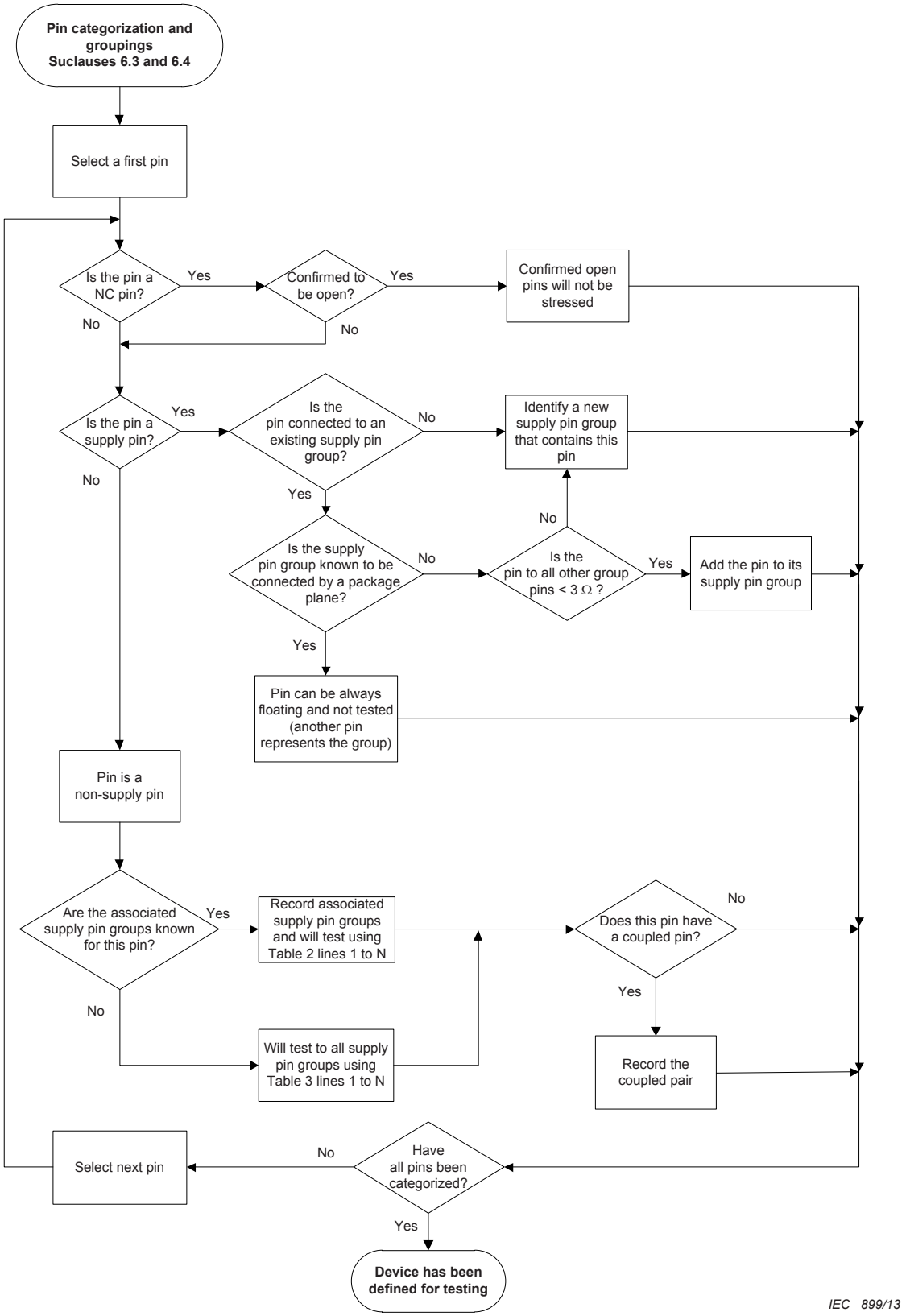
Classification	Voltage Range (V)
0A	< 125
0B	125 to < 250
1A	250 to < 500
1B	500 to < 1 000
1C	1 000 to < 2 000
2	2 000 to < 4 000
3A	4 000 to < 8 000
3B	≥ 8 000

Annex A
(informative)

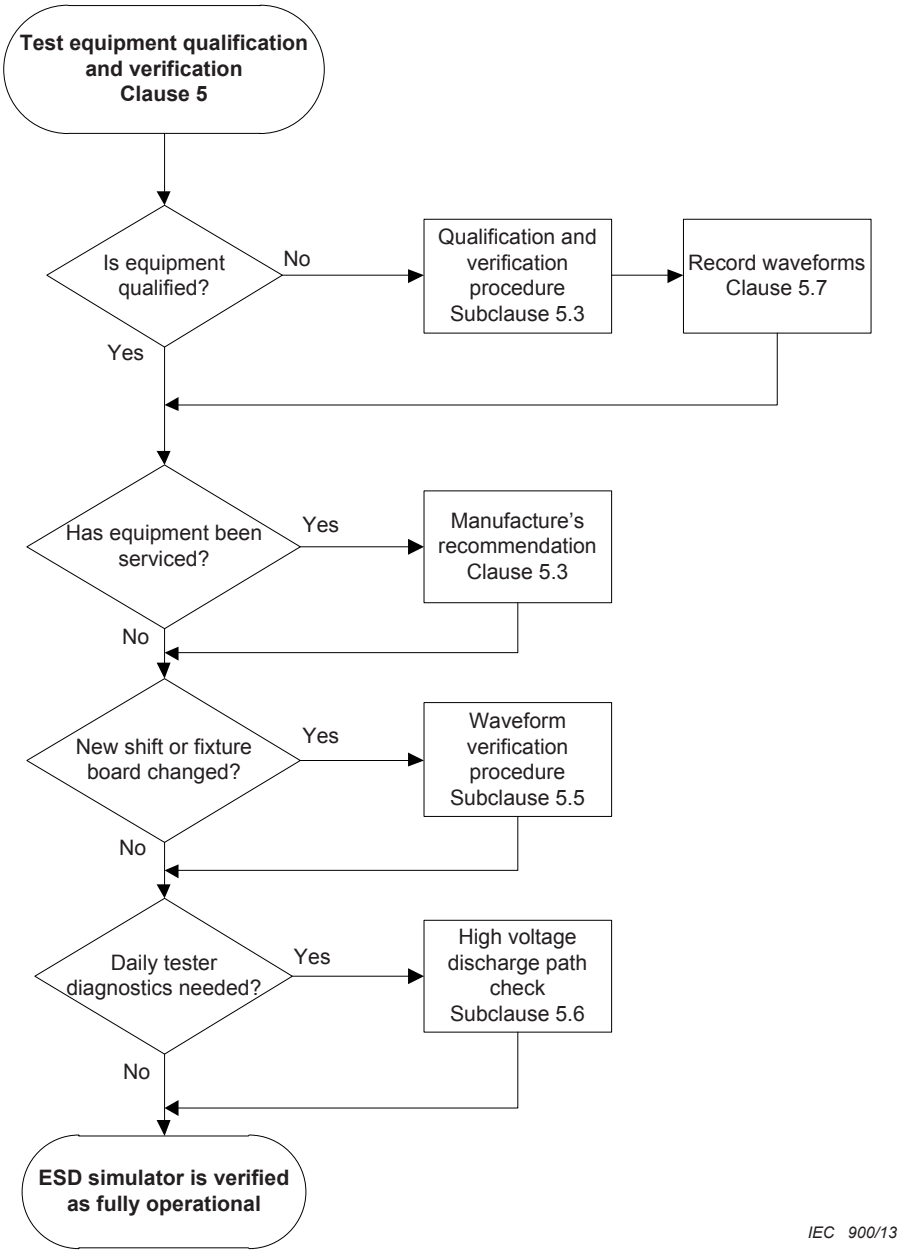
HBM test method flow chart



HBM test method flow chart (continued).



HBM test method flow chart (continued).



Annex B
(informative)

HBM test equipment parasitic properties

B.1 Optional trailing pulse detection equipment / apparatus

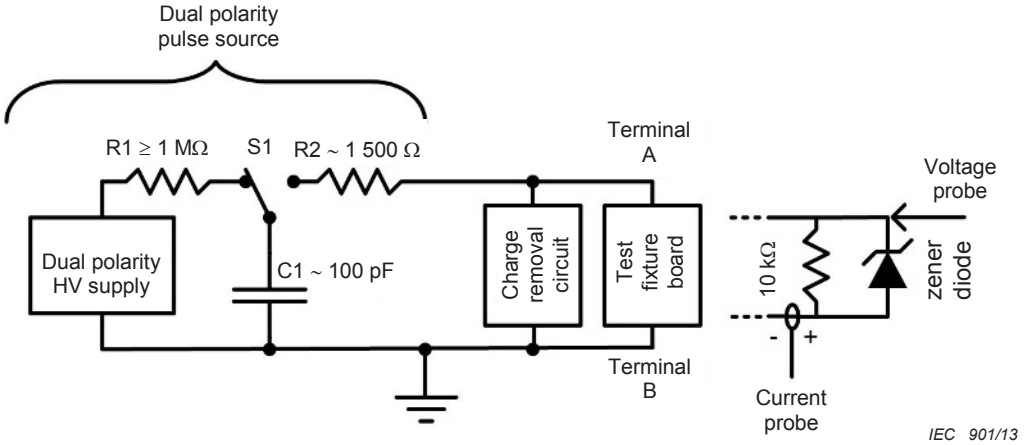


Figure B.1 – Diagram of trailing pulse measurement setup

The maximum trailing current pulse level is defined as the maximum peak current level observed through a 10 kΩ test load (current = voltage across test load divided by 10 kΩ) after the normal HBM pulse(s). The time period to be evaluated for after-pulse leakage, is from 0,1 ms to 1 ms after the decay of the HBM current pulse. In the case that a spurious current pulse is observed, begin the 0,1 ms measurement point from the start of the spurious current pulse.

The magnitude of the trailing current pulse shall be less than 4 μA when the applied HBM stress voltage is at 4 000 V. This includes both positive and negative polarities. (See Figures B.2 and B.3 for sample waveforms).

A circuit for measuring the trailing current pulse is shown in Figure B.1. The voltage probe shall have input impedance no less than 10 MΩ, an input capacitance no larger than 10 pF, a bandwidth better than 1 MHz, and a voltage rating to withstand at least 100 V. The evaluation load resistance is 10 kΩ in value with tolerance of ± 1 % and can withstand up to 4 000 V. The Zener diode has a breakdown voltage range from 6 V to 15 V and a power rating from 0,25 W to 1 W.

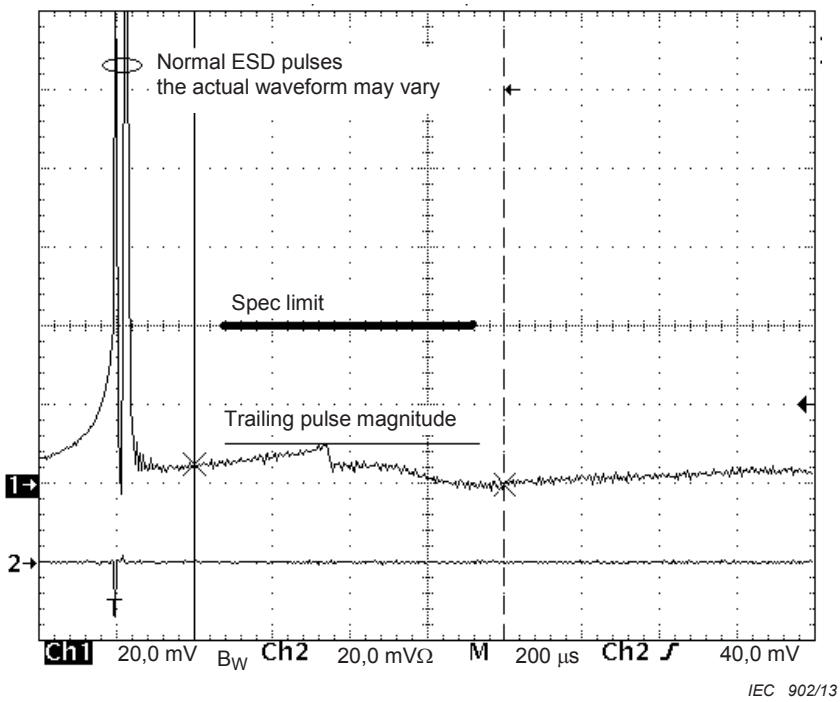


Figure B.2 – Positive stress at 4 000 V

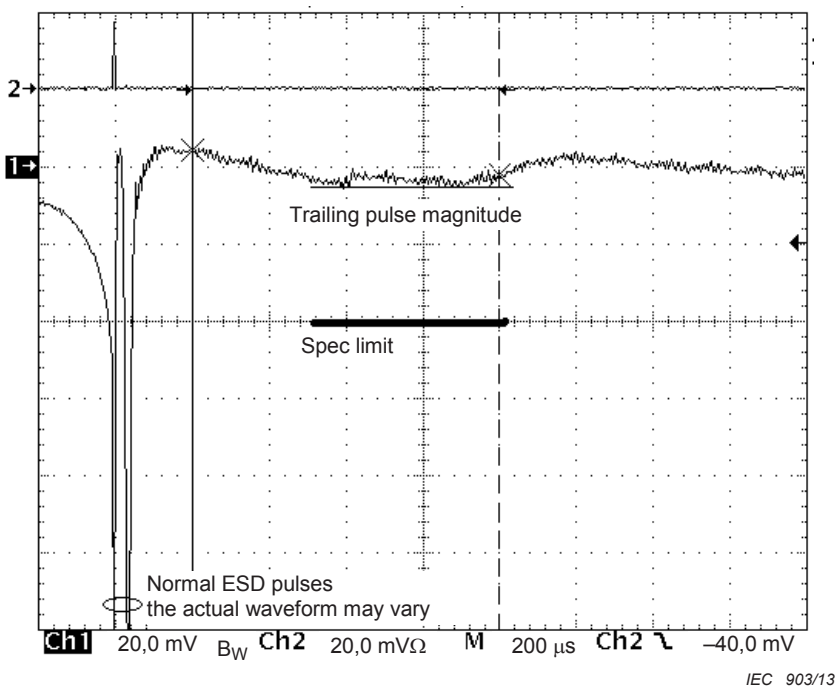


Figure B.3 – Negative stress at 4 000 V

B.2 Optional pre-pulse voltage rise test equipment

HBM events may exhibit a phenomenon which generates a voltage rise at the stressed pin prior to the main HBM current pulse if the pin impedance is high. In some ESD simulators this phenomenon is unrealistically severe and may lead to inconsistent ESD threshold results. The

characteristics of this pre-current pulse voltage event depend on the conditions and the environment of the arcing associated with the HBM discharge, the parasitic capacitances of the tester, as well as the pin impedance of the device under test. To determine the magnitude of the resulting voltage rise the following test equipment and apparatus is required. (see Figure B.4 for measurement setup).

The worst-case condition will be measured for a low capacitance Zener diode with a voltage in the 8 V to 10 V range. The Zener diode will provide protection for the voltage probe and its low capacitance will not reduce the voltage buildup appreciably. The current transducer on the groundside of the diode is used to trigger an oscilloscope. The voltage probe, connected to a second channel of the oscilloscope, should have high resistance such as a 10 MΩ 10X probe. Sample data is shown in Figure B.5 for a 9,4 V Zener diode. The HBM current pulse occurs at time zero and cannot be seen at this time scale. At the time scale of an HBM event, tens to hundreds of nanoseconds, the voltage before the HBM current pulse would appear as a DC voltage across the diode. To measure the voltage across a device the Zener diode is replaced by the device of interest.

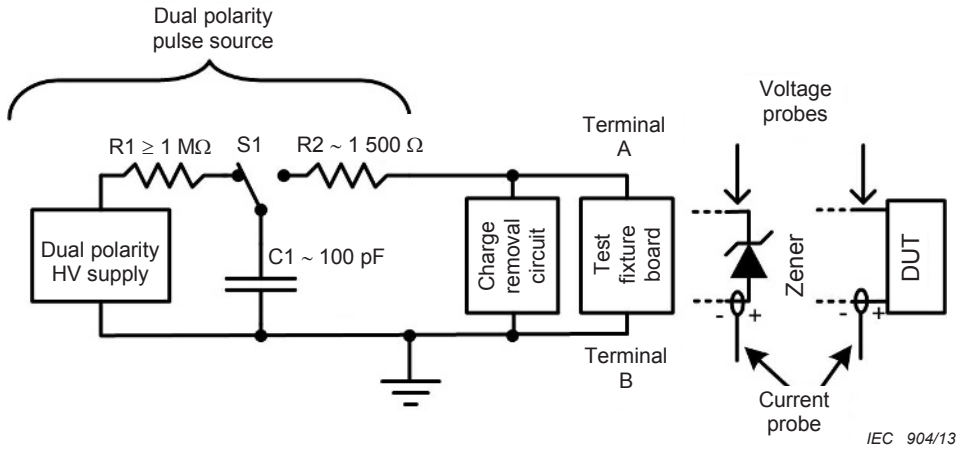


Figure B.4 – Illustration of measuring voltage before HBM pulse with a Zener diode or a device

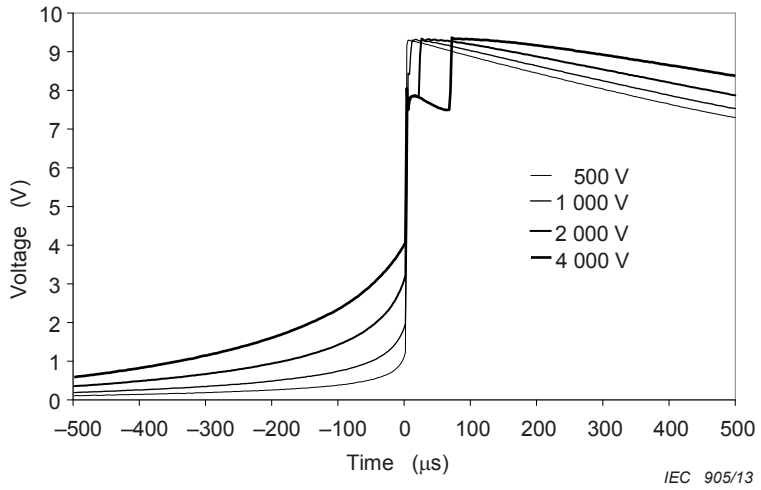


Figure B.5 – Example of voltage rise before the HBM current pulse across a 9,4 V Zener diode

B.3 Open-relay tester capacitance parasitics

The HBM stressing of a single supply pin is complicated when the pin is part of a group of multiple like-name supply pins (balls) that are shorted together via the DUT (e.g., via a package plane). When the component is placed in the socket only one pin can be connected to terminal A. The other supply pins are left “floating” as the HBM simulator’s connect relays are opened so the other supply pins do not connect to terminal A or B.

Recent HBM tester research on package-plane-shorted pins has found that when a single pin is stressed, the other “floating” supply pins act like small capacitors. Since the relays are open, no DC current will flow to ground, but the open-relay capacitors will charge. This parasitic capacitance per pin is quite small (4 pF/pin – 8 pF/pin) and will vary among HBM simulators. Since each floating pin is placed in parallel, the parasitic capacitance grows as the number of supply pins connected to the power plane increases. This tester parasitic capacitance will be in parallel with the test board capacitance and will have the effect of slowing down the HBM peak current rise time and will reduce the HBM peak currents. All relay matrix HBM simulators have this property.

The impact on HBM test results is difficult to determine as it depends on the sensitivity of the ESD circuits of the supply pins to slow di/dt rise times. For some designs and equipment, the HBM levels may either increase or decrease. If failure levels are lower than expected, the best option is to retest the supply pins on a 2-pin manual tester. If the 2-pin HBM levels are much higher, then the open-relay capacitance is probably causing the lower HBM failure levels. In some cases, tester channels can be isolated by adding insulators or removing pogo pins from the HBM tester. This effectively “floats” the parallel supply pins. If there is a known problem for a given package, then special test fixture boards can be designed that connect only one supply pin from the socket to the HBM simulator. This modified test fixture board will not wire the floating pins to the HBM simulator, so these pins will not be able to charge up the open-relay capacitors.

B.4 HBM stressing with a low parasitic simulator

A low parasitic HBM simulator will have nearly identical peak currents and rise times on terminal A and terminal B when testing devices. When parasitics are sufficiently small, which pin of a stressed pair is on terminal A and which is on terminal B would be irrelevant. Thus, when stressing a pin pair using an ideal low parasitic HBM simulator, using both polarities, the pins would not need to be reversed and stressed again. For example, if pin X is stressed on terminal A to pin Y on terminal B with both voltage polarities, it is unnecessary to stress pin Y on terminal A with pin X on terminal B.

NOTE One way to achieve low parasitics is to contact only the pins to be tested and to assure that pins which should be floating are truly isolated from the tester. This can be done by a 2-pin tester with mechanical switching. Testers that do not completely isolate floating pins, but have floating pins connected to test fixture board traces, simulator wiring and open-relay matrix contact capacitances, can degrade terminal B peak currents and increase terminal B rise times and are not low parasitic HBM simulators.

Annex C
(informative)

Example of testing a product using Table 2, Table 3, or Table 2 with a two-pin HBM tester

C.1 General

Devices with multiple supply pin groups can be stressed in different ways depending on the information available. A simple device with several typical properties is used to illustrate the different procedures (see Figure C.1):

A 16 pin device has the following attributes:

- Partition 1 with supply pin groups: VDD1 (1 pin), VSS1 (1 pin) and 2 I/O-pins.
- Partition 2 with supply pin groups: VDD2 (2 pins), VSS2[A,B] (2 pins), 2 I/O-pins, 1 input pin and 1 output pin (4 non-supply pins).
- Partition 3 with supply pin groups: VDD3 (1 pin), VSS3/VSS4 (1 pin) and no I/O-pins.
- Partition 4 with supply pin groups: VDD4 (1 pin), VSS3/VSS4 (1 pin) and 1 I/O-pin.
- VSS1, VSS2-A and VSS2-B are electrically shorted in the package, therefore only one of these pins needs to be stressed. For simplification VSS1 (pin 4) is selected.
- VDD2-A and VDD2-B are electrically shorted on the die with a resistance between them of less than 3 Ω. Each pin shall be stressed, but they may be grouped to the same supply pin group.
- I/O-11 and I/O-12 form a coupled non-supply pin pair in partition 1.
- I/O-21 and I/O-22 form a coupled non-supply pin pair in partition 2.

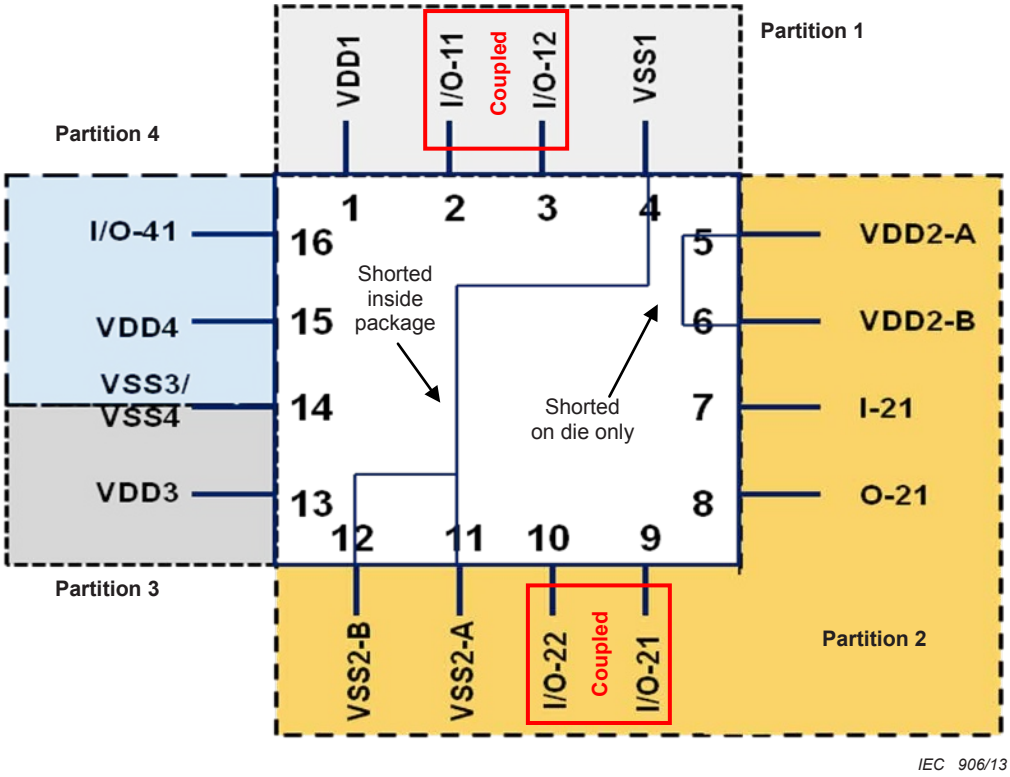


Figure C.1 – Example to demonstrate the idea of the partitioned test

VSS3/VSS4 belongs to the set of supply pin groups VDD3 as well as to the set of supply pin groups VDD4.

C.2 Procedure A (following Table 2):

When the information concerning which I/O-pin is associated with which supply pin groups is available the device can be tested, in accordance with Table C.1, by dividing the stress into three sections:

a) The non-supply pin test, where all non-supply pins are only stressed to their associated supply pin groups. This can be done by partitioning the device into functional blocks.

b) The supply pin test, where every supply pin is stressed to all other supplies.

c) The I/O test, where the non-supply pins are tested to other non-supply pins as described in Table 2 row N+1.

For the non-supply pin test, devices are stressed so that for each supply pin group, all non-supply pins associated with this supply pin group are stressed separately only against their own supply. For example, for the set of supply pin group VDD1 pin 2 and pin 3 are stressed against pin 1 as well as against pin 4 (the same procedure is used for the other sets of supply pin groups).

For the supply pin test, devices are stressed so that only all power and ground pins (VDD1, VDD2-A, VDD2-B, VDD3, VDD4, VSS1 (as representative of the group VSS1, VSS2-A, VSS2-B) and VSS3 are stressed separately against each other.

For the I/O test only the two coupled non-supply pin pairs are stressed against each other.

Table C.1 – Product testing in accordance with Table 2

Pin combination set number	Pin(s) connected to terminal B	Pin connected to terminal A (single pins, tested one at a time)	Number of zaps (1pos/1neg)
1	VDD1 (pin 1)	VSS1 (pin 4), VDD2-A (pin 5), VDD2-B (pin 6), VDD3 (pin 13), VSS3/VSS4 (pin 14), VDD4 (pin 15)	12
		I/O-11 (pin 2), I/O-12 (pin 3)	4
2	VSS1 (pin 4)	VDD1 (pin 1), VDD2-A (pin 5),VDD2-B (pin 6), VDD3 (pin 13), VSS3/VSS4 (pin 14), VDD4 (pin 15)	12
		I/O-11 (pin 2), I/O-12 (pin 3), I-21 (pin7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10)	12
3	VDD2-A (pin 5), VDD2-B (pin 6)	VDD1 (pin 1), VSS1 (pin 4), VDD3 (pin 13), VSS3/VSS4 (pin 14), VDD4 (pin 15)	10
		I-21 (pin 7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10)	8
4	VDD3 (pin 13)	VDD1 (pin 1), VSS1 (pin 4), VDD2-A (pin 5), VDD2-B (pin 6), VSS3/VSS4 (pin 14), VDD4 (pin 15)	12
		(No associated non-supply pins)	0
5	VDD4 (pin 15)	VDD1 (pin 1), VSS1 (pin 4), VDD2-A (pin 5), VDD2-B (pin 6), VDD3 (pin 13), VSS3/VSS4 (pin 14)	12
		I/O-41 (pin 16)	2
6	VSS3/VSS4 (pin 14)	VDD1 (pin 1), VSS1 (pin 4), VDD2-A (pin 5), VDD2-B (pin 6), VDD3 (pin 13), VDD4 (pin 15)	12
		I/O-41 (pin 16)	2
7 (i.e., N+1)	I/O-11 (pin 2)	I/O-12 (pin 3)	2
	I/O-12 (pin 3)	I/O-11 (pin 2)	2
	I/O-21 (pin 9)	I/O-22 (pin 10)	2
	I/O-22 (pin 10)	I/O-21 (pin 9)	2
NOTE Performing the stress in such a way a device would see in total 106 zaps per voltage level.			

C.3 Alternative procedure B (following Table 3):

The required stress combinations if coupled-pair information and non-supply pin associations are not available. This is the legacy method of testing, in accordance with Table C.2.

Table C.2 – Product testing in accordance with Table 3

Pin combination set number	Pin(s) connected to terminal B	Pin connected to terminal A (single pins, tested one at a time)	Number of zaps (1pos/1neg)
1	VDD1 (pin 1)	VSS1 (pin 4), VDD2-A (pin 5), VDD2-B (pin 6), VDD3 (pin 13), VSS3/VSS4 (pin 14), VDD4 (pin 15)	12
		I/O-11 (pin 2), I/O-12 (pin 3), I-21 (pin7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10), I/O-41 (pin 16)	14
2	VSS1 (pin 4)	VDD1 (pin 1), VDD2-A (pin 5), VDD2-B (pin 6), VDD3 (pin 13), VSS3/VSS4 (pin 14), VDD4 (pin 15)	12
		I/O-11 (pin 2), I/O-12 (pin 3), I-21 (pin 7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10), I/O-41 (pin 16)	14
3	VDD2-A (pin 5), VDD2-B (pin 6)	VDD1 (pin 1), VSS1 (pin 4), VDD3 (pin 13), VSS3/VSS4 (pin 14), VDD4 (pin 15)	10
		I/O-11 (pin 2), I/O-12 (pin 3), I-21 (pin 7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10), I/O-41 (pin 16)	14
4	VDD3 (pin 13)	VDD1 (pin 1), VSS1 (pin 4), VDD2-A (pin 5), VDD2-B (pin 6), VSS3/VSS4 (pin 14), VDD4 (pin 15)	12
		I/O-11 (pin 2), I/O-12 (pin 3), I-21(pin 7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10), I/O-41 (pin 16)	14
5	VDD4 (pin 15)	VDD1 (pin 1), VSS1 (pin 4), VDD2-A (pin 5), VDD2-B (pin 6), VDD3 (pin 13), VSS3/VSS4 (pin 14)	12
		I/O-11 (pin 2), I/O-12 (pin 3), I-21 (pin 7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10), I/O-41 (pin 16)	14
6	VSS3/VSS4 (pin 14)	VDD1 (pin 1), VSS1 (pin 4), VDD2-A (pin 5), VDD2-B (pin 6), VDD3 (pin 13), VDD4 (pin 15)	12
		I/O-11 (pin 2), I/O-12 (pin 3),), I-21 (pin7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10), I/O-41 (pin 16)	14

Pin combination set number	Pin(s) connected to terminal B	Pin connected to terminal A (single pins, tested one at a time)	Number of zaps (1pos/1neg)
7 (i.e., N+1)	I/O-11 (pin 2), I/O-12 (pin 3), I-21 (pin7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10), I/O-41 (pin 16) Except for the pin being stressed (i.e., connected to terminal A)	I/O-11 (pin 2)	2
		I/O-12 (pin 3)	2
		I-21 (pin 7)	2
		O-21 (pin 8)	2
		I/O-21 (pin 9)	2
		I/O-22 (pin 10)	2
		I/O-41 (pin 16)	2
NOTE Performing the stress in such a way a device would see in total 156 zaps per voltage level.			

C.4 Alternative procedure C (following Table 2):

An example of the stress combinations using a two-pin HBM tester with coupled non-supply pin information and non-supply pin associations is provided in Table C.3. For this example, it is assumed that the parasitics are low enough to take advantage of nearly identical waveforms on terminals A and B as discussed in B.4.

Table C.3 – Alternative product testing in accordance with Table 2

Pin combination set number	Pin(s) connected to terminal B	Pin connected to terminal A (single pins, tested one at a time)	Number of zaps (1pos/1neg)
1	VDD1 (pin 1)	VSS1 (pin 4), VDD2-A (pin 5), VDD2-B (pin 6), VDD3 (pin 13), VSS3/VSS4 (pin 14), VDD4 (pin 15)	12
		I/O-11 (pin 2), I/O-12 (pin 3)	4
2	VSS1 (pin 4)	VDD2-A (pin 5), VDD2-B (pin 6), VDD3 (pin 13), VSS3/VSS4 (pin 14), VDD4 (pin 15)	10
		I/O-11 (pin 2), I/O-12 (pin 3), I-21(pin 7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10)	12
3	VDD2-A (pin 5)	VDD3 (pin 13), VSS3/VSS4 (pin 14), VDD4 (pin 15)	6
		I-21(pin 7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10)	8
4	VDD2-B (pin 6)	VDD3 (pin 13), VSS3/VSS4 (pin 14), VDD4 (pin 15)	6
		I-21(pin 7), O-21 (pin 8), I/O-21 (pin 9), I/O-22 (pin 10)	8
5	VDD3 (pin 13)	VSS3/VSS4 (pin 14), VDD4 (pin 15)	4
		(No associated non-supply pins)	0
6	VDD4 (pin 15)	VSS3/VSS4 (pin 14)	2
		I/O-41 (pin 16)	2
7	VSS3/VSS4 (pin 14)	(All supply to supply combinations have been stressed)	0
		I/O-41 (pin 16)	2

Pin combination set number	Pin(s) connected to terminal B	Pin connected to terminal A (single pins, tested one at a time)	Number of zaps (1pos/1neg)
8	I/O-11 (pin 2)	I/O-12 (pin 3)	2
(i.e., N+1)	I/O-21 (pin 9)	I/O-22 (pin 10)	2
NOTE When the stressing is performed this way, a device would see 80 zaps per voltage level.			

Annex D
(informative)

Examples of coupled non-supply pin pairs

Pin names and engineering judgment can be a guide to identify coupled non-supply pin pairs. Examples of names used with coupled non-supply pin pairs are:

- USB data pins, such as:
  - D+ and D-
  - DP and DM
- PCI pins, such as:
  - TxP and TxN
  - RxP and RxN
  - DMI_TXN and DMI_TXP
  - DMI_RXN and DMI_RXP
- Crystal pin pairs, such as:
  - XTALin/XTALout
  - XTAL_+ and XTAL_-
  - XTAL_1 and XTAL_2
  - XTAL_A and XTAL_B
- Signal pin pairs that end with P and N, such as:
  - OUT_P and OUT_N
  - IN_P and IN_N
  - VREF_P and VREF_N
  - PEG_RXN and PEG_RXP
  - PEG_TXN and PEG_TXP
  - CCP_DP and CCN_DN
  - BCLK_DN and BCLK_DP
  - x_CLK_N and x_CLK_P
  - QPI_RX_N and QPI_RX_P
- Signal pin pairs that have X added to the signal name for the inverted signal, such as:
  - BT_RFIO and BT_RFIOX
  - FMR_RTX and FMR_RTXX
  - RX12 and RX12X
- LNA_IN and LNA_OUT
- RF_IN and RF_OUT
- THERMDA/THERMDC (thermal diode anode and cathode)

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