BS EN 60747-15:2012

BSI Standards Publication

Semiconductor devices — Discrete devices

Part 15: Isolated power semiconductor devices

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National foreword

This British Standard is the UK implementation of EN 60747-15:2012. It is identical to IEC 60747-15:2010. It supersedes BS EN 60747-15:2004 which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

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Discrete devices -
Part 15: Isolated power semiconductor devices
(IEC 60747-15:2010)

Dispositifs à semi-conducteurs -
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Partie 15: Dispositifs de puissance à semiconducteurs isolés
(CEI 60747-15:2010)

Halbleiterbauelemente -
Einzel-Halbleiterbauelemente -
Teil 15: Isolierte Leistungshalbleiter
(IEC 60747-15:2010)

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Foreword

The text of document 47E/403/FDIS, future edition 2 of IEC 60747-15, prepared by SC 47E, "Discrete semiconductor devices", of IEC TC 47, "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 60747-15:2012.

The following dates are fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2012-09-16
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2014-01-20

This European Standard supersedes EN 60747-15:2004.

The main changes with respect to EN 60747-15:2004 are listed below.

a) Clause 3, 4 and 5 were re-edited and some of them were combined to other sub clauses.

b) Clause 6, 7 were re-edited as a part of “Measuring methods” with amendment of suitable addition and deletion.

c) Clause 8 was amended by suitable addition and deletion.

d) Annex C, D and Bibliography were deleted.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 60747-15:2010 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60112	NOTE	Harmonized as EN 60112.
IEC 61287-1:2005	NOTE	Harmonized as EN 61287-1:2006 (not modified).

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 60270	-	High-voltage test techniques - Partial discharge measurements	EN 60270	-
IEC 60664-1	2007	Insulation coordination for equipment within low-voltage systems - Part 1: Principles, requirements and tests	EN 60664-1	2007
IEC 60721-3-3	1994	Classification of environmental conditions - Part 3: Classification of groups of environmental parameters and their severities - Section 3: Stationary use at weatherprotected locations	EN 60721-3-3	1995
IEC 60747-1	2006	Semiconductor devices - Part 1: General	-	-
IEC 60747-2	-	Semiconductor devices - Discrete devices and integrated circuits - Part 2: Rectifier diodes	-	-
IEC 60747-6	-	Semi conductor devices - Part 6: Thyristors	-	-
IEC 60747-7	-	Semiconductor devices - Part 7: Bipolar transistors	-	-
IEC 60747-8	-	Semiconductor devices - Part 8: Field-effect transistors	-	-
IEC 60747-9	-	Surface mounting technology - Discrete devices - Part 9: Insulated-gate bipolar transistors (IGBTs)	-	-
IEC 60749-5	-	Semiconductor devices - Mechanical and climatic test methods - Part 5: Steady-state temperature humidity bias life test	EN 60749-5	-
IEC 60749-6	-	Semiconductor devices - Mechanical and climatic test methods - Part 6: Storage at high temperature	EN 60749-6	-
IEC 60749-10	-	Semiconductor devices - Mechanical and climatic test methods - Part 10: Mechanical shock	EN 60749-10	-
IEC 60749-12	-	Semiconductor devices - Mechanical and climatic test methods - Part 12: Vibration, variable frequency	EN 60749-12	-

Publication	Year	Title	EN/HD	Year
IEC 60749-15	-	Semiconductor devices - Mechanical and climatic test methods - Part 15: Resistance to soldering temperature for through-hole mounted devices	EN 60749-15	-
IEC 60749-21	-	Semiconductor devices - Mechanical and climatic test methods - Part 21: Solderability	EN 60749-21	-
IEC 60749-25	-	Semiconductor devices - Mechanical and climatic test methods - Part 25: Temperature cycling	EN 60749-25	-
IEC 60749-34	-	Semiconductor devices - Mechanical and climatic test methods - Part 34: Power cycling	EN 60749-34	-

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SEMICONDUCTOR DEVICES –
DISCRETE DEVICES –

Part 15: Isolated power semiconductor devices

1 Scope

This part of IEC 60747 gives the requirements for isolated power semiconductor devices excluding devices with incorporated control circuits. These requirements are additional to those given in other parts of IEC 60747 for the corresponding non-isolated power devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60270, *High-voltage test techniques – Partial discharge measurements*

IEC 60664-1:2007, *Insulation coordination for equipment within low-voltage systems – Part 1: Principles, requirements and tests*

IEC 60721-3-3:1994, *Classification of environmental conditions – Part 3-3: Classification of groups of environmental parameters and their severities – Stationary use at weather protected locations*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-2, *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*

IEC 60747-6, *Semiconductor devices – Part 6: Thyristors*

IEC 60747-7, *Semiconductor discrete devices and integrated circuits – Part 7: Bipolar transistors*

IEC 60747-8, *Semiconductor devices – Part 8: Field-effect transistors*

IEC 60747-9, *Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)*

IEC 60749-5, *Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test*

IEC 60749-6, *Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature*

IEC 60749-10, *Semiconductor devices – Mechanical and climatic test methods – Part 10: Mechanical shock*

IEC 60749-12, *Semiconductor devices – Mechanical and climatic test methods – Part 12: Vibration, variable frequency*

IEC 60749-15, *Semiconductor devices – Mechanical and climatic test methods – Part 15: Resistance to soldering temperature for through-hole mounted devices*

IEC 60749-21, *Semiconductor devices – Mechanical and climatic test methods – Part 21: Solderability*

IEC 60749-25, *Semiconductor devices – Mechanical and climatic test methods – Part 25: Temperature cycling*

IEC 60749-34, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
isolated power semiconductor device
semiconductor power device that contains an integral electrical insulator between the cooling surface or base plate and any isolated circuit elements

3.2 Constituent parts of the isolated power semiconductor device

3.2.1
switch
any single component that performs a switching function in a electrical circuit, e.g. diode, thyristor, MOSFET, etc.

NOTE A switch might be a parallel or series connection of several chips with a single functionality.

3.2.2
base plate
part of the package having a cooling surface that transfers the heat from inside to outside

3.2.3
main terminal
terminal having a high potential of the power circuit and carrying the main current. The main terminal can comprise more than one physical connector.

3.2.4
control terminal
terminal having a low current capability for the purpose of control function, to which the external control signals are applied or from which sensing parameters are taken

3.2.4.1
high voltage control terminal
terminal electrically connected to an isolated circuit element, but carrying only low current for control function

NOTE Examples include current shunts and collector sense terminals having the high potential of the main terminals.

3.2.4.2
low voltage control terminal
terminal having a control function and isolated from the high voltage control terminals

NOTE Examples include the terminals of isolated temperature sensors and isolated gate driver inputs etc.

3.2.5
insulation layer
integrated part of the device case that insulates any part having high potential from the cooling surface or external heat sink and any isolated circuit element

3.3
peak case non-rupture current
peak current, which will not lead to a rupture of the package, ejecting plasma and massive particles under specified conditions

3.4
thermal interface material
heat conducting material between base plate and external heat sink

4 Letter symbols

4.1 General

General letter symbols are defined in Clause 4 of IEC 60747-1:2006.

4.2 Additional subscripts/symbols

p = parasitic

t = terminal

isol = isolation

m = mount

4.3 List letter symbols

4.3.1 Voltages and currents

Terminal current	I_{tRMS}
Isolation voltage	V_{isol}
Partial discharge inception voltage	V_i
Partial discharge extinction voltage	V_e
Isolation leakage current	I_{isol}
Peak case non-rupture current (for diode and thyristor devices)	I_{RSMC}
Peak case non-rupture current (for IGBT and MOSFET devices)	I_{CNR}

4.3.2 Mechanical symbols

Mounting torque for screws to heat sink	M_s
Mounting torque for terminal screws	M_t
Mounting force	F
Maximum acceleration in all 3 axis (x, y, z)	a
Mass	m
Flatness of the case (base-plate)	e_c
Flatness of the cooling surface (heat sink)	e_s
Roughness of the case (base plate)	R_{Zc}
Roughness of the cooling surface (heat sink)	R_{Zs}
Thickness of thermal interface material (case - sink)	$d_{(c-s)}$

4.3.3 Other symbols

Total maximum power dissipation per switch at T_c = 25 °C	P_{tot}
Parasitic inductance, effective between terminals and chips (to be specified)	L_p
Parasitic capacitance between terminals and cooling surface (case, base plate, ground)	C_p
Lead resistance between terminal x and related switch x’	$r_{xx'}$
Terminal temperature	T_t
Number of power load cycles until failure of a percentage p of a population of devices	$N_{f;p}$

5 Essential ratings (limiting values) and characteristics

5.1 General

Isolated power semiconductor devices should be specified as case rated or heat-sink rated devices. The ratings and characteristics should be quoted at a temperature of 25 °C or another specified elevated temperature. Requirements for multiple devices having a common encapsulation see 5.12 of IEC 60747-1:2006.

5.2 Ratings (limiting values)

5.2.1 Isolation voltage (V_{isol})

Maximum r. m. s. or d. c. value between main terminals and high voltage control terminals at one side and low voltage control terminals (where appropriate) and base plate at the other side for a specified time

5.2.2 Peak case non-rupture current (I_{RSMC} or I_{CNR}) (where appropriate)

Maximum value for each main terminal that does not cause the bursting of the case or emission of plasma and particles

5.2.3 Terminal current (I_{tRMS}) (where appropriate),

Maximum r. m. s. value of the current through the main terminal under specified conditions at minimum mounting torque M_t and maximum allowed terminal temperature ($T_{tmax} = T_{stg}$ or $T_{tmax} \leq T_{vjmax}$)

5.2.4 Total power dissipation (P_{tot})

Maximum value per switch at T_c = 25 °C (or T_s = 25 °C), when $T_{vj} = T_{vjmax}$, at d.c. load.

5.2.5 Temperatures

5.2.5.1 Solder temperature (T_{sold})

Maximum solder temperature T_{sold} during solder process over a specified solder processing time t_{sold}

5.2.5.2 Storage temperature (T_{stg})

Minimum and maximum storage temperature

5.2.6 Mechanical ratings

5.2.6.1 Mounting torque of screws to heat sink (M_s)

Minimum mounting torque that shall be applied to the fixing screws to the heat sink

5.2.6.2 Mounting torque of screws to terminals (M_t)

Minimum mounting torque that shall be applied to screwed terminals

5.2.6.3 Mounting force (F)

Minimum mounting force for pressure mounted devices, fixed by clips, that shall be applied to the isolated pressure contact device

5.2.6.4 Terminal pull-out force (F_t)

Maximum force

5.2.6.5 Acceleration (a)

Maximum value along each axis (x, y, z)

5.2.6.6 Flatness of the heatsink surface (e_S) (where appropriate)

Maximum deviation from flatness for the heatsink surface over the whole mounting area

5.2.6.7 Roughness of the heatsink surface (R_{ZS}) (where appropriate)

Maximum roughness of the heatsink surface over the whole mounting area

5.2.7 Climatic ratings (where appropriate)

Limiting values of environmental parameters for the final application as follows

- ambient temperature
- humidity
- speed and pressure of air
- irradiation by sun and other heat sources
- mechanical active substances
- chemically active substances
- biological issues

shall be described in classes as specified in IEC 60721-3-3:1994, Table 1.

5.3 Characteristics

5.3.1 Mechanical characteristics

5.3.1.1 Creepage distance along surface (d_s)

Minimum value of distance along surface of the insulating material of the device between terminals of different potential and to base plate

NOTE 1 IEC 60112 (details to comparative tracking index “CTI”) and IEC 60664-1:2007 Subclause 5.2 apply.

NOTE 2 Air gaps between plastic surface and grounded metal or between terminals of opposite polarity smaller than 1,0 mm (for pollution degree 2), or 1,5 mm (pollution degree 3) shorten the countable creepage distance considerably (details see 60664-1:2007, examples). This is essential, if dust, moisture or dirt starts to cover the

surface and increases the leakage current over surface, which might start burning the plastic encapsulation material.

5.3.1.2 Clearance distance in air (d_a)

Minimum value of distance through air between terminals of different potential of the isolated device and to base plate

NOTE For details, see IEC 60664-1:2007, (Subclause 4.6 and Subclause 5.1) which shows typical examples of various shapes of clearance distances.

5.3.1.3 Mass (m) of the device

Maximum value excluding accessories (mounting hardware).

5.3.1.4 Flatness of the base plate (e_C) (where appropriate)

Maximum and minimum allowed deviation from flatness for the base plate and its direction (convex or concave).

5.3.2 Parasitic inductance (L_p)

Maximum or typical value between the main terminals of each main current path.

5.3.3 Parasitic capacitances (C_p)

Maximum value of parasitic capacitance between the specified main terminal(s) and the cooling surface.

5.3.4 Partial discharge inception voltage (V_{iM} or $V_{i(RMS)}$) (where appropriate)

Minimum peak value V_{iM} or r.m.s. value $V_{i(RMS)}$ between the isolated terminals and the base plate (details, see IEC 60270).

5.3.5 Partial discharge extinction voltage (V_{eM} or $V_{e(RMS)}$) (where appropriate)

Minimum peak value V_{eM} or r.m.s. value $V_{e(RMS)}$ between the isolated terminals and the base plate (for details, see IEC 60270).

5.3.6 Thermal resistances

5.3.6.1 Thermal resistance junction to case for case rated devices ($R_{th(j-c)X}$)

Maximum value of thermal resistance junction to a specified reference point at the case (base plate) per switch “X” (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)).

5.3.6.2 Thermal resistance case to heat sink ($R_{th(c-s)}$) (where appropriate)

Maximum or typical value of thermal resistance between two specified points at the case and at the heat sink of the case rated device (“module”), when the case is mounted according to manufacturer’s mounting instructions.

5.3.6.3 Thermal resistance case to heat sink per switch ($R_{th(c-s)X}$) (where appropriate)

Maximum or typical value of thermal resistance between the two specified points of the case and the heat sink of the switch “X” (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)) of the isolated case rated devices (“module”), when the case is mounted according to the manufacturer’s mounting instructions.

5.3.6.4 Thermal resistance junction to heat sink for heat sink rated devices ($R_{th(j-s)X}$)

Maximum or typical value of thermal resistance junction to a specified point at the heat sink per switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)), when the device is mounted according to the manufacturer's mounting instructions.

5.3.6.5 Thermal resistance junction to sensor ($R_{th(j-r)}$) (where appropriate)

Value of thermal resistance junction to an integrated temperature sensor, when the device is mounted according to the manufacturer's mounting instructions.

NOTE The position of this thermal resistance should be shown in the thermal resistance equivalent circuit.

5.3.7 Transient thermal impedance (Z_{th})

Thermal impedance as a function of the time elapsed after a step change of power dissipation for each thermal resistance specified in Subclause 5.3.6 and shall be specified in one of the following ways.

6 Measurement methods

6.1 Verification of isolation voltage rating between terminals and base plate (V_{isol})

– **Purpose**

Proof of the ability of the isolated power device to withstand the rated isolation voltage

– **Circuit diagram**

See Figure 1 below.

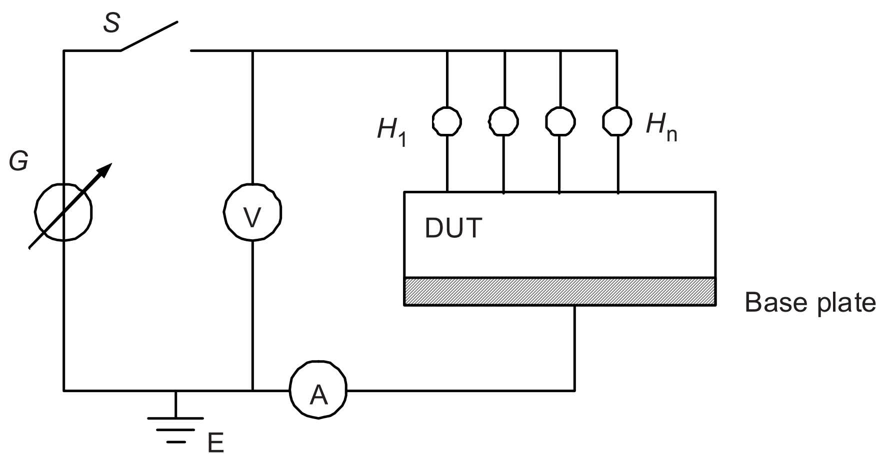


Figure 1 – Basic circuit diagram for isolation breakdown withstand voltage test ("high pot test") with V_{isol}

– **Circuit description and requirements**

DUT = Device under test

G = voltage source with high impedance, capable to supply V_{isol}

S = main switch

V = voltmeter for V_{isol}

A = ammeter or current probe for I_{isol}

$H_1 \ldots H_n$ = high potential terminal

The voltage source *G* is capable to supply the isolation voltage V_{isol} as the a. c. or d. c. voltage with a high internal impedance to limit the possible breakthrough current in case of breakdown of the DUT.

All main terminals and high voltage control terminals are connected together and connected to the high potential output terminal *H* of the voltage source *G*. The base plate of the DUT, respectively its metallized cooling surface and all low voltage terminals are connected to ground potential E. An amperemeter or current probe A is applied to measure the isolation leakage current.

– **Test procedure**

Switch *S* is closed and the voltage is slowly raised to the specified value and maintained at that value for the specified time. The current measured on ammeter A shall not exceed the specified value. The voltage is then reduced to zero.

– **Specified conditions**

Specified in IEC 60664-1:2007.

- Ambient or case temperature
- V_{isol}
- I_{isol} as maximum test limit
- Test time *t*, if less than 60 s

6.2 Methods of measurement

6.2.1 Partial discharge inception and extinction voltages (V_i) (V_e)

Between high potential terminals and base plate (where appropriate). See IEC 60270 and IEC 60664-1:2007.

6.2.2 Parasitic inductance (L_p)

– **Purpose**

To measure the parasitic inductance between two main terminals

– **Circuit diagram**

See Figure 2 below.

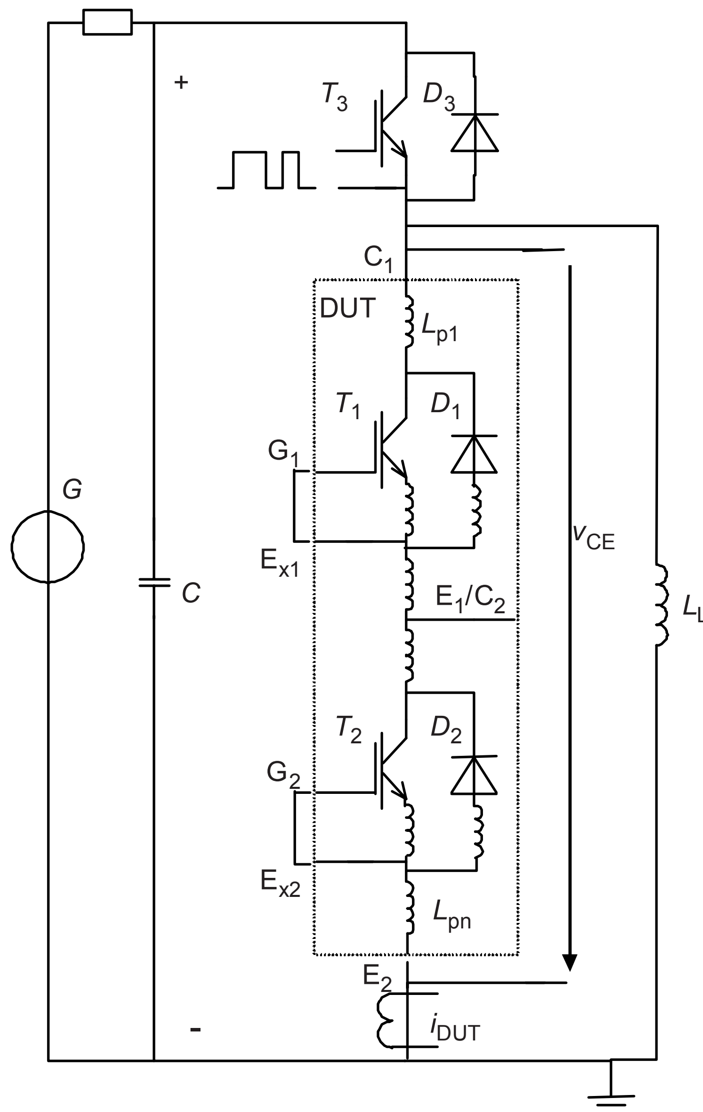


Figure 2 – Circuit diagram for measurement of parasitic inductances (L_p)

Key

DUT = device under test T1+T2, for example IGBT (Single or Dual – shown – or branch of a three phase arrangement), fast diode or MOSFET device

C = main capacitor bank as reservoir

L_L = load inductance, at least 100 times the parasitic inductance

$L_{p1} \dots L_{pn}$ = portions of parasitic inductance L_p

I_{DUT} = current probe

G = voltage source to charge the capacitor

T_1 = DUT, top switch (shown as IGBT in Figure 2)

T_2 = DUT, bottom switch (shown as IGBT in Figure 2), optional

T_3 = auxiliary IGBT switch

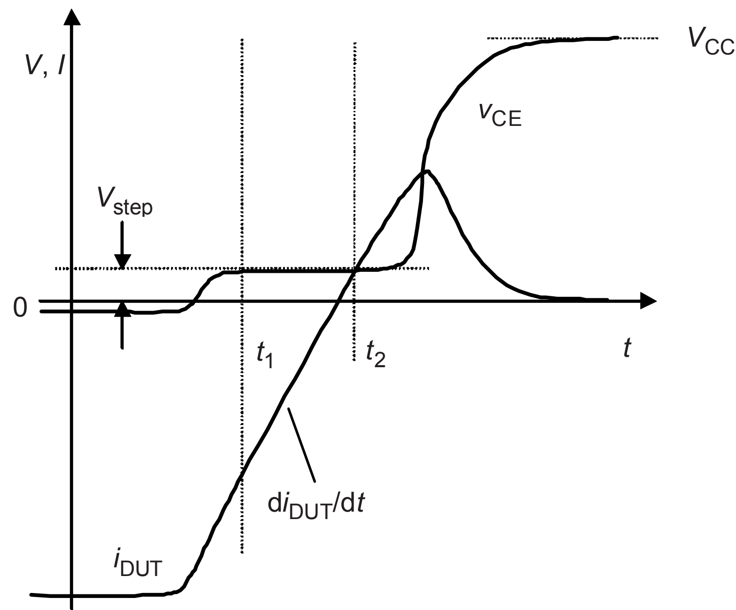


Figure 3 – Wave forms

– **Circuit description and requirements**

The circuit of Figure 2 consists of a DC supply *G* for the charge reservoir C; T_3 is an auxiliary switch, a gate drive unit for T_3, the DUT inserted into the test set-up with the gate control terminals shorted, a dual channel oscilloscope, which senses the voltage V_{CE} between main terminals "C_1" and "E_2", a current probe, which senses the current I_{DUT} through the diode path of the DUT, connected to the dual channel oscilloscope. This measuring method uses reduced voltage V_{CC} and the d*i*/dt of diodes incorporated in the device at switch-off, sensing the voltage at outside main terminals. This is usable for single switch devices as well as for half bridge circuit devices (DUAL modules).

– **Measurement procedure**

A pulsed current method is used. Auxiliary transistor T_3 switches the load current to the inductor L_L on and off. When T_3 is off, the current freewheels via the diodes of the DUT. When T_3 switches on again, it causes the current through the diodes to fall at an almost linear rate di_{DUT}/dt. During this time (t_1 –t_2), the voltage across the DUT forms at step of V_{step} caused by the internal parasitic inductance at current decline (di_{DUT}/dt). The value of the parasitic inductance of the main current path can be calculated from

$$L_p = V_{step} / |(di_{DUT}/dt)| \quad (1)$$

NOTE Use low inductance (sheeted) bus baring and low inductance current probe.

6.2.3 Parasitic capacitance terminal to case (C_p)

– **Purpose**

To measure the parasitic capacitance C_p between specified main terminal(s) and the case (base plate)

– **Circuit diagram**

See Figure 4 below.

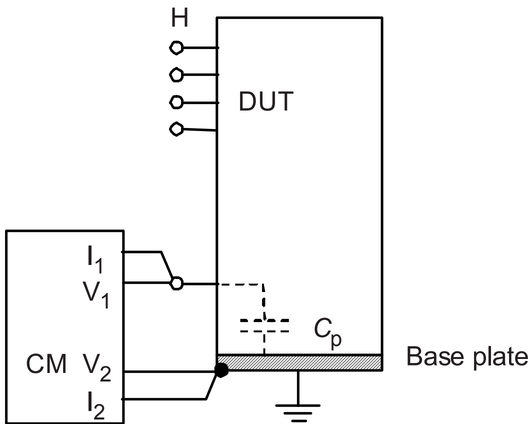


Figure 4 – Circuit diagram for measurement of parasitic capacitance (C_p)

– **Circuit description and requirements**

C_p = parasitic capacitance

H = high potential terminal

CM = capacitance meter

– **Measurement procedure**

Mount the device to a grounded heat sink according to the manufacturer's mounting instructions. Connect the current source connector "I_1" of the capacitance meter CM to the specified terminal and connector "I_2" to ground (base plate) of the DUT. Connect the voltage sensing connector of the capacitance meter to test points "V_1" and "V_2" to ground. CM is set to the specified frequency. The capacitance C_p can be read on CM. For the measurement of the total coupling capacitance C_p connect all main terminals to each other and proceed with the measurement like described above.

– **Specified conditions**

- Measurement frequency *f* of the CM

6.2.4 Thermal characteristics

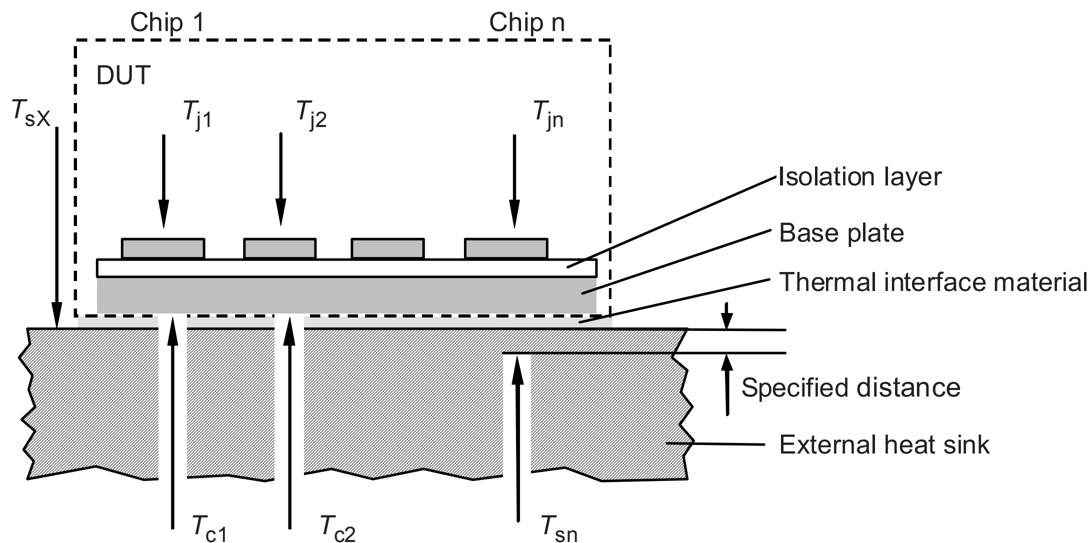
6.2.4.1 General description of measuring methods

– **Purpose**

To measure thermal characteristics between the switch and the cooling system

– **Reference points for temperature measurement and description**

Same methods should be used as for the corresponding non-isolated device. Thermal resistance and impedance are measured in the same way as described in the documents for diodes IEC 60747-2, thyristors IEC 60747-6, bipolar transistors IEC 60747-7, FETs IEC 60747-8 and IGBTs IEC 60747-9.



Key

$T_{j1...n}$ = junction temperature of chip 1 to n

$T_{c1...n}$ = case temperature under chip 1 to n

$T_{s1...n}$ = heatsink temperature under chip 1 to n

T_{sX} = heatsink temperature at a specified surface point

Figure 5 – Cross-section of an isolated power device with reference points for temperature measurement of T_c and T_s

– **Measurement procedure**

T_c is measured by a temperature measuring instrument from underneath through a small hole through the heat sink and any thermal interface material underneath the switch (chip). T_s is taken from above at hottest accessible point, nearest to the switch (chip) or from underneath through a specified sack hole ending at 2 (+/-1) mm below the heat sink surface (to be specified, type test feature). T_j is determined using indirect methods like described in the individual documents.

NOTE The thermal resistance $R_{th(j-s)}$ and $R_{th(c-s)}$ depends on several mechanical parameters such as type and thickness of the used thermal interface material (should be specified in manufacturer's mounting instructions, for example 30 to 50µm), the max. deviation of flatness of the cooling surface of the device's base plate and of the heat sink and the mounting torque of the fixing screws, as per specified mounting instructions.

6.2.4.2 Thermal resistance junction to case per switch $R_{th(j-c)}$

$$R_{th(j-c)} = (T_j - T_c)/P \qquad (2)$$

where

T_j is the virtual junction temperature of the switch;

T_c is the temperature of the case (base plate) under the switch (chip);

P is the power dissipation of a switch (see Figure 5).

6.2.4.3 Thermal resistance case to heat sink per switch (X) $R_{th(c-s)X}$ or per device $R_{th(c-s)}$

$$R_{th(c-s)(X)} = (T_c - T_s)/P_X \qquad (3)$$

where

X is the D (Diode), I (IGBT); M (MOSFET)

T_c is the temperature taken at the specified point of the case (as above) under the chip

T_s is the temperature of the heat sink, taken at the reference point for testing T_s specified

P_X is the complete power dissipation of the switch

P is the power dissipation of the complete device

– **Specified conditions**
  - Mounting according manufacturer's instructions
  - Thermal conductivity of the thermal interface material
  - Reference points for thermal measurement

NOTE See Annex B for Measuring method of the thickness of thermal interface material.

6.2.4.4 Thermal resistance junction to heat sink per switch $R_{th(j-s)}$ (for heat sink rated devices)

$$R_{th(j-s)} = (T_j - T_{sn})/P \quad (4)$$

where

T_j is the virtual junction temperature of the switch;

T_{sn} is taken at the specified reference point n at the heatsink (see Figure 5);

P is the power dissipation of the switch.

– **Specified conditions**
  - Mounting according manufacturer's instructions
  - Thermal conductivity of the thermal interface material
  - Reference points for thermal measurement

6.2.4.5 Transient thermal impedance Z_{th}

– **Measurement circuit and procedure**

These are based on former Subclause 6.2.4.2 to 6.2.4.4. Individual documents of the non-insulated devices apply.

$$Z_{th(j-c)} = (|T_j(0) - T_c(0)| - |T_j(t) - T_c(t)|)/P \quad (5)$$

$$Z_{th(c-s)} = (|T_c(0) - T_s(0)| - |T_c(t) - T_s(t)|)/P \quad (6)$$

$$Z_{th(j-s)} = (|T_j(0) - T_s(0)| - |T_j(t) - T_s(t)|)/P \quad (7)$$

– **Specified conditions**
  - Mounting according manufacturer's instructions
  - Thermal conductivity of the thermal interface material
  - Reference points for thermal measurement

7 Acceptance and reliability

7.1 General requirements

In addition to the following subclauses, the requirements applicable to the non-isolated devices as given in the other relevant parts of IEC 60747 apply.

7.2 List of endurance tests

See Table 1.

Table 1 – Endurance tests

Subclause	Environmental Testing – designation	Short form	Normative references
7.2.1	High temperature reverse bias or high temperature blocking	HTRB	IEC 60749-5
7.2.2	High humidity and high temperature reverse bias or high humidity and high temperature blocking	H^3TRB	IEC 60749-5
7.2.3	Power cycling (load) capability		IEC 60749-34
7.2.4	High temperature storage	HTS	IEC 60749-6
7.2.5	Low temperature storage	LTS	IEC 60068-2-48[1]
7.2.6	Thermal cycling	TC	IEC 60749-25;
7.2.7	Resistance to solder heat		IEC 60749-15
7.2.8	Solderability		IEC 60749-21
7.2.9	Mechanical shock		IEC 60749-10
7.2.10	Vibration (variable frequency)		IEC 60749-12

7.3 Acceptance defining criteria

Table 2 – Acceptance defining characteristics for endurance and reliability tests

Acceptance defining characteristic	Acceptance criteria	Measurement conditions
I_{isol}	< USL	Specified V_{isol}
R_{th}	< USL	Mounting instructions
USL: upper specification limit		

7.4 Type tests and routine tests

7.4.1 Type tests

The experience which has been obtained with other isolated power semiconductor devices, using the same or similar components such as switches or packages, should be considered when deciding which tests are mandatory.

Type tests are carried out on new products on a sample basis, in order to determine the electrical and thermal and mechanical and climatic ratings (limiting values) characteristics to be given in the data sheet and to establish the test limits for future routine tests. Some or all of the tests should be repeated from time to time on samples drawn from current production or deliveries so as to confirm that the quality of the product continuously meets the requirements.

The minimum type tests to be carried out are as follows:

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1 *Withdrawn in 2008.*

New isolated power semiconductor devices should undergo the type tests listed in Table 3, marked with “X” (X = mandatory). Some of the type tests are destructive.

Table 3 – Minimum type and routine tests for isolated power semiconductor devices

Subclause		Type test	Routine test	Destructive
5.2.1	Isolation voltage test V_{isol}	X	X	X
5.2.2	Peak case non-rupture current I_{RSMC} ; I_{CNR}	X [a]		
5.3.1	outline dimensions, creepage, clearance	X		
5.3.1.4	flatness of base-plate or of cooling surface	X	X [b]	
5.3.6	thermal resistances R_{th}	X		
5.3.7	transient thermal impedance Z_{th}	X		
5.3.2	parasitic inductance L_p	X [a]		
5.3.3	parasitic capacitance C_p	X [a]		
5.3.4/5	partial discharge voltages	X [a]		
5.2.6.4	terminal pull out force	X	X [b]	
7.2.6[c]	thermal cycling	X		
7.2.3[c]	power cycling (load)	X		
7.2.9/10[c]	mechanical tests	X		
5.2.7	climatic characteristics classification	X [a]		

NOTE Tests for isolation voltage, partial discharge voltage, creepage and clearance distance should be based on each standard which should be applied to any final equipment using the isolated power semiconductor device. For example see IEC 60950 (Safety information technology, IEC 61287 (rolling stock) etc..

[a] Type test only for devices with specified maximum values.

[b] Routine test only for devices with specified maximum or minimum values.

c See Table 1 for normative references of test.

7.4.2 Routine tests

The routine tests should be carried out on the current production or deliveries normally on a 100 % basis. The ratings and characteristics specified in the data sheet should be verified for each criterion or specimen. Routine test may comprise a selection of the isolated devices into groups of routine tests in Table 3. The minimum routine tests to be carried out on isolated devices are listed in Table 3. Other routine tests are carried out as described in the other parts of the IEC 60747, which is valid for the particular switch.

Annex A
(informative)

Test method of peak case non-rupture current[2]

– **Purpose**

To prove the ability of the isolated power device containing bipolar transistors, IGBTs or MOSFETs as switches to withstand the rated peak case non-rupture current I_{CNR} without causing a rupture (an "explosion") of the case or an emission of plasma beam or ejecting massive particles. This is a destructive test.

NOTE 1 Case rupture is caused by inside arc or vapour pressure, when the supplied energy or current from outer source exceeds the specified limit. The arc or vapour pressure is induced in a package (encapsulation) of failed power devices by being supplied with stored energy or current from an outer circuit power source. Critical current or energy for packages after the device failure should be issued as an item of the package environmental properties, and in addition the semiconductor and also other electrical parts should avoid an explosion by accident.

– **Circuit diagram**

See Figure A.1 below.

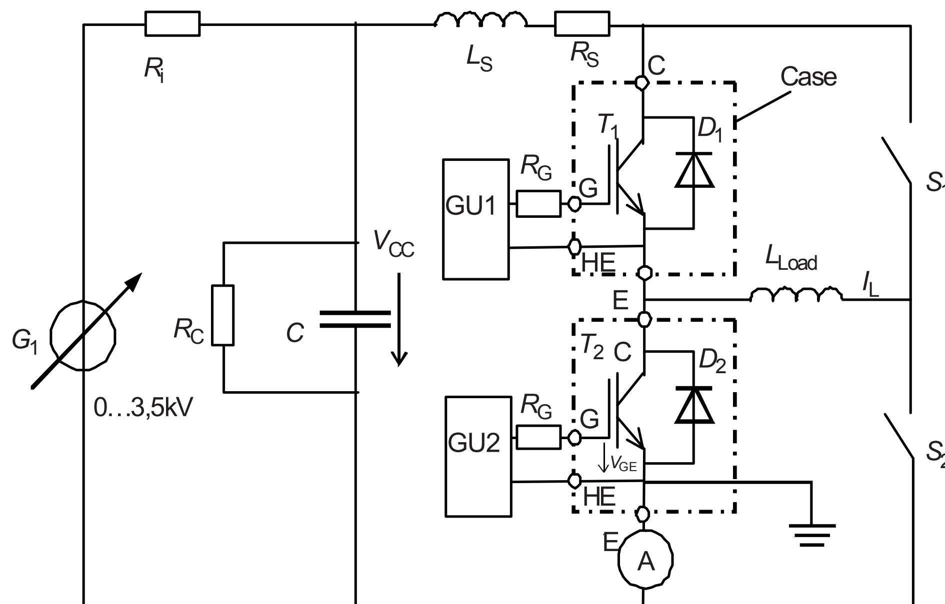

Figure A.1 – Circuit diagram for test of peak case non-rupture current I_{CNR}

– **Circuit description and requirements**

A = Ammeter to measure the device current which can be I_{CNR}, if the case just did not burst, monitored by a current probe having low inductance

C = line capacitor bank, chargeable to full voltage

D_1 = inverse diode of T_1, high side

D_2 = inverse diode of T_2, low side

G_1 = DC supply voltage source V_{CC}, which can be switched off from mains under all conditions

GU1 = gate drive unit of T_1

2 *still under discussion.*

GU2 = gate drive unit of T_2

L_{Load} = load inductance

L_s = parasitic inductance of the circuit (40 nH to 250 nH)

R_c = discharge resistor for protection purposes

R_G = gate resistor

R_i = internal source resistance

R_s = fuse resistor, mostly set to zero

S_1 = auxiliary switch (IGBT), high side

S_2 = auxiliary switch (IGBT), low side

T_1 = high side IGBT switch = device under test (DUT)

T_2 = low side IGBT switch

I_L = load current

V_{GE} = gate voltage

The set-up consists of a two-quadrant converter with two identical isolated IGBT devices. S_1 and S_2 are auxiliary switches, for example IGBT devices, used to establish the desired load current and to induce a short circuit failure. T_1 and T_2 are identical isolated IGBT devices (SINGLE switch or both in a half bridge circuit as DUAL switch).

– **Test procedure**

Test A:

First, close switch S_2, turn on T_1, the load current increases as defined by load inductance L_{Load}. After I_L have exceeded the safe operating area (SOA) for turn-off of T_1, it is attempted to turn off T_1. The initial part of the turn-off process takes place, the current in the device is reduced and part of the current is commuted to the diode D_2. The device T_1 then undergoes a turn-off failure. The diode in the low side device D_2 carries substantial current at this instant. The failure of T_1 forces the diode D_2 to turn off at virtually unlimited di/dt, drawn by L_{Load}. This is outside the diode SOA, and the diode D_2 also fails.

Test B:

T_1 is turned on until a substantial load current is reached. At this moment the device T_2 is turned on. It is induced to fail, because it sees the full voltage together with full current. The device T_1 then goes into desaturation and also fails. (Top-bottom shoot-through- which creates a short circuit between plus bus bar and minus bus bar, discharging the capacitor bank, creating an arc in the devices. This leads to production of gases of the surrounding plastic gel etc. until the energy of the capacitor bank is used). In reality such a failure could be due to cosmic ray or due to thermal overload. Manipulating the device can artificially induce it.

Tests C and further tests:

These tests are executed until a value of stored energy of the capacitor bank and of peak current is found, which is not high enough to rupture or break the case. The values of achieved peak current $I_C = I_{CNR}$, V_{CC}, C_{max} and of $E_C = ½ CV_{CC}^2$ are monitored. The value I_{CNR} is the value of a percentage (10 % = 2/20) of a tested population (minimum 10 pieces) of devices, at which the case did not burst, or case split, but did not eject internal particles.

– **Post test measurements and criteria**

The DUT is subjected to a visual test, whether cracks and signs of plasma from arcing inside are visible from outside. There shall be no signs of particles thrown out nor shall there be evidence that the device has externally melted or burst into flames.

NOTE 2 The ejection of particles is unavoidable for energies higher than about 10 kJ. What can be achieved by good design is that no massive parts are ejected, which can cause severe consequential damage.

– **Specified conditions**

- Case or virtual junction temperature (T_c = 25 °C, T_{vj} = 25 °C or 125 °C)
- Supply voltage V_{CC}
- Capacitance of capacitor bank C
- Stored energy of capacitor bank E_C
- Parasitic inductance of short circuit L_{SC}
- Load current I_L
- Gate voltage V_{GEon} and V_{GEoff}
- Gate resistance R_{Gon} and R_{Goff}
- Percentage of tested devices not burst to total number of tested devices

NOTE 3 Lit.: S. Gekenides, et al.: Explosion Tests on IGBT High voltage Modules, ISPSD '99 Toronto .

Annex B
(informative)

Measuring method of the thickness of thermal compound paste

The measuring gauge is a comb out of stainless steal or suitable plastic, which is not solvable by the fluid material of the thickness of layer to be tested. The outer teeth of the comb – those at the edges of the hexagon in Figure B.1 - form a base line. The inner teeth – those between the outer teeth - are progressively shortened, so that a space of distances is achieved between the teeth and the base line. The size of the distance can be read on a scale on the instrument. A typical measuring gauge is shown here in Figure B.1.

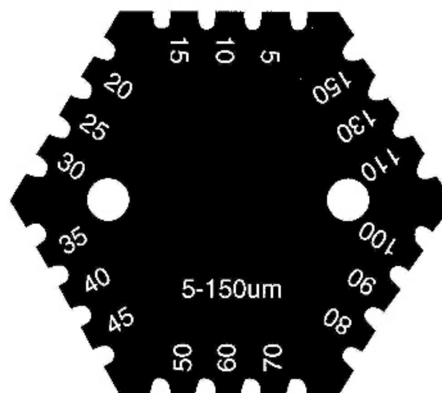

Figure B.1 – Example of a measuring gauge for a layer of thermal compound paste of a thickness between 5 μm and 150 μm

Measuring method

Immediately after applying the layer, the measuring comb is pressed upon the substrate, so that the teeth are vertical to the surface and the measuring comb does not slip. Remove the comb and look at the teeth to ensure that is the shortest tooth that still touched the fluid layer. The thickness of the layer corresponds to the average mean value of the last touching tooth and the first non-touching tooth. At least two further measurements at different parts on the surface are to be executed in same way to get representative values for the covered area.

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