BS EN 60424-3:2016

BSI Standards Publication

Ferrite cores — Guidelines on the limits of surface irregularities

Part 3: ETD-cores, EER-cores, EC-cores and E-cores

National foreword

This British Standard is the UK implementation of EN 60424-3:2016. It is identical to IEC 60424-3:2015. It supersedes BS EN 60424-3:1999 which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee EPL/51, Transformers, inductors, magnetic components and ferrite materials.

A list of organizations represented on this committee can be obtained on request to its secretary.

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Ferrite cores - Guidelines on the limits of surface irregularities - Part 3: ETD-cores, EER-cores, EC-cores and E-cores (IEC 60424-3:2015)

Noyaux ferrites - Lignes directrices relatives aux limites des irrégularités de surface - Partie 3: Noyaux ETD, EER, EC et E
(IEC 60424-3:2015)

Ferritkerne - Leitfaden für Grenzwerte von sichtbaren Beschädigungen der Kernoberfläche - Teil 3: ETD-Kerne, EER-Kerne, EC-Kerne und E-Kerne
(IEC 60424-3:2015)

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Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Avenue Marnix 17, B-1000 Brussels

European foreword

The text of document 51/1099/FDIS, future edition 2 of IEC 60424-3, prepared by IEC/TC 51 “Magnetic components and ferrite materials" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 60424-3:2016.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2016-08-26
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2018-11-26

This document supersedes EN 60424-3:1999.

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Endorsement notice

The text of the International Standard IEC 60424-3:2015 was approved by CENELEC as a European Standard without any modification.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu

Publication	Year	Title	EN/HD	Year
IEC 60424-1	2015	Ferrite cores - Guidelines on the limits of surface irregularities - Part 1: General Specification	EN 60424-1 [1)]	-
IEC 60647	-	Dimensions for magnetic oxide cores intended for use in power supplies (EC-cores)	-	-
IEC 61185	-	Ferrite cores (ETD-cores) intended for use in power supply applications - Dimensions	EN 61185	-
IEC 62317-7	-	Ferrite cores - Dimensions - Part 7: EER-cores	EN 62317-7	-
IEC 62317-8	-	Ferrite cores - Dimensions - Part 8: E-cores	EN 62317-8	-

[1)] To be published.

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

FERRITE CORES – GUIDELINES ON THE LIMITS OF SURFACE IRREGULARITIES –

Part 3: ETD-cores, EER-cores, EC-cores and E-cores

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International Standard IEC 60424-3 has been prepared IEC technical committee 51: Magnetic components and ferrite materials.

This second edition cancels and replaces the first edition published in 1999. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) addition of allowable areas of chips for EC-cores in Table 3,
b) addition of crystallites in 4.5 and pores in 4.6.

The text of this standard is based on the following documents:

FDIS	Report on voting
51/1099/FDIS	51/1114/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60424 series, published under the general title *Ferrite cores – Guidelines on the limits of surface irregularities*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

FERRITE CORES – GUIDELINES ON THE LIMITS OF SURFACE IRREGULARITIES –

Part 3: ETD-cores, EER-cores, EC-cores and E-cores

1 Scope

This part of IEC 60424 gives guidelines on allowable limits of surface irregularities applicable to ETD-cores, EER-cores, EC-cores and E-cores in accordance with the relevant general specification.

This standard is a specification useful in the negotiations between ferrite core manufacturers and customers about surface irregularities.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60424-1[1], *Ferrite cores – Guidelines on the limits of surface irregularities – Part 1: General specification*

IEC 60647, *Dimensions for magnetic oxide cores intended for use in power supplies (EC-cores)*

IEC 61185, *Ferrite cores (ETD-cores) intended for use in power supply applications – Dimensions*

IEC 62317-7, *Ferrite cores – Dimensions – Part 7: EER-cores*

IEC 62317-8, *Ferrite cores – Dimensions – Part 8: E-cores*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
pore
hole left on the surface of cores after sintering and surface finishing

3.2
crystallite
grain of abnormal size distinguishable on the surface, often with sparkling facets

[1] To be published.

4 Limits of surface irregularities

4.1 Chips and ragged edges

4.1.1 General

Chips and ragged edges are defined in IEC 60424-1.

4.1.2 Chips and ragged edges on the mating surfaces

The areas of the chips located on the mating surfaces (chip1 and chip1′ irregularities of Figures 1 and 2) shall not exceed the following limits:

– the cumulative area of the chips shall be less than 6 % of the mating surface (whether gapped or ungapped) of the centre leg;
– the total length of the ragged edges shall be less than 25 % of the perimeter of the relevant surface.

4.1.3 Chips and ragged edges on other surfaces

The allowable areas of chips are doubled as compared to the limits for the mating surface (see Table 1 for ETD-cores, Table 2 for EER-cores, Table 3 for EC-cores and Table 4 for E-cores).

The rule for ragged edges is the same as for the mating surface.

The allowable areas of chips for a given core are summarized in Tables 1, 2, 3 and 4.

The core sizes given in Tables 1 and 2 correspond to the cores defined in IEC 61185, IEC 62317-7, IEC 60647 and IEC 62317-8.

Table 1 – Allowable areas of chips for ETD-cores in mm^2

Core size	Mating surfaces	Other surfaces
ETD19	< 2,5	< 5
ETD24	< 3,5	< 7
ETD29	< 4	< 8
ETD34	< 6	< 12,5
ETD39	< 8	< 15
ETD44	< 10	< 20
ETD49	< 12,5	< 25
ETD54	< 17,5	< 35
ETD59	< 25	< 45

Table 2 – Allowable areas of chips for EER-cores in mm^2

Core size	Mating surfaces	Other surfaces
EER25,5	< 2,5	< 5
EER28	< 4	< 8
EER28L	< 4	< 8
EER35	< 6	< 12,5
EER39	< 7	< 15
EER40	< 8	< 15
EER42	< 10	< 20
EER49	< 12.5	< 25

Table 3 – Allowable areas of chips for EC-cores in mm^2

Core size	Mating surfaces	Other surfaces
EC35	< 4	< 8
EC41	< 6	< 12,5
EC52	< 8	< 15
EC70	< 12,5	< 25
EC90	< 25	< 50
EC120	< 25	< 50

Table 4 – Allowable areas of chips for E-cores in mm²

Core size	Mating surfaces	Other surfaces
E5,3/2	< 0,5	< 0,5
E6,3/2	< 0,5	< 0,5
E8/2	< 0,5	< 1
E8,3/4	< 0,5	< 1
E8,8/2	< 0,5	< 1
E10/3	< 1	< 1,5
E10,2/5	< 1	< 1,5
E13/4	< 1	< 2
E13/6	< 1	< 2
E16/4,8	< 1,5	< 3
E16/5	< 1,5	< 3
E19/5	< 1,5	< 3
E19,3/4,8	< 1,5	< 3
E20/6	< 2	< 4
E25/7	< 4	< 7
E25,4/6	< 2,5	< 5
E25,4/6,3	< 2,5	< 5
E30/11	< 7	< 14
E32/9	< 5	< 10
E33/13	< 7	< 14
E34,6/9	< 6	< 10
E35/10	< 6	< 12,5
E40/11	< 6	< 12,5
E41/13	< 10	< 20
E42/15	< 12,5	< 25
E42/20	< 15	< 30
E47/16	< 15	< 30
E50/15	< 12,5	< 25
E55/21	< 20	< 40
E55/25	< 25	< 50
E60/16	< 15	< 30
E65/27	< 30	< 60

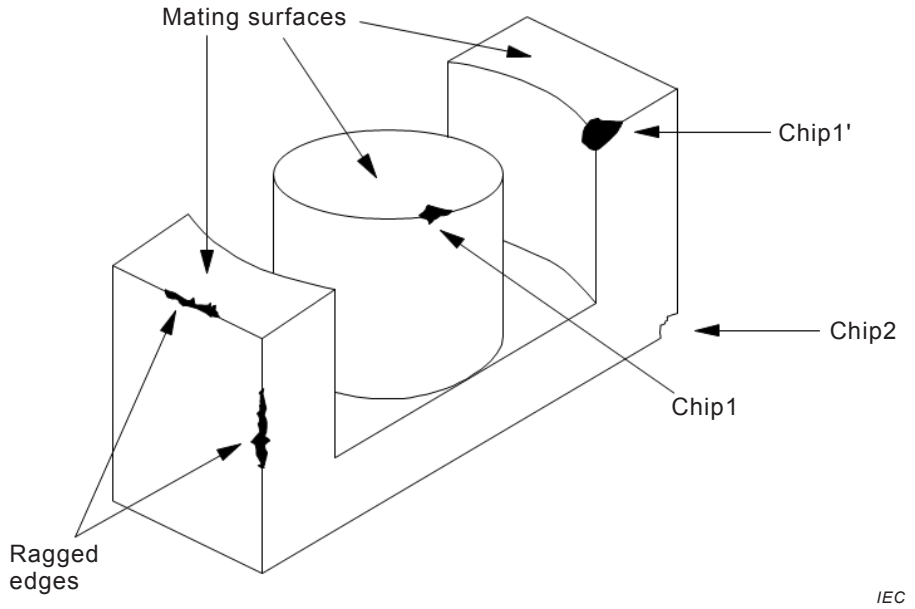


Figure 1 – Chip location for ETD-cores, EER-cores and EC-cores

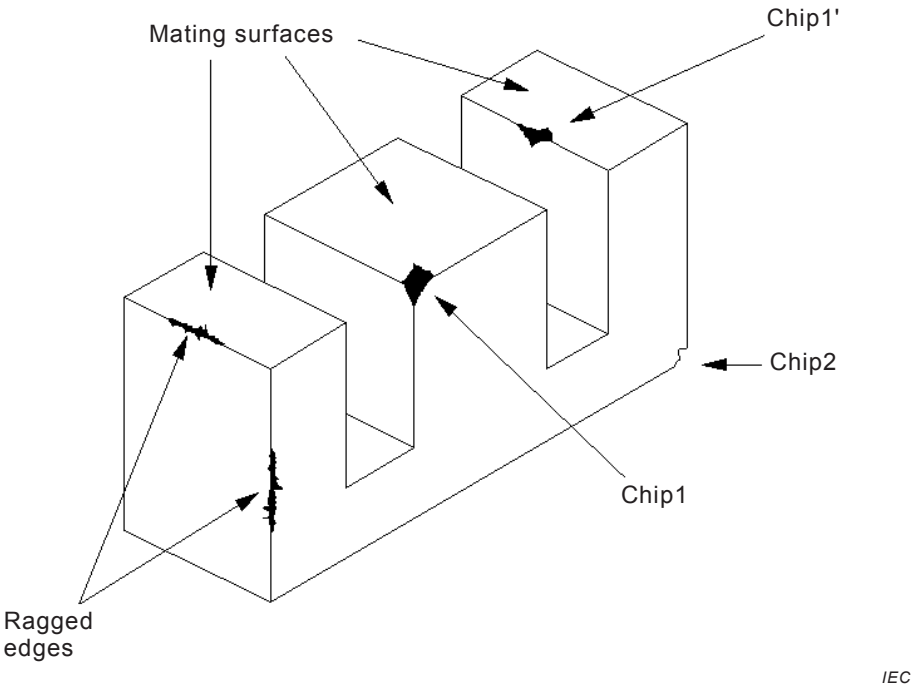
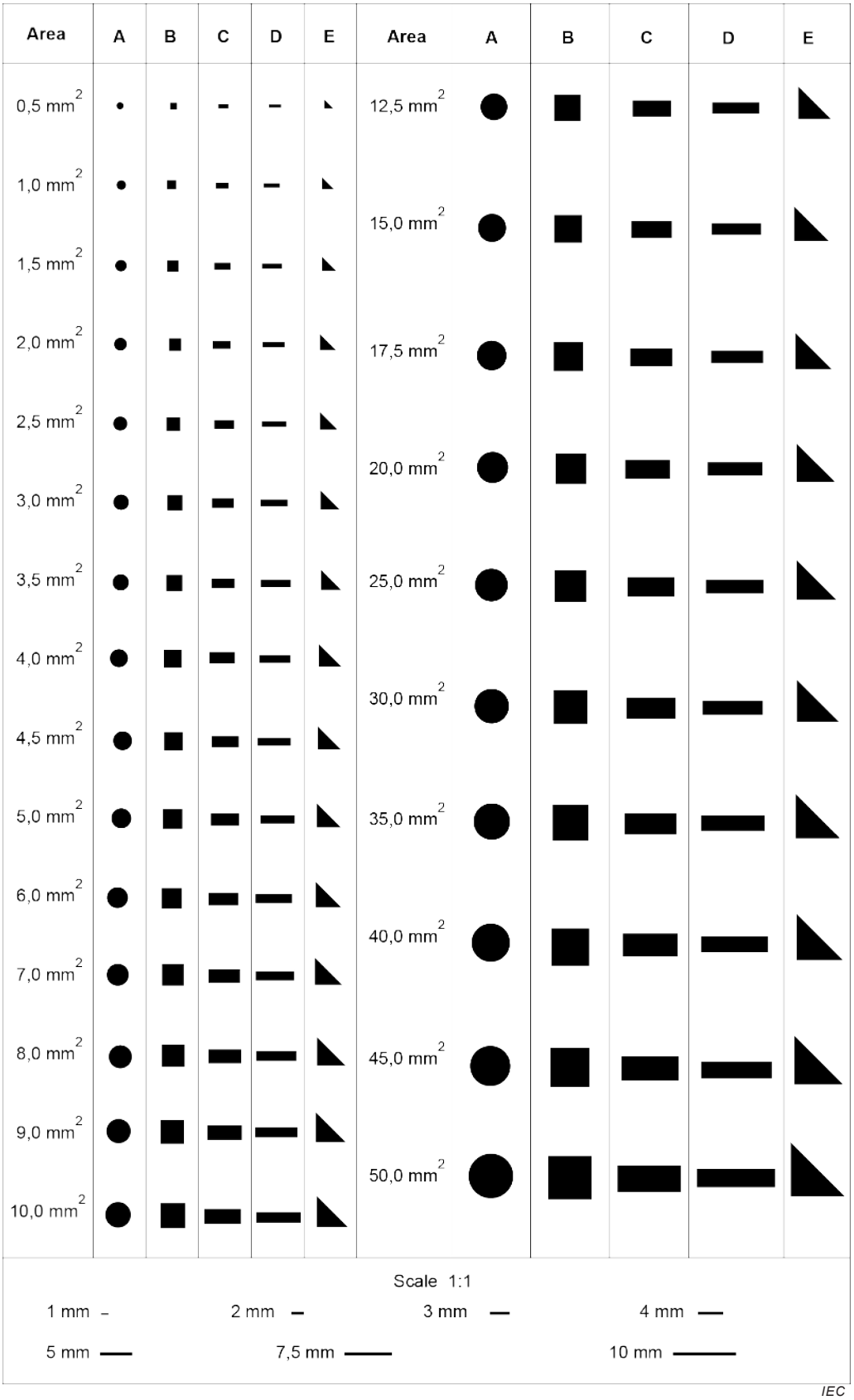


Figure 2 – Chip location for E-cores

The area and length reference for visual inspection is given in Table 5.

Table 5 – Area and length reference for visual inspection



4.2 Cracks

Cracks are defined in IEC 60424-1.

The limits for cracks at various locations shown in Figures 3 or 4 are given in Table 6.

4.3 Flash

Flash is defined in IEC 60424-1.

There shall be no flash extending from the core into the wire-slot.

4.4 Pull-outs

Pull-outs are defined in IEC 60424-1.

For ETD-cores, EER-cores and EC-cores the cumulative area of pull-outs of the core shall be less than 25 % of the total area of bottom surfaces.

For E-cores the cumulative area of pull-outs of the core shall be less than 25 % of the total area of a side surface.

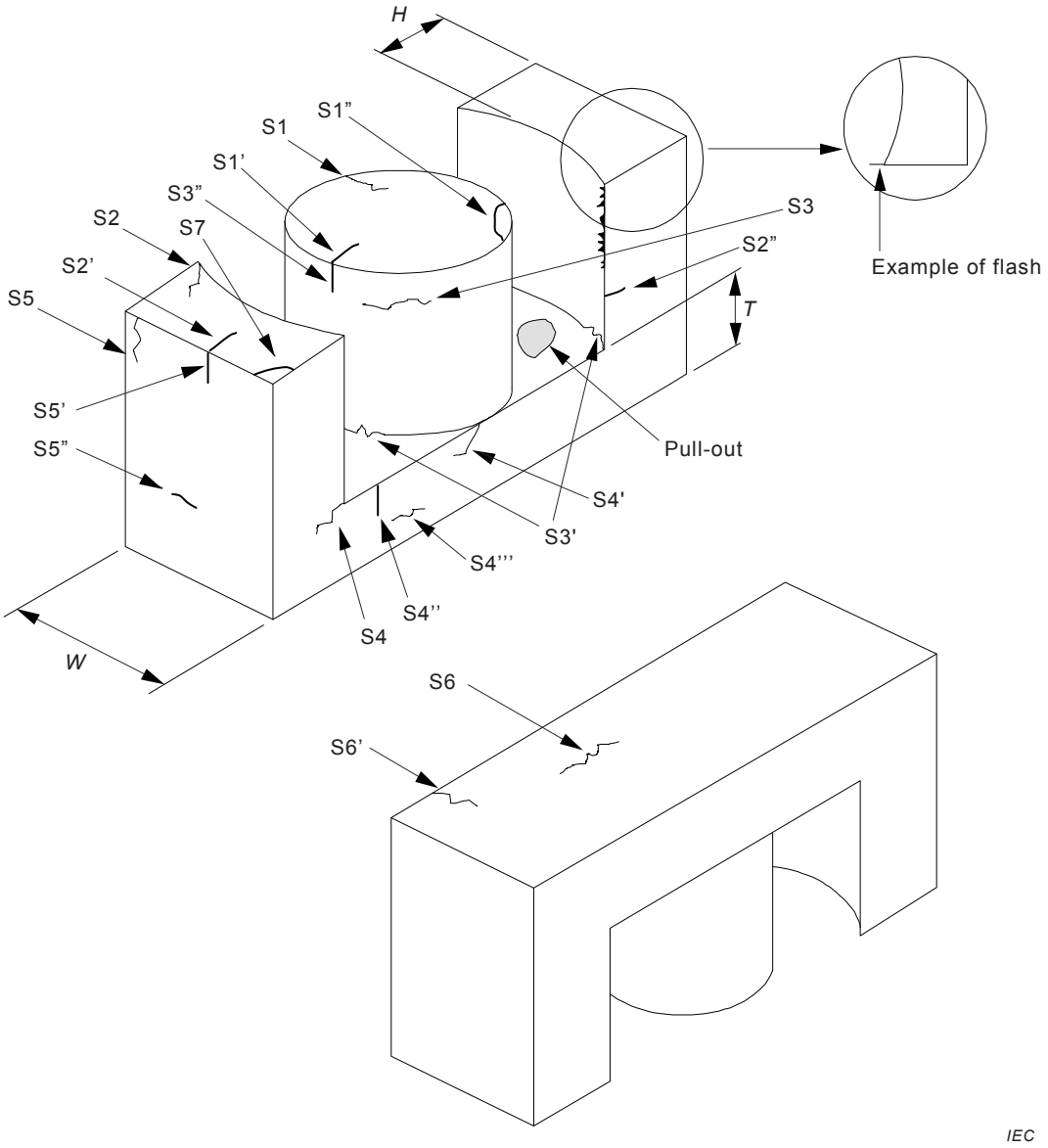


Figure 3 – Cracks and pull-out location for ETD-cores, EER-cores and EC-cores

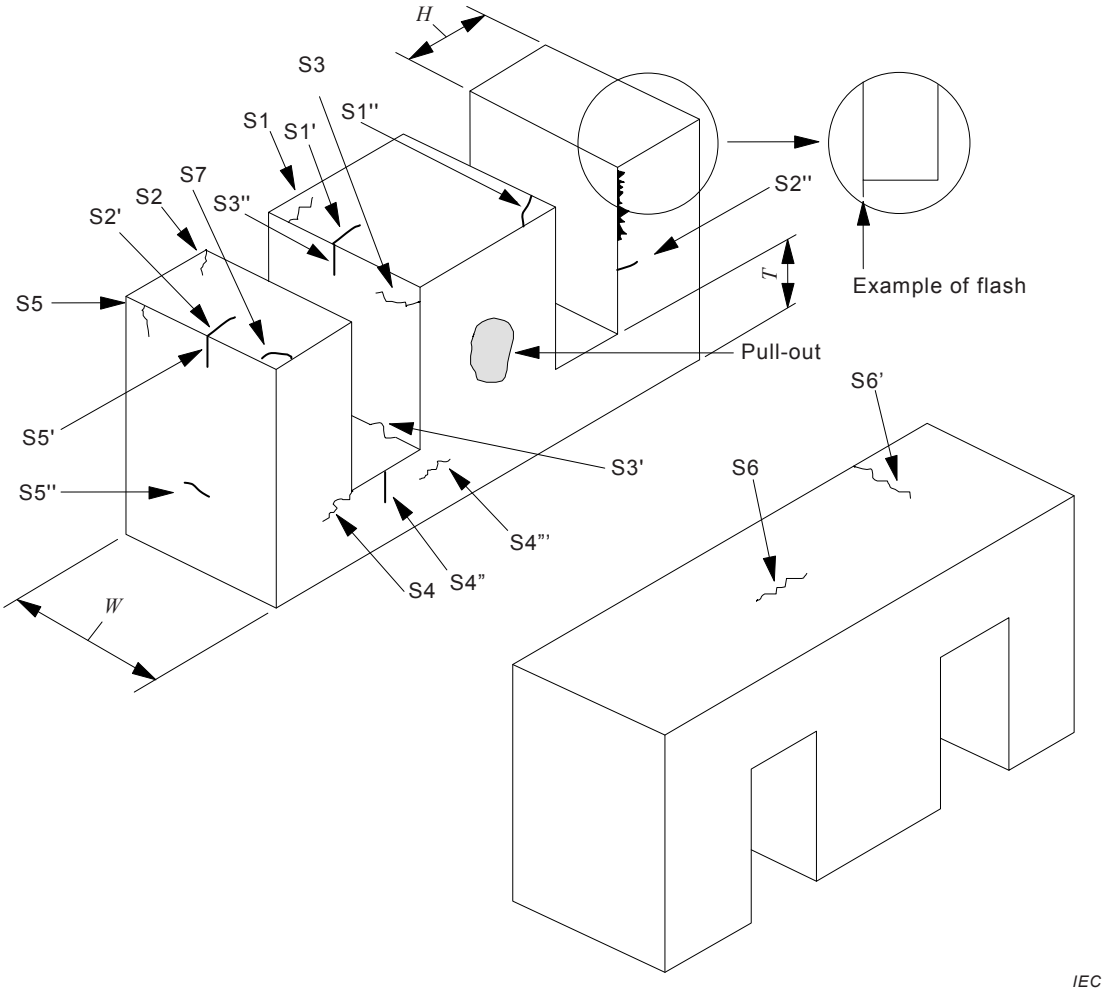


Figure 4 – Cracks and pull-out location for E-cores

Table 6 – Limits for cracks

Type	Location	Limits for single crack	Limits for multiple cracks
S1 and S1'	Mating surface of centre post	< 25 % of dimension W	<50 % of dimension W
S1"	Corner of centre post	Not acceptable	Not acceptable
S2 and S2'	Mating surface of outer leg	< 25 % of dimension H	< 25 % of dimension H
S2"	Side of outer leg	< 25 % of dimension H	< 25 % of dimension H
S3 and S3"	Centre post	< 25 % of dimension W	< 25 % of dimension W
S3'	Bottom corner of centre post/back wall and outer leg/back wall	< 25 % of dimension W	< 25 % of dimension W
S4	Bottom corner of outer leg/back wall	< 25 % of dimension T	< 25 % of dimension T
S4' and S4"	Back wall	< 25 % of dimension T	< 25 % of dimension T
S4"'	Back wall	< 50 % of dimension W	< 100 % of dimension W
S5 and S5' and S5"	Outer leg	< 50 % of dimension W	< 100 % of dimension W
S6	Back surface	< 50 % of dimension W	< 100 % of dimension W
S6'	Back surface	< 25 % of dimension W	< 25 % of dimension W
S7	Corner of outer leg	Not acceptable	Not acceptable

4.5 Crystallites

Crystallites are defined in 3.2.

Figures 5 and 6 show examples of crystallites location on ETD-cores, EER-cores, EC-cores and E-cores.

– A single area of the crystallites located on any surface shall be less than 2 % of the respective surface area.
– The cumulative area of the crystallites located on any surface shall be less than 4 % of the respective surface area.

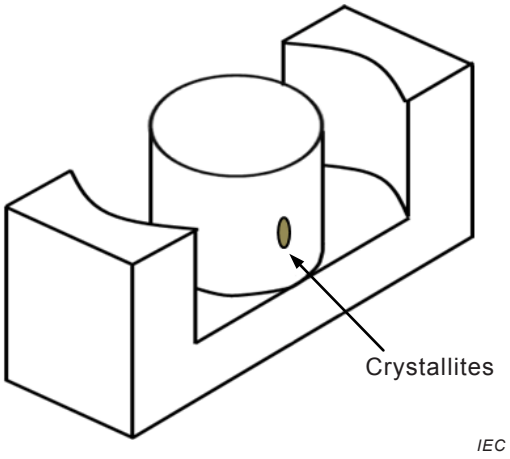


Figure 5 – Crystallites location for ETD-cores, EER-cores and EC-cores

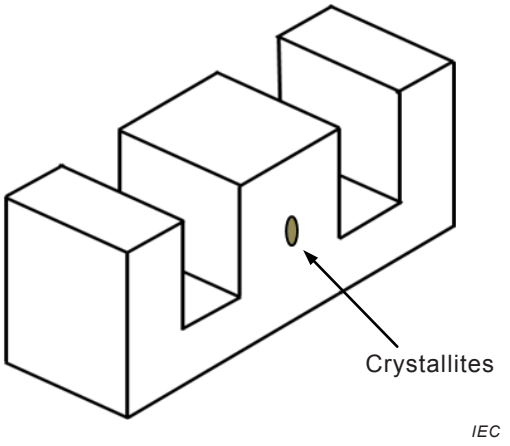


Figure 6 – Crystallites location for E-cores

4.6 Pores

Pores are defined in 3.1.

Figures 7 and 8 show examples of pores location on ETD-cores, EER-cores, EC-cores and E-cores.

– The number of pores located on the same surface shall not exceed 2; the total number of pores located on all surfaces shall not exceed 5.
– A hole with an area larger than 1 mm^2 on any surface is not acceptable.

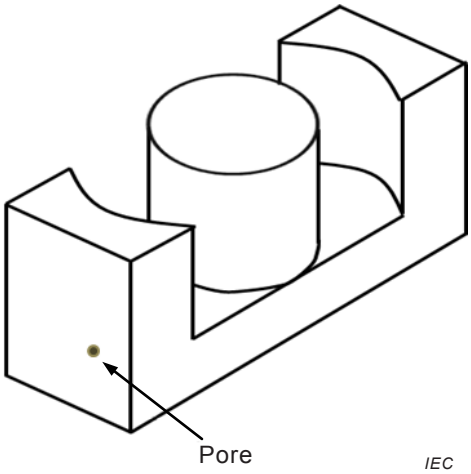


Figure 7 – Pores location for ETD-cores, EER-cores and EC-cores

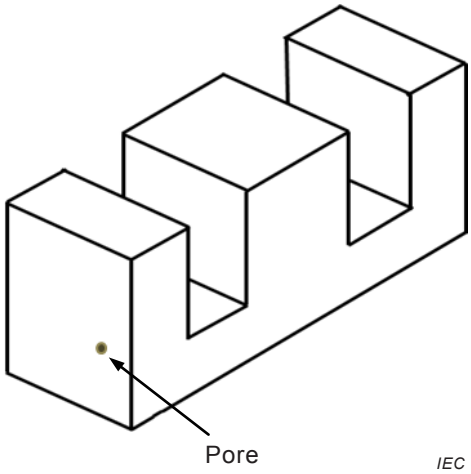


Figure 8 – Pores location for E-cores

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