Designation: F 1771 – 97

Standard Test Method for Evaluating Gate Oxide Integrity by Voltage Ramp Technique[1]

This standard is issued under the fixed designation F 1771; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 The techniques outlined in this standard are for the purpose of standardizing the procedure of measurement, analysis, and reporting of oxide integrity data between interested parties. This test method makes no representation regarding actual device failure rates or acceptance/rejection criteria. While some suggestions for data analysis are included in later sections of this test method, interpretation of results is beyond the scope of this standard. Any such interpretations should be agreed upon between interested parties prior to testing. For example, a variety of failure criteria are included to permit separation of so-called intrinsic and extrinsic oxide failures.

1.2 This test method covers the procedure for gaging the electrical strength of silicon dioxide thin films with thicknesses ranging from approximately 3 nm to 50 nm. In the analysis of films of 4 nm or less, the impact of direct tunneling on the current-voltage characteristics, and hence the specified failure criteria defined in 5.4, must be taken into account. Since oxide integrity strongly depends on wafer defects, contamination, cleanliness, as well as processing, the users of this test method are expected to include wafer manufacturers and device manufacturers.

1.3 This test method is not structure specific, but notes regarding options for different structures may be found in the appendix. The three most likely structures are simple planar metal-oxide semiconductor (MOS-capacitors) (fabricated or mercury probe), various isolation structures (for example, local oxidation of silicon (LOCOS)), and field effect transistors. This test method assumes that a low resistance ohmic contact is made to the backside of each wafer in each case. For a more detailed discussion of the design and evaluation of test structures for this test method, the reader is referred to the EIA/JEDEC Standard 35-1.[2]

1.4 Failure criteria specified in this test method include both the fixed current limit (soft) and destructive (hard) types. In the past, use of a fixed current limit of 1 μA or more virtually ensured measurement of hard failure, as the thicker, more heavily contaminated oxides of those days typically failed catastrophically as soon as measurable currents were passed. The cleaner processing of thinner oxides now means that oxides will sustain relatively large currents with little or no evidence of failure. While use of fixed current limit testing may still be of value for assessing uniformity issues, it is widely felt that failure to continue oxide breakdown testing to the point of catastrophic oxide failure may mask the presence of defect tails, which are of critical importance in assessing long-term oxide reliability. For this reason, this test method makes provision for use of fixed limit failure criteria if desired and agreed upon by the parties to the testing, but specifies that testing be continued until hard failure is sensed.

1.5 This test method specifically does not include measurement of a charge-to-breakdown (Q_{bd}) parameter. Industry experience with this parameter measured in a ramp-to-failure test such as this indicates that Q_{bd} values so obtained may be unreliable indicators of oxide quality. This is because a large fraction of the value determined is collected in the last steps of the test, and the result is subject to large deviations. Q_{bd} should be measured in a constant current or bounded current ramp test.

1.6 This test method is applicable to both *n*-type and *p*-type wafers, polished or having an epitaxial layer. In wafers with epitaxial layers, the conductivity type of the layer should be the same as that of the bulk wafer. While not excluding depletion polarity, it is preferred that measurement polarity should be in accumulation to void the complication of a voltage drop across the depletion layer.

1.7 While this test method is primarily intended for use in characterizing the SiO_2-silicon systems as stated above, it may be applied in general terms to the measurement of other metal-insulator-semiconductor structures if appropriate consideration of the characteristics of the other materials is made.

1.8 Measurement conditions specified in this test method are conservative, intended for thorough analysis of high quality oxide-silicon systems, and to provide a regime in which new users may safely begin testing without encountering undue experimental artifacts. It is recognized that some experienced users may be working in applications where less precise data is required and a more rapid test is desirable. An example of this situation is the evaluation of silicon wafer quality, where a staircase voltage step providing 0.5 MV/cm oxide field strength resolution and a voltage step duration of 0.2 s has been used. Such test conditions may be specified when agreed upon

[1] This test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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[2] Available from Electronic Industries Assoc., Washington, DC.

as adequate by all participants to the testing. Because the dependence of measured parameters upon test conditions may increase as these conditions depart from those specified in this test method, it is important that all parties to these tests use the same set of test conditions, so that their results will be comparable.

1.9 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *EIA/JEDEC Standards:*

Standard 35, Procedure for the Wafer-Level Testing of Thin Dielectrics[2]

Standard 35-1, General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics[2]

Standard 35-2, Test Criteria for the Wafer-Level Testing of Thin Dielectrics[2]

3. Terminology

3.1 *Definitions:*

3.1.1 *hard failure*—destructive failure of an MOS capacitor associated with rupture of the oxide film.

3.1.1.1 *Discussion*—This is sensed by an abrupt, irreversible change in the current-voltage characteristics of the capacitor. In this test method, hard failure is determined by a relatively large change in dc conduction level between voltage steps, or as a change in the logarithmic slope of the current density-voltage characteristic. Hard failure conditions for this test method are defined in 5.4.

3.1.2 *soft failure*—failure of an MOS capacitor sensed by its passage of an electrical current equal to or greater than a predetermined value.

3.1.2.1 *Discussion*—This type of failure may be either destructive or nondestructive, as in the case of Fowler-Nordheim or direct tunneling currents.

3.1.3 *failure modes A, B, and C*—in the reporting of hard and soft breakdown failure results, data is sometimes summarized in terms of ranges of oxide field strength in which the breakdown occurred. One set of categories widely used[3,4] is as follows:

A mode failure: V_{bd}=> E_{ox}< 1 MV/cm
B mode failure: V_{bd}=> E_{ox}< 1 MV/cm, <=8 mV/cm
C mode failure: V_{bd}=> E_{ox}< 8 MV/cm.

3.1.3.1 *Discussion*—These categories have traditionally been used for oxides thicker than about 20 nm. For thinner films, care must be taken in their use and in proper derivation of the oxide field strengths as described in 10.2.

4. Summary of Test Method

4.1 *Overview*—This is a voltage ramp test. It is most useful in determining changes in a given process. It is intended to be applied to arrays of similar capacitors on a silicon wafer or group of wafers representing a process condition specified by the user. Following an optional pretest of capacitor leakage, the voltage applied to the capacitor under test is increased linearly with time at a specified rate, with measurements of current made at intervals that must correspond to oxide electric field changes less than a maximum specified value. The voltage ramp continues until hard failure (destructive breakdown), as defined by one of several specified failure criteria, is sensed. During the measurement cycle, soft failures corresponding to predetermined current levels are sensed and stored. At the end of the measurement of this unit, hard and soft failure conditions are stored for that unit, along with the appropriate hard failure criterion. After hard failure is detected or when the upper voltage limit of the test is reached, a post-test is performed to evaluate hard failure by sensing current at a low voltage. The test cycle is then repeated for the next capacitor in the array, and this is continued until all units in the specified group have been tested. When testing is complete, calculations and categorizing of data is done as described in Sections 10, 11, and a report of the results is generated.

4.2 *Voltage Ramp*—While this test can, and might best be done using a true linear voltage ramp, constraints of the automated test equipment most often used in its performance lead to widespread use of a staircase of voltage steps to simulate the ramp. The ramp rate is specified in terms of the rate of increase of the oxide electric field, 1.0 ± 0.1 mV/cm/s. Other ramp rates may be used if it can be shown that it does not affect the results, or if it is agreed upon by all parties to the test. For oxides thicker than about 20 nm, the oxide electric field has been commonly estimated by dividing the applied voltage by the oxide thickness, but for thinner films, significant errors may be introduced by ignoring the effects of non-zero flat band voltage of the MOS capacitor and voltages developed across the silicon substrate (and the gate electrode as well, if it is polysilicon) due to band bending and series resistance. One approach to estimation of the relationship between sample parameters and oxide field strength is found in 10.2.

4.3 *Current Sampling*—In order to provide adequate breakdown field strength resolution, it is specified that current readings be taken after a maximum electric field change of 0.1 MV/cm. Taken together with the specified voltage ramp rate, this leads to a maximum time between current readings of 100 ms. In the case in which the test is done using a voltage staircase, this implies use of a 100-ms voltage step duration, with one current reading taken at each step.

4.4 *Failure Criteria*—As previously mentioned, both "hard" and "soft" failure criteria are provided for in this test methods (see Section 3 on Terminology). Techniques for detection of hard oxide failure for thin dielectrics may require high resolution, low noise current-voltage data. For this reason, hard failure criteria are defined in two measurement regimes, one below and one above a threshold current level where noise is reduced. This current level is commonly in the range 1 nA to 0.1 μA for most test systems. Hard failure criteria below the noise threshold level are defined as follows:

4.4.1 *Current greater than or equal to 0.98 times the*

[3] Yamabe, K., Ozawa, Y., Nadahara, S., and Imai, K., "Thermally Grown Silicon Dioxide with High Reliability," in"Semiconductor Silicon 1990", Proceedings of the 1990 Spring Meeting of The Electrochemical Society, p. 349.

[4] Yamabe, K., Taniguchi, K., and Matsushita, Y., "Thickness Dependence of Dielectric Breakdown Failure of Thermal SiO_2 Films," *Reliability Physics—21st Annual Proceedings*, 1983, p. 184.

compliance limit of the current score: This condition signals total collapse of the capacitor.

4.4.2 *Current change by a factor of 1000 in a single voltage step:* Units with gross defects failing at low voltages where currents are below the noise threshold commonly fail with very large increases in current.

4.4.3 *Consecutive current increases by a factor of 10 in each of two voltage steps:* Test capacitors that are initially highly conductive, as from a pinhole, often do not display destructive breakdown, but rather show steeply rising diodic leakage currents. This failure criterion is designed to identify these defective units at low voltage. Above the noise threshold current level, the two criteria above remain in force, and two others are added, as follows:

4.4.4 *Current change by a factor of 10 in a single step:* In the Fowler-Nordheim regime, current changes are much less than this value for the small increment in oxide field associated with a single voltage step.

4.4.5 *Change in the logarithmic slope of the J-V curve by a factor of 3:* This criterion becomes of increasingly great value for oxide films thinner than 10 nm, where destructive breakdown is often accompanied by very small changes in current, because of the very low resistance of these oxides at very high fields (see EIA/JEDEC 35-2). Calculation of this parameter is described in 10.4. Another parameter associated with hard failure is specified as follows:

4.4.6 *Hard failure current density:* This parameter is defined as the value of the current at the last measurement point prior to detection of hard failure, divided by the area of the capacitor.

4.4.6.1 As defined in Section 3, "soft" failures are associated with the passage of a predetermined current through the capacitor under test. This type of criterion has been traditionally used, since in the past, passage of any measurable current through an oxide was normally associated with hard failure. More recently, where oxides have commonly been capable of sustaining Fowler-Nordheim tunneling conduction, use of such a criterion yields results indicative of the uniformity of the samples being tested. As such, soft failure criteria may be agreed upon between users of this test method in order to meet individual needs of the testing. For examples of commonly used criteria see 4.4.7, 4.4.8 and 4.4.9.

4.4.7 *Vcrit:* The voltage associated with the noise threshold current level.

4.4.8 *Vsoft fail = V at J = 100 mA/cm^2:* For many oxides, this current level is close to hard failure, but avoids the dispersion associated with high resistance voltage drops at high breakdown currents.

4.4.9 *Vsoft fail = V at I = 1.5 μA:* This criterion is widely used in Japan.[3] Other values of current or current density may be used as soft failure criteria by agreement of the parties to the test.

5. Significance and Use

5.1 The technique outlined in this test method is meant to standardize the procedure, analysis and reporting of oxide integrity data via the voltage ramp technique among interested parties. However, since the values obtained cannot be entirely divorced from the process of fabricating the test structure, suitable correlations should be performed based on process needs and structure selection. This correlation should include sample size as well as device geometry.

5.2 Measurement of the electrical integrity of oxides grown on silicon wafers may also be used in-house as a means of monitoring the quality of furnaces and other processing steps as well as judging the impact of changing some processing steps.

5.3 Selection of various edge and area intensive structures is crucial for isolating the nature of the defects. Techniques for using such structures to isolate the nature of detected defects is beyond the scope of this test method.

5.4 The actual results will be somewhat dependent on the choice of gate electrode. Polysilicon gates have the advantage of being identical to finished product in many instances. Even for polysilicon gates, exact results will depend upon values chosen for polysilicon thickness, doping, and sheet resistance.

6. Interferences

6.1 Since this is a dc measurement, care must be taken to make sure that the wafer has a low resistance ohmic return contact. This is preferably done with a metallized contact to the back side of the wafer under test. In cases where testing must be done on capacitors in diffused wells of conductivity type opposite to the substrate, top side contacts carefully designed to provide uniform, low resistance to all parts of the test capacitor should be used. A discussion of these design criteria is given in Standard 35-1.[2]

6.2 It is strongly suggested that testing be done with a voltage polarity that will accumulate the silicon surface underlying the oxide; positive voltages for *n*-type substrates and negative voltages for *p*-type substrates. If this is not done, a topside contact to a diffused region of opposite conductivity type surrounding the capacitor (a gated diode or transistor) should be used to minimize the problem of uncontrolled voltage drops across the inversion layer during testing. This is an absolute requirement for testing *p*-type substrate capacitors under positive bias, where sufficient electrons to support conduction and breakdown will not be available without the *n*-type region.

6.3 Evaluation and control of electrical noise in the current-voltage data taken as part of this test method is crucial to the proper identification of the failure criteria, particularly the ln *J-V* slope change criterion defined in 9.9.4. Approaches for minimizing electrical noise in the measurements are suggested in Section 7 on Apparatus, and an approach for noise evaluation is given in 10.3.

6.4 Control of the voltage step time may be difficult when using automated electrometers in a voltage staircase regime. While the required 100-ms step time may be set using a delay in the measurement loop, an additional, uncontrolled delay may be incurred due to autoranging of the electrometer. The effect is most pronounced for very low currents, where the measured value is several orders of magnitude below the minimum range set by the electrometer software. An example of this effect is discussed in 10.3.

6.5 The method of probing the device may affect the results. Examples of possible variables are probe pressure and use of a contact pad versus direct contact to the gate.

6.6 Use of gate electrode material other than polysilicon may mask differences in materials and make the material look worse than it might otherwise appear if polysilicon gates are used. This is because the process of forming a gate electrode on an oxide sample may affect the integrity of that oxide either for better or for worse. Sputtering or radiation damage accompanying metal gate deposition may degrade oxide integrity, while the high temperature annealing and gettering associated with polysilicon deposition and doping may improve oxide quality. On the other hand, stress arising from crystal formation in the polysilicon, or impurity diffusion along polysilicon grain boundaries may degrade oxide integrity. Changes of gate-substrate work function difference may also affect the breakdown and wearout mechanisms in the oxide. Therefore, potential effects of gate electrode material choice on test results must not be neglected.

6.7 The actual values obtained will depend somewhat on the processing involved in fabricating the test structure. Care must be taken to ensure a consistent processing.

6.8 Wafer temperature during testing should be clearly defined. While oxide breakdown voltages are not strongly temperature-dependent, the oxide wearout mechanism is temperature-sensitive, and large temperature variations might have an impact on results.

6.9 **Precaution:** Since the voltage and currents involved are potentially dangerous, appropriate means of preventing the operator from coming into contact with the probe tip or other charged surfaces should be in place before testing.

6.10 When testing very thin oxides, those 10 nm or less in thickness, special care must be taken to account for effects arising from the very high specific capacitance of these films. These may include voltage drops across the polysilicon gate electrode and the silicon substrate, and high conduction due to direct tunneling.

6.11 When using a mercury probe for measurements of this type, care must be taken in the preparation and control of the oxide surface. Adsorbed organic contaminant films may affect the electric field distribution in the oxide. Such films may sometimes be removed with hot SC-1 cleaning solution; a mixture of NH_4OH-H_2O_2-H_2O. Use of a dry nitrogen purge of the probing ambient is also recommended to minimize surface contamination effects.

7. Apparatus

NOTE 1—The test methodology is independent of equipment configuration. However, the use of computer controlled probing equipment is essential as the measurement speed precludes manual data gathering. What is included here should be considered a minimum.

7.1 *Voltage Source and Sink* should be used that is capable of delivering/receiving between 0 and± 100 V in the form of an effective ramp rate of 1.0 ± 0.1 $MV/cm^{-1}/s^{-1}$ either automatically or under computer control. If use of other ramp rates is mutually agreed upon as mentioned in 5.2, it must be established that hardware is available to perform the measurement adequately. This voltage source/sink may consist of two source-measurement units (SMU's) with a common ground, or just a single SMU with a dedicated sink. The voltage source should be capable of sourcing at least 100 mA of current.

7.2 *Shielded Triaxial Cables*, involving guarding will minimize the noise when measuring low current values.

7.3 *Wafer Chuck*, electrically isolated from its case/probe platen. While the chuck may be connected to the reference voltage (zero, not ground), lower electrical noise may be obtained by connecting the voltage ramp source to the chuck and measuring the current through the probe connection.

7.4 *Hard Needle-Type Probe*, (such as tungsten carbide) is needed to contact the gate electrode. This may be a single probe or a probe card.

NOTE 2—This only applies to fabricated gates; such probes are not used when using a mercury probe contact to the oxide.

8. Sampling

8.1 Sampling is the responsibility of the user of this test method. However, if testing is done as part of a comparison or correlation, sampling should be agreed upon in advance by all participants.

NOTE 3—Refer to the appendix of JEDEC Standard No. 35[2] for a good discussion of sampling plan statistics.

9. Procedure

9.1 Before the measurement, record the following information for each sample: sample identity, date, time, operator, instrument station identity (if any), average oxide thickness, gate area in square centimetres, gate material, oxide type (example thermal versus deposited), structure type, conductivity type (*n* or *p*), bias mode (accumulation or depletion), test temperature.

9.2 Establish the test parameters relevant to the test system and the sample. These include the voltage ramp rate, computed as shown in 10.2, the noise threshold level, and in some instances the ln *J-V* slope ratio for the hard failure criterion in 9.9.5. Determination of these latter two parameters is illustrated in 10.3.

9.3 Set the applied voltage to zero volts.

9.4 Recognizing that some information on extrinsic defects may be lost, perform a pretest as follows. If it is desired not to lose the information on extrinsic defects, proceed to 9.5.

9.4.1 Bias the gate into accumulation at the voltage of use. If the measured current exceeds a value equivalent to 1.0×10^{-5} A/cm^2 (or a current value of 10 nA if the device area is at or below 10^{-3} cm^2), record this device as a Category 0 failure and proceed to 9.11.

9.5 From the starting bias condition (zero if no pretest was done, or the voltage of use if a pretest was used) record voltage and current.

9.6 Begin increasing the voltage bias at a rate equivalent to an electric field increment of 1.0 ± 0.1 $MV\text{-}cm^{-1}\text{-}s^{-1}$.

9.7 Record current-voltage data at an interval no more than 0.1 s between readings, or at least once near the end of each voltage step.

9.8 After each current reading, test to see if any of the soft failure criteria have been met. If so, store the appropriate value.

9.9 After each current reading, check to see if one of the hard failure criteria (as defined in 5.4) has been reached.

9.9.1 Check to see if the current has increased to a value greater than or equal to 0.98 times the compliance limit of the voltage ramp source. If so, record the previous voltage level as the hard failure voltage, and set the failure category to 1.

Divide the current level at the previous measurement point by the capacitor area, and record this value as the hard failure current density for this unit.

9.9.2 Check to see if the current has increased by a factor of 1000 or more from the previous reading. If so, record the previous voltage level as the hard failure voltage, and set the failure category to 2. Divide the current value measured at the previous point by the capacitor area, and record this value as the hard failure current density.

9.9.3 Check to see if the current has increased by a factor of 10 or more in two consecutive voltage steps. If so, record the previous voltage level as the hard failure voltage, and set the failure category to 3. Divide the current value measured at the previous point by the capacitor area, and record this value as the hard failure current density.

9.9.4 If the current is above the noise threshold level, check for an abrupt increase in the current by a factor of ten. If this has occurred, record the previous voltage level as the hard failure voltage, and set the failure category to 4. Divide the current value measured at the previous point by the capacitor area, and record this value as the hard failure current density.

9.9.5 If the current is above the noise threshold level, check for an abrupt change in the logarithmic slope of the current density-voltage characteristic of the unit. To minimize the chance of detecting a false reading, use the average of the previous five (V,I) data pairs to compute the established slope, and the current and previous (V,I) data pairs to compute the new slope. A change by a factor of three (3) shall constitute a failure. If this has occurred, record the previous voltage level as the hard failure voltage, and set the failure category to 5. Divide the current value measured at the previous point by the capacitor area, and record this value as the hard failure current density.

9.10 After hard failure has been detected by one of the criteria in 9.9 or the upper test voltage limit has been reached, perform a post-test using the same criteria defined for the pretest in 9.4.1. This is to be done whether a pretest was elected in 9.4 or not. If the unit fails the post-test conditions, modify the failure category in some way to reflect this observation. For example, one may change the sign of the failure category number, or add an asterisk.

9.11 Proceed to the next device to be tested, and repeat 9.3-9.10 until all devices are tested.

9.12 A flow diagram outlining the procedure for this test method is given in Fig. 1.

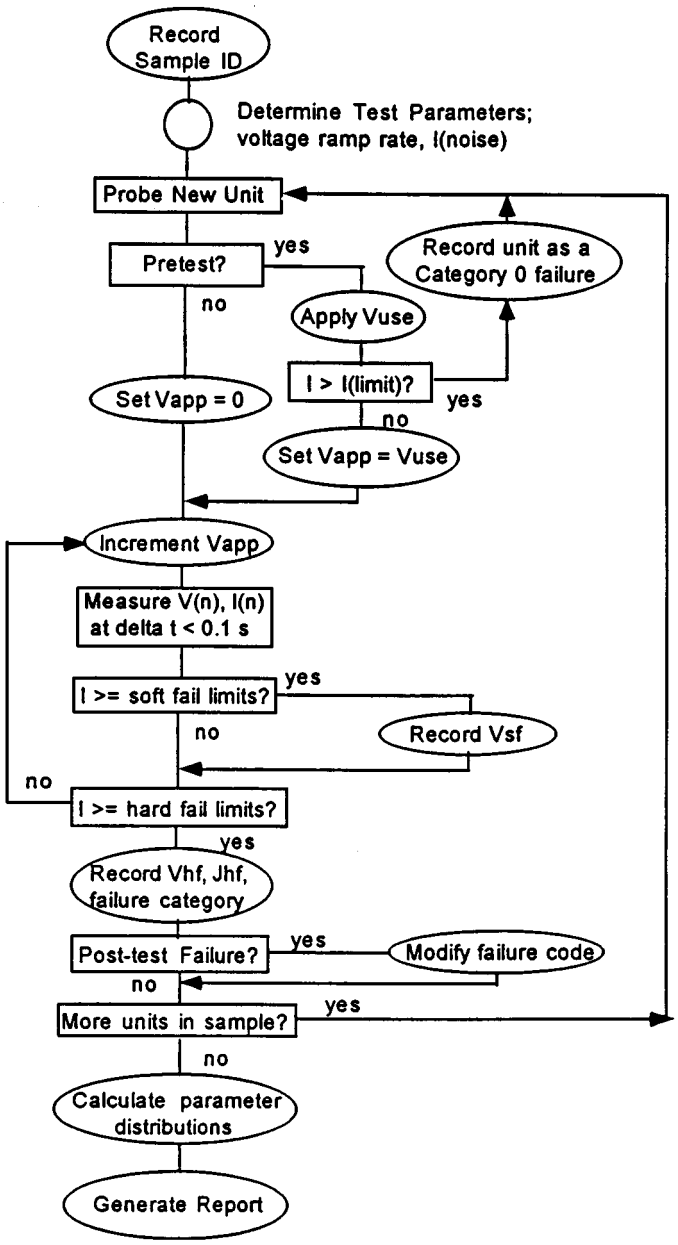

FIG. 1 Flow Diagram for Ramp Voltage Test Method

10. Calculation

10.1 *Current and Current Density:* To calculate current (I) from a current density (J), multiply the current density by the area of gate contact (A) as follows:

$$\text{Symbolically: } I = J \times A \tag{1}$$

Example: Given a current density (J) of 1 μA/cm^2 and a gate area (A) of 0.08 cm^2, the current would be 80 nA.
Similarly, compute current density (J, [A/cm^2]) from measured current (I, [A]) and area (A, [cm^2]) using

$$J = I/A\ [A/cm^2] \tag{2}$$

10.2 *Oxide Voltage and Electric Field Strength as a Function of Applied Voltage:* Since ramp voltage test increments and ramp rates as well as some breakdown voltage data analyses are specified in terms of oxide electric field strength, it is important to consider the conversion of applied voltages to oxide voltage and electric field values for these two cases. Historically, oxide electric field strength has been approximated simply by dividing the applied voltage by the thickness of the oxide. This approximation is in error because it neglects the offset in the zero values of applied and oxide voltage brought about by the work function difference between gate electrode and silicon substrate, and the voltages dropped across the substrate (and the gate electrode, if it is non-metallic) when the capacitor is strongly biased during breakdown testing. These voltage drops are made up of two components; one associated with band bending at the interfaces with the oxide that establishes the high fields required for testing, and another

involving additional voltage drops due to series resistances that become significant at very high currents. These corrections, which together normally range up to 1 to 2 V in magnitude, might reasonably be neglected for samples with oxides greater than 20-nm thick, as the correction amounted to only a few percent of the breakdown voltage values. For thinner oxides, these additional voltage components must be taken into account.

10.2.1 The voltage V_{app} applied across an MOS capacitor with a given gate-substrate work function difference Φ_{ms} and oxide fixed charge Q_r may be expressed as follows:

$$V_{app} = (V_{ox} - (Q_f/C_{ox} + \Phi_{ms})) + V_{sub} + V_{gate} \quad (3)$$

where:

V_{ox} = voltage across the oxide,
C_{ox} = oxide capacitance, F/cm^2,
V_{sub} = voltage across the substrate, V,
V_{gate} = voltage across the gate electrode (arising from polysilicon depletion or series resistance, V.

10.2.2 At zero volts applied, the offset due to the work function difference and oxide charge appears predominantly across the oxide. For setting a voltage ramp rate, the incremental change in V_{ox} with changing V_{app} is not affected by this offset, but may be decreased by voltage increases across the silicon substrate or the gate electrode due to band bending and series resistance drops. For a sample in which the applied bias voltage polarity accumulates the substrate, and the gate electrode is metallic or of the opposite conductivity type from the substrate (for example, *p*-type silicon substrate and *n*+ polysilicon gate), these effects are appreciable only for very small and very large applied voltages. At low bias, silicon bands will bend until the surface becomes degenerate, after which the rate of band bending becomes very low. At high biases, significant resistive voltage drops may develop if the test structure design is not optimized. Over the largest portion of the test in which neither of these effects are large, ramp rates may be computed assuming that voltage increments applied to the device under test appear completely across the oxide, and ΔE_{ox}, the electric field increment across the oxide, is given as follows:

$$\Delta E_{ox} = \Delta V_{app}/W_{ox} \quad (4)$$

where:

W_{ox} = oxide thickness, cm.

10.2.3 For computations of oxide field strength associated with the various hard and soft failure criteria, all corrections indicated in Eq 3 must be taken into account.

10.3 *Determination of Noise Threshold Current Level and ln J-V Slope Ratio Specification:* Useable values of noise threshold current level and ln *J-V* slope ratio depend upon properties of the test system as well as the samples to be evaluated, and a preliminary test may be required in order to specify them properly. To do this, it is necessary to store all the current-voltage data pairs as well as the incremental voltage step time readings in data arrays. This is not required for performance of the bulk of the testing, but is sometimes useful for more thorough analysis of the test results. When such data is stored, it is possible to construct a figure like that shown in Fig. 2, which is a semi-logarithmic plot of sample current, step time, and slope ratio versus applied voltage. Data given here

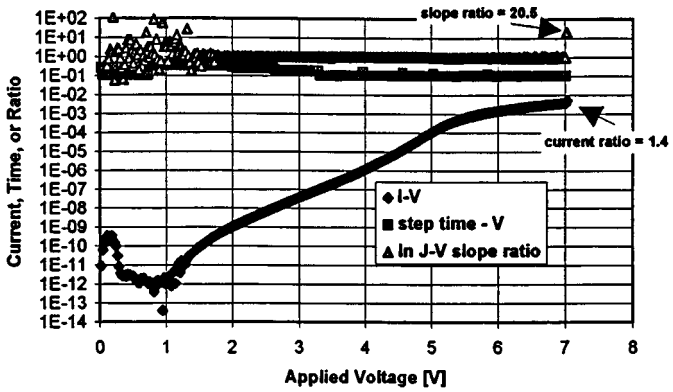

FIG. 2 Determination of Noise Threshold Current Level, Slope Ratio Applicability, and Voltage Step Time Variations

was taken on a 3-nm oxide on a *p*-type silicon substrate, so the current and voltage values are magnitudes of negative readings. Both direct and Fowler-Nordheim tunneling components are seen in the I-V data.

10.3.1 To determine the noise threshold current level, examine the ln *J-V* slope ratio, shown as open triangles in Fig. 2. It is seen to be quite noisy for this test system and sample up to a current level just below 1 nA. This value, 1 nA, is thus a good choice for noise threshold current level for this test. Further analysis of the slope ratio data shows that its maximum value in the range from 1 nA up to catastrophic failure is 1.21, so the standard specified ratio value of three (3) will be adequate to avoid significant noise interference.

10.3.2 The step time-voltage dependence plotted as light squares in Fig. 2 illustrates shortcomings in the step time control for this configuration of the measurement system. A voltage step time of 0.1 s is specified for this test method in 5.3 and 9.7. Because of the high, time-dependent currents measured below 0.5 V, there is a regime below 1 V where this is observed, but most readings from there up to a current value of 0.1 μA fall in the range 0.2 to 0.4 s. Also, for higher current values, there are singular points at electrometer range changes where 0.2-s delays are encountered. It has been shown (Klema[5]) that deviations of this amount will not have large effects on breakdown voltage distributions, but these extended delays will affect total measurement time, and it would be worthwhile to eliminate them if possible. Approaches will depend upon measurement hardware being used, but trading off low current resolution for electrometer autoranging time and look-ahead range changing code are possibilities.

10.4 *ln J-V Slope Hard Failure Criterion:* Hard breakdown failure of oxides is increasingly difficult to detect as oxide thickness decreases below 10 nm. Fowler-Nordheim emission, the dominant current transport mechanism for SiO_2 films in this thickness range, predicts that at a given field strength, the logarithmic slope of the *J-V* characteristic will increase for decreasing film thickness, but will decrease with increasing field strength for a given oxide thickness. Thus, a change in ln *J-V* slope may be a more sensitive detector of failure for these

[5] Klema, J., "Ramp Rate Effect on Dielectric Breakdown," *International Reliability Workshop Final Report*, 1989, p. 87.

very thin films, where high failure current density, low oxide impedance at failure, and high voltage drops in series resistances might lead to very small current changes when the oxide ruptures.

10.4.1 Experience with this failure criterion for oxide thicknesses ranging down to 3 nm indicates that a change by a factor of 3 provides good detection of failure while remaining above the noise level in the data. Users may verify this condition for their particular sample and test conditions, and change the failure factor accordingly. Any such change must be agreed upon by the parties to the test, and clearly identified in the report of the data.

10.4.2 In order to minimize noise in the calculated values and optimize the sensitivity of the failure detection, it has been found advisable to use a set of five data points to calculate the established and new values of the ln *J-V* slope. This illustrated in Fig. 3, which shows the last few data points in the ramp voltage test of a 50-nm oxide. Data points are spaced at 0.1 MV/cm increments, as dictated by this test method.

10.4.3 In particular, the last five data points are labeled (V (n), I (n)) through (V (n – 5), I (n – 5) respectively. The established logarithmic slope is as follows:

$$\text{abs}((\ln(\text{abs}(I(n-1)/I(n-5)))/(V(n-1)-V(n-5))), \quad (5)$$

while the new slope is computed from the last two points,

$$\text{abs}((\ln(\text{abs}(I(n)/I(n-1)))/(V(n)-V(n-1))), \quad (6)$$

10.4.4 Testing for the failure criterion is done by taking the ratio of Eq 6 to Eq 5. As can be seen from Fig. 3, this failure would be identified by failure criteria 9.9.2 and 9.9.3, as well as the slope criterion 9.9.5.

10.5 *Defect Density:* To calculate a defect density, a minimum criterion must be chosen by either the user or negotiated with the user's customer. This criterion can take the form of a minimum breakdown voltage or electric field strength, or a discontinuity in the breakdown voltage distribution of the sample. Given the fraction of devices reaching this criterion, the defect density calculation may be based on a Poisson relationship (see Standard 35) using the following equation:

$$Y = \exp(-AD), \quad (7)$$

where:

Y = yield of good units in terms of the defined failure criterion,
A = area of sample, cm^2, and
D = defect density, defects/cm^2.

Example: Given a total of 100 devices tested with 87 devices passing the minimum criterion for success and a gate area of 0.08 cm^2, the defect density would be as follows:

$$D = -\ln(87/100)/.08 = 1.7 \text{ defects/cm}^2 \quad (8)$$

10.5.1 An undefined condition will result if the number of successes is zero. It may be necessary to change the area of the test capacitor chosen for testing in order to resolve meaningful defect densities. Fig. 4 shows the relationship between defect density and test capacitor area required for resolution in terms of a minimum of 10 % good or defective units in the sample.

10.5.2 For example, a test capacitor with an area of 0.1 cm^2 will resolve defect densities between 1 and 25 defects/cm^2, with 10 and 90 % defective samples.

10.6 *Weibull Distributions:* To convert cumulative percentages to Weibull format (sometimes referred to as "smallest extreme value probability distribution III"), use the following equation:

$$\ln(-\ln(1-F)) \quad (9)$$

where ln is the natural log operator and F is the fraction of accumulated failures. Care should be taken so that F is never exactly 1 since this will result in an undefined situation.

11. Report

11.1 Report the following for each wafer, as appropriate for the test conditions and as agreed upon by the parties to the test:

11.1.1 *Test Description*:

(*a*) Date,
(*b*) Time,
(*c*) Operator,
(*d*) Instrument station identity (if any),
(*e*) Test temperature, and
(*f*) Total number of devices tested.

11.1.2 *Sample Description*:

(*a*) Average oxide thickness,
(*b*) Gate area, cm^2,

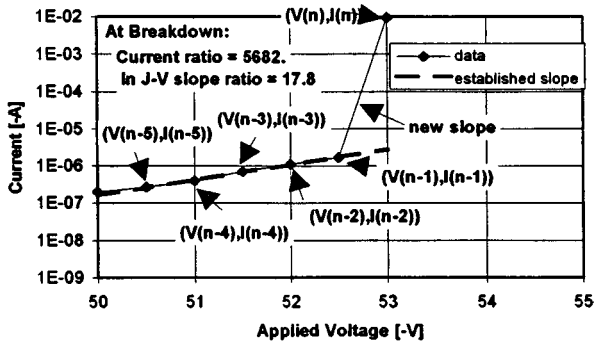

FIG. 3 Calculation of ln J-V Slope Ratio Failure Criterion for a *p*-Type Sample with 50-nm Gate Oxide

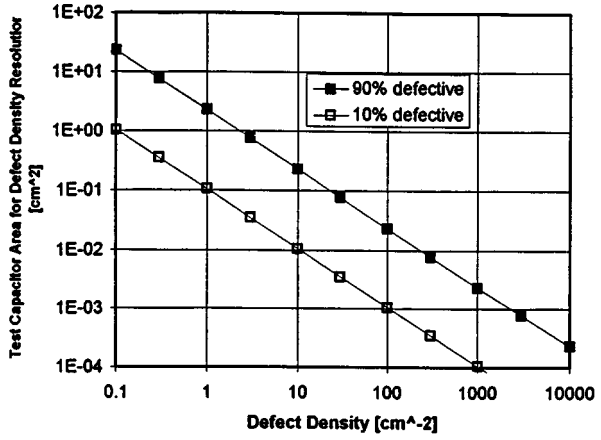

FIG. 4 Test Capacitor Area Required to Resolve Various Oxide Defect Densities, Assuming Poisson Statistics

(*c*) Gate material,
(*d*) Oxide type (example thermal versus deposited),
(*e*) Structure type,
(*f*) Conductivity type (*n* or *p*),
(*g*) Bias mode (accumulation or depletion), and
(*h*) Average computed series resistance (R_s) if performed.

11.1.3 *Test Results*:

(*a*) Medians and means for the hard and soft breakdown voltage distributions (V_{BD}) and the current densities at breakdown (J_{BD}),

(*b*) Create histograms of the hard and soft breakdown voltage and breakdown current density data. These results may also be presented in Weibull plot format,

(*c*) Report percentage of devices falling into each failure mode category by hard or soft failure voltage, or by oxide electric field. Include results of the post-test for each category, and

(*d*) Defect densities computed as described in 10.5, and as agreed upon by participating parties, should be included.

NOTE 4—For homogenous groups, data can be combined for the purposes of comparison.

12. Precision and Bias

12.1 At this time, precision has not been established. Round robin testing is planned to address to obtain these values.[6]

13. Keywords

13.1 current density; defect density; electric field strength; extrinsic breakdown; intrinsic breakdown; oxide breakdown

[6] Suehle, John S., "Reproducibility of JEDEC Standard Current and Voltage Ramp Test Procedures for Thin-Dielectric Breakdown Characterization," *International Reliability Workshop Final Report*, 1993, pp. 22–34.

APPENDIX

(Nonmandatory Information)

X1. SAMPLES AND TEST STRUCTURES

X1.1 Proper choice and fabrication of test structures to be used with this test method is crucial to the success of the testing. Because of the diverse group of intended users, specific types of test devices or fabrication procedures have not been stipulated. It is emphasized that planning of any test procedure must include a complete definition of the test structures, including fabrication parameters such as silicon starting material, insulator material, deposition technique, thickness, isolation technique (planar, LOCOS, or direct moat), electrode material, including thickness doping technique and level, sheet resistance, and sample geometry (capacitor shape and area). All these parameters must be included in the completed report of the experiment. A good discussion of factors affecting the choice and fabrication of test structures for this test may be found in EIA/JEDEC Standard 35-1.